PE43712

Product Specification

UltraCMOS® RF Digital Step Attenuator, 9 kHz–6 GHz

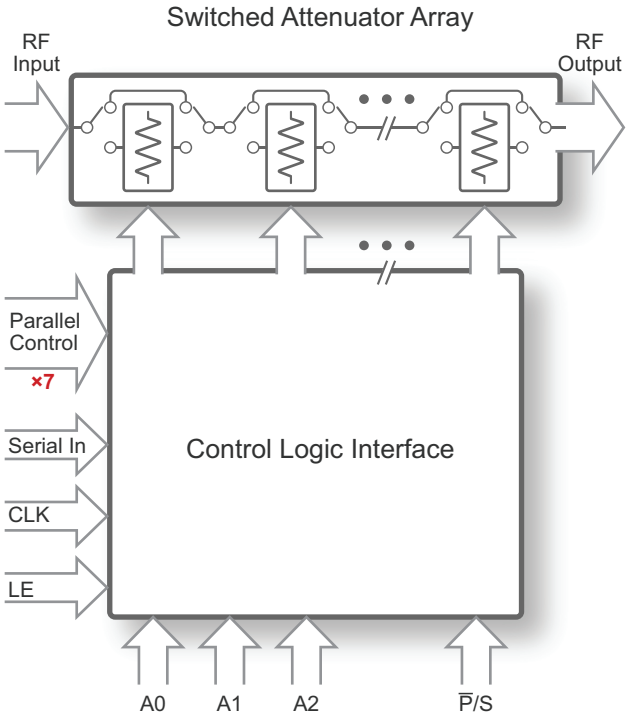
Features

- Flexible attenuation steps of 0.25 dB, 0.5 dB and 1 dB up to 31.75 dB
- Glitch-less attenuation state transitions
- Monotonicity: 0.25 dB up to 4 GHz, 0.5 dB up to 5 GHz and 1 dB up to 6 GHz
- Extended +105 °C operating temperature
- Parallel and Serial programming interfaces with Serial Addressability
- Packaging—32-lead 5 × 5 mm QFN

Applications

- 3G/4G wireless infrastructure
- Land mobile radio (LMR) system
- Point-to-point communication system

Figure 1 • *PE43712 Functional Diagram*



Product Description

The PE43712 is a 50Ω, HaRP™ technology-enhanced,7-bit RF digital step attenuator (DSA) that supports a broad frequency range from 9 kHz to 6 GHz. It features glitch-less attenuation state transitions and supports 1.8V control voltage and an extended operating temperature range to +105 °C, making this device ideal for many broadband wireless applications.

The PE43712 is a pin-compatible upgraded version of the PE43601 and PE43701. An integrated digital control interface supports both Serial Addressable and Parallel programming of the attenuation, including the capability to program an initial attenuation state at power-up.

The PE43712 covers a 31.75 dB attenuation range in 0.25 dB, 0.5 dB and 1 dB steps. It is capable of maintaining 0.25 dB monotonicity through 4GHz, 0.5 dB monotonicity through 5 GHz and 1 dB monotonicity through 6 GHz. In addition, no external blocking capacitors are required if 0 VDC is present on the RF ports.

The PE43712 is manufactured on pSemi's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate.

pSemi's HaRP technology enhancements deliver high linearity and excellent harmonics performance. It is an innovative feature of the UltraCMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

Absolute Maximum Ratings

Exceeding absolute maximum ratings listed in **Table 1** may cause permanent damage. Operation should be restricted to the limits in **Table 2**. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

ESD Precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in **Table 1**.

Latch-up Immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1 • *Absolute Maximum Ratings for PE43712*

Parameter/Condition	Min	Max	Unit
Supply voltage, V_{DD}	–0.3	5.5	V
Digital input voltage	–0.3	3.6	V
RF input power, 50Ω 9 kHz–48 MHz >48 MHz–6 GHz		 **Figure 5** +31	 dBm dBm
Storage temperature range	–65	+150	°C
ESD voltage HBM, all pins(1)		3000	V
ESD voltage CDM, all pins(2)		1000	V

Notes:
1) Human body model (MIL–STD 883 Method 3015).
2) Charged device model (JEDEC JESD22–C101).

Recommended Operating Conditions

Table 2 lists the recommending operating condition for the PE43712. Devices should not be operated outside the recommended operating conditions listed below.

Table 2 • *Recommended Operating Condition for PE43712*

Parameter	Min	Typ	Max	Unit
Supply voltage, V_{DD}	2.3		5.5	V
Supply current, I_{DD}		150	200	µA
Digital input high	1.17		3.6	V
Digital input low	–0.3		0.6	V
Digital input current			17.5	µA
RF input power, CW[1] 9 kHz–48 MHz >48 MHz–6 GHz			 **Figure 5** +23	 dBm dBm
RF input power, pulsed[2] 9 kHz–48 MHz >48 MHz–6 GHz			 **Figure 5** +28	 dBm dBm
Operating temperature range	–40	+25	+105	°C

Notes:
1) 100% duty cycle, all bands, 50Ω.
2) Pulsed, 5% duty cycle of 4620 µs period, 50Ω.

Electrical Specifications

Table 3 provides the PE43712 key electrical specifications at 25 °C, V_{DD} = 3.3V, RF1 = RF_{IN}, RF2 = RF_{OUT} (Z_S = Z_L = 50Ω), unless otherwise specified.

Table 3 • *PE43712 Electrical Specifications*

Parameter	Condition	Frequency	Min	Typ	Max	Unit
Operating frequency			9 kHz		6 GHz	As shown
Attenuation range	0.25 dB step 0.5 dB step 1 dB step			0–31.75 0–31.50 0–31.00		dB dB dB
Insertion loss		9 kHz–1.0 GHz 1.0–2.2 GHz 2.2–4.0 GHz 4.0–6.0 GHz		1.3 1.6 1.95 2.45	1.5 1.85 2.4 2.8	dB dB dB dB
Attenuation error	**0.25 dB step**					
	0–8 dB	9 kHz–2.2 GHz			± (0.20 + 1.5% of attenuation setting)	dB
	8.25–31.75 dB	9 kHz–2.2 GHz			± (0.20 + 2.0% of attenuation setting)	dB
	0–31.75 dB	>2.2–3.0 GHz			± (0.15 + 3.0% of attenuation setting)	dB
	0–31.75 dB	>3.0–4.0 GHz			± (0.25 + 3.5% of attenuation setting)	dB
	0.50 dB step					
	0–8 dB	9 kHz–2.2 GHz			± (0.20 + 1.5% of attenuation setting)	dB
	8.5–31.5 dB	9 kHz–2.2 GHz			± (0.20 + 2.0% of attenuation setting)	dB
	0–31.5 dB	>2.2–3.0 GHz			± (0.15 + 3.0% of attenuation setting)	dB
	0–31.5 dB	>3.0–5.0 GHz			± (0.25 + 5.0% of attenuation setting)	dB

Table 3 • *PE43712 Electrical Specifications (Cont.)*

Parameter	Condition	Frequency	Min	Typ	Max	Unit
Attenuation error	**1 dB step**					
	0–8 dB	9 kHz–2.2 GHz			± (0.20 + 1.5% of attenuation setting)	dB
	9–31 dB	9 kHz–2.2 GHz			± (0.20 + 2.0% of attenuation setting)	dB
	0–31 dB	>2.2–3.0 GHz			± (0.15 + 3.0% of attenuation setting)	dB
	0–31 dB	>3.0–5.0 GHz			± (0.25 + 5.0% of attenuation setting)	dB
	0–31 dB	>5.0–6.0 GHz			± (0.25 + 5.0% of attenuation setting)	dB
Return loss	Input port or output port	9 kHz–4 GHz 4–6 GHz		13 15		dB dB
Relative phase	All states	9 kHz–4 GHz 4–6 GHz		27 42		deg deg
Input 0.1dB compression point(*)		48 MHz–6 GHz		31		dBm
Input IP3	Two tones at +18 dBm, 20 MHz spacing	4 GHz 6 GHz		57 56		dBm dBm
RF T_{rise}/T_{fall}	10%/90% RF			200		ns
Settling time	RF settled to within 0.05 dB of final value			1.6		µs
Switching time	50% CTRL to 90% or 10% RF			275		ns
Attenuation transient (envelope)		2 GHz		0.3		dB

Note: * The input 0.1dB compression point is a linearity figure of merit. Refer to **Table 2** for the operating RF input power (50Ω).

Switching Frequency

The PE43712 has a maximum 25 kHz switching rate.

Switching frequency is defined to be the speed at which the DSA can be toggled across attenuation states. Switching time is the time duration between the point the control signal reaches 50% of the final value and the point the output signal reaches within 10% or 90% of its target value.

Spurious Performance

The typical spurious performance of the PE43712 is –130 dBm.

Glitch-less Attenuation State Transitions

The PE43712 features a novel architecture to provide the best-in-class glitch-less transition behavior when changing attenuation states. When RF input power is applied, the output power spikes are greatly reduced (≤0.3 dB) during attenuation state changes when comparing to previous generations of DSAs.

Truth Tables

Table 4–Table 6 provide the truth tables for the PE43712.

Table 4 • *Parallel Truth Table*

Parallel Control Setting							Attenuation Setting RF1–RF2
D6	D5	D4	D3	D2	D1	D0	
L	L	L	L	L	L	L	Reference IL
L	L	L	L	L	L	H	0.25 dB
L	L	L	L	L	H	L	0.5 dB
L	L	L	L	H	L	L	1 dB
L	L	L	H	L	L	L	2 dB
L	L	H	L	L	L	L	4 dB
L	H	L	L	L	L	L	8 dB
H	L	L	L	L	L	L	16 dB
H	H	H	H	H	H	H	31.75 dB

Table 5 • *Serial Address Word Truth Table*

Address Word								Address Setting
A7 (MSB)	A6	A5	A4	A3	A2	A1	A0	
X	X	X	X	X	L	L	L	000
X	X	X	X	X	L	L	H	001
X	X	X	X	X	L	H	L	010
X	X	X	X	X	L	H	H	011
X	X	X	X	X	H	L	L	100
X	X	X	X	X	H	L	H	101
X	X	X	X	X	H	H	L	110
X	X	X	X	X	H	H	H	111

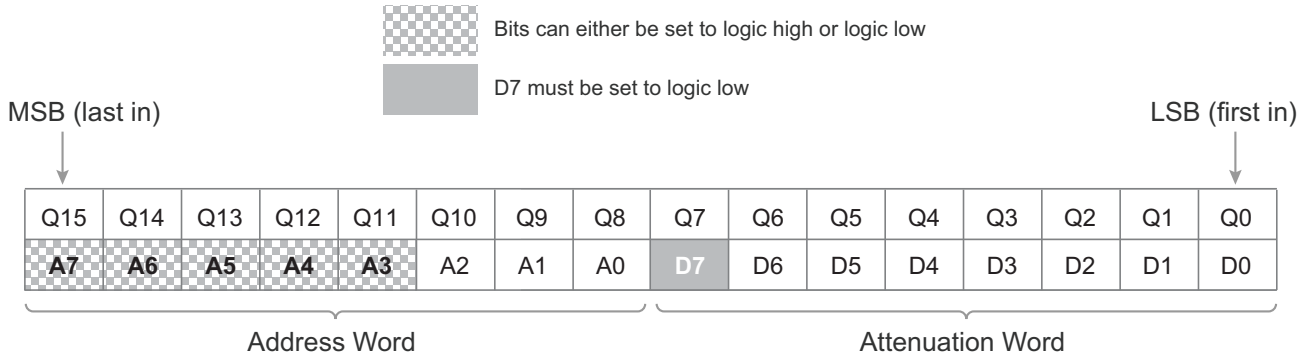
Table 6 • *Serial Attenuation Word Truth Table*

Attenuation Word								Attenuation Setting RF1–RF2
D7	D6	D5	D4	D3	D2	D1	D0 (LSB)	
L	L	L	L	L	L	L	L	Reference IL
L	L	L	L	L	L	L	H	0.25 dB
L	L	L	L	L	L	H	L	0.5 dB
L	L	L	L	L	H	L	L	1 dB
L	L	L	L	H	L	L	L	2 dB
L	L	L	H	L	L	L	L	4 dB
L	L	H	L	L	L	L	L	8 dB
L	H	L	L	L	L	L	L	16 dB
L	H	H	H	H	H	H	H	31.75 dB

Serial Addressable Register Map

Figure 2 provides the Serial Addressable register map for the PE43712.

Figure 2 • *Serial Addressable Register Map*



The attenuation word is derived directly from the value of the attenuation state. To find the attenuation word, multiply the value of the state by four, then convert to binary.

For example, to program the 18.25 dB state at address 3:

$$4 \times 18.25 = 73$$
$$73 \rightarrow 01001001$$

Address Word: XXXXX011
Attenuation Word: 01001001
Serial Input: XXXXX01101001001

Programming Options

Parallel/Serial Selection

Either a Parallel or Serial addressable interface can be used to control the PE43712. The $\overline{P}$/S bit provides this selection, with $\overline{P}$/S = LOW selecting the Parallel interface and $\overline{P}$/S = HIGH selecting the Serial interface.

Parallel Mode Interface

The Parallel interface consists of seven CMOS-compatible control lines that select the desired attenuation state, as shown in **Table 4**.

The Parallel interface timing requirements are defined by **Figure 4** (Parallel Interface Timing Diagram), **Table 9** (Parallel and Direct Interface AC Characteristics) and switching time (**Table 3**).

For Latched Parallel programming, the Latch Enable (LE) should be held LOW while changing attenuation state control values, then pulse LE HIGH to LOW (per **Figure 4**) to latch new attenuation state into the device.

For Direct Parallel programming, the LE line should be pulled HIGH. Changing attenuation state control values will change device state to new attenuation. Direct mode is ideal for manual control of the device (using hardwire, switches, or jumpers).

Serial-Addressable Interface

The Serial-Addressable interface is a 16-bit Serial-In, Parallel-Out shift register buffered by a transparent latch. The 16-bits make up two words comprised of 8-bits each. The first word is the Attenuation Word, which controls the state of the DSA. The second word is the Address Word, which is compared to the static (or programmed) logical states of the A0, A1 and A2 digital inputs. If there is an address match, the DSA changes state; otherwise its current state will remain unchanged. **Figure 3** illustrates an example timing diagram for programming a state. It is required that all Parallel control inputs be grounded when the DSA is used in Serial-Addressable mode.

The Serial-Addressable interface is controlled using three CMOS-compatible signals: SI, Clock (CLK) and LE. The SI and CLK inputs allow data to be serially entered into the shift register. Serial data is clocked in LSB first.

The shift register must be loaded while LE is held LOW to prevent the attenuator value from changing as data is entered. The LE input should then be toggled HIGH and brought LOW again, latching the new data into the DSA. The Address Word truth table is listed in **Table 5**. The Attenuation Word truth table is listed in **Table 6**. A programming example of the serial register is illustrated in **Figure 2**. The Serial timing diagram is illustrated in **Figure 3**.

Power-up Control Settings

The PE43712 will always initialize to the maximum attenuation setting (31.75 dB) on power-up for both the Serial Addressable and Latched Parallel modes of operation and will remain in this setting until the user latches in the next programming word. In Direct Parallel mode, the DSA can be preset to any state within the 31.75 dB range by pre-setting the Parallel control pins prior to power-up. In this mode, there is a 400 µs delay between the time the DSA is powered-up to the time the desired state is set. During this power-up delay, the device attenuates to the maximum attenuation setting (31.75 dB) before defaulting to the user defined state. If the control pins are left floating in this mode during power-up, the device will default to the minimum attenuation setting (insertion loss state).

Dynamic operation between Serial and Parallel programming modes is possible.

If the DSA powers up in Serial mode ($\overline{P}$/S = HIGH), all the Parallel control inputs DI[6:0] must be set to logic LOW. Prior to toggling to Parallel mode, the DSA must be programmed serially to ensure D[7] is set to logic LOW.

If the DSA powers up in either Latched or Direct Parallel mode, all Parallel pins DI[6:0] must be set to logic LOW prior to toggling to Serial Addressable mode ($\overline{P}$/S = HIGH), and held LOW until the DSA has been programmed serially to ensure bit D[7] is set to logic LOW.

The sequencing is only required once on power-up. Once completed, the DSA may be toggled between Serial and Parallel programming modes at will.

Figure 3 • *Serial Timing Diagram*

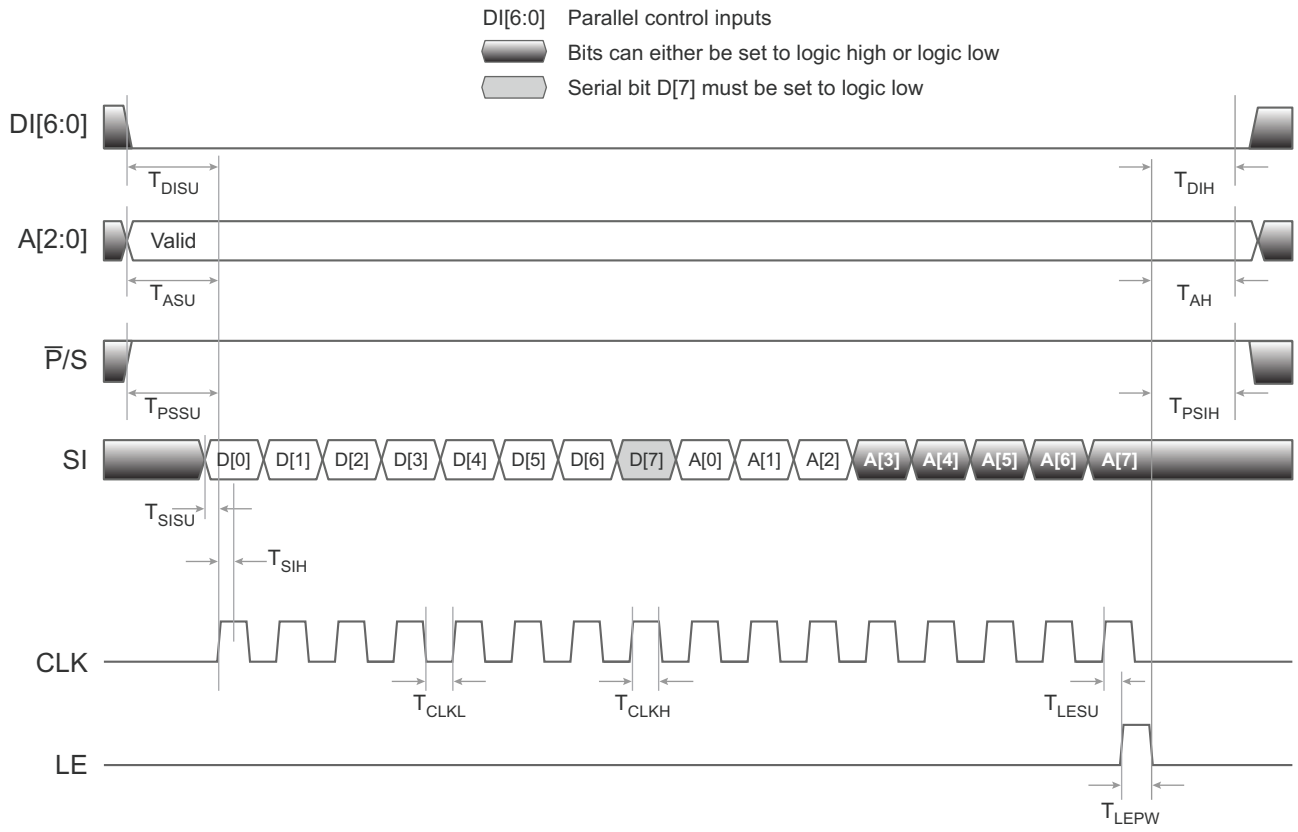


Figure 4 • *Latched Parallel/Direct Parallel Timing Diagram*

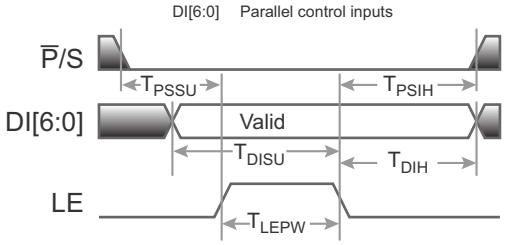


Table 7 • *Latch and Clock Specifications*

Latch Enable	Shift Clock	Function
0	↑	Shift register clocked
↑	X	Contents of shift register transferred to attenuator core

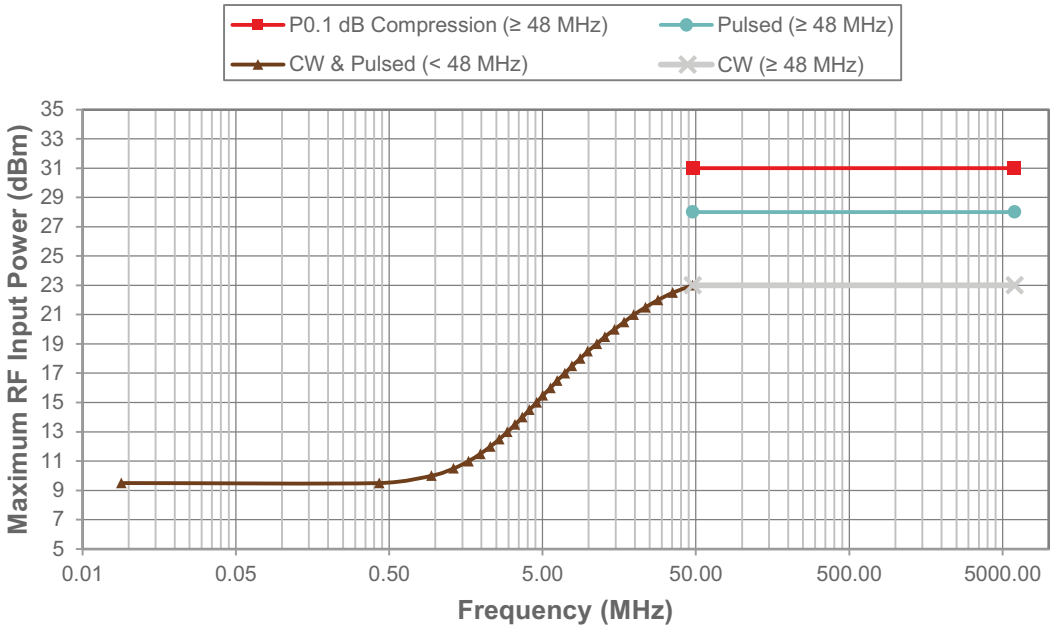
Table 8 • *Serial Interface AC Characteristics*(*)

Parameter/Condition	Min	Max	Unit
Serial clock frequency, F_{CLK}		10	MHz
Serial clock HIGH time, T_{CLKH}	30		ns
Serial clock LOW time, T_{CLKL}	30		ns
Last Serial clock rising edge setup time to Latch Enable rising edge, T_{LESU}	10		ns
Latch Enable minimum pulse width, T_{LEPW}	30		ns
Serial data setup time, T_{SISU}	10		ns
Serial data hold time, T_{SIH}	10		ns
Parallel data setup time, T_{DISU}	100		ns
Parallel data hold time, T_{DIH}	100		ns
Address setup time, T_{ASU}	100		ns
Address hold time, T_{AH}	100		ns
Parallel/Serial setup time, T_{PSSU}	100		ns
Parallel/Serial hold time, T_{PSIH}	100		ns
Note: * V_{DD} = 3.3V or 5.0V, –40 °C < T_A < +105 °C, unless otherwise specified.			

Table 9 • *Parallel and Direct Interface AC Characteristics*(*)

Parameter/Condition	Min	Max	Unit
Latch Enable minimum pulse width, T_{LEPW}	30		ns
Parallel data setup time, T_{DISU}	100		ns
Parallel data hold time, T_{DIH}	100		ns
Parallel/Serial setup time, T_{PSSU}	100		ns
Parallel/Serial hold time, T_{PSIH}	100		ns
Note: * V_{DD} = 3.3V or 5.0V, –40 °C < T_A < +105 °C, unless otherwise specified.			

Figure 5 • *Power De-rating Curve, 9 kHz–6 GHz, –40 to +105 °C Ambient, 50Ω*



Typical Performance Data

Figure 6–Figure 32 show the typical performance data at 25 °C and V_{DD} = 3.3V, RF1 = RF_{IN}, RF2 = RF_{OUT} (Z_S = Z_L = 50Ω) unless otherwise specified.

Figure 6 • ***Insertion Loss vs Temperature***

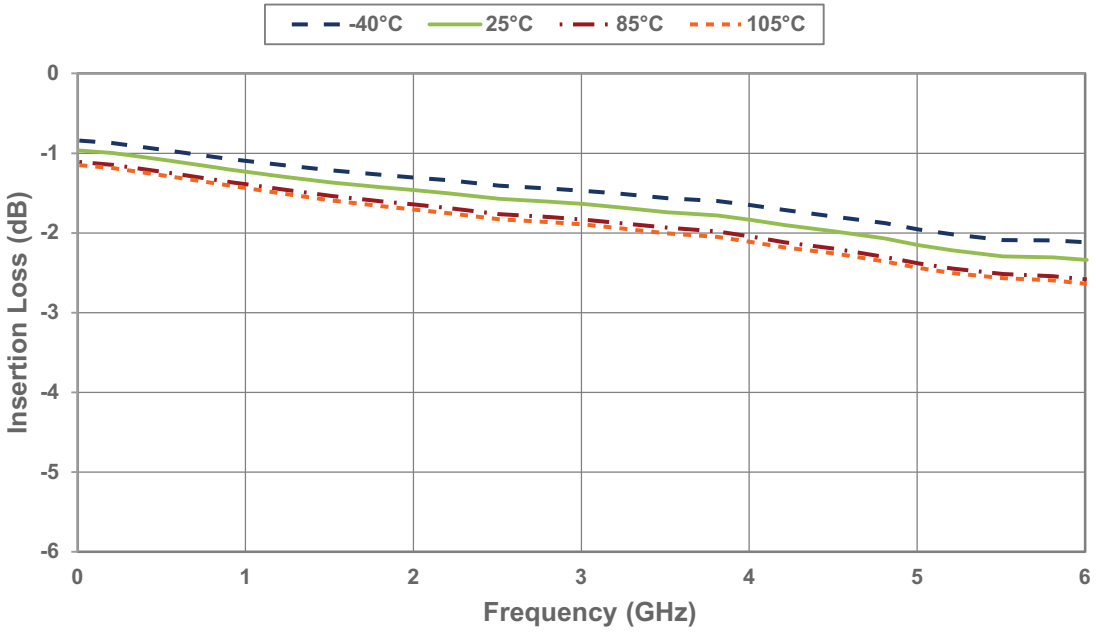


Figure 7 • *Input Return Loss vs Attenuation Setting*

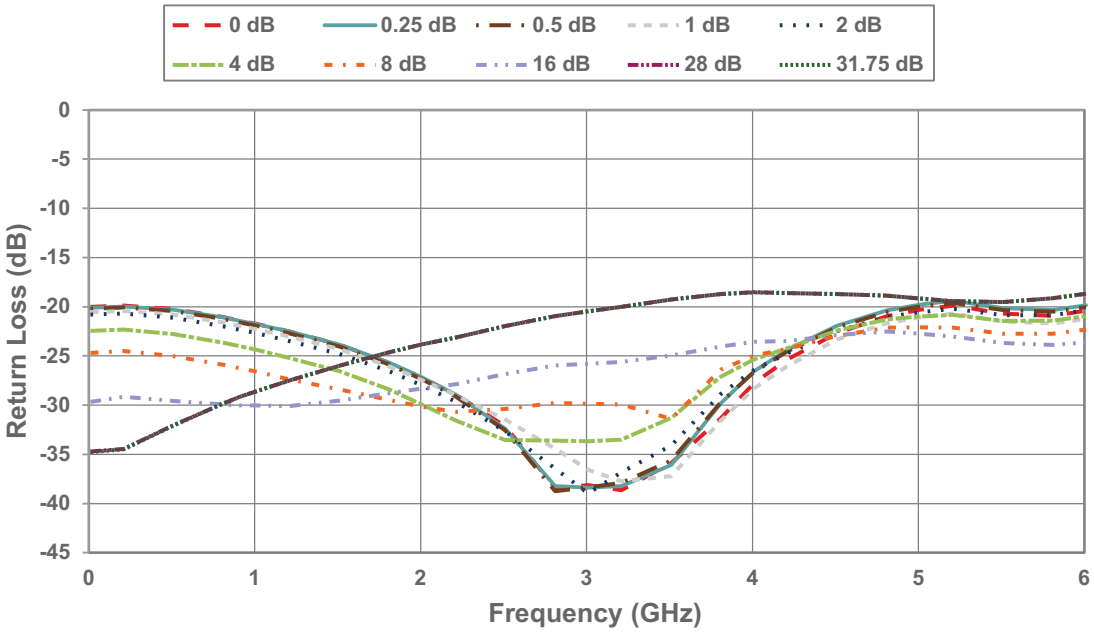


Figure 8 • *Output Return Loss vs Attenuation Setting*

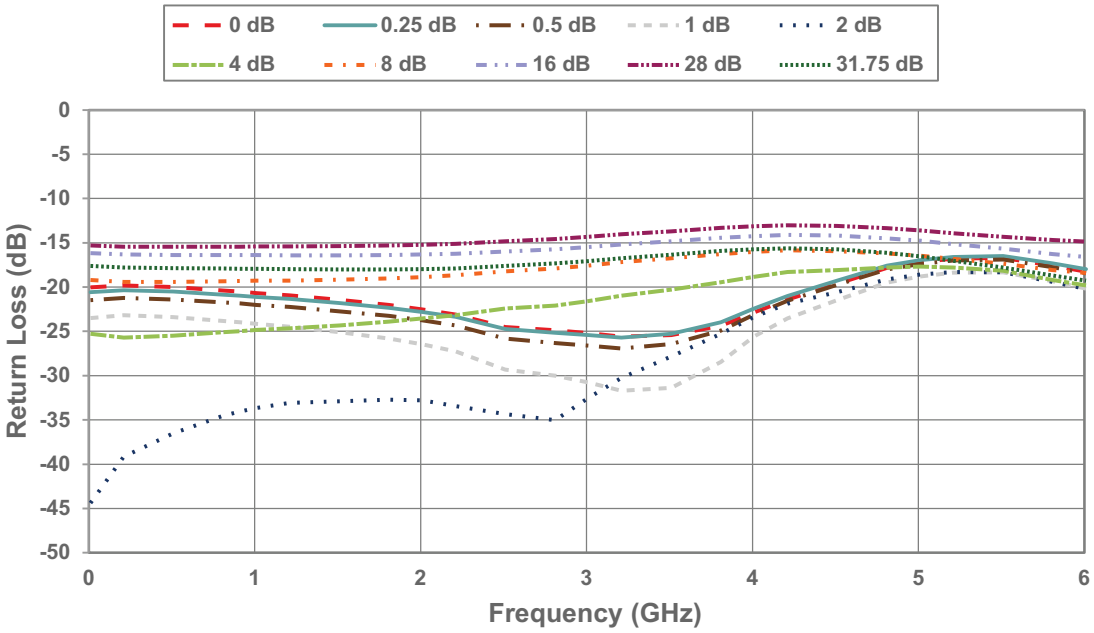


Figure 9 • *Input Return Loss for 16 dB Attenuation Setting vs Temperature*

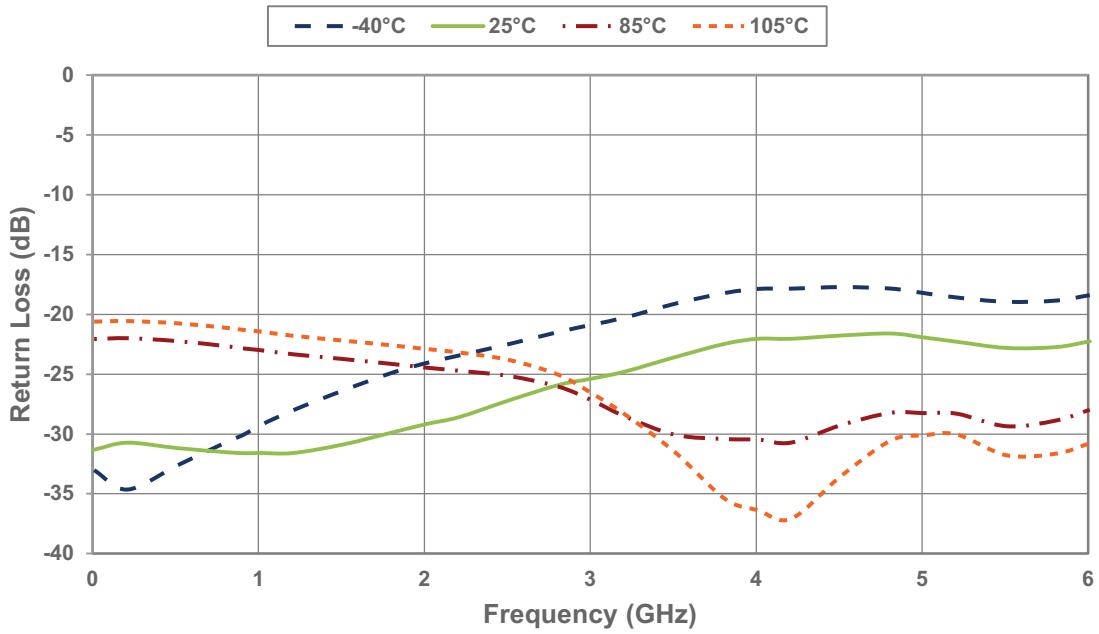


Figure 10 • *Output Return Loss for 16 dB Attenuation Setting vs Temperature*

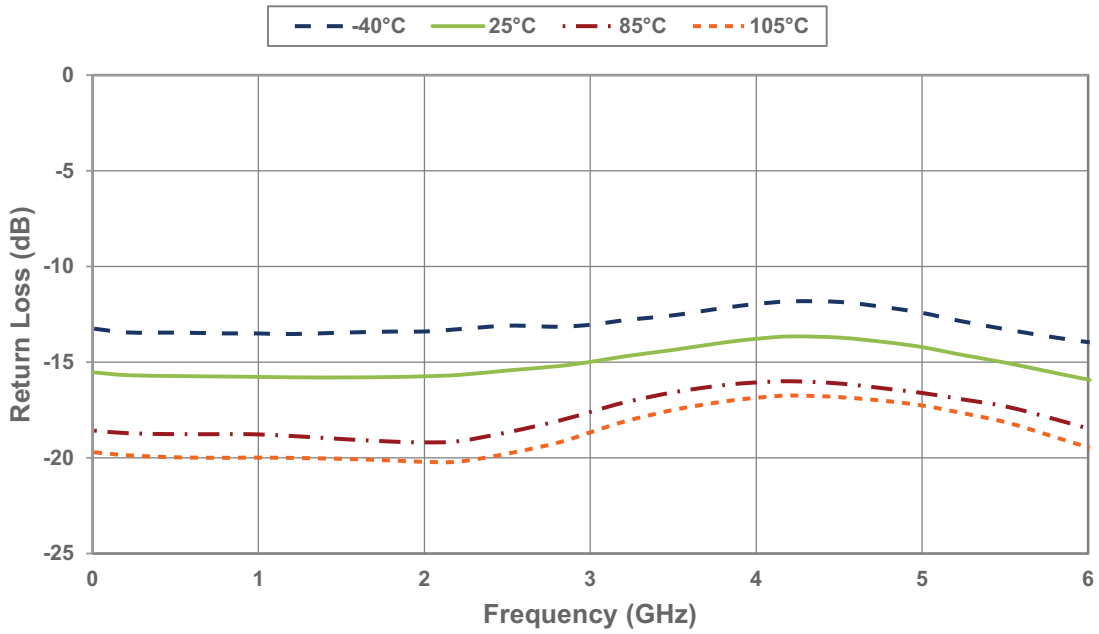


Figure 11 • *Relative Phase Error vs Attenuation Setting*

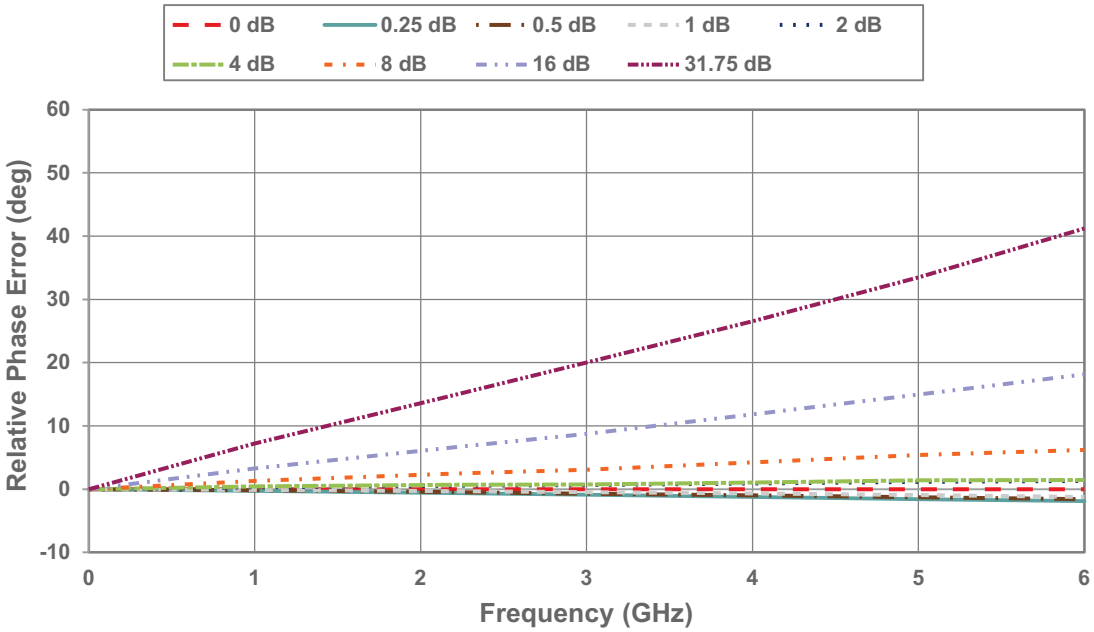


Figure 12 • *Relative Phase Error for 31.75 dB Attenuation Setting vs Frequency*

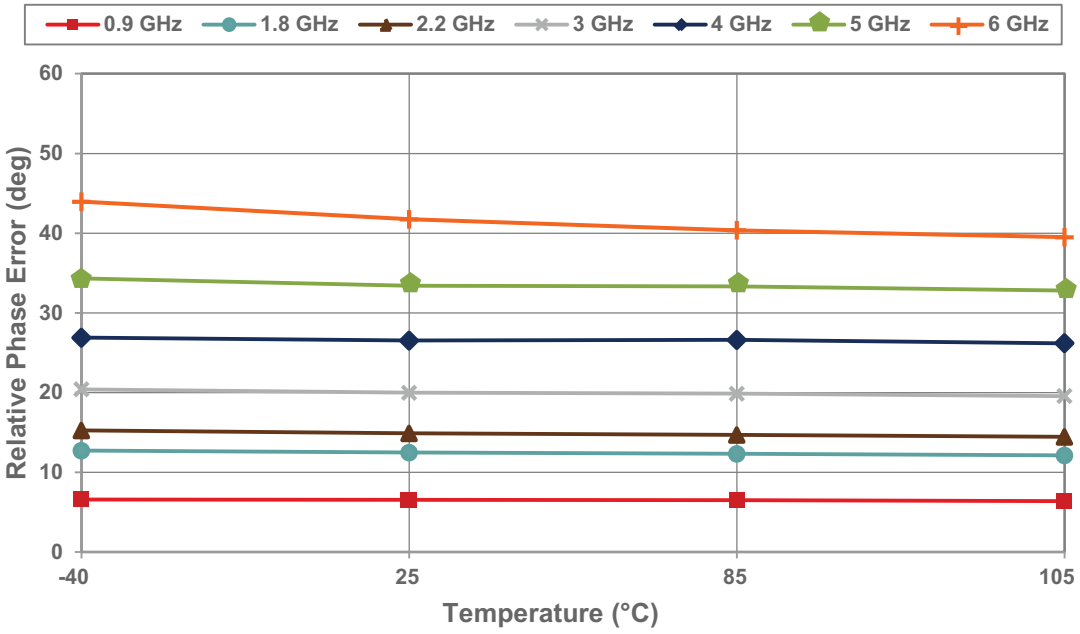


Figure 13 • *Attenuation Error @ 900 MHz vs Temperature*

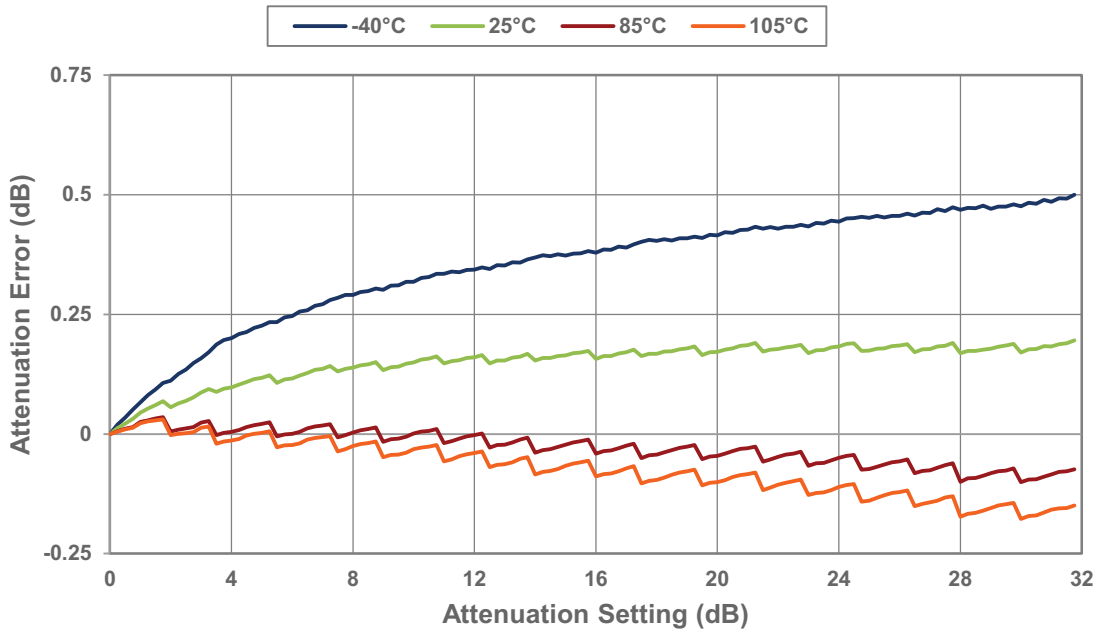


Figure 14 • *Attenuation Error @ 1800 MHz vs Temperature*

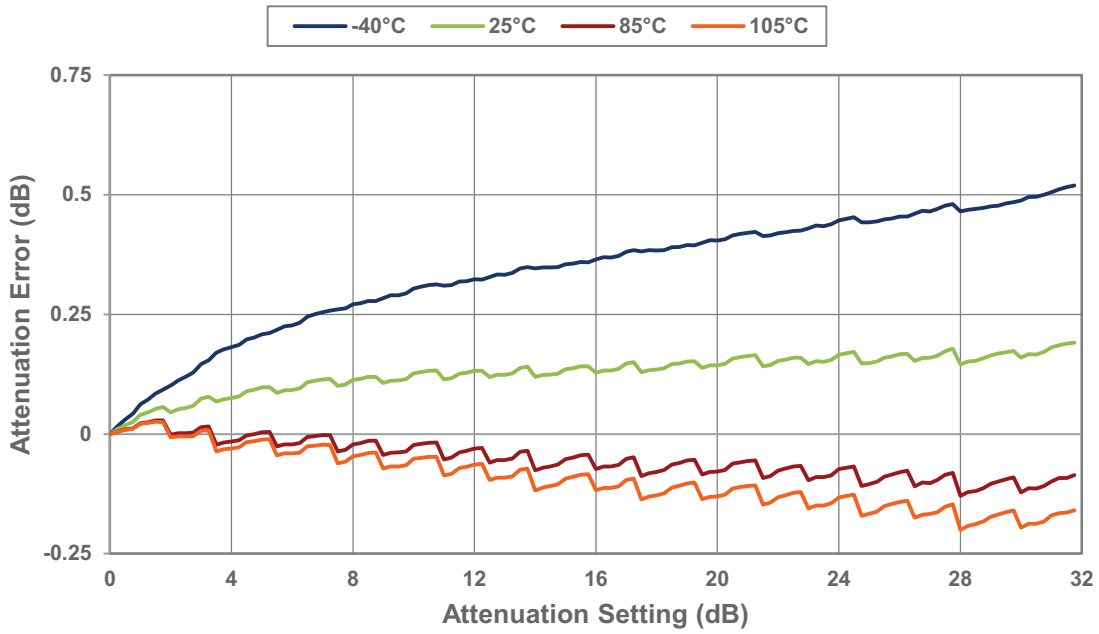


Figure 15 • *Attenuation Error @ 2200 MHz vs Temperature*

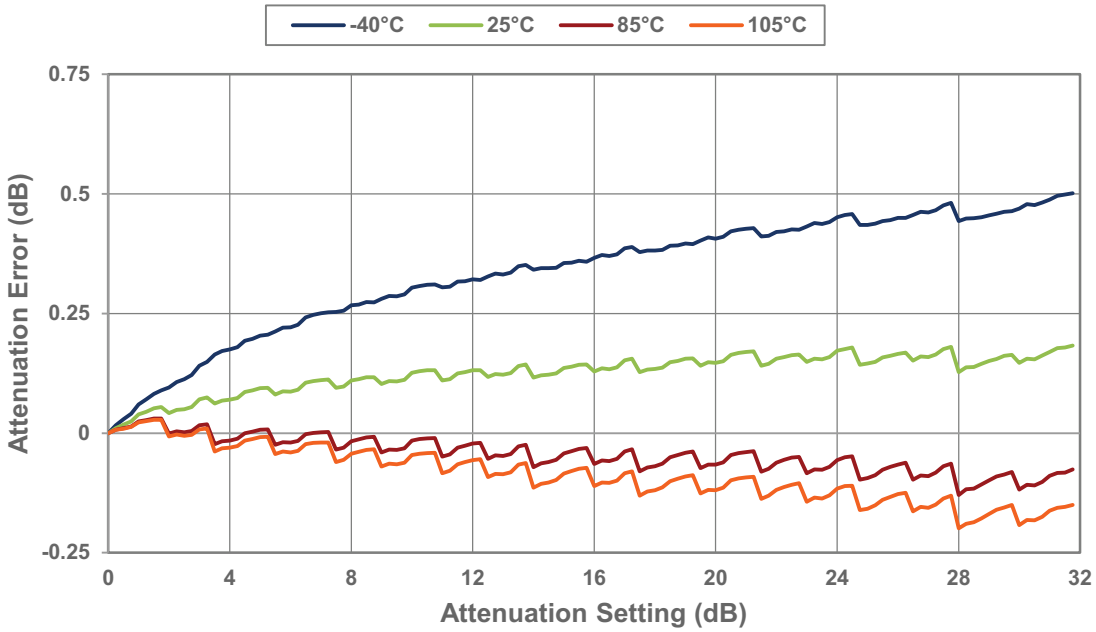


Figure 16 • *Attenuation Error @ 3000 MHz vs Temperature*

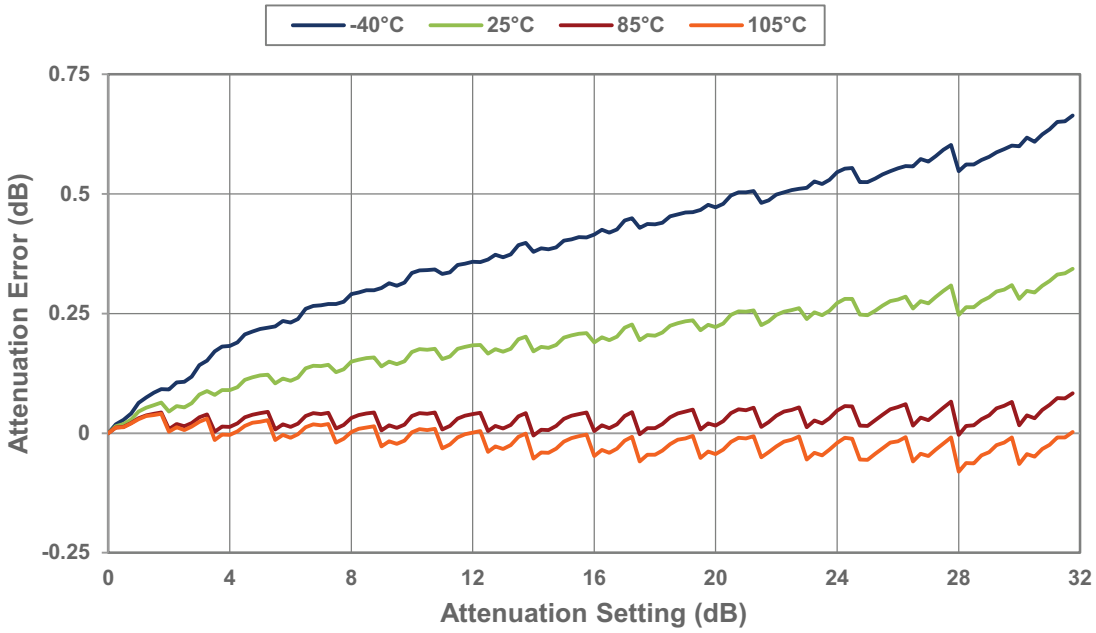


Figure 17 • *Attenuation Error @ 4000 MHz vs Temperature*

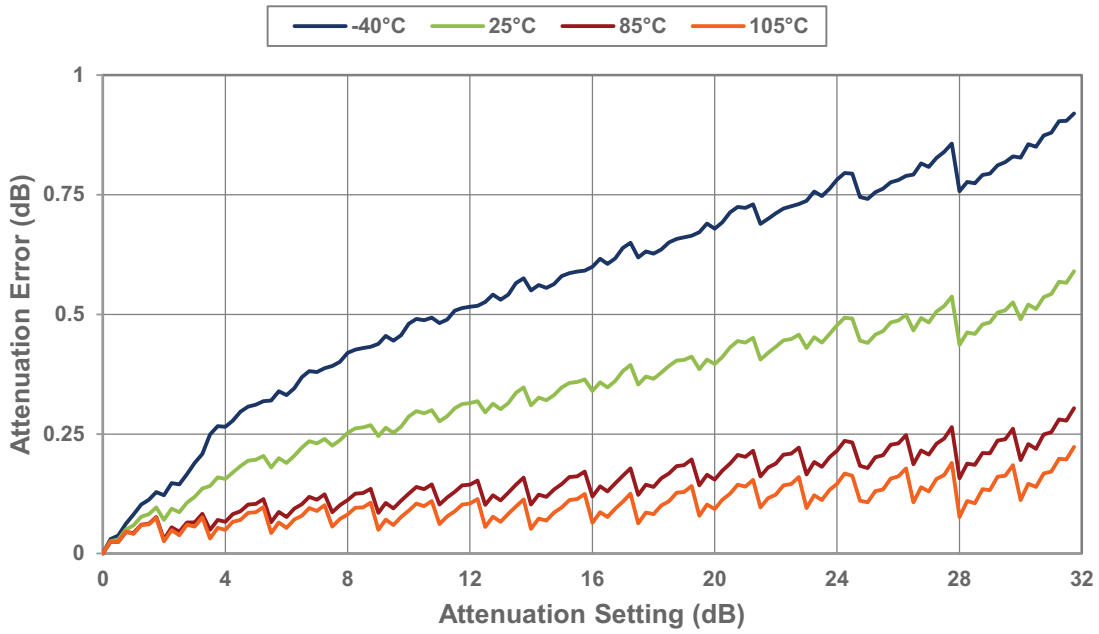


Figure 18 • *IIP3 vs Attenuation Setting*

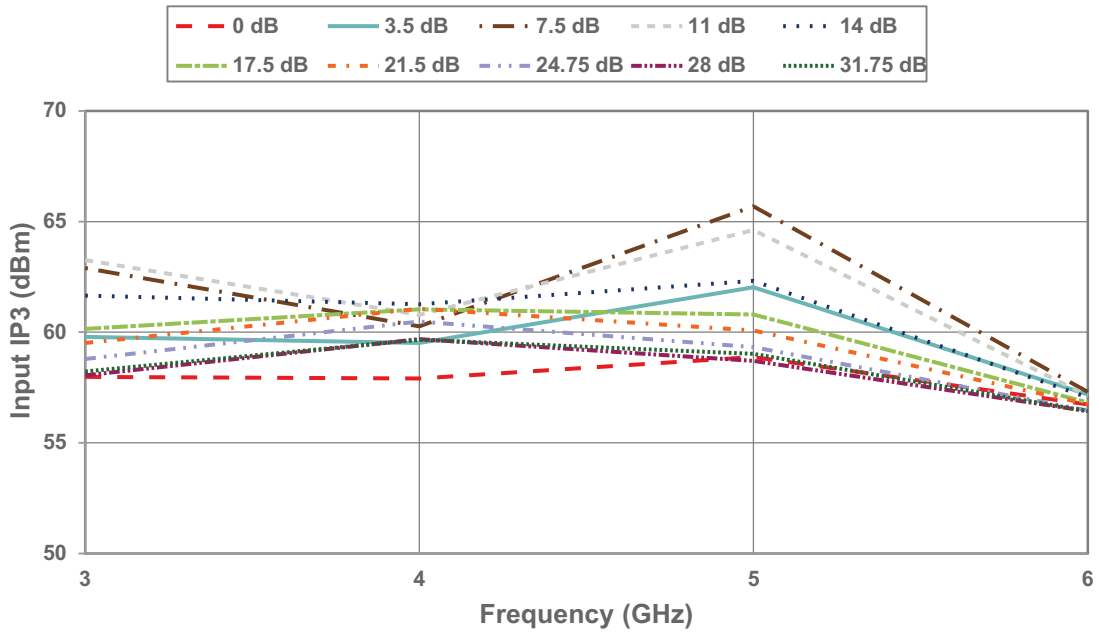
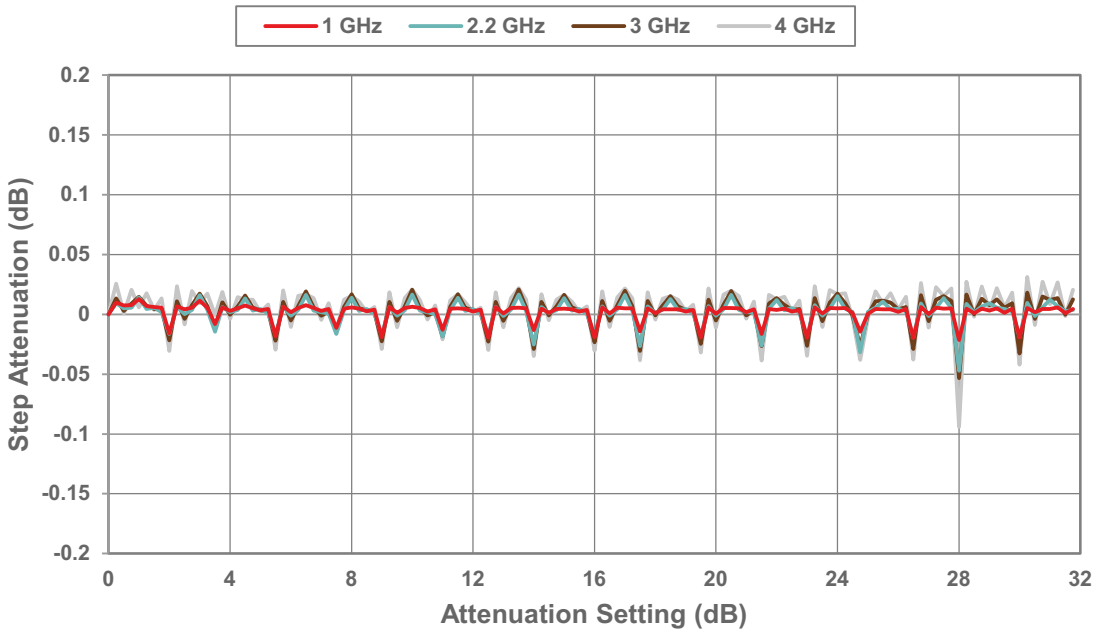


Figure 19 • *0.25 dB Step Attenuation vs Frequency*(*)



Note: * Monotonicity is held so long as step attenuation does not cross below –0.25 dB.

Figure 20 • *0.25 dB Step, Actual vs Frequency*

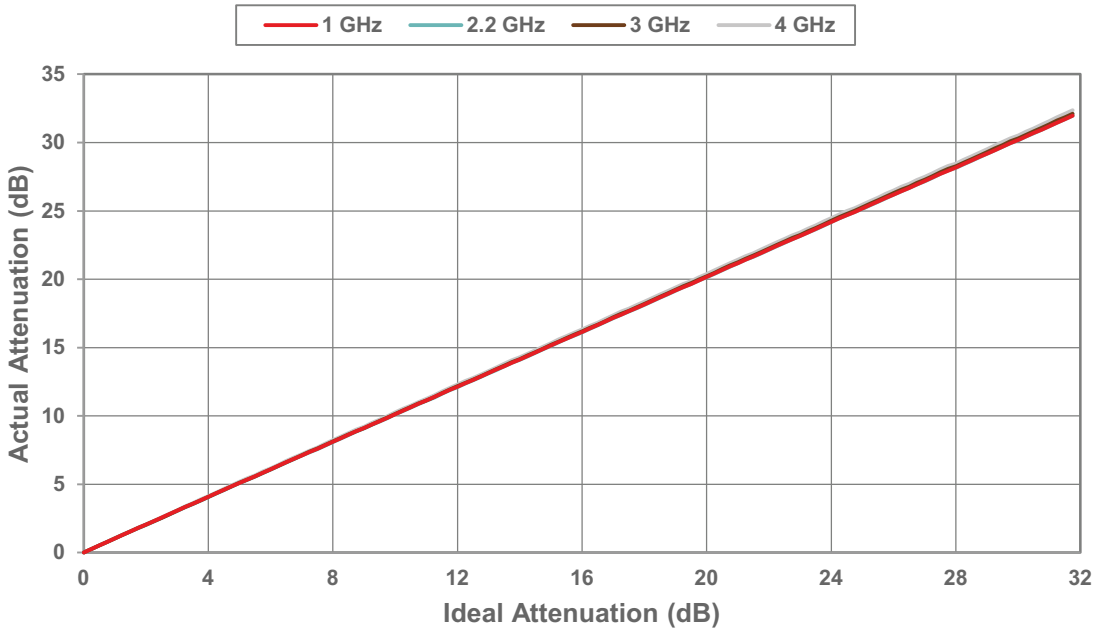


Figure 21 • *0.25 dB Major State Bit Error vs Attenuation Setting*

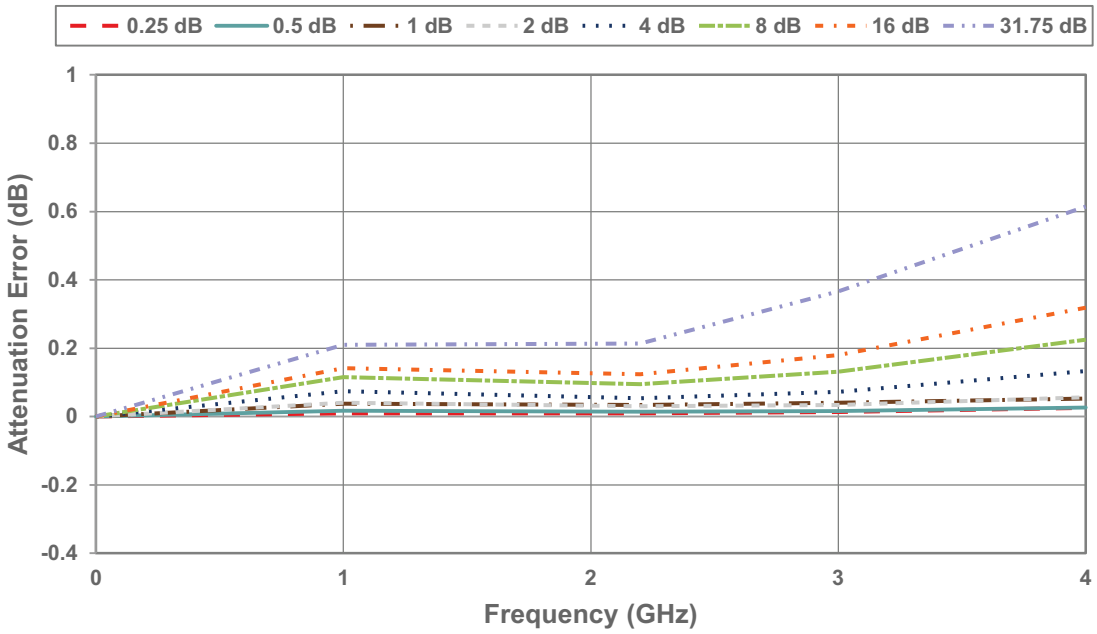


Figure 22 • *0.25 dB Attenuation Error vs Frequency*

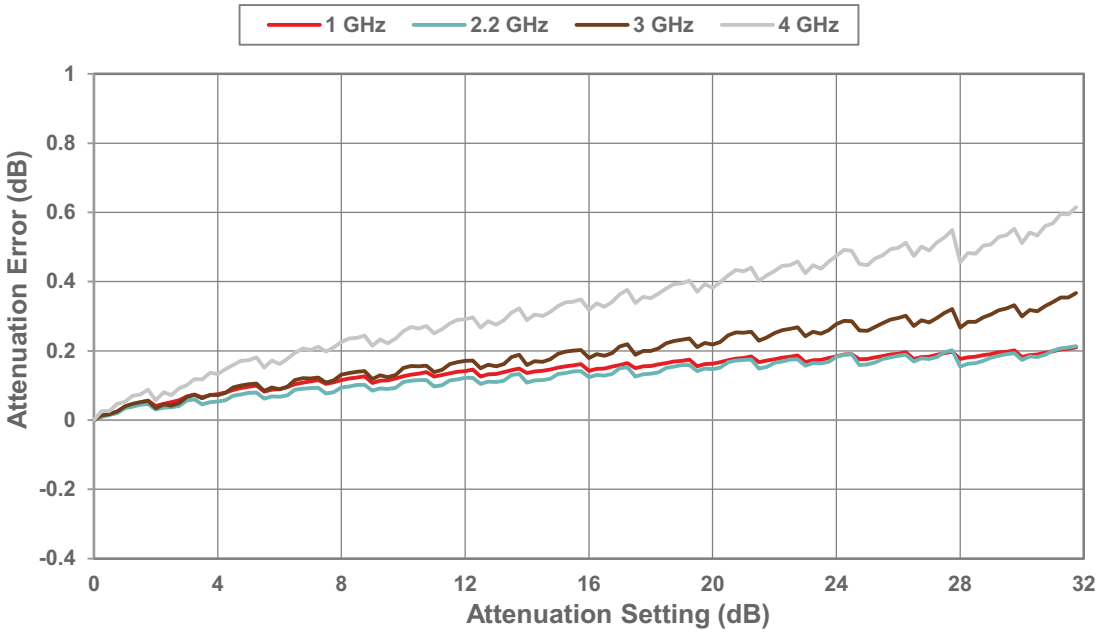
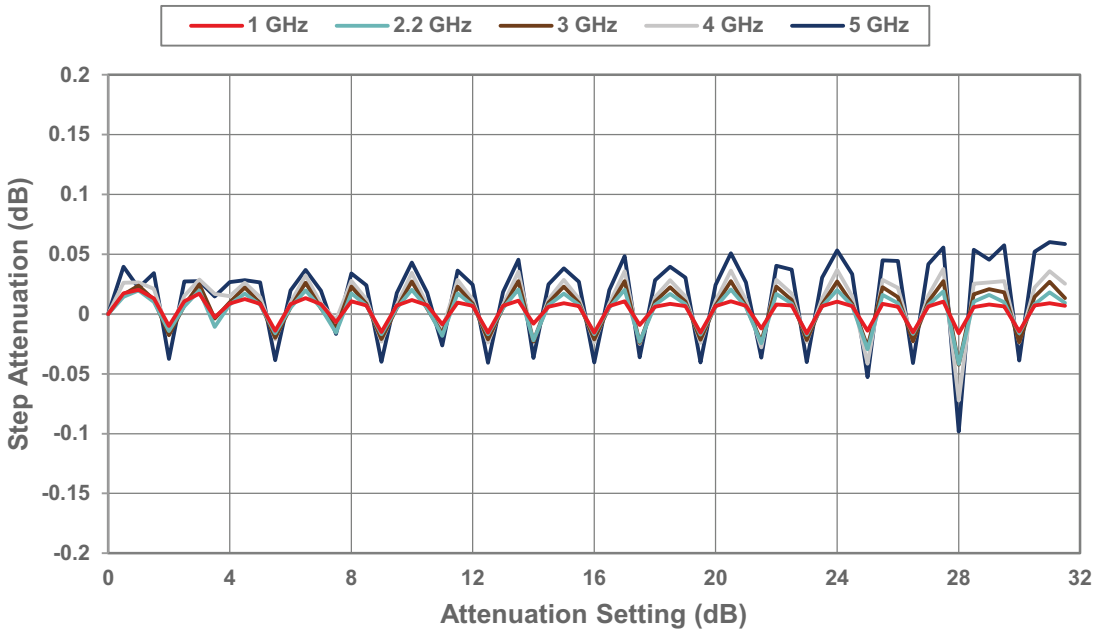


Figure 23 • *0.5 dB Step Attenuation vs Frequency*(*)



Note: * Monotonicity is held so long as step attenuation does not cross below –0.5 dB.

Figure 24 • *0.5 dB Step, Actual vs Frequency*

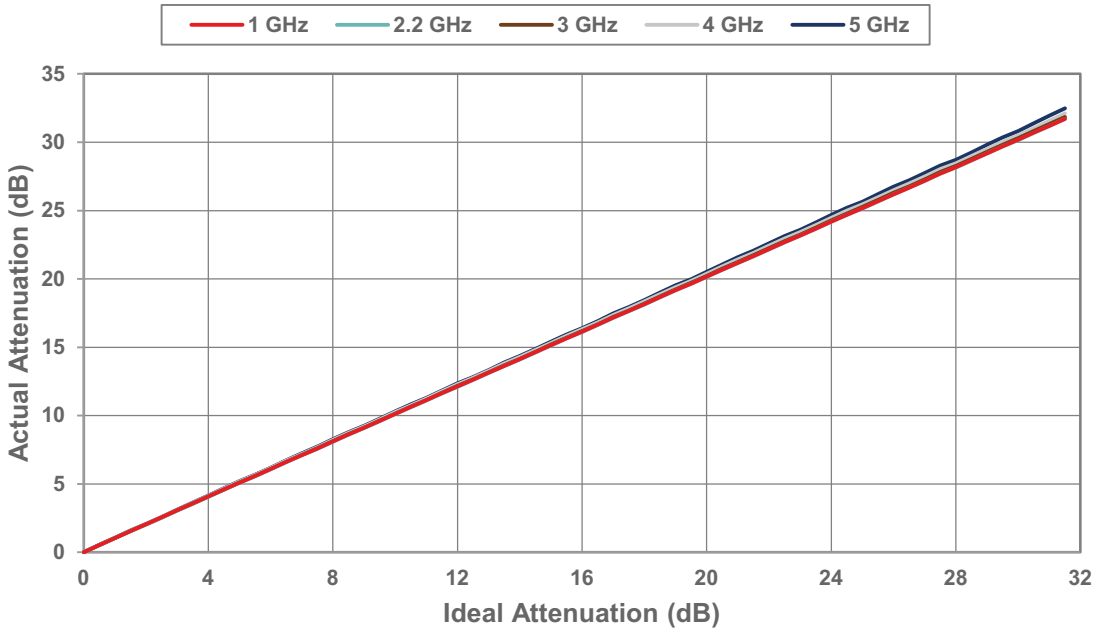


Figure 25 • *0.5 dB Major State Bit Error vs Attenuation Setting*

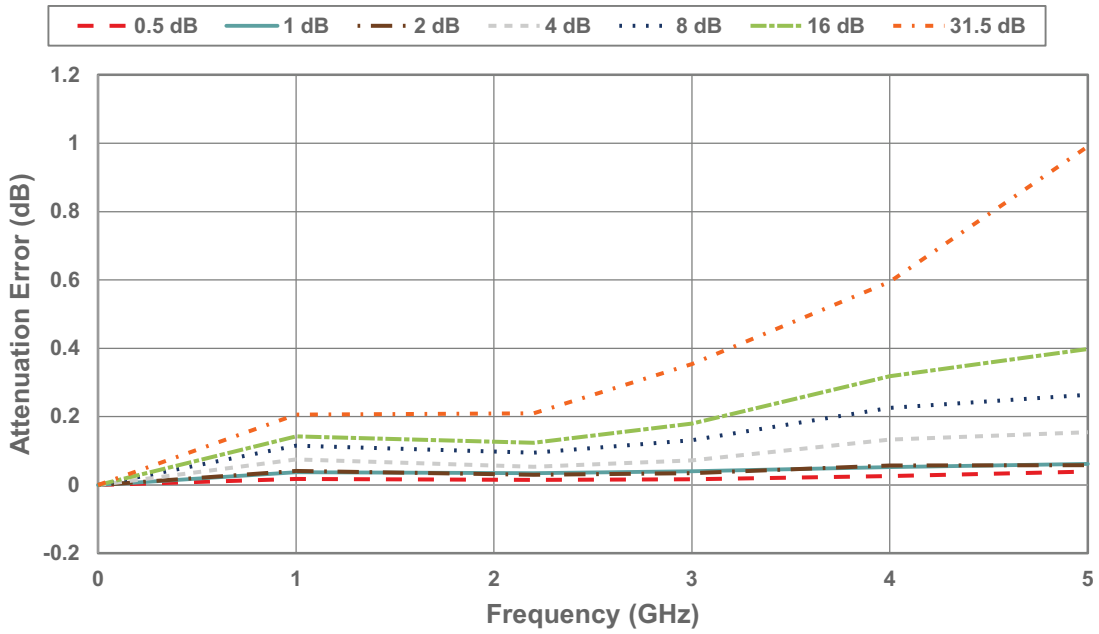


Figure 26 • *0.5 dB Attenuation Error vs Frequency*

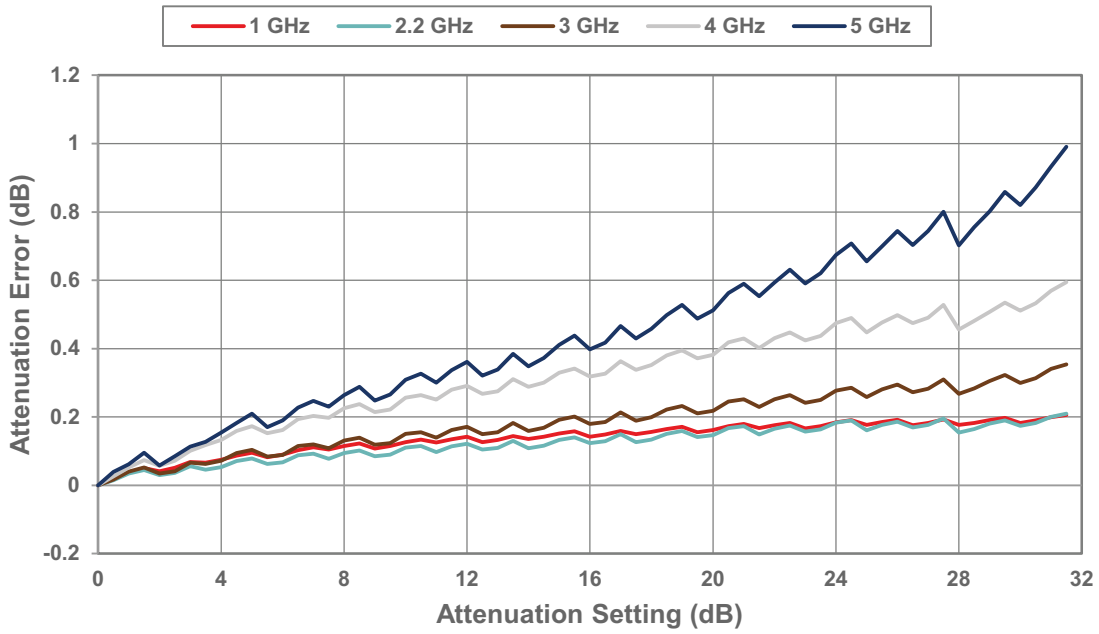
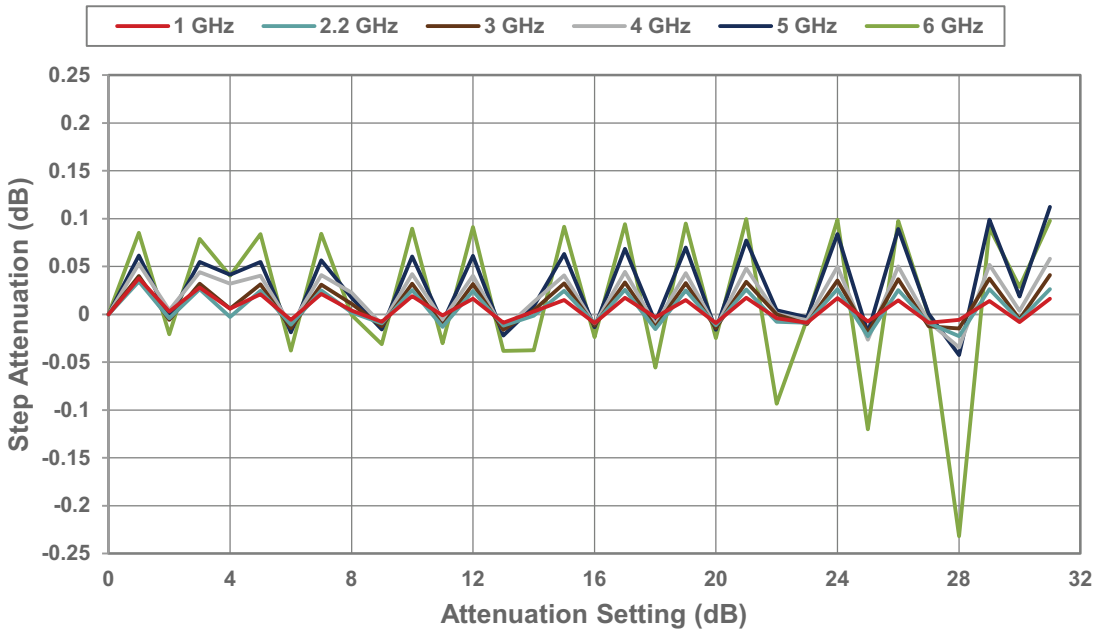


Figure 27 • *1 dB Step Attenuation vs Frequency*(*)



Note: * Monotonicity is held so long as step attenuation does not cross below –1 dB.

Figure 28 • *1 dB Step, Actual vs Frequency*

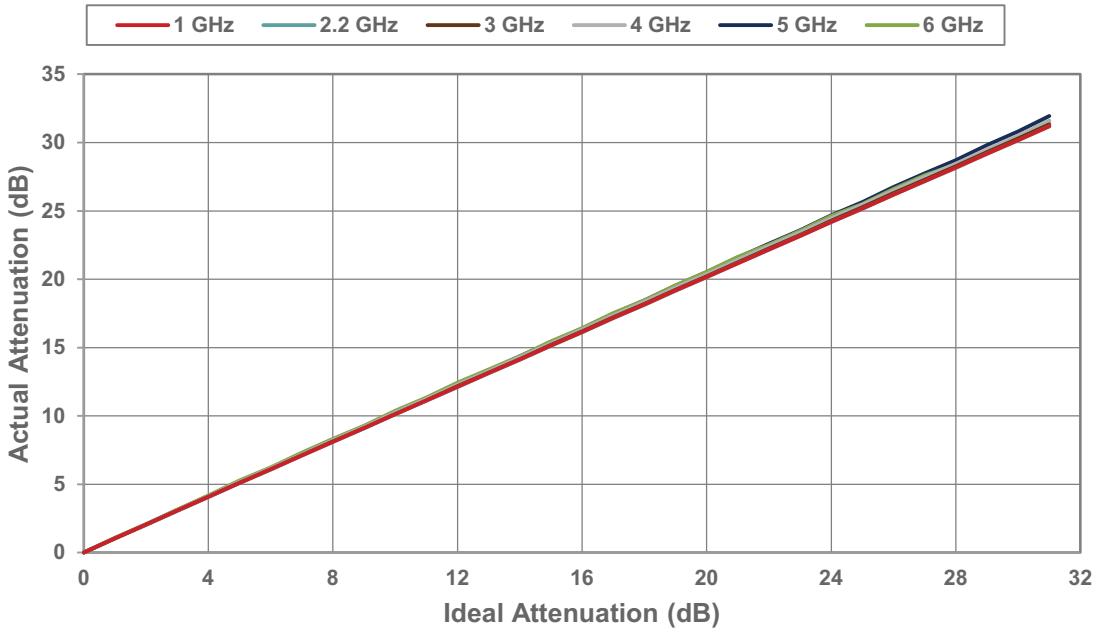


Figure 29 • *1 dB Major State Bit Error vs Attenuation Setting*

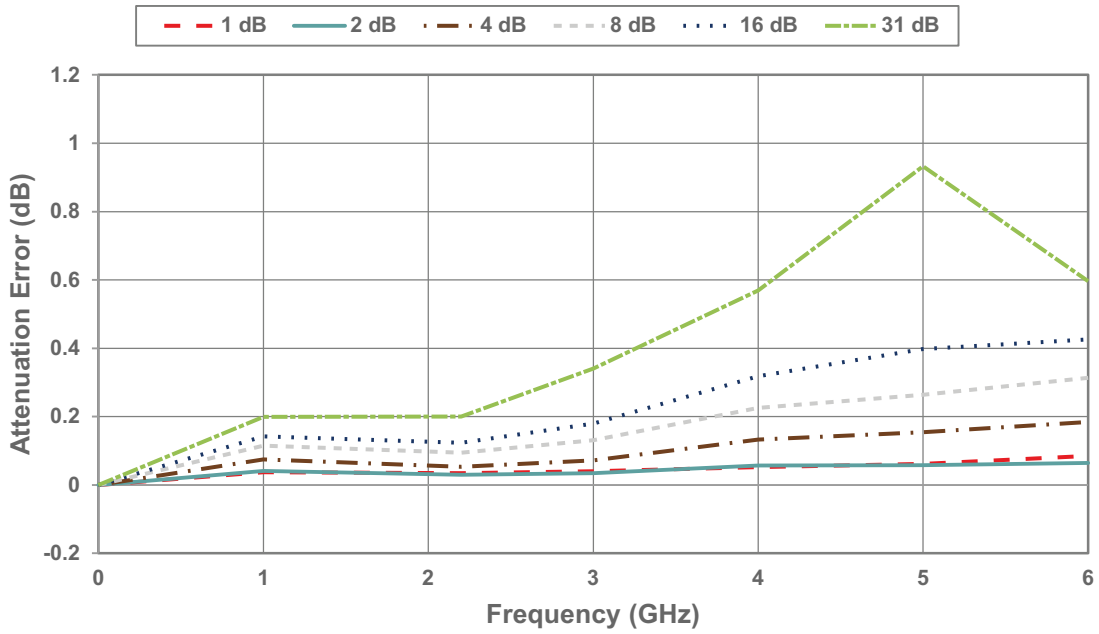


Figure 30 • *1 dB Attenuation Error vs Frequency*

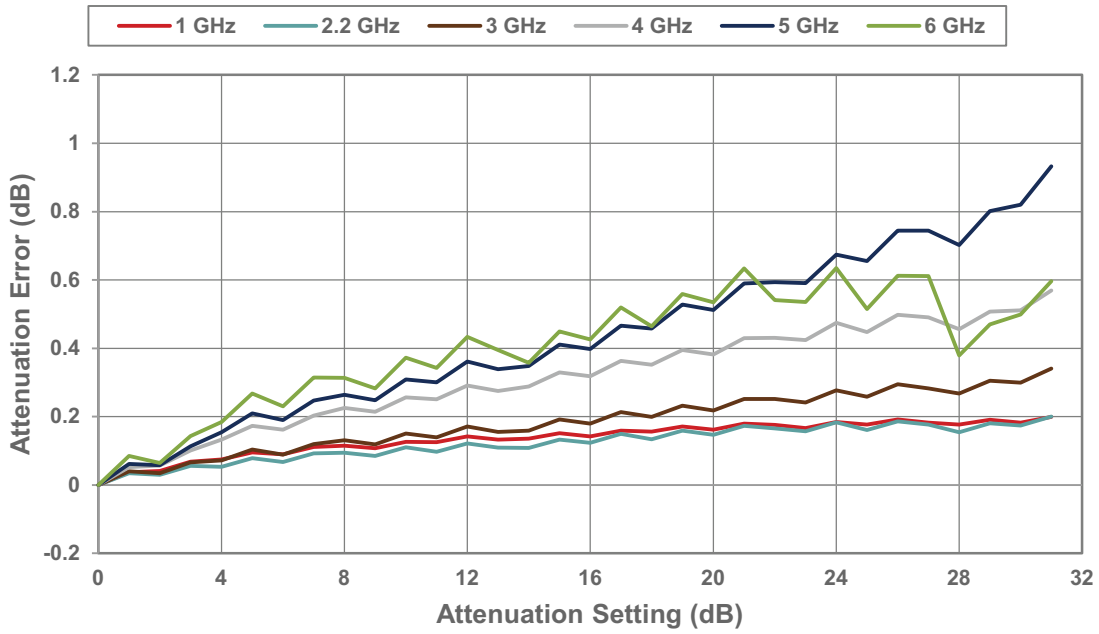


Figure 31 • *Attenuation Transient (15.75–16 dB), Typical Switching Time = 275 ns*

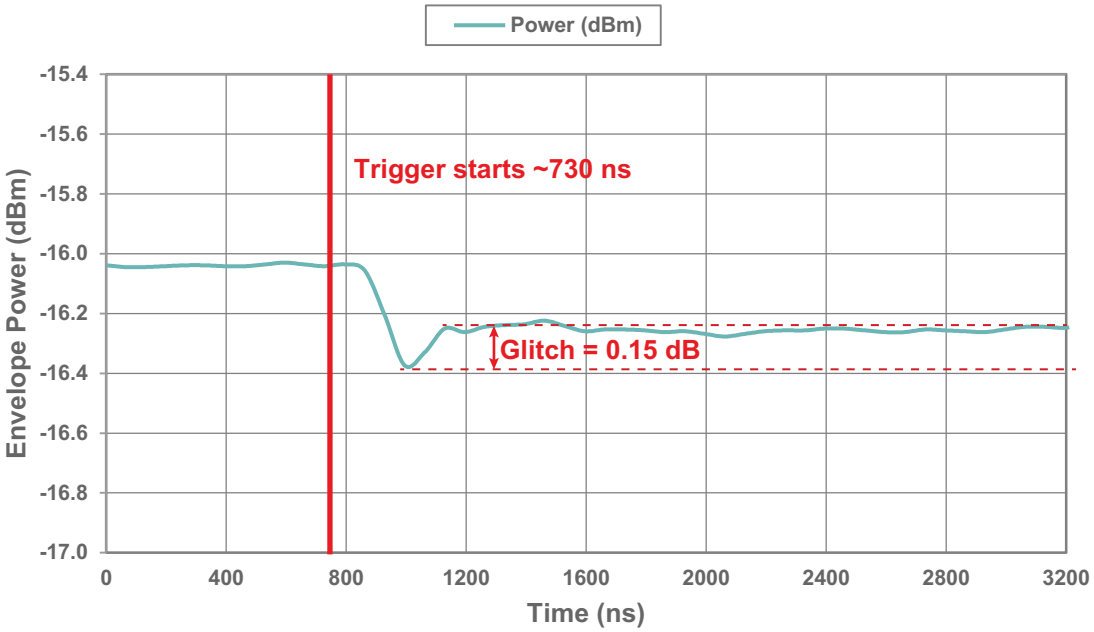
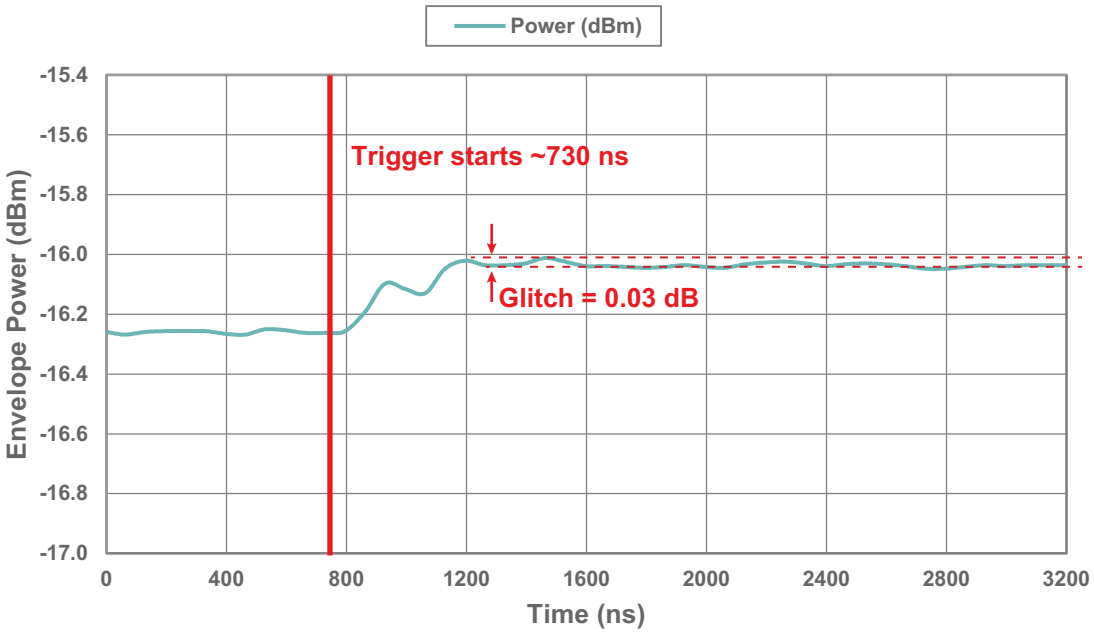


Figure 32 • *Attenuation Transient (16–15.75 dB), Typical Switching Time = 275 ns*



Evaluation Kit

The digital step attenuator evaluation board (EVB) was designed to ease customer evaluation of the PE43712 digital step attenuator. The PE43712 EVB supports Direct Parallel, Latched Parallel and Serial modes.

Evaluation Kit Setup

Connect the EVB with the USB dongle board and USB cable as shown in **Figure 33**.

Direct Parallel Programming Procedure

Direct Parallel programming is suitable for manual operation without software programming. For manual Direct Parallel programming, position the Parallel/Serial (P/S) select switch to the Parallel position. The LE switch must be switched to HIGH position. Switches D0–D6 are SP3T switches that enable the user to manually program the parallel bits. When D0–D6 are toggled to the HIGH position, logic high is presented to the parallel input. When toggled to the LOW position, logic low is presented to the parallel input. Setting LE and D0–D6 to the EXT position presents as OPEN, which is set for software programming of Latched Parallel and Serial modes. **Table 4** depicts the Parallel truth table.

Latched Parallel Programming Procedure

For automated Latched Parallel programming, connect the USB dongle board and cable that is provided with the evaluation kit (EVK) from the USB port of the PC to the J5 header of the PE43712 EVB, and set the LE and D0–D6 SP3T switches to the EXT position. Position the Parallel/Serial (P/S) select switch to the Parallel position. The evaluation software is written to operate the DSA in Parallel mode. Ensure that the software GUI is set to Latched Parallel mode. Use the software GUI to enable the desired attenuation state. The software GUI automatically programs the DSA each time an attenuation state is enabled.

Serial Addressable Programming Procedure

For automated Serial programming, connect the USB dongle board and cable that is provided with the EVK from the USB port of the PC to the J5 header of the PE43712 EVB, and set the LE and D0–D6 SP3T switches to the EXT position. Position the Parallel/Serial (P/S) select switch to the Serial position. Prior to programming, the user must define an address setting using the HDR2 header pin. Jump the middle column of pins on the HDR2 header (A0–A2) to the left column of pins to set logic LOW, or jump the middle row of pins to the right column of pins to set logic HIGH. If the HDR2 pins are left open, then 000 becomes the default address. The software GUI is written to operate the DSA in Serial mode. Use the software GUI to enable each setting to the desired attenuation state. The software GUI automatically programs the DSA each time an attenuation state is enabled.

Figure 33 • ***Evaluation Kit for PE43712***

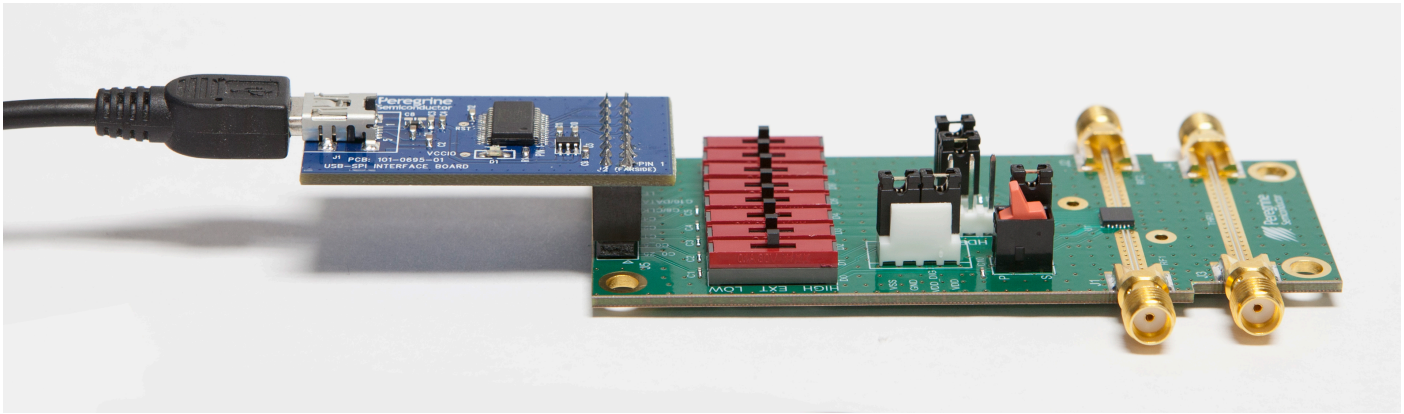
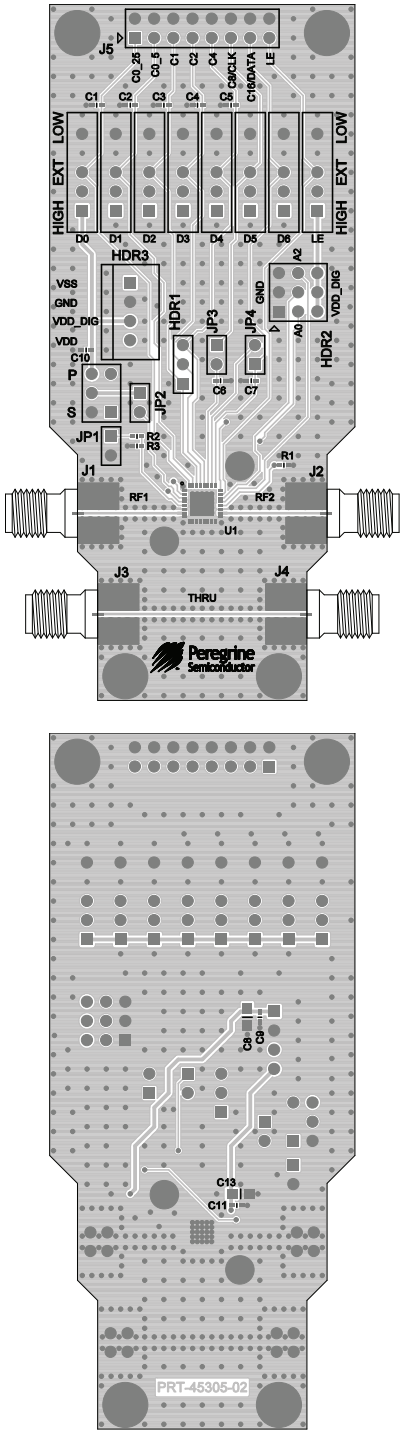


Figure 34 • *Evaluation Kit Layout for PE43712*



Pin Information

This section provides pinout information for the PE43712. **Figure 35** shows the pin map of this device for the available package. **Table 10** provides a description for each pin.

Figure 35 • *Pin Configuration (Top View)*

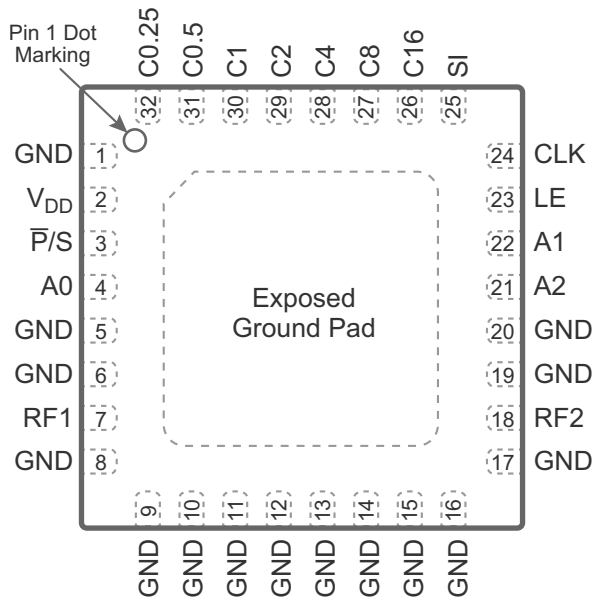


Table 10 • *Pin Descriptions for PE43712*

Pin No.	Pin Name	Description
1, 5, 6, 8–17, 19, 20	GND	Ground
2	V_{DD}	Supply voltage
3	$\overline{P}$/S	Serial/Parallel mode select
4	A0	Address bit A0 connection
7	RF1(1)	RF1 port (RF input)
18	RF2(1)	RF2 port (RF output)
21	A2	Address bit A2 connection
22	A1	Address bit A1 connection
23	LE	Serial interface Latch Enable input
24	CLK	Serial interface Clock input
25	SI	Serial interface Data input
26	C16 (D6)(2)	Parallel control bit, 16 dB
27	C8 (D5)(2)	Parallel control bit, 8 dB
28	C4 (D4)(2)	Parallel control bit, 4 dB
29	C2 (D3)(2)	Parallel control bit, 2 dB
30	C1 (D2)(2)	Parallel control bit, 1 dB
31	C0.5 (D1)(2)	Parallel control bit, 0.5 dB
32	C0.25 (D0)(2)	Parallel control bit, 0.25 dB
Pad	GND	Exposed pad: ground for proper operation

Notes:
1) RF pins 7 and 18 must be at 0 VDC. The RF pins do not require DC blocking capacitors for proper operation if the 0 VDC requirement is met.
2) Ground C0.25, C0.5, C1, C2, C4, C8 and C16 if not in use.

Packaging Information

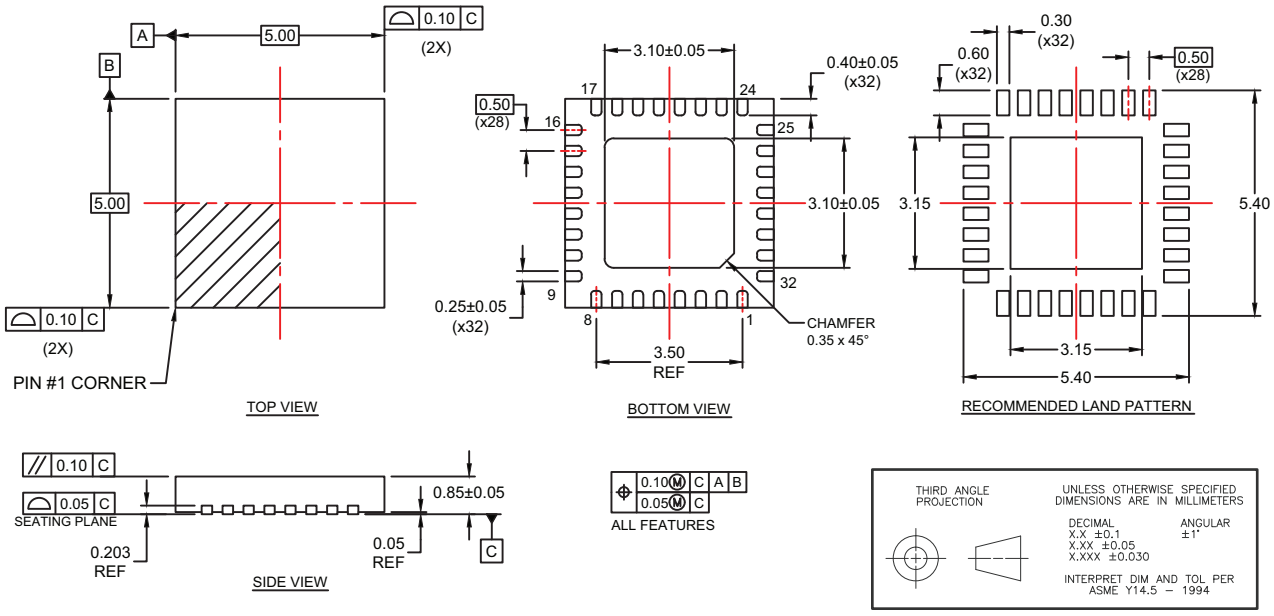
This section provides packaging data including the moisture sensitivity level, package drawing, package marking and tape-and-reel information.

Moisture Sensitivity Level

The moisture sensitivity level rating for the PE43712 in the 32-lead 5 × 5 mm QFN package is MSL1.

Package Drawing

Figure 36 • ***Package Mechanical Drawing for 32-lead 5 × 5 × 0.85 mm QFN***



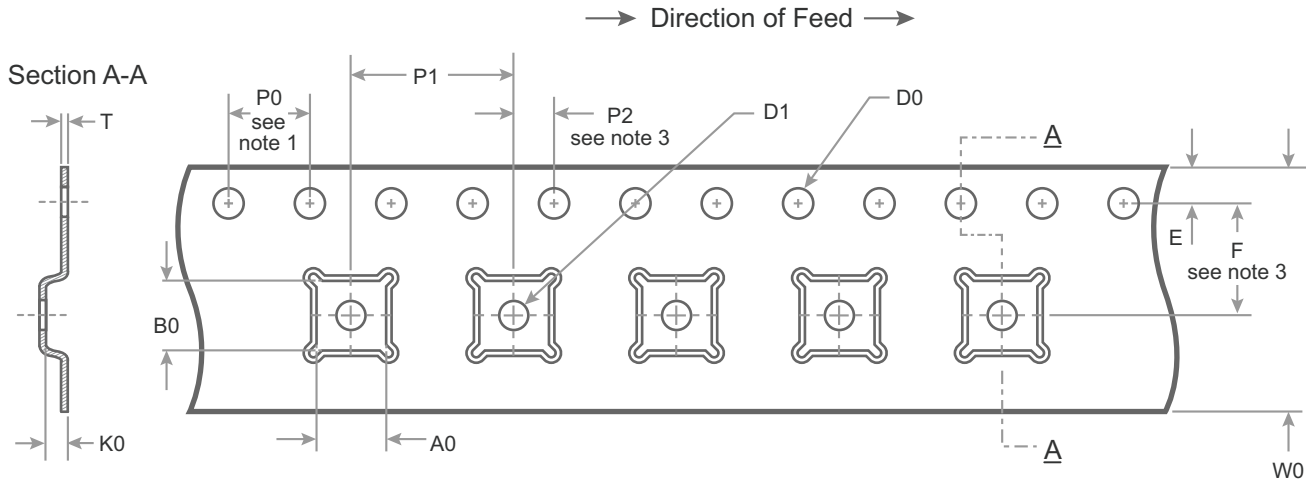
Top-Marking Specification

Figure 37 • ***Package Marking Specifications for PE43712***

● = Pin 1 indicator
YY = Last two digits of assembly year
WW = Assembly work week
ZZZZZZZ = Assembly lot code (maximum seven characters)

Tape and Reel Specification

Figure 38 • *Tape and Reel Specifications for 32-lead 5 × 5 × 0.85 mm QFN*

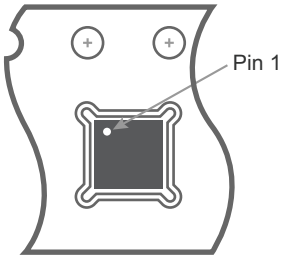


A0	5.25
B0	5.25
K0	1.10
D0	1.50 + 0.1/ -0.0
D1	1.5 min
E	1.75 ± 0.10
F	5.50 ± 0.05
P0	4.00
P1	8.00
P2	2.00 ± 0.05
T	0.30 ± 0.05
W0	12.00 ± 0.30

Notes:

1. 10 Sprocket hole pitch cumulative tolerance ±0.2
2. Camber in compliance with EIA 481
3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole

Dimensions are in millimeters unless otherwise specified



Device Orientation in Tape