PE46120

Document Category: Product Specification

Monolithic Phase & Amplitude Controller, 1.8–2.2 GHz

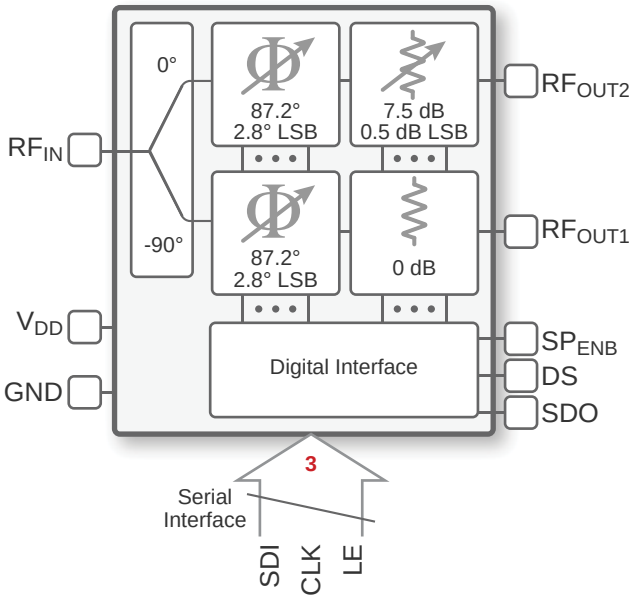
Features

- 90° phase splitter
- 5-bit digital phase shifter, 87.2° range, 2.8° resolution
- 4-bit digital step attenuator, 7.5 dB range, 0.5 dB resolution
- High power handling and linearity
  - P0.1dB of +35 dBm
  - Input IP3 of +60 dBm
- Packaging – 32-lead 6 × 6 × 0.85 mm QFN

Applications

- Wireless infrastructure
  - Macro cells
  - Small cells (micro, pico)
  - Distributed antenna systems (DAS)
- Precision phase shifter
- Dual polarization antenna alignment
- Analog linearization techniques

Figure 1 • *PE46120 Block Diagram*



Product Description

The PE46120 is a HaRP™ technology-enhanced monolithic phase and amplitude controller (MPAC) designed for precise phase and amplitude control of two independent RF paths. It optimizes system performance while reducing manufacturing costs of transmitters that use symmetric or asymmetric power amplifier designs to efficiently process signals with large peak-to-average ratios.

This monolithic RFIC integrates a 90° RF splitter, digital phase shifters and a digital step attenuator along with a low voltage CMOS serial interface. It can cover a phase range of 87.2° in 2.8° steps and an attenuation range of 7.5 dB in 0.5 dB steps, while providing excellent phase and amplitude accuracy from 1.8–2.2 GHz.

The PE46120 also features exceptional linearity, high output port-to-port isolation and extremely low power consumption relative to competing module solutions. It is offered in a 32-lead 6 × 6 × 0.85 mm QFN package.

The PE46120 is manufactured on Peregrine's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS. Peregrine's HaRP™ technology enhancements deliver high linearity and excellent harmonics performance.

Absolute Maximum Ratings

Exceeding absolute maximum ratings listed in**Table 1** may cause permanent damage. Operation should be restricted to the limits in **Table 2**. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

ESD Precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in **Table 1**.

Latch-up Immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1 • *Absolute Maximum Ratings for PE46120*

Parameter/Condition	Min	Max	Unit
Supply voltage, V_{DD}	–0.3	5.5	V
Digital input voltage	–0.3	3.6	V
Maximum input power		35	dBm
Storage temperature range	–65	+150	°C
ESD voltage HBM[1] All pins RF pins to GND		 500 1000	 V V
ESD voltage CDM, all pins[2]		1000	V

Notes:
1) Human body model (MIL-STD 883 Method 3015.7).
2) Charged device model (JEDEC JESD22-C101).

Recommended Operating Conditions

Table 2 lists the recommending operating condition for PE46120. Devices should not be operated outside the recommended operating conditions listed below.

Table 2 • *Recommended Operating Condition for PE46120*

Parameter	Min	Typ	Max	Unit
Supply voltage, V_{DD}[1]	2.3		5.5	V
Supply current		350	500	µA
Digital input high	1.17		3.6	V
Digital input low	0		0.6	V
Digital input leakage		10	20	µA
RF input power, CW			29	dBm
RF input power, pulsed[2]			32	dBm
Operating temperature range	–40	+25	+105	°C

Notes:
1) Product performance does not vary over V_{DD}.
2) Pulsed, 5% duty cycle of 4620 µs period.

Electrical Specifications

Table 3 provides the PE46120 key electrical specifications at +25 °C, V_{DD} = 2.3–5.5V, 50Ω, unless otherwise specified.

Table 3 • *PE46120 Electrical Specifications*

Parameter	Path	Condition	Min	Typ	Max	Unit
Operating frequency			1.8		2.2	GHz
Insertion loss	RF_{IN} to RF_{OUTX}	Reference phase and minimum attenuation state. Includes 3 dB from power divider.		6.9	7.4	dB
Input return loss	RF_{IN}	1.8–2.2 GHz		15		dB
Output return loss	RF_{OUT1} or RF_{OUT2}	1.8–2.2 GHz		15		dB
Isolation	RF_{OUT1} to RF_{OUT2}	1.8–2.2 GHz Reference phase and minimum attenuation state.	27.5	30		dB
Input 0.1dB compression point(1)	RF_{IN} to RF_{OUT1} or RF_{OUT2}	1.8–2.2 GHz		35		dBm
Input IP3	RF_{IN} to RF_{OUT1} or RF_{OUT2}	1.8–2.2 GHz		60		dBm
Switching time(2)		50% LE to 90% or 10% RF final value		980	1220	ns
Phase shift range	RF_{IN} to RF_{OUT1} or RF_{OUT2}			87.2		deg
Phase step				2.8		deg
Relative phase shift	RF_{OUT1} to RF_{OUT2}	Phase (RF_{OUT1})–Phase (RF_{OUT2}) [same state]		–90		deg
Attenuation range	RF_{IN} to RF_{OUT2}			7.5		dB
Attenuation step				0.5		dB

Notes:
1) The input 0.1dB compression point is a linearity figure of merit. Refer to **Table 2** for the operating RF input power (50Ω).
2) Worst case state transition. All bits changing.

Table 4 provides the PE46120 key electrical specifications at +105 °C, V_{DD} = 2.3–5.5V, 50Ω, unless otherwise specified.

Table 4 • *PE46120 Electrical Specifications*

Parameter	Path	Condition	Min	Typ	Max	Unit
Operating frequency			1.8		2.2	GHz
Insertion loss	RF_{IN} to RF_{OUTX}	Reference phase and minimum attenuation state. Includes 3 dB from power divider.		7.4	7.9	dB
Input return loss	RF_{IN}	1.8–2.2 GHz		15		dB
Output return loss	RF_{OUT1} or RF_{OUT2}	1.8–2.2 GHz		15		dB
Isolation	RF_{OUT1} to RF_{OUT2}	1.8–2.2 GHz Reference phase and minimum attenuation state.	27.5	30		dB
Input 0.1dB compression point(1)	RF_{IN} to RF_{OUT1} or RF_{OUT2}	1.8–2.2 GHz		35		dBm
Input IP3	RF_{IN} to RF_{OUT1} or RF_{OUT2}	1.8–2.2 GHz		60		dBm
Switching time(2)		50% LE to 90% or 10% RF final value		980	1220	ns
Phase shift range	RF_{IN} to RF_{OUT1} or RF_{OUT2}			87.2		deg
Phase step				2.8		deg
Relative phase shift	RF_{OUT1} to RF_{OUT2}	Phase (RF_{OUT1})–Phase (RF_{OUT2}) [same state]		–90		deg
Attenuation range	RF_{IN} to RF_{OUT2}			7.5		dB
Attenuation step				0.5		dB

Notes:
1) The input 0.1dB compression point is a linearity figure of merit. Refer to Table 2 for the operating RF input power (50Ω).
2) Worst case state transition. All bits changing.

Switching Frequency

The PE46120 has a maximum 25 kHz switching frequency.

The switching frequency is defined to be the rate at which the PE46120 can be continuously toggled across attenuation and phase states.

Control Logic

Table 5–Table 11 provide the control logic truth tables for the PE46120.

Table 5 • *Bit Descriptions*

C0	Channel register select
	C0 = L, channel RF_{OUT1} register select
	C0 = H, channel RF_{OUT2} register select
M0–M3	Attenuation setting per channel
P0–P4	Phase shift setting per channel
S0–S3	Spare bits

Table 6 • *14-Bit Word*

Q13	Q12	Q11	Q10	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
C0	S3	S2	M3	M2	M1	M0	P4	P3	P2	P1	P0	S1	S0
1	—	—	—	—	—	—	45	22.5	11.2	5.6	2.8	—	—
2	—	—	4	2	1	0.5	45	22.5	11.2	5.6	2.8	—	—

Table 7 • *Serial Truth Table – Phase Setting*

Q13	Q12	Q11	Q10	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Phase Shift Setting
C0	S3	S2	M3	M2	M1	M0	P4	P3	P2	P1	P0	S1	S0	
1/2	—	—	4	2	1	0.5	45	22.5	11.2	5.6	2.8	—	—	
X	X	X	X	X	X	X	L	L	L	L	L	X	X	Ref Phase
X	X	X	X	X	X	X	L	L	L	L	H	X	X	2.8 deg
X	X	X	X	X	X	X	L	L	L	H	L	X	X	5.6 deg
X	X	X	X	X	X	X	L	L	H	L	L	X	X	11.25 deg
X	X	X	X	X	X	X	L	H	L	L	L	X	X	22.5 deg
X	X	X	X	X	X	X	H	L	L	L	L	X	X	45 deg
X	X	X	X	X	X	X	H	H	H	H	H	X	X	87.2 deg

Table 8 • *Serial Truth Table – Attenuation Setting (RF_{OUT2})*

Q13	Q12	Q11	Q10	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Amplitude Setting
C0	S3	S2	M3	M2	M1	M0	P4	P3	P2	P1	P0	S1	S0	
1	—	—	—	—	—	—	45	22.5	11.2	5.6	2.8	—	—	
2	—	—	4	2	1	0.5	45	22.5	11.2	5.6	2.8	—	—	
H	X	X	L	L	L	L	X	X	X	X	X	X	X	Ref Insertion Loss
H	X	X	L	L	L	H	X	X	X	X	X	X	X	0.5 dB
H	X	X	L	L	H	L	X	X	X	X	X	X	X	1 dB
H	X	X	L	H	L	L	X	X	X	X	X	X	X	2 dB
H	X	X	H	L	L	L	X	X	X	X	X	X	X	4 dB
H	X	X	H	H	H	H	X	X	X	X	X	X	X	7.5 dB

Table 9 • *Default State Settings at Power Up (RF_{OUT1})*

DS Setting	Q13	Q12	Q11	Q10	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Default Setting at Power Up
	C0	S3	S2	M3	M2	M1	M0	P4	P3	P2	P1	P0	S1	S0	
	1/2	—	—	4	2	1	0.5	45	22.5	11.2	5.6	2.8	—	—	
DS = 0	—	—	—	—	—	—	—	L	L	L	L	L	—	—	0 dB 0 deg
DS = 1	—	—	—	—	—	—	—	H	L	L	L	L	—	—	0 dB 45 deg

Table 10 • *Default State Settings at Power Up (RF_{OUT2})*

DS Setting	Q13	Q12	Q11	Q10	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Default Setting at Power Up
	C0	S3	S2	M3	M2	M1	M0	P4	P3	P2	P1	P0	S1	S0	
	1/2	—	—	4	2	1	0.5	45	22.5	11.2	5.6	2.8	—	—	
DS = 0	—	—	—	L	L	L	L	L	L	L	L	L	—	—	0 dB 0 deg
DS = 1	—	—	—	H	H	H	H	H	L	L	L	L	—	—	7.5 dB 45 deg

Table 11 • *Serial Interface Timing Characteristics*[1]

Parameter/Condition	Min	Max	Unit
Serial clock frequency, F_{CLK}[2]	0.032	26	MHz
Serial clock period, T_{SCLK}	40		ns
Serial clock HIGH time, T_{SCLKH}	20		ns
Serial clock LOW time, T_{SCLKL}	20		ns
Serial data output propagation delay from CLK falling edge, T_{OV} (10 pF)		9	ns
Latch clock pulse width high, T_{LCLKH}	10		ns
Serial data input setup time from CLK rising edge, T_{SU}		5	ns
Serial data input hold time from CLK rising edge, T_H		2	ns
Serial data output hold time from CLK rising edge, T_{OH}	1.6		ns
Serial clock rising edge setup time to latch clock rising edge, T_{SETTLE}		27	ns
SDO drive strength[3]		15	pF

Notes:

1) V_{DD} = 2.3V–5.5V, –40 °C < T_A < +105 °C, unless otherwise specified.
2) Limited by test duration not static logic design. Synchronous to clock. Minimum clock frequency tested = 32 kHz.
3) SDO maximum capacitive load drive strength for F_{CLK} = 26 MHz with a 1.8V swing.

Programming Options

Serial Interface

The serial interface is a 14-bit serial-in shift register with two parallel-out channel registers RF_{OUT1} and RF_{OUT2} buffered by a transparent latch. The 14 bits are comprised of four bits defining the attenuation setting and five bits for the phase shift setting. Channel register RF_{OUT1} and RF_{OUT2} selection is determined by the value of the C0 bit contained as part of the 14-bit program word.

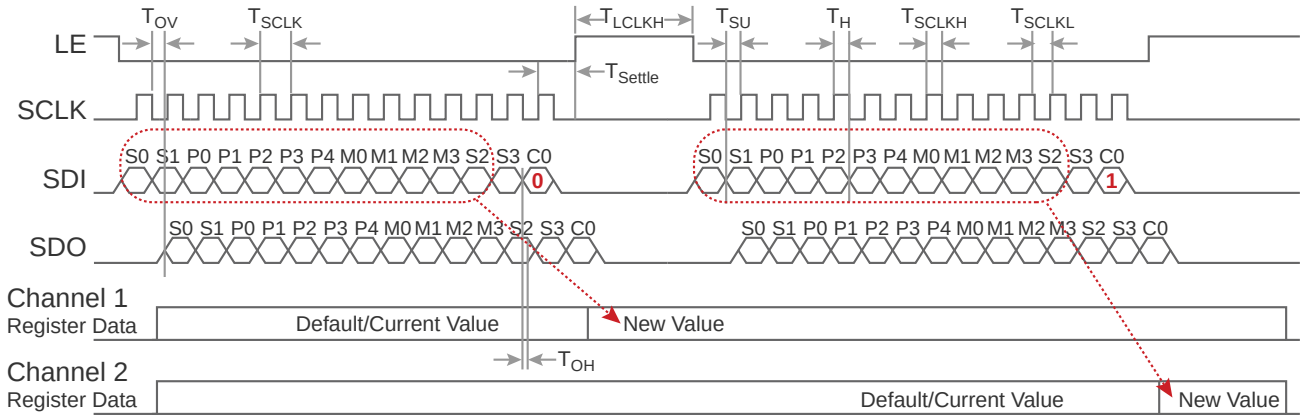
The serial interface is controlled using three CMOS compatible signals: serial data in (SDI), clock (CLK) and latch enable (LE). The SDI and CLK inputs allow data to be serially entered into the shift register. Serial data is clocked in starting with two spare bits first and then the phase setting LSB. The shift register must be loaded while LE is held LOW to prevent the internal channel register values from changing as data is entered. The LE input should then be toggled HIGH, latching the new data into the PE46120. SDO is a clock delayed reply of the user's input SDI command for functional confirmation.

Phase shift and attenuation setting truth tables are listed in **Table 7** and **Table 8**. The serial timing diagram is illustrated in **Figure 2** and associated AC characteristics are listed in **Table 11**.

Power-up Control Settings

The PE46120 will power up in one of two default states depending upon the setting of the default state (DS) pin, as defined in **Table 9** and **Table 10**. No specific signal sequencing is required for the default state to be set and active once V_{DD} is applied.

Figure 2 • ***Latched Buffered SDO Serial Interface***



Typical Performance Data

Figure 3–Figure 23 show the typical performance data at +25 °C and V_{DD} = 2.3–5.5V, 50Ω, unless otherwise specified

Figure 3 • ***Relative Phase Shift (RF_{OUT1}–RF_{OUT2})***

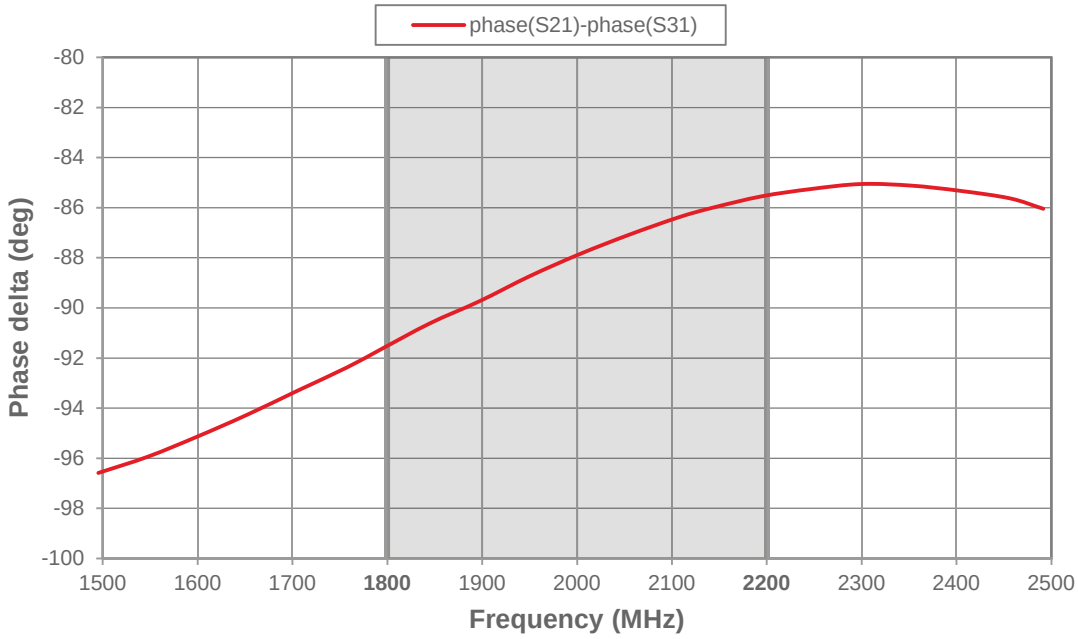


Figure 4 • *Insertion Loss (RF_{IN} to RF_{OUT1})*

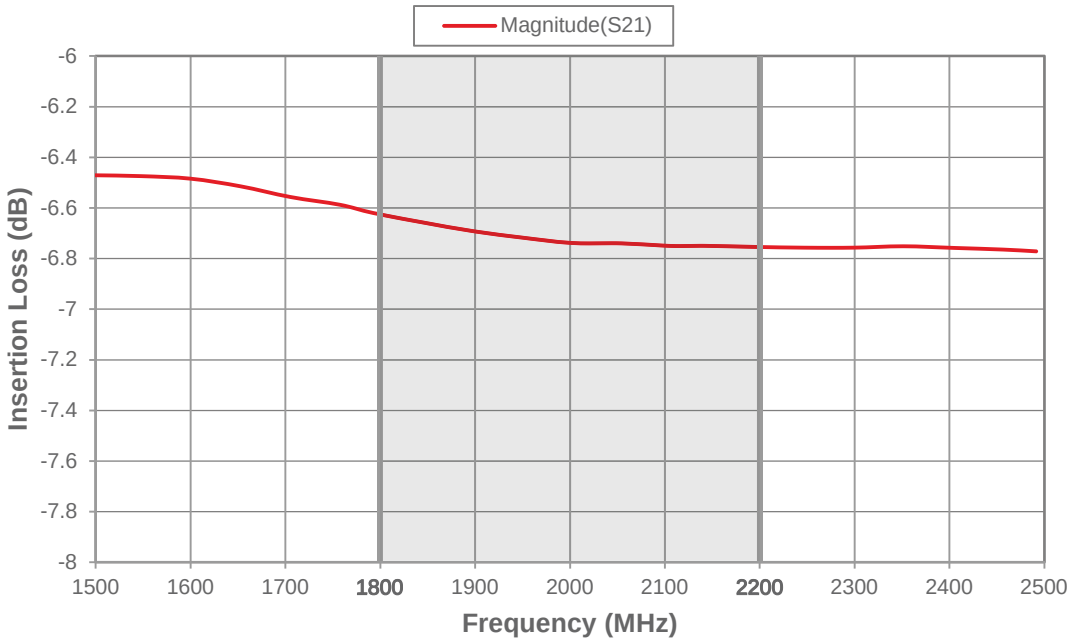


Figure 5 • *Insertion Loss (RF_{IN} to RF_{OUT2})*

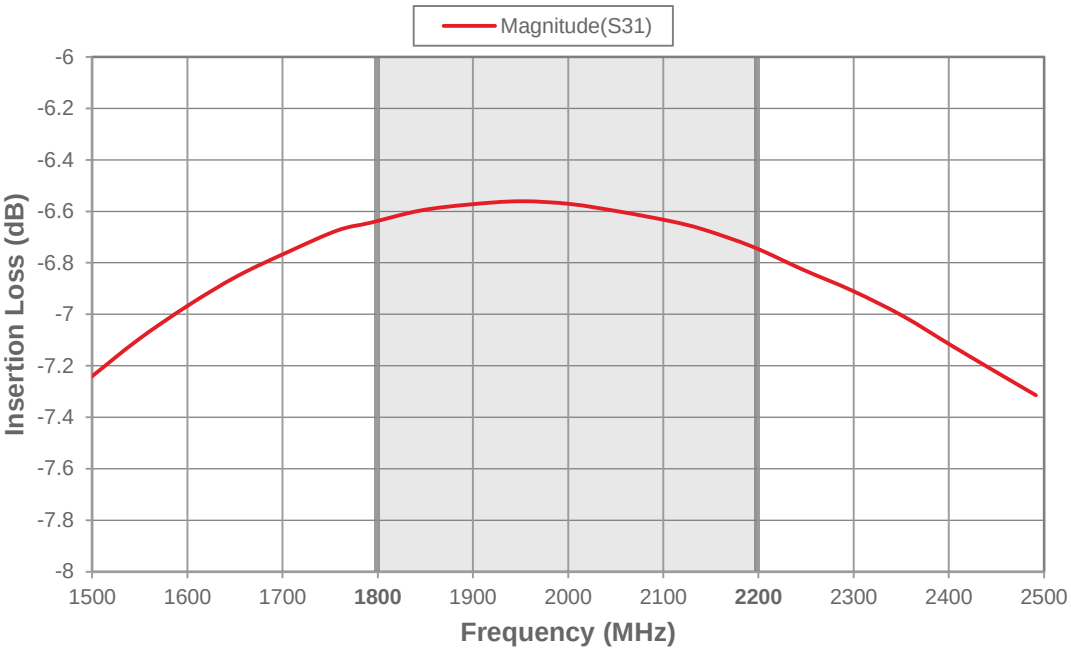


Figure 6 • *Insertion Loss RF_{IN} to RF_{OUT2} (All RF_{OUT2} Attenuation States)*

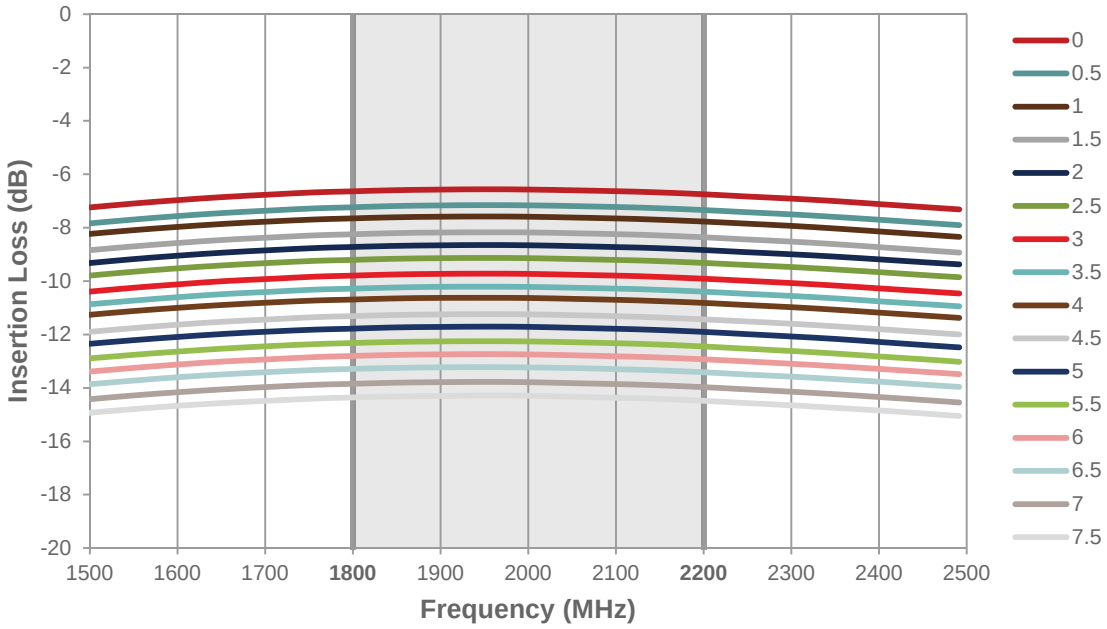


Figure 7 • *Relative Phase RF_{IN} to RF_{OUT1} (All RF_{OUT1} Phase States)*

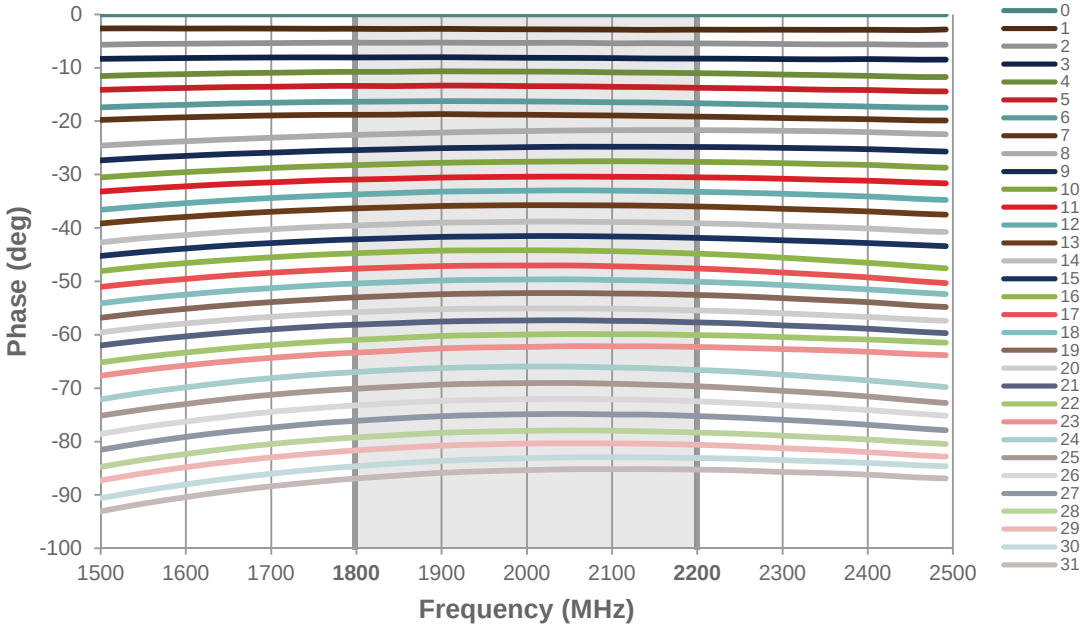


Figure 8 • *Relative Phase RF_{IN} to RF_{OUT2} (All RF_{OUT2} Phase States)*

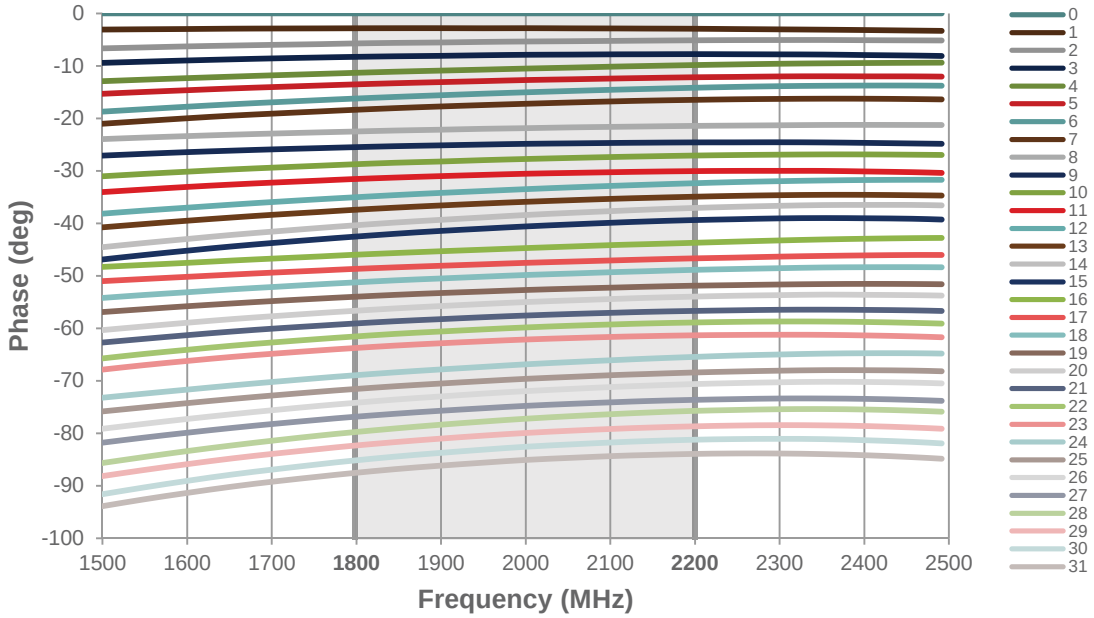


Figure 9 • *Input Return Loss (All States)*

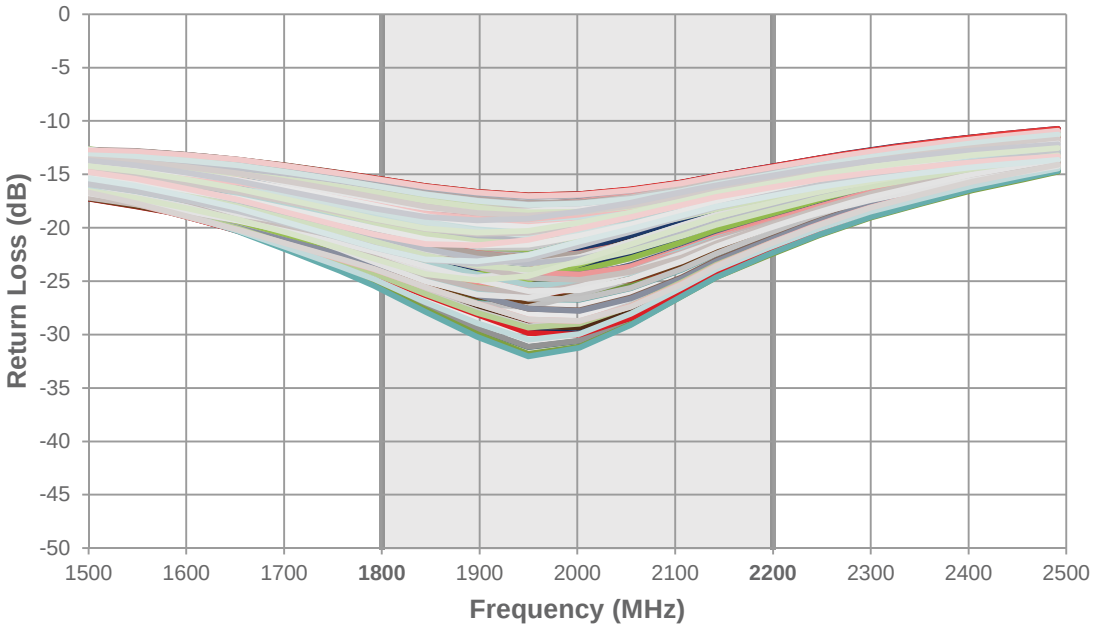


Figure 10 • *Output Return Loss RF_{OUT1} (All RF_{OUT1} Phase States)*

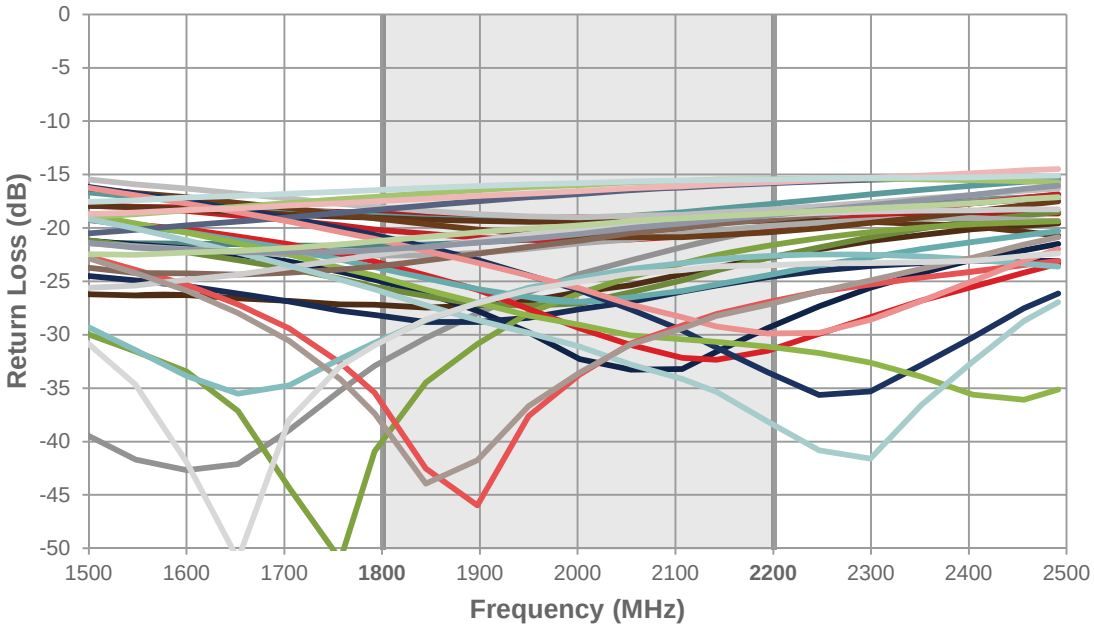


Figure 11 • *Output Return Loss RF_{OUT2} (All RF_{OUT2} States)*

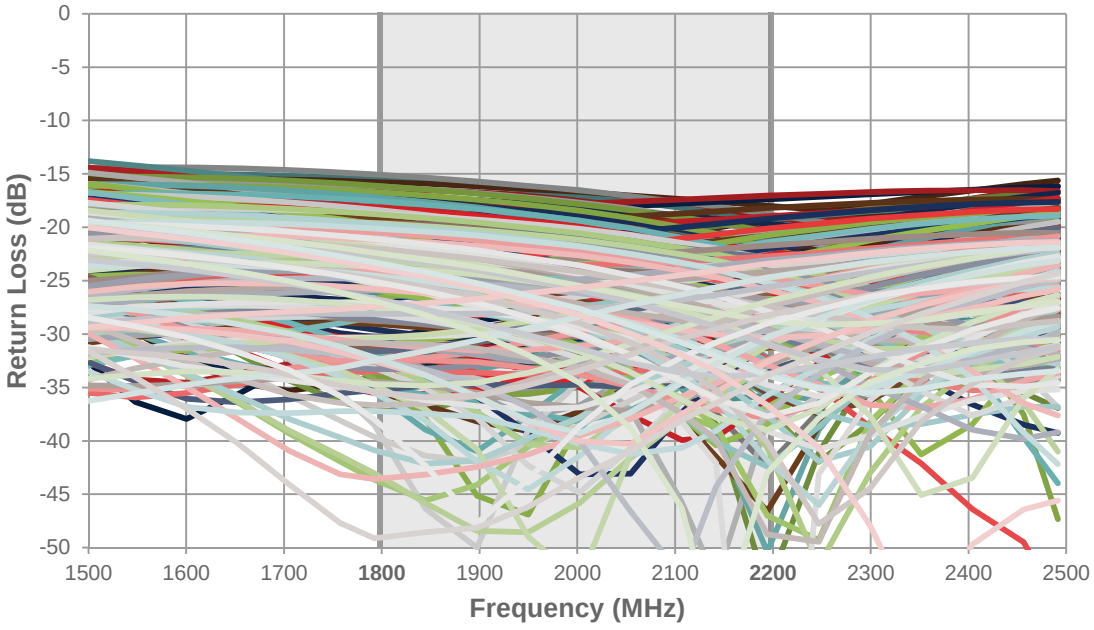


Figure 12 • *Isolation Output Ports (All States)*

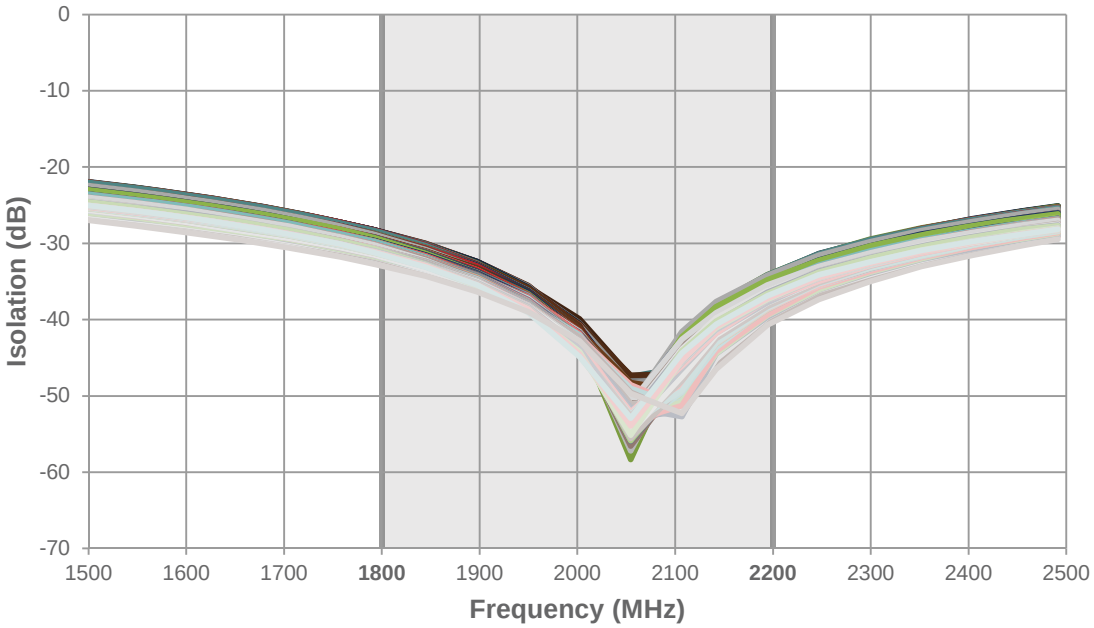


Figure 13 • *RF_{OUT1} Insertion Loss Variation Across All RF_{OUT2} States*

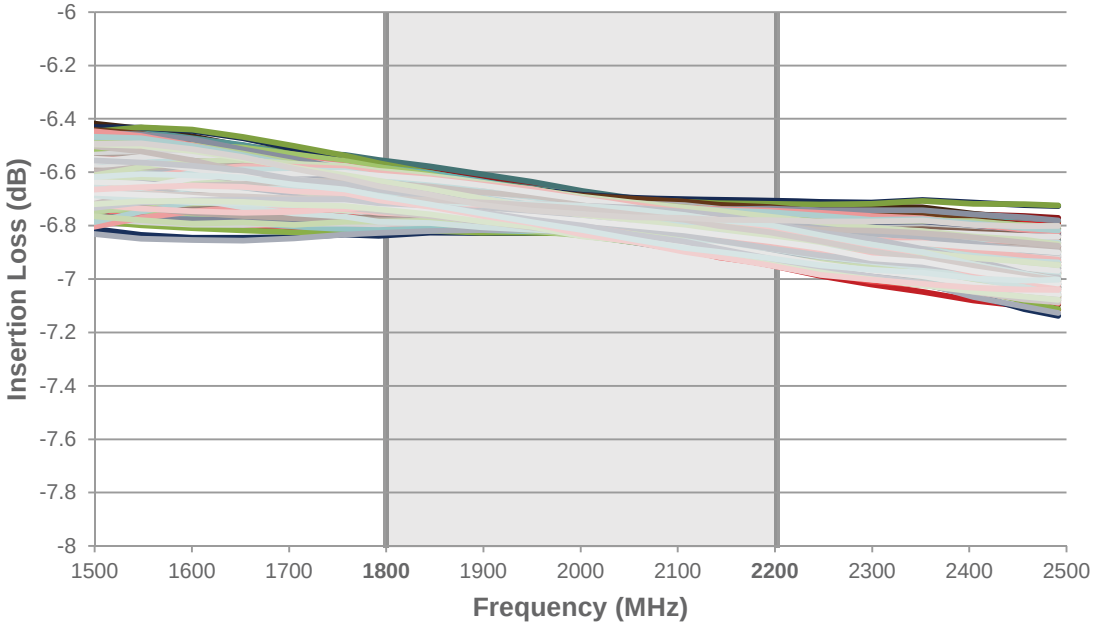


Figure 14 • *RF_{OUT1} Phase Variation Across All RF_{OUT2} Phase States*

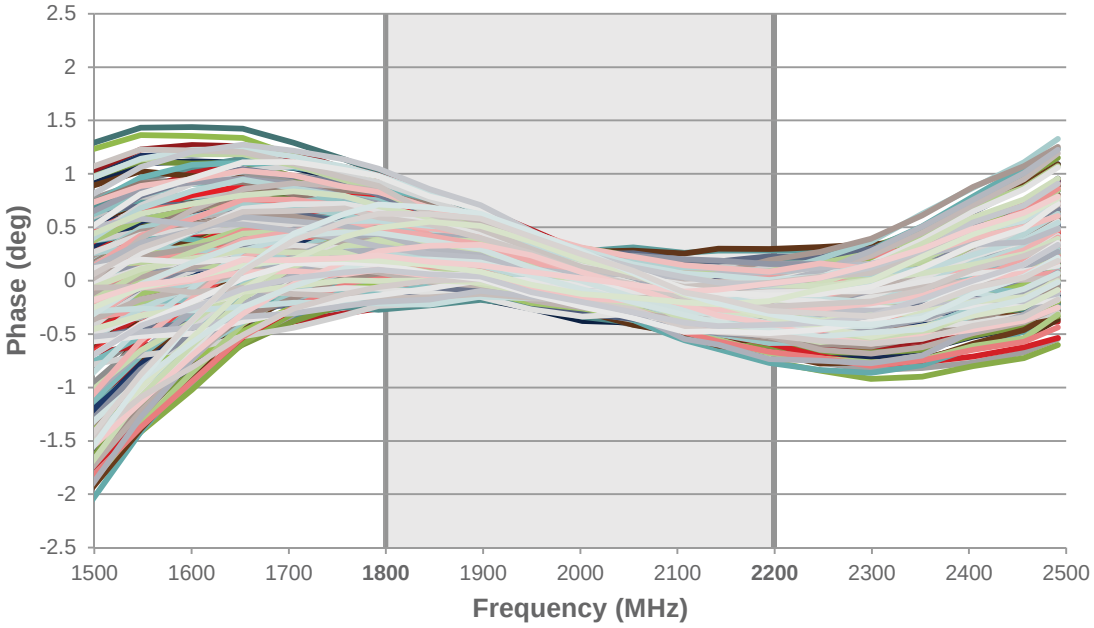


Figure 15 • *RF_{OUT1} Insertion Loss Variation Across RF_{OUT1} Phase State*

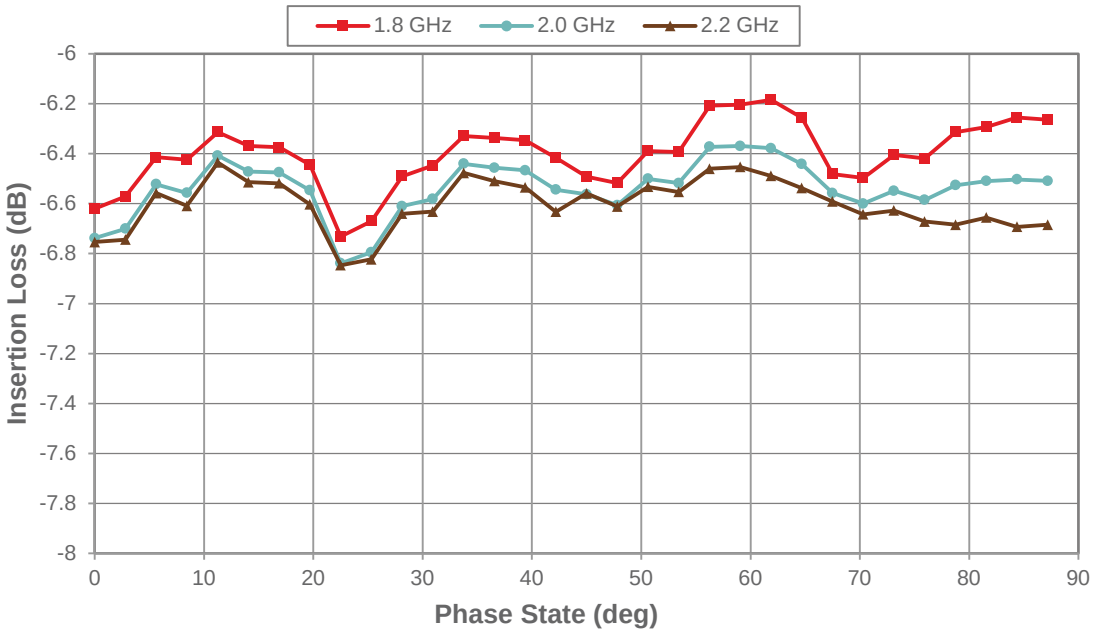


Figure 16 • *RF_{OUT2} Insertion Loss Variation Across RF_{OUT2} Phase State*

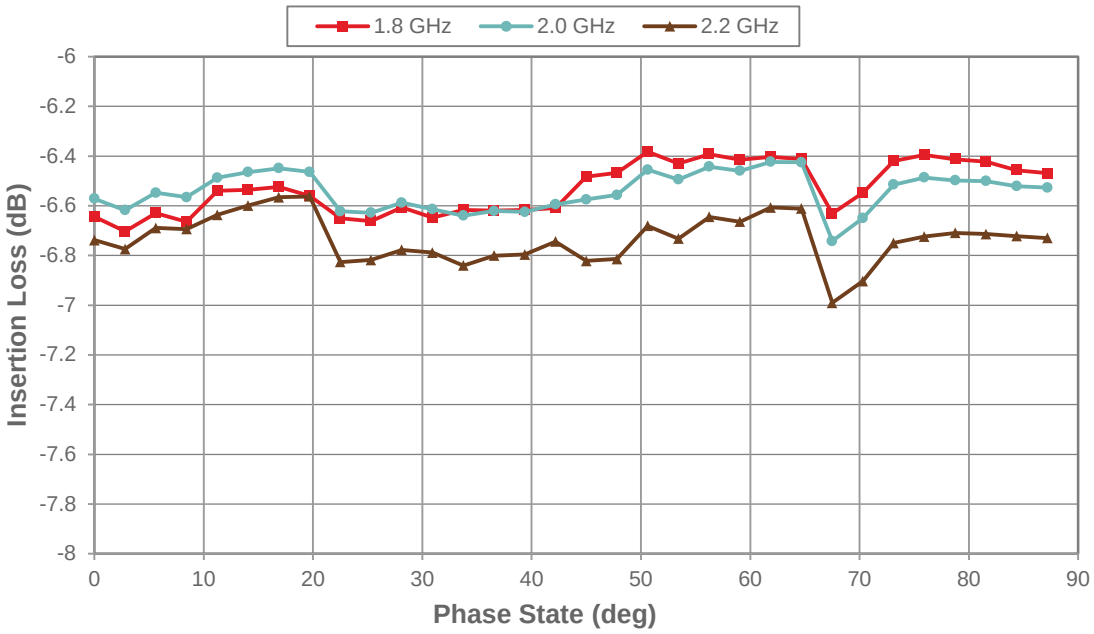
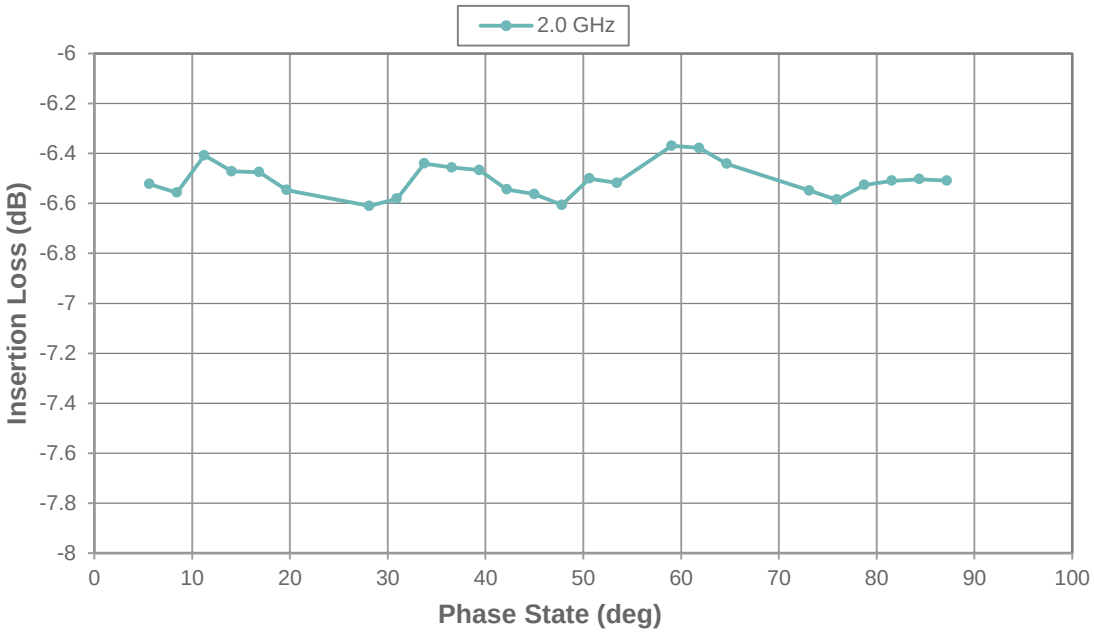
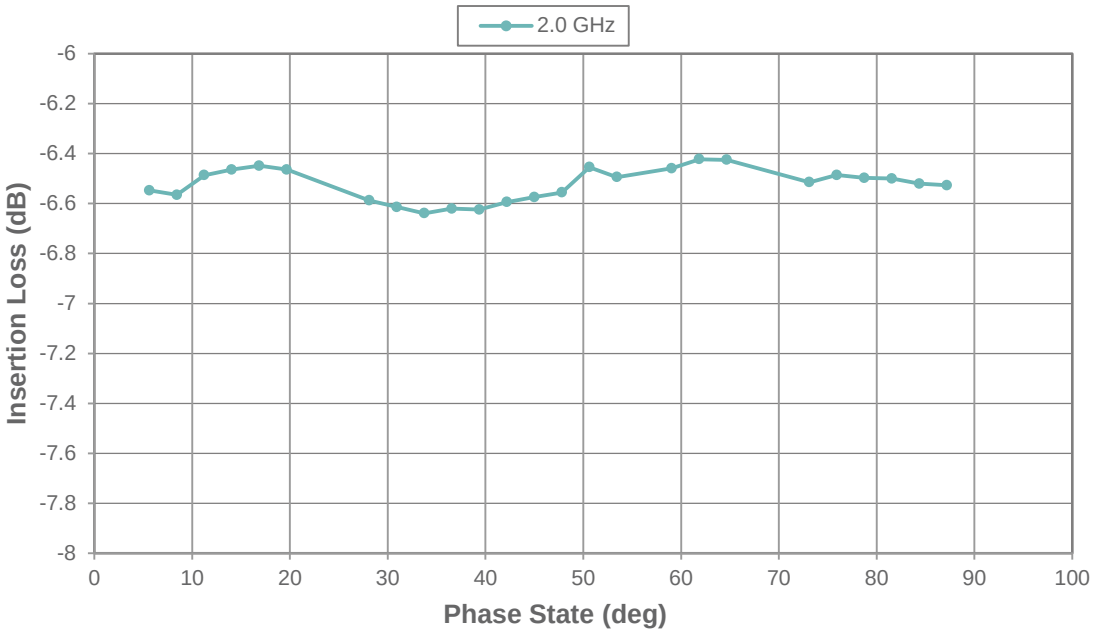


Figure 17 • *RF_{OUT1} Insertion Loss Variation Across Phase State*(*)



Note: * Across recommended RF_{OUT1} phase states for minimum insertion loss variation.

Figure 18 • *RF_{OUT2} Insertion Loss Variation Across Phase State*(*)



Note: * Across recommended RF_{OUT2} phase states for minimum insertion loss variation.

Figure 19 • *RF_{OUT2} Phase Variation Across RF_{OUT2} Attenuation State*

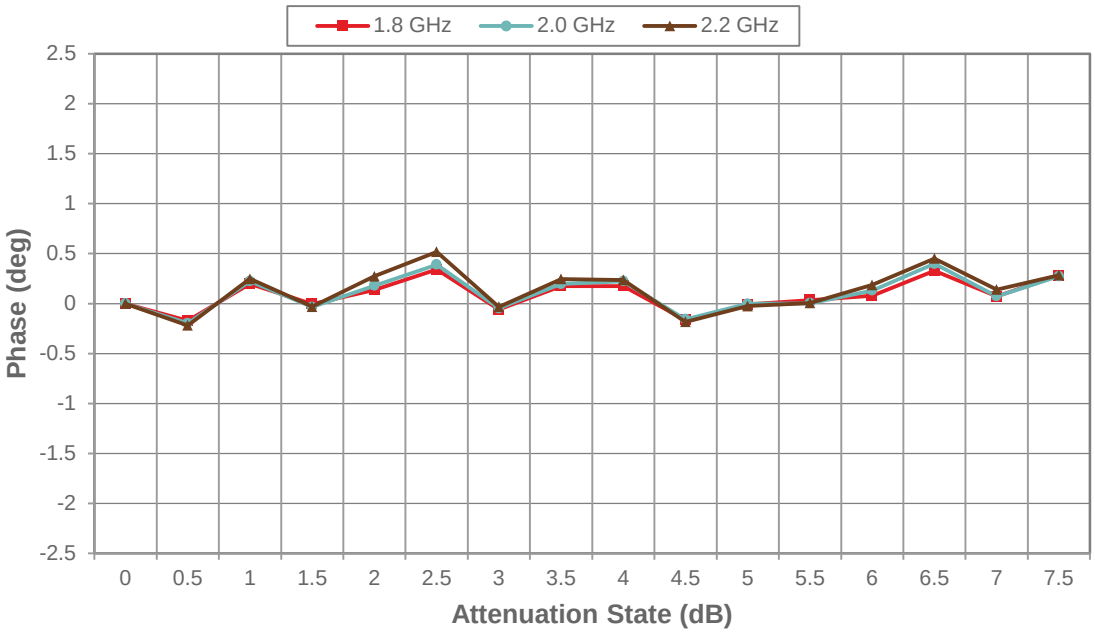


Figure 20 • *RF_{OUT2} Insertion Loss Across RF_{OUT2} Attenuation State vs V_{DD}, Frequency = 2 GHz*

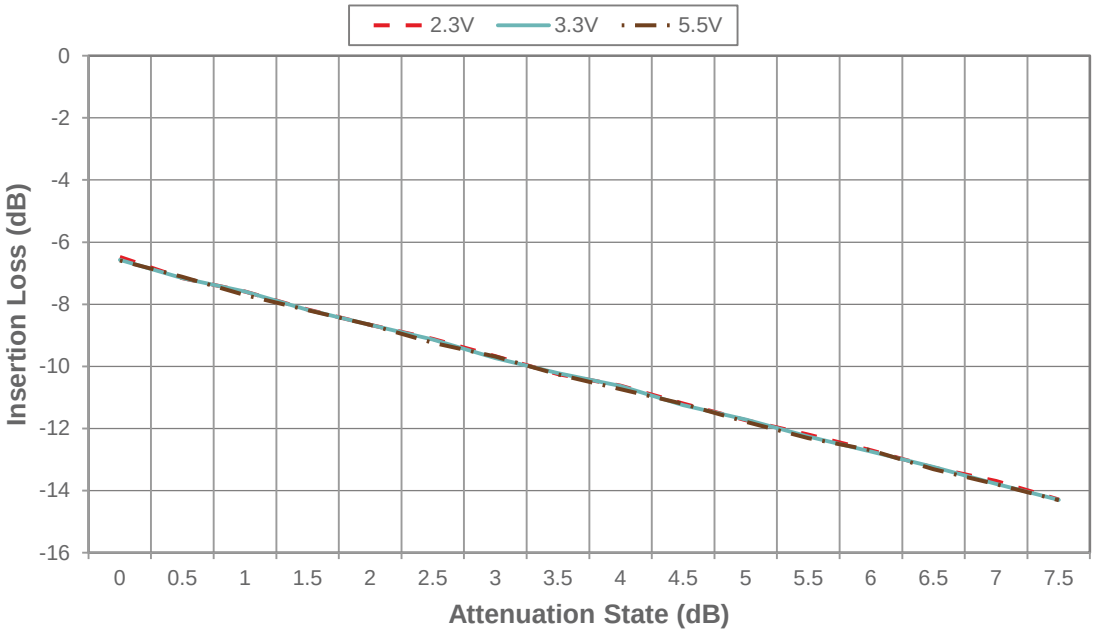


Figure 21 • *RF_{OUT2} Insertion Loss Across RF_{OUT2} Attenuation State vs Temperature, Frequency = 2 GHz*

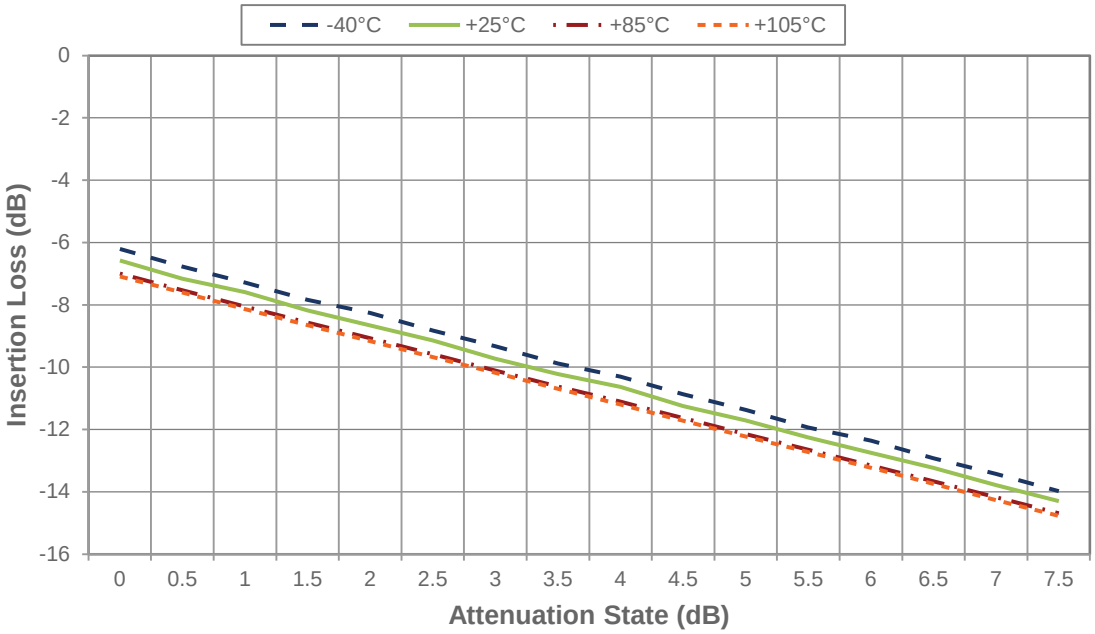


Figure 22 • *RF_{OUT2} Relative Phase Across RF_{OUT2} Phase State vs V_{DD}, Frequency = 2 GHz*

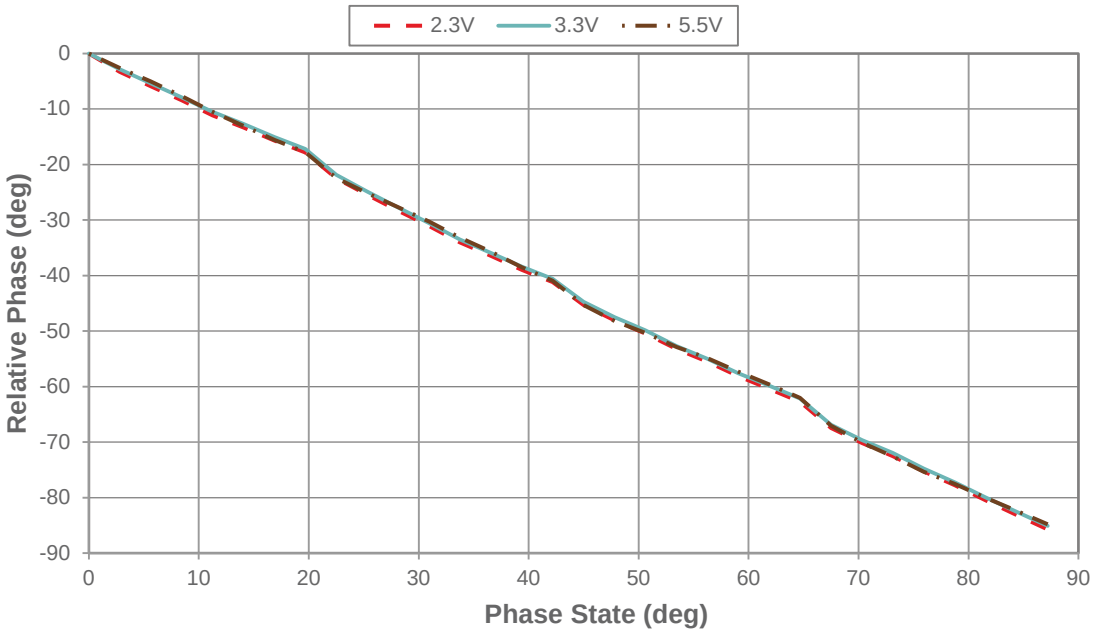
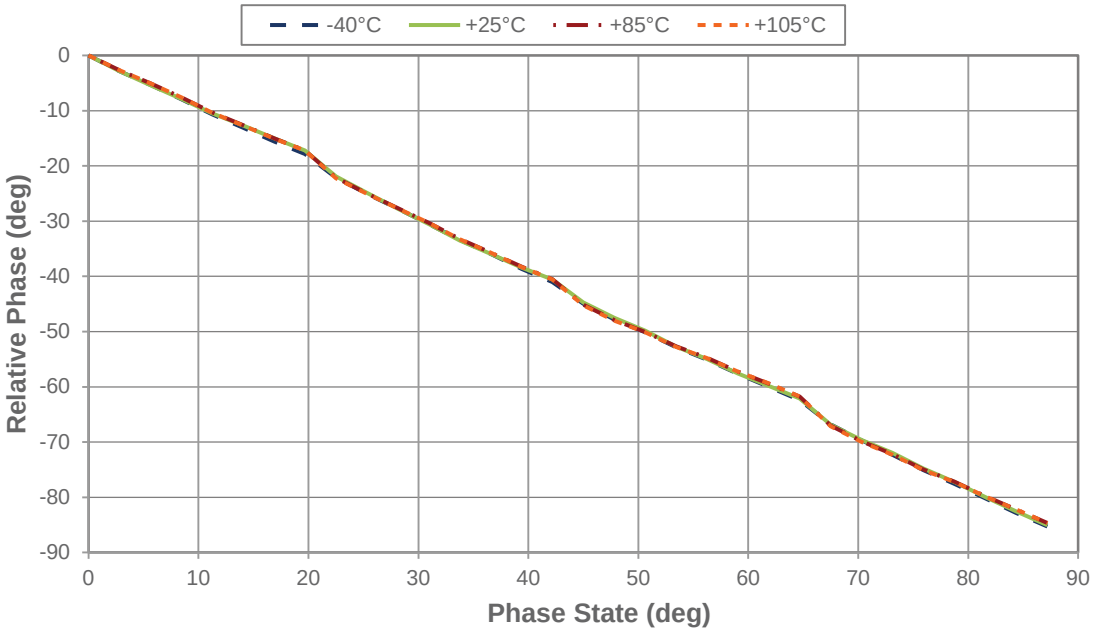


Figure 23 • *RF_{OUT2} Relative Phase Across RF_{OUT2} Phase State vs Temperature, Frequency = 2 GHz*



Pin Information

This section provides pinout information for the PE46120. **Figure 24** shows the pin map of this device for the available package. **Table 12** provides a description for each pin.

Figure 24 • *Pin Configuration (Top View)*

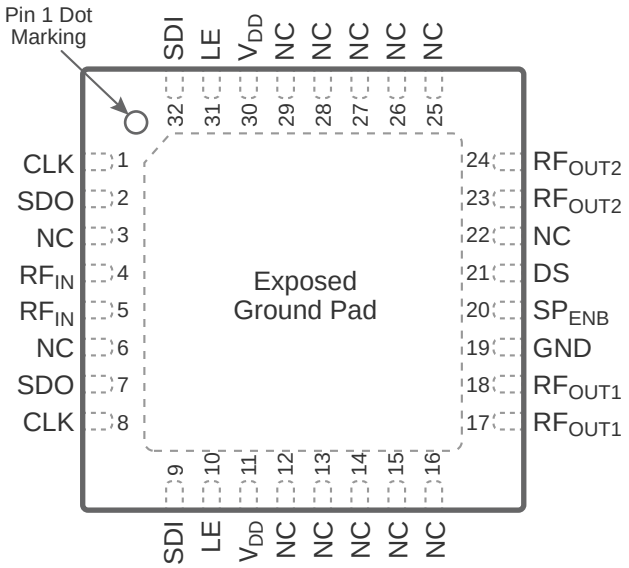


Table 12 • *Pin Descriptions for PE46120*

Pin No.	Pin Name	Description
1, 8	CLK(1)	Clock input
2, 7	SDO(2)	Serial data output
3, 6, 12–16, 22, 25–29	NC	No connect
4, 5	RF_{IN}(3)	RF input
9, 32	SDI(1)	Serial data input
10, 31	LE(1)	Latch enable
11, 30	V_{DD}(1)	Supply voltage
17, 18	RF_{OUT1}(3)	RF output 1
19	GND(4)	Ground
20	SP_{ENB}(5)(6)	Serial port enable
21	DS(6)	Default state at power up select
23, 24	RF_{OUT2}(3)	RF output 2
Pad	GND	Exposed pad: ground for proper operation

Notes:

1) Pins are internally connected, signal only needs to be applied to one of the pins. The alternate unused pin needs to be left floating.
2) SDOs are independently buffered outputs of the same signal.
3) RF pins 4, 5, 17 and 18 must be at 0 VDC. The RF pins do not require DC blocking capacitors for proper operation if the 0 VDC requirement is met.
4) Pin 19 must be grounded for proper function.
5) Must be active low for normal SPI operation. Logic high programs 0 dB attenuation setting and 0° phase setting. Setting back to logic low returns to the previously programmed state.
6) Pin has an internal 100 kΩ pull-up resistor.

Packaging Information

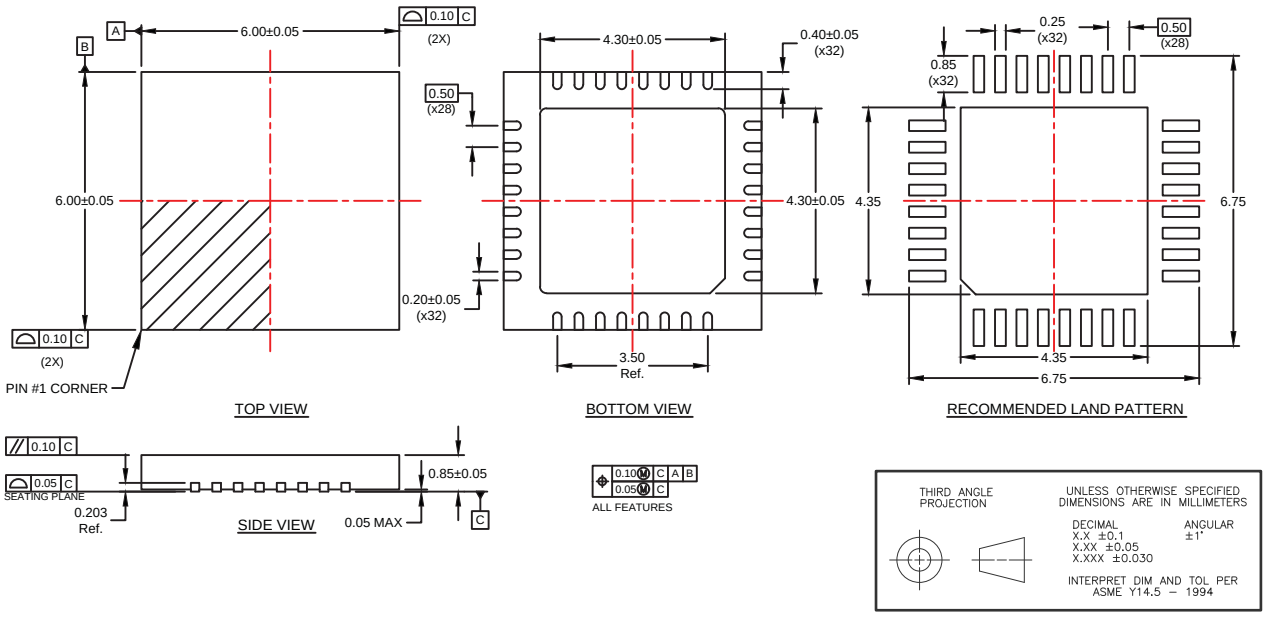
This section provides packaging data including the moisture sensitivity level, package drawing, package marking and tape-and-reel information.

Moisture Sensitivity Level

The moisture sensitivity level rating for the PE46120 in the 32-lead 6 × 6 × 0.85 mm QFN package is MSL1.

Package Drawing

Figure 25 • *Package Mechanical Drawing for 32-lead 6 × 6 × 0.85 mm QFN*



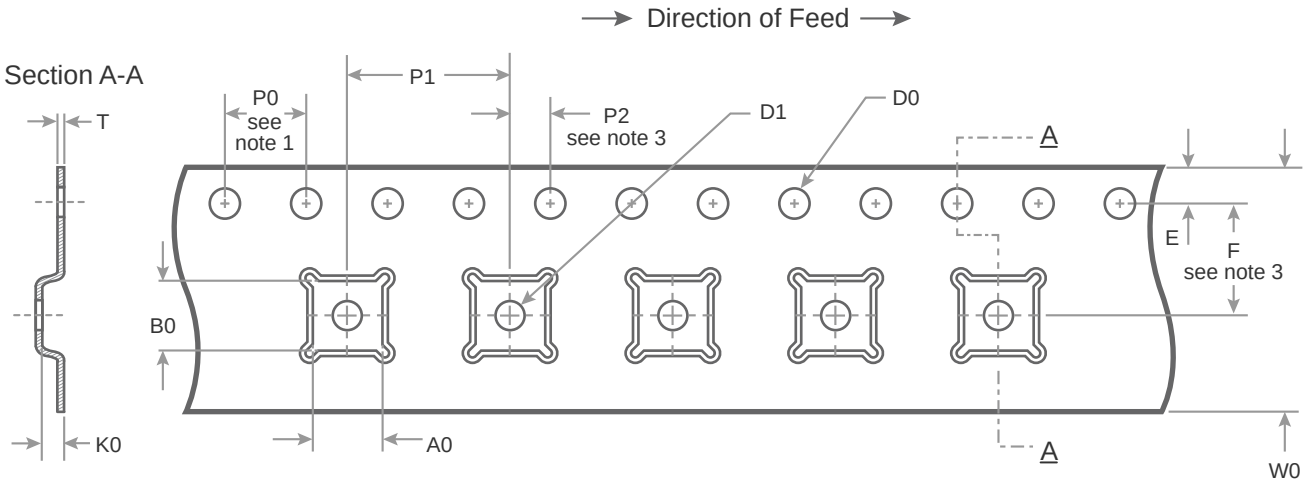
Top-Marking Specification

Figure 26 • *Package Marking Specifications for PE46120*

● = Pin 1 indicator
YY = Last two digits of assembly year
WW = Assembly work week
ZZZZZZZZ = Assembly lot code (maximum eight characters)

Tape and Reel Specification

Figure 27 • *Tape and Reel Specifications for 32-lead 6 × 6 × 0.85 mm QFN*

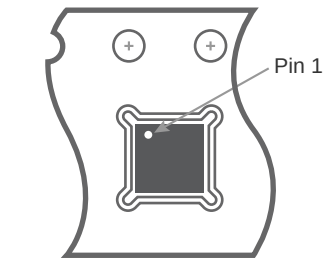


A0	6.30 ± 0.10
B0	6.30 ± 0.10
K0	1.10 ± 0.10
D0	1.50 + 0.1/ -0.0
D1	1.5 min
E	1.75 ± 0.10
F	7.50 ± 0.10
P0	4.00
P1	12.00 ± 0.10
P2	2.00 ± 0.10
T	0.30 ± 0.05
W0	16.00 ± 0.30

Notes:

1. 10 Sprocket hole pitch cumulative tolerance ±0.2
2. Camber in compliance with EIA 481
3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole

Dimensions are in millimeters unless otherwise specified



Device Orientation in Tape