



PESD42VS2UT

Double ESD protection diode array

24 January 2019

Product data sheet

1. General description

Unidirectional double ElectroStatic Discharge (ESD) protection diode in a SOT23 (TO-236AB) small Surface-Mounted Device (SMD) plastic package designed to protect up to two signal lines from the damage caused by ESD and other transients.

2. Features and benefits

- Unidirectional ESD protection of two lines
- High reverse standoff voltage: $V_{RWM} = 42\text{ V}$
- Low leakage current: $I_{RM} \leq 50\text{ nA}$
- ESD protection up to 23 kV
- AEC-Q101 qualified

3. Applications

- ESD protection for standard capacitance signals or supply lines

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per diode						
V_{RWM}	reverse standoff voltage	$T_{amb} = 25\text{ °C}$	-	-	42	V
I_{PPM}	rated peak pulse current	$t_p = 8/20\text{ }\mu\text{s}$	[1]	-	1.8	A
V_{CL}	clamping voltage	$I_{PPM} = 1.8\text{ A}$; $t_p = 8/20\text{ }\mu\text{s}$; $T_{amb} = 25\text{ °C}$	[2] [1]	80	95	V

[1] Device stressed with 8/20 μs exponential decay waveform according to IEC 61000-4-5.

[2] Measured from pin 1 or 2 to pin 3.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K1	cathode (diode 1)	<p>SOT23</p>	<p>006aaa154</p>
2	K2	cathode (diode 2)		
3	A	common anode		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD42VS2UT	SOT23	plastic, surface-mounted package; 3 terminals; 1.9 mm pitch; 2.9 mm x 1.3 mm x 1 mm body	SOT23

7. Marking

Table 4. Marking codes

Type number	Marking code
PESD42VS2UT	GK

8. Limiting values

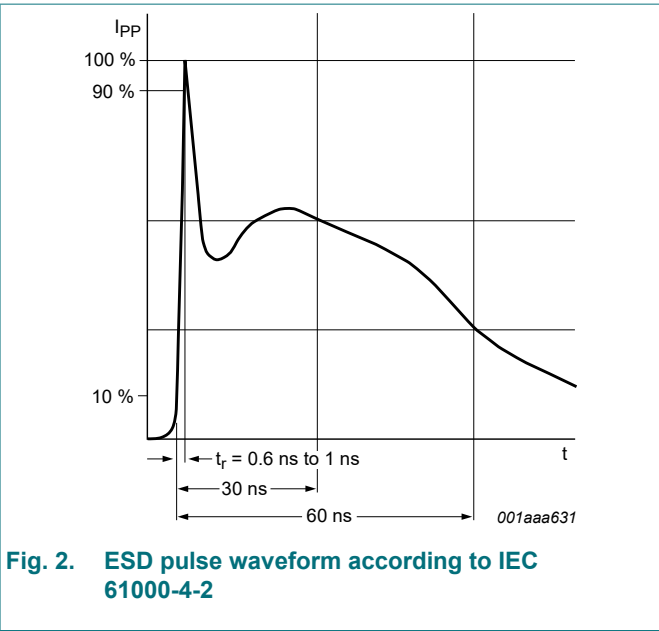
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per diode						
I_{PPM}	rated peak pulse current	$t_p = 8/20 \mu s$	[1]	-	1.8	A
Per device						
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C
ESD maximum ratings						
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 (contact discharge)	[2]	-	23	kV

[1] Device stressed with 8/20 μs exponential decay waveform according to IEC 61000-4-5.

[2] Device stressed with ten non-repetitive ESD pulses.



9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
Per diode							
V _{RWM}	reverse standoff voltage	T _{amb} = 25 °C	-	-	42	V	
V _{BR}	breakdown voltage	I _R = 2 mA; T _{amb} = 25 °C	46.1	47	47.9	V	
I _{RM}	reverse leakage current	V _{RWM} = 42 V; T _{amb} = 25 °C	-	1	50	nA	
C _d	diode capacitance	f = 1 MHz; V _R = 0 V; T _{amb} = 25 °C	[1]	17	20	pF	
V _{CL}	clamping voltage	I _{PP} = 1 A; t _p = 8/20 μs; T _{amb} = 25 °C	[1] [2]	-	60	-	V
		I _{PPM} = 1.8 A; t _p = 8/20 μs; T _{amb} = 25 °C	[1] [2]	-	80	95	V
		I _{PP} = 16 A; t _p = TLP; T _{amb} = 25 °C	[1] [3]	-	167	-	V

[1] Measured from pin 1 or 2 to pin 3.

[2] Device stressed with 8/20 μs exponential decay waveform according to IEC 61000-4-5.

[3] Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008.

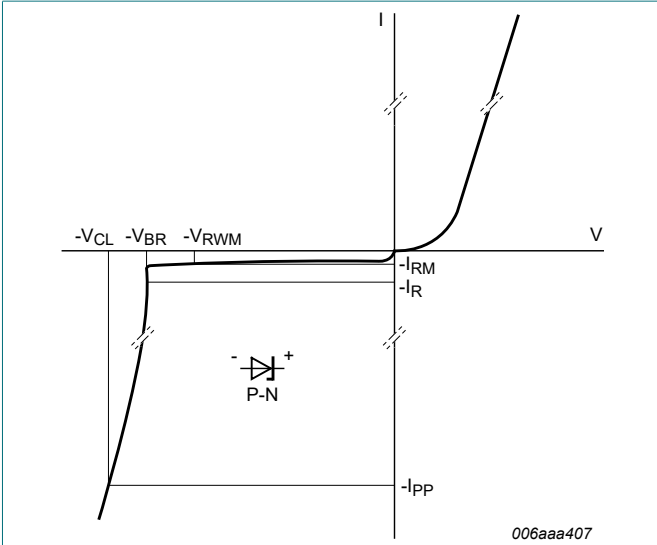


Fig. 3. V-I characteristics for a unidirectional ESD protection diode

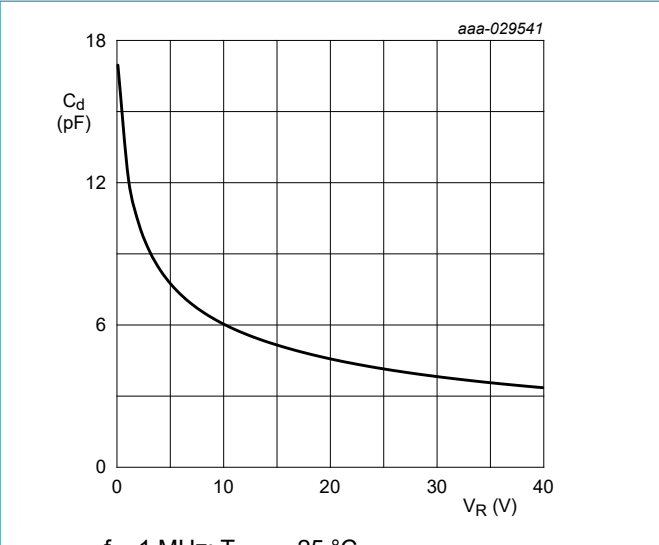


Fig. 4. Diode capacitance as a function of reverse voltage; typical values

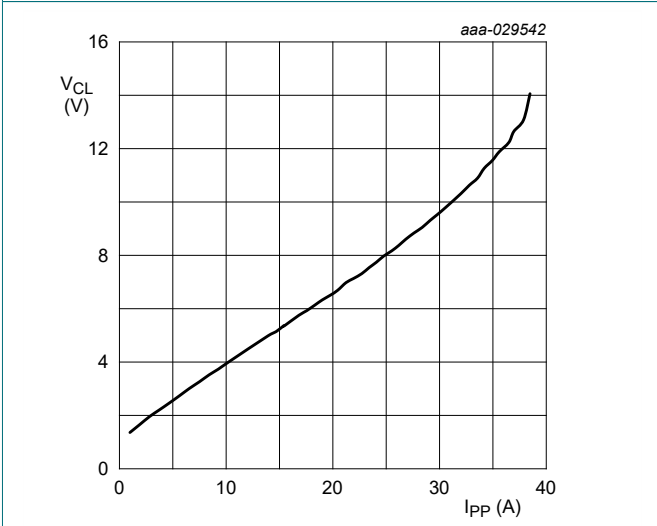


Fig. 5. Positive clamping voltage (8/20 μs pulse); typical values

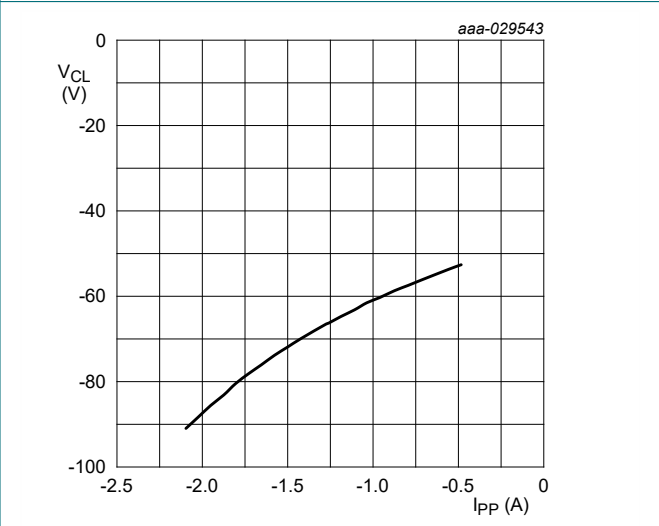


Fig. 6. Negative clamping voltage (8/20 μs pulse); typical values



Fig. 7. ESD clamping test setup and waveforms

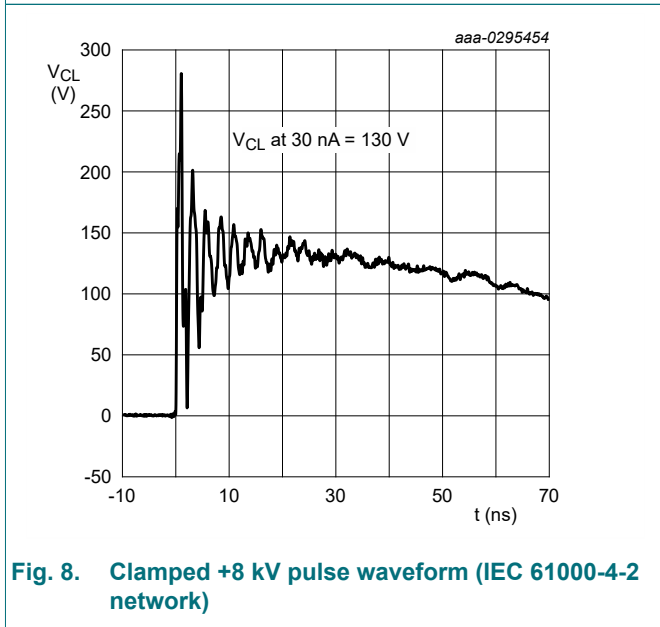


Fig. 8. Clamped +8 kV pulse waveform (IEC 61000-4-2 network)

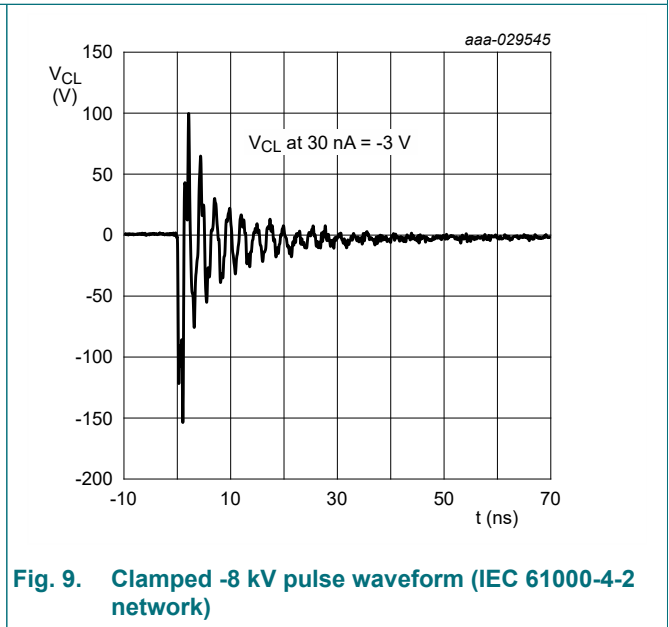


Fig. 9. Clamped -8 kV pulse waveform (IEC 61000-4-2 network)

10. Application information

The device is designed for the protection of up to two unidirectional data or signal lines from the damage caused by ESD and surge pulses. The devices may be used on lines where the signal polarities are either positive or negative with respect to ground.

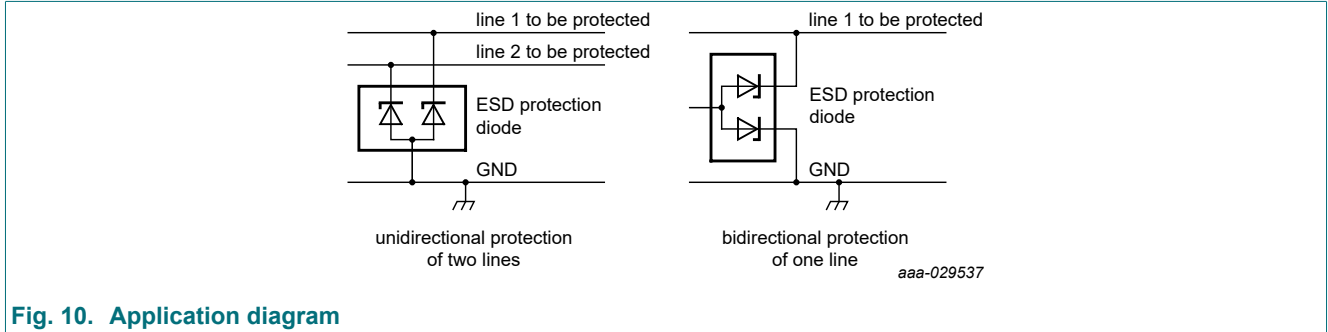


Fig. 10. Application diagram

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

11. Package outline

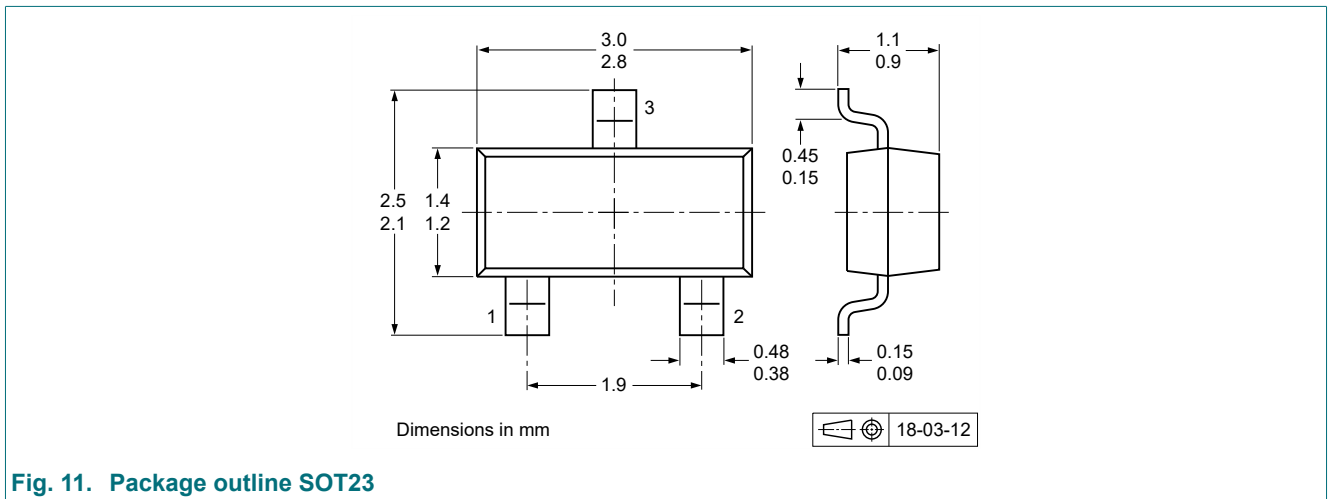


Fig. 11. Package outline SOT23

12. Soldering

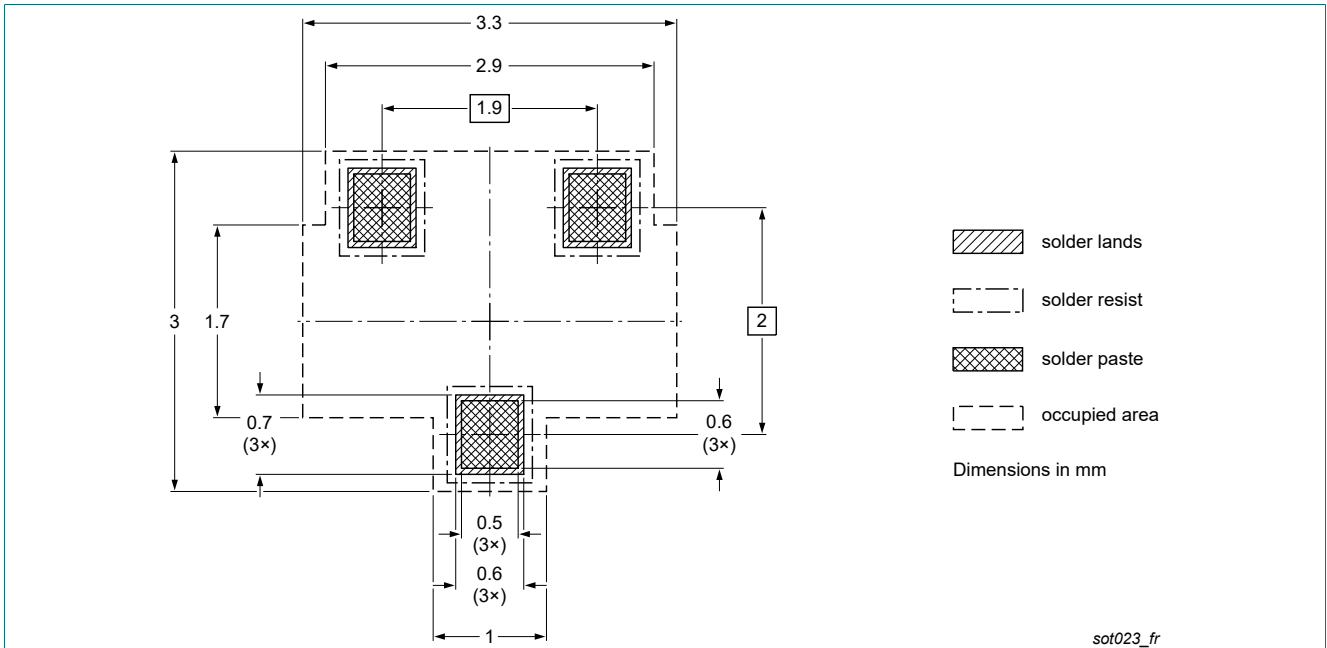


Fig. 12. Reflow soldering footprint for SOT23

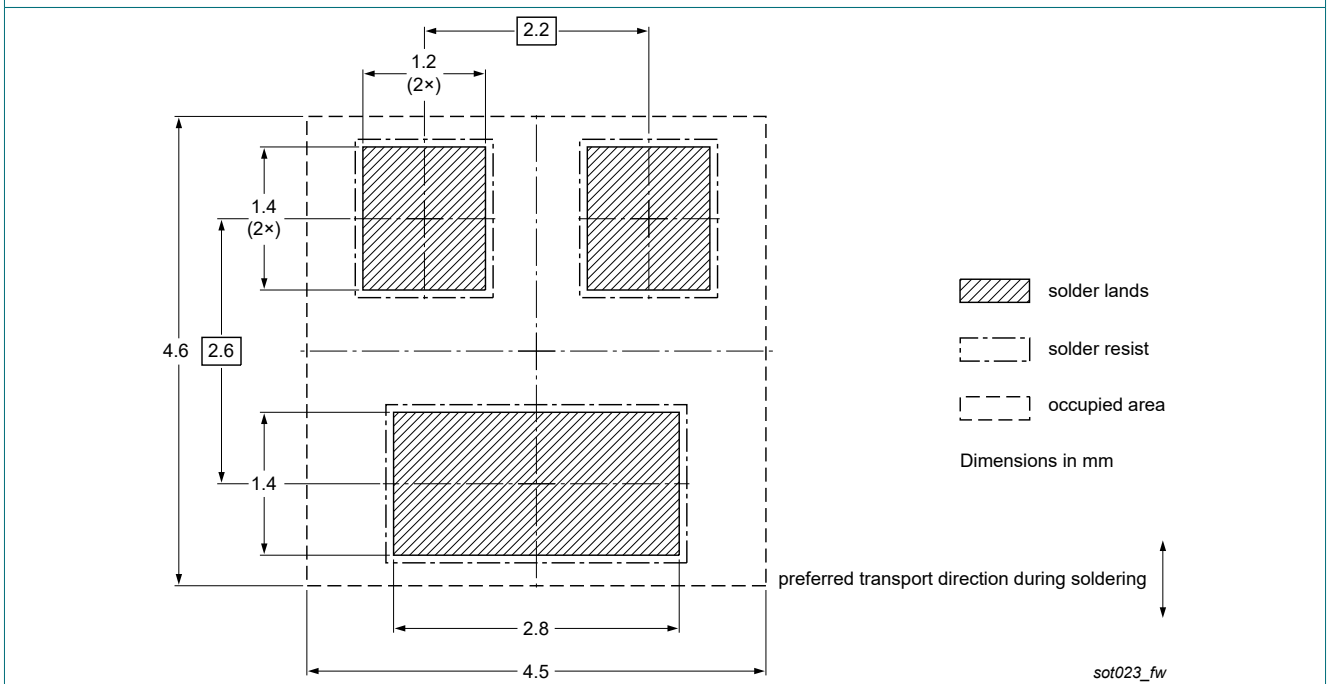


Fig. 13. Wave soldering footprint for SOT23

13. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PESD42VS2UT_v.2	20190124	Product data sheet	-	PESD42VS2UT_v.1
Modifications:	• Product status changed			
PESD42VS2UT_v.1	20190117	Objective data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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