1. General description

Ultra low capacitance bidirectional ElectroStatic Discharge (ESD) protection diode, part of the TrEOS Protection family. This device is housed in a DSN0603-2 (SOD962) leadless ultra small Surface-Mounted Device (SMD) package. The TrEOS Protection family is optimized for safeguarding very sensitive high-speed interfaces against ESD pulses with a high level of robustness.

2. Features and benefits

- Bidirectional ESD protection of one line
- Extremely low diode capacitance C_d = 0.1 pF
- ESD protection up to ±10 kV according to IEC 61000-4-2
- Ultra small SMD package

3. Applications

ESD and surge protection for:

- ultra high-speed datalines
- very sensitive interface lines
- generic interface lines

in portable electronics, communication, consumer and computing devices.

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
C _d	diode capacitance	f = 1 MHz; V _R = 0 V; T _{amb} = 25 °C	-	0.1	0.15	pF
V _{RWM}	reverse standoff voltage	T _{amb} = 25 °C	-	-	5	V



5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode		1 1 2
2	K	cathode		sym045
			Transparent top view	
			DSN0603-2 (SOD962-2)	

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD5V0R1BSF	DSN0603-2	Leadless ultra small package; 2 terminals; body 0.6 x 0.3 x 0.3 mm	SOD962-2

7. Marking

Table 4. Marking codes

Type number	Marking code
PESD5V0R1BSF	В

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

		, ,				
Symbol	Parameter	Conditions		Min	Max	Unit
I _{PPM}	rated peak pulse current	t _p = 8/20 μs	[1]	-	4.5	Α
Tj	junction temperature			-	150	°C
T _{amb}	ambient temperature			-40	125	°C
T _{stg}	storage temperature			-65	150	°C
ESD maxim	um ratings		'	_		_
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2; contact discharge	[2]	-	10	kV
		IEC 61000-4-2; air discharge	[2]	-	15	kV

- [1] According to IEC 61000-4-5 and IEC 61643-321.
- [2] Device stressed with ten non-repetitive ESD pulses.

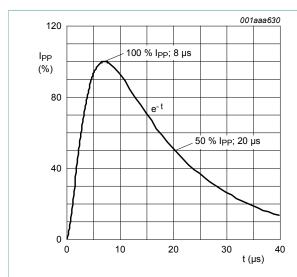


Fig. 1. 8/20 μs pulse waveform according to IEC 61000-4-5 and IEC 61643-321

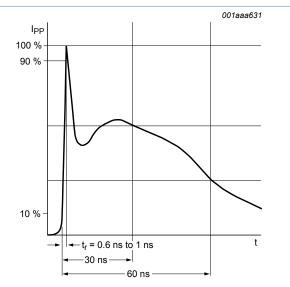


Fig. 2. ESD pulse waveform according to IEC 61000-4-2

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V_{RWM}	reverse standoff voltage	T _{amb} = 25 °C		-	-	5	V
C _d	diode capacitance	f = 1 MHz; V _R = 0 V; T _{amb} = 25 °C		-	0.1	0.15	pF
		f = 2.5 GHz; V _R = 0 V; T _{amb} = 25 °C		-	0.1	-	pF
V_{BR}	breakdown voltage	I _R = 1 mA; T _{amb} = 25 °C		6	10	-	V
V _{CL}	clamping voltage	T_{amb} = 25 °C; I_{PPM} = 4.5 A; t_p = 8/20 μ s	[1]	-	-	5	V
		T_{amb} = 25 °C; I_{PP} = 8 A; t_p = TLP	[2]	-	6	-	V
		T_{amb} = 25 °C; I_{PP} = 15 A; t_p = TLP	<u>[2]</u>	-	9.2	-	V
R _{dyn}	dynamic resistance	T _{amb} = 25 °C; I _R = 10 A	[2]	-	0.45	-	Ω
I _{RM}	reverse leakage current	V _{RWM} = 5 V; T _{amb} = 25 °C		-	1	50	nA

- [1] According to IEC 61000-4-5 and IEC 61643-321.
- [2] Non-repetitive current pulse, Transmission Line Pulse (TLP) t_p = 100 ns; square pulse; ANSI / ESD STM5.5.1-2008.

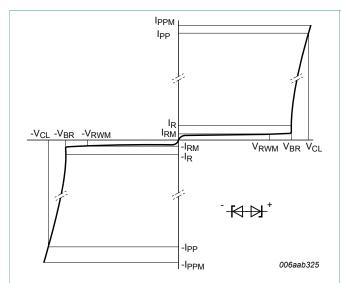


Fig. 3. V-I characteristics for a bidirectional ESD protection diode

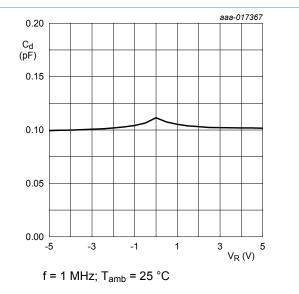


Fig. 4. Diode capacitance as a function of reverse voltage; typical values

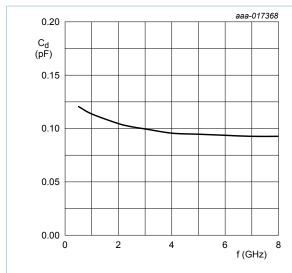


Fig. 5. Diode capacitance as a function of frequency; typical values

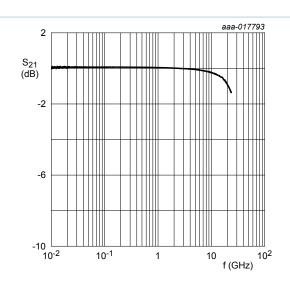


Fig. 6. Insertion loss; typical values

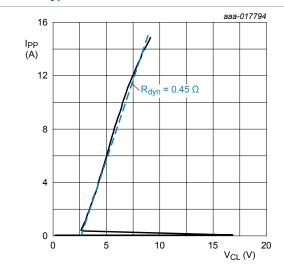


Fig. 7. Dynamic resistance with positive clamping voltage

 t_p = 100 ns; Transmission Line Pulse (TLP)

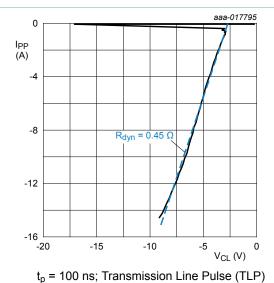
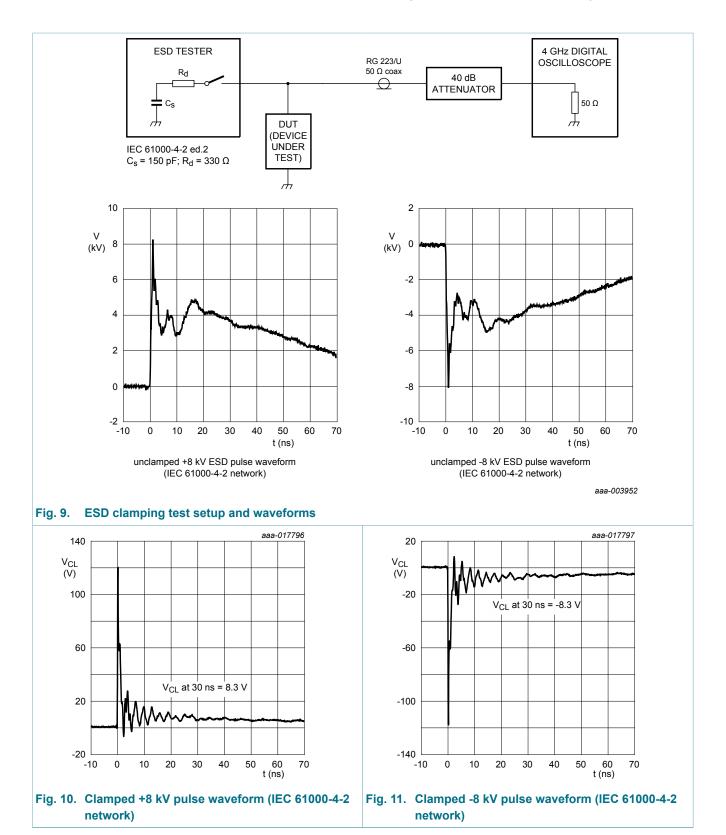
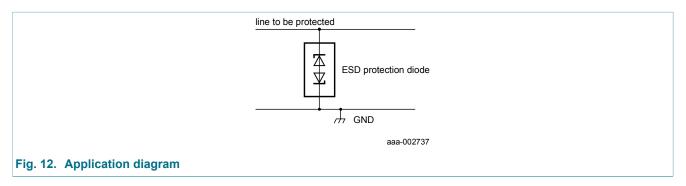


Fig. 8. Dynamic resistance with negative clamping voltage



10. Application information

The device is designed for the protection of one bidirectional data line from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are both positive and negative with respect to ground. The device is not designed to be used on lines connected to a DC supply.

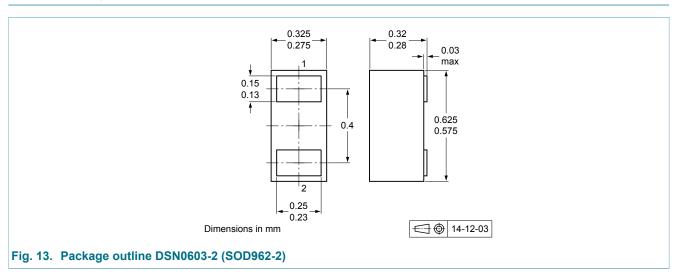


Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

- 1. Place the device as close to the input terminal or connector as possible.
- 2. Minimize the path length between the device and the protected line.
- 3. Keep parallel signal paths to a minimum.
- 4. Avoid running protected conductors in parallel with unprotected conductors.
- Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
- 6. Minimize the length of the transient return path to ground.
- 7. Avoid using shared transient return paths to a common ground point.
- 8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

11. Package outline

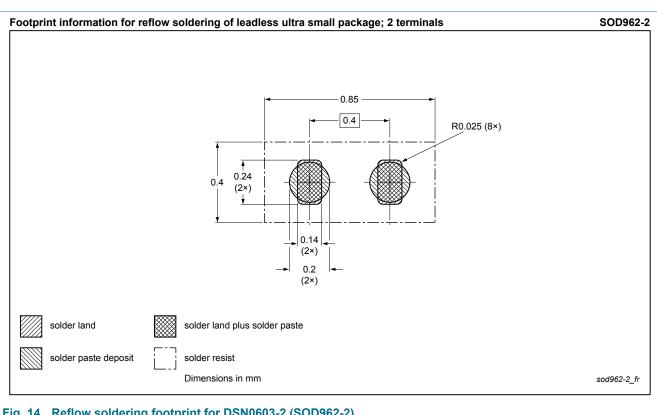


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12. Soldering



13. Revision history

Table 7. Revision history

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Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PESD5V0R1BSF v.2	20150507	Product data sheet	-	PESD5V0R1BSF v.1
Modifications:	Product status char	nged		
PESD5V0R1BSF v.1	20150429	Preliminary data sheet	-	-

14. Legal information

14.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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