# PHE13005X

## Silicon diffused power transistor

Rev.03 - 26 April 2018 Product data sheet

## 1. General description

High-voltage, high-speed planar-passivated, NPN power switching transistor in SOT186A (TO-220F) plastic package for use in high frequency electronic lighting ballast applications

## 2. Features and benefits

- Fast switching
- High voltage capability of 700 V
- Low thermal resistance
- Isolated package

## 3. Applications

- Electronic lighting ballasts

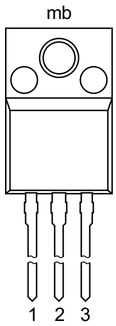
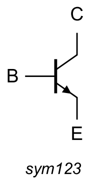
## 4. Quick reference data

**Table 1. Quick reference data**

| Symbol | Parameter | Conditions | | Values | | Unit |
|---|---|---|---|---|---|---|
| **Absolute maximum rating** | | | | | | |
| $V_{CESM}$ | collector-emitter peak voltage | $V_{BE}$ = 0 V | | 700 | | V |
| $I_C$ | collector current | DC; Fig. 1; Fig. 2; Fig. 3 | | 4 | | A |
| $P_{tot}$ | total power dissipation | $T_h$ ≤ 25 °C; Fig. 4 | | 26 | | W |
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| **Static characteristics** | | | | | | |
| $h_{FE}$ | DC current gain | $I_C$ = 1 A; $V_{CE}$ = 5 V; $T_h$ = 25 °C; Fig. 11 | 12 | 20 | 40 | |
| | | $I_C$ = 2 A; $V_{CE}$ = 5 V; $T_h$ = 25 °C; Fig. 11 | 10 | 17 | 28 | |

# 5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|---|---|---|---|---|
| 1 | B | base |  |  |
| 2 | C | collector | | |
| 3 | E | emitter | | |
| mb | n.c. | isolated | | |

# 6. Ordering information

Table 3. Ordering information

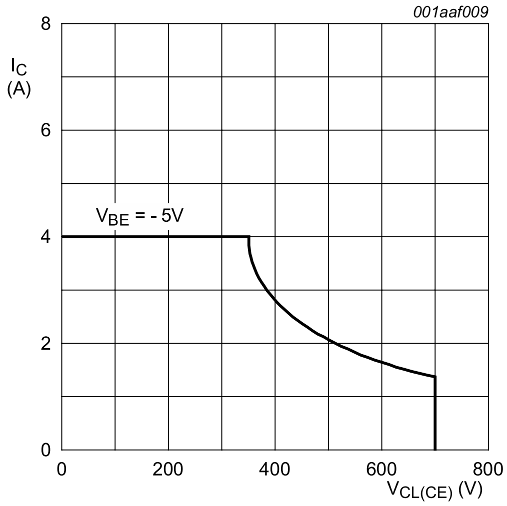
| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| PHE13005X | TO-220F | plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack" | SOT186A |

# 7. Limiting values

**Table 4. Limiting values**

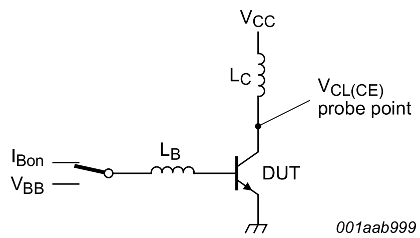
*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Values | Unit |
|---|---|---|---|---|
| $V_{CESM}$ | collector-emitter peak voltage | $V_{BE}$ = 0 V | 700 | V |
| $V_{CBO}$ | collector-base voltage | $I_E$ = 0 A | 700 | V |
| $V_{CEO}$ | collector-emitter voltage | $I_B$ = 0 A | 400 | V |
| $I_C$ | collector current | DC; Fig. 1; Fig. 2; Fig. 3 | 4 | A |
| $I_{CM}$ | peak collector current | | 8 | A |
| $I_B$ | base current | | 2 | A |
| $I_{BM}$ | peak base current | | 4 | A |
| $P_{tot}$ | total power dissipation | $T_h \leq$ 25 °C; Fig. 4 | 26 | W |
| $T_{stg}$ | storage temperature | | -65 to 150 | °C |
| $T_j$ | junction temperature | | 150 | °C |



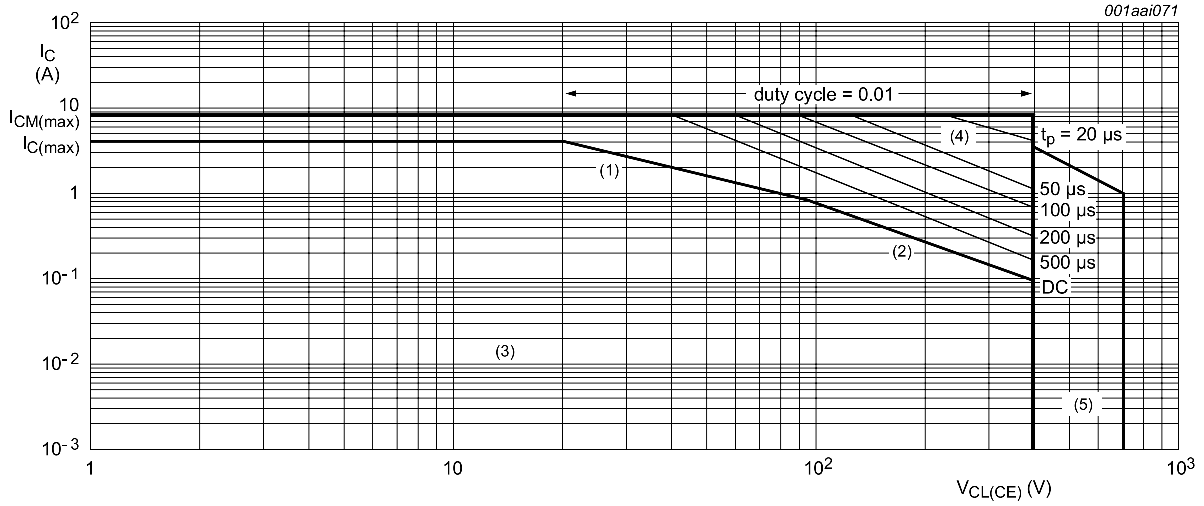

$T_j = T_{j\,(max)}$ °C

**Fig. 1. Reverse bias safe operating area**



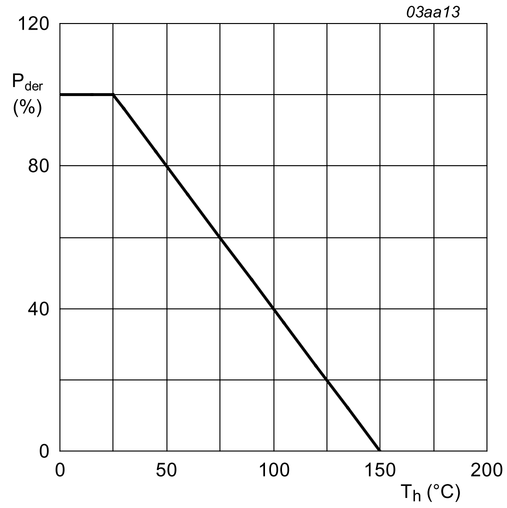

$V_{CL(CE)} \leq$ 1000V; $V_{CC}$ = 150 V; $V_{BB}$ = - 5 V;
$L_C$ = 200 µH; $L_B$ = 1 µH

**Fig. 2. Test circuit for reverse bias safe operating area**




$T_h \leq 25$ °C
Mounted with heatsink compound and (30 ± 5) N force on the center of the envelope
(1) $P_{tot}$ maximum and $P_{tot}$ peak maximum lines
(2) Second breakdown limits
(3) Region of permissible DC operation
(4) Extension of operating region for repetitive pulse operation
(5) Extension of operating region during turn-on in single transistor converters provided that $R_{BE} \leq 100\ \Omega$ and $t_p \leq 0.6$ µs.

**Fig. 3. Forward bias safe operating area**




$$P_{der}(\%) = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\%$$

**Fig. 4. Normalized total power dissipation as a function of heatsink temperature**

## 8. Thermal characteristics

**Table 5. Thermal characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $R_{th(j-mb)}$ | thermal resistance from junction to heatsink | with heatsink compound; Fig. 5 | | - | - | 4.8 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | | | - | 55 | - | K/W |

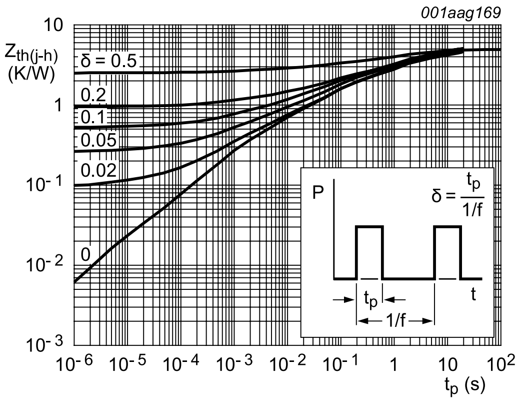



**Fig. 5. Transient thermal impedance from junction to heatsink as a function of pulse duration**

# 9. Characteristics

**Table 6. Characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | | |
| $I_{CES}$ | collector-emitter cut-off current | $V_{BE}$ = 0 V; $V_{CE}$ = 700 V; $T_j$ = 25 °C | | - | - | 1 | mA |
| | | $V_{BE}$ = 0 V; $V_{CE}$ = 700 V; $T_j$ = 100 °C | | - | - | 5 | mA |
| $I_{CBO}$ | collector-base cut-off current | $V_{CB}$ = 700 V; $I_E$ = 0 A; $T_h$ = 25 °C | | - | - | 1 | mA |
| $I_{CEO}$ | collector-emitter cut-off current | $V_{CEO}$ = 400 V; $I_B$ = 0 A; $T_h$ = 25 °C | | - | - | 0.1 | mA |
| $I_{EBO}$ | emitter-base cut-off current | $V_{EB}$ = 9 V; $I_C$ = 0 A; $T_h$ = 25 °C | | - | - | 1 | mA |
| $V_{CEOsus}$ | collector-emitter sustaining voltage | $I_B$ = 0 A; $I_C$ = 10 mA; $L_C$ = 25 mH; $T_h$ = 25 °C; Fig. 6; Fig. 7 | | 400 | - | - | V |
| $V_{CEsat}$ | collector-emitter saturation voltage | $I_C$ = 1 A; $I_B$ = 0.2 A; $T_h$ = 25 °C; Fig. 8; Fig. 9 | | - | 0.1 | 0.5 | V |
| | | $I_C$ = 2 A; $I_B$ = 0.5 A; $T_h$ = 25 °C; Fig. 8; Fig. 9 | | - | 0.2 | 0.6 | V |
| | | $I_C$ = 4 A; $I_B$ = 1 A; $T_h$ = 25 °C; Fig. 8; Fig. 9 | | - | 0.3 | 1 | V |
| $V_{BEsat}$ | base-emitter saturation voltage | $I_C$ = 1 A; $I_B$ = 0.2 A; $T_h$ = 25 °C; Fig. 10 | | - | 0.85 | 1.2 | V |
| | | $I_C$ = 2 A; $I_B$ = 0.5 A; $T_h$ = 25 °C; Fig. 10 | | - | 0.92 | 1.6 | V |
| $h_{FE}$ | DC current gain | $I_C$ = 1 A ; $V_{CE}$ = 5 V; $T_h$ = 25 °C; Fig. 11 | | 12 | 20 | 40 | |
| | | $I_C$ = 2 A ; $V_{CE}$ = 5 V; $T_h$ = 25 °C; Fig. 11 | | 10 | 17 | 28 | |
| **Dynamic characteristics** | | | | | | | |
| $t_s$ | storage time | $I_C$ = 2 A; $I_{Bon}$ = 0.4 A; $I_{Boff}$ = -0.4 A; $R_L$ = 75 Ω;$T_h$ = 25 °C; resistive load; Fig. 12; Fig. 13 | | - | 2.7 | 4 | μs |
| | | $I_C$ = 2 A; $I_{Bon}$ = 0.4 A; $V_{BB}$ = -5 V; $L_B$ = 1 μH; $T_h$ = 25 °C; inductive load; Fig. 14; Fig. 15 | | - | 1.2 | 2 | μs |
| | | $I_C$ = 2 A; $I_{Bon}$ = 0.4 A; $V_{BB}$ = -5 V; $L_B$ = 1 μH; $T_h$ = 100 °C; inductive load; Fig. 14; Fig. 15 | | - | 1.4 | 4 | μs |
| $t_f$ | fall time | $I_C$ = 2 A; $I_{Bon}$ = 0.4 A; $I_{Boff}$ = -0.4 A; $R_L$ = 75 Ω;$T_h$ = 25 °C; resistive load; Fig. 12; Fig. 13 | | - | 0.3 | 0.9 | μs |
| | | $I_C$ = 2 A; $I_{Bon}$ = 0.4 A; $V_{BB}$ = -5 V; $L_B$ = 1 μH; $T_h$ = 25 °C; inductive load; Fig. 14; Fig. 15 | | - | 0.1 | 0.5 | μs |
| | | $I_C$ = 2 A; $I_{Bon}$ = 0.4 A; $V_{BB}$ = -5 V; $L_B$ = 1 μH; $T_h$ = 100 °C; inductive load; Fig. 14; Fig. 15 | | - | 0.16 | 0.9 | μs |

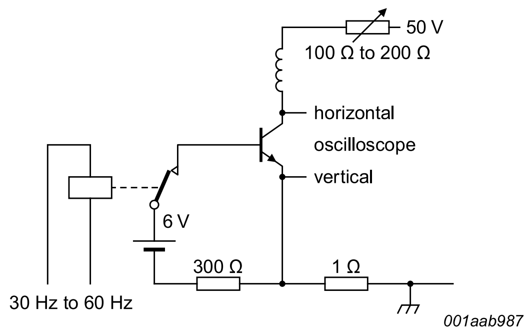



**Fig. 6. Test circuit for collector-emitter sustaining voltage**

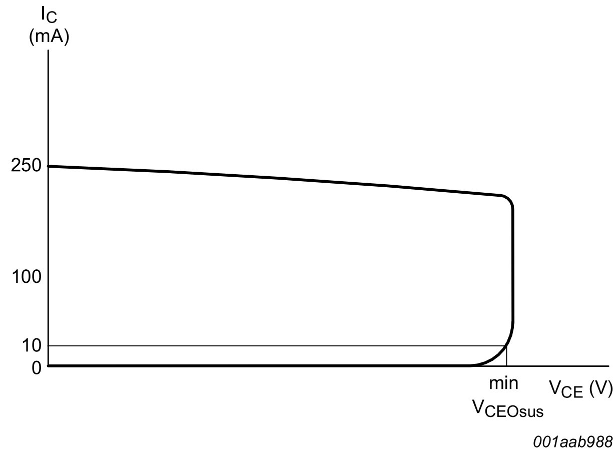
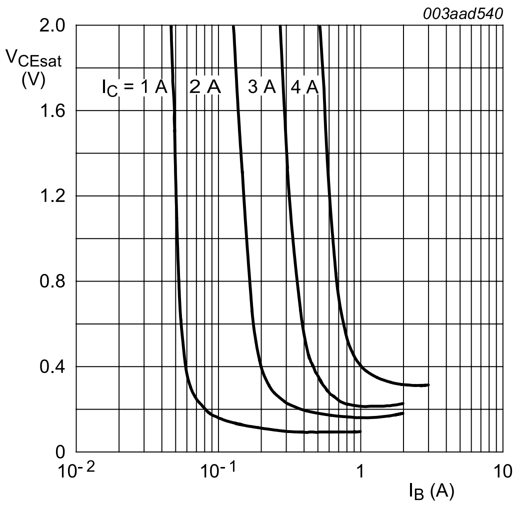
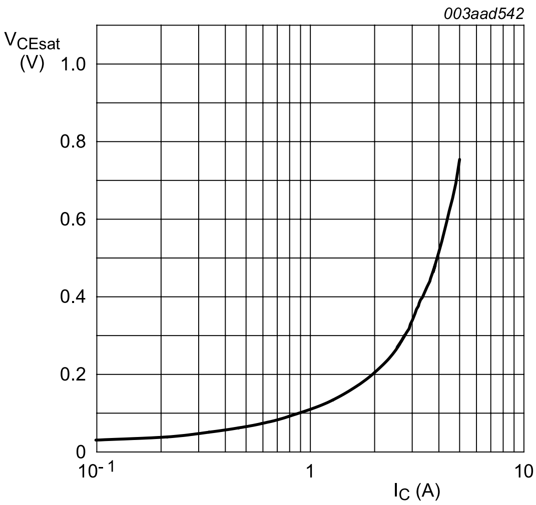



**Fig. 7. Oscilloscope display for collector-emitter sustaining voltage test waveform**




$T_j$ = 25 °C

**Fig. 8. Collector-emitter saturation voltage; typical values**




$I_C$ / $I_B$ = 4

**Fig. 9. Collector-emitter saturation voltage as a function of collector current; typical values**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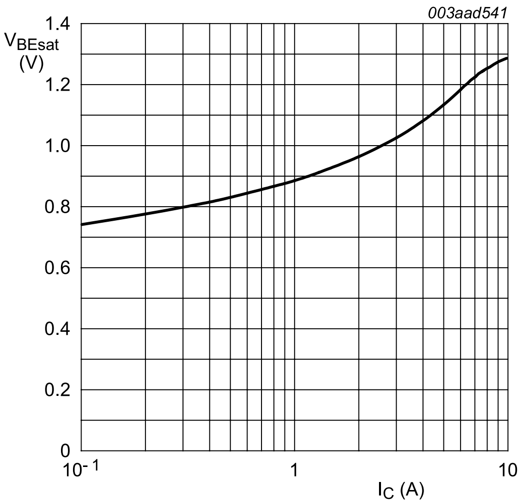
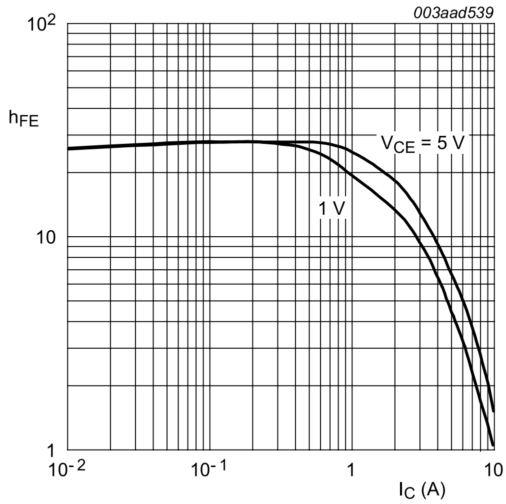



$I_C / I_B = 4$

**Fig. 10. Base-emitter saturation voltage; typical values**




$T_j = 25$ °C

**Fig. 11. DC current gain as a function of collector current; typical values**

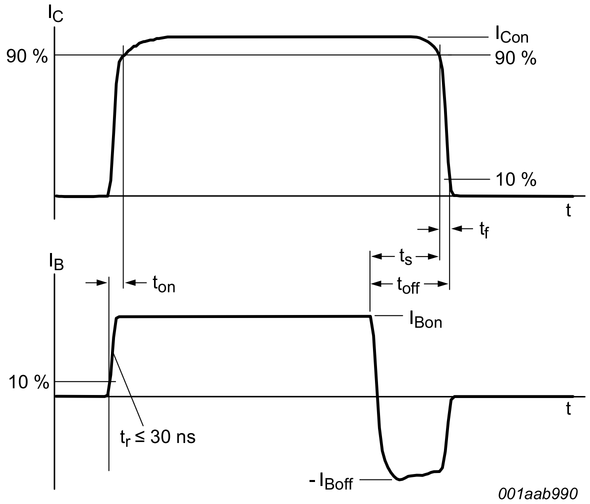
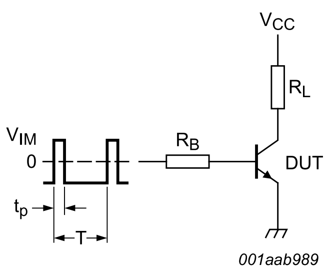



**Fig. 12. Switching times waveforms for resistive load**




$V_{IM}$ = - 6 to + 8 V; $V_{CC}$ = 250 V; $t_p$ = 20 µs;
δ = $t_p$ / T = 0.01
$R_B$ and $R_L$ calculated from $I_{Con}$ and $I_{Bon}$ requirements.

**Fig. 13. Test circuit for resistive load switching**

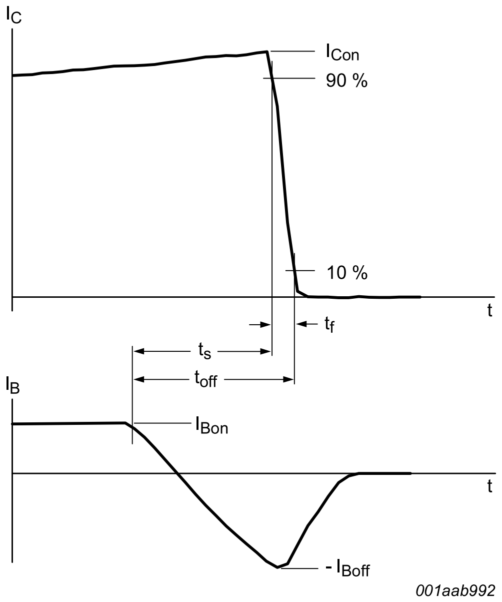
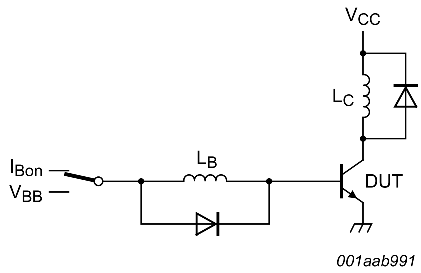



Fig. 14. Switching times waveforms for inductive load




$V_{CC}$ = 300 V; $V_{BB}$ = - 5 V; $L_C$ = 200 μH; $L_B$ = 1 μH

Fig. 15. Test circuit for inductive load switching

## 10. Isolation characteristics

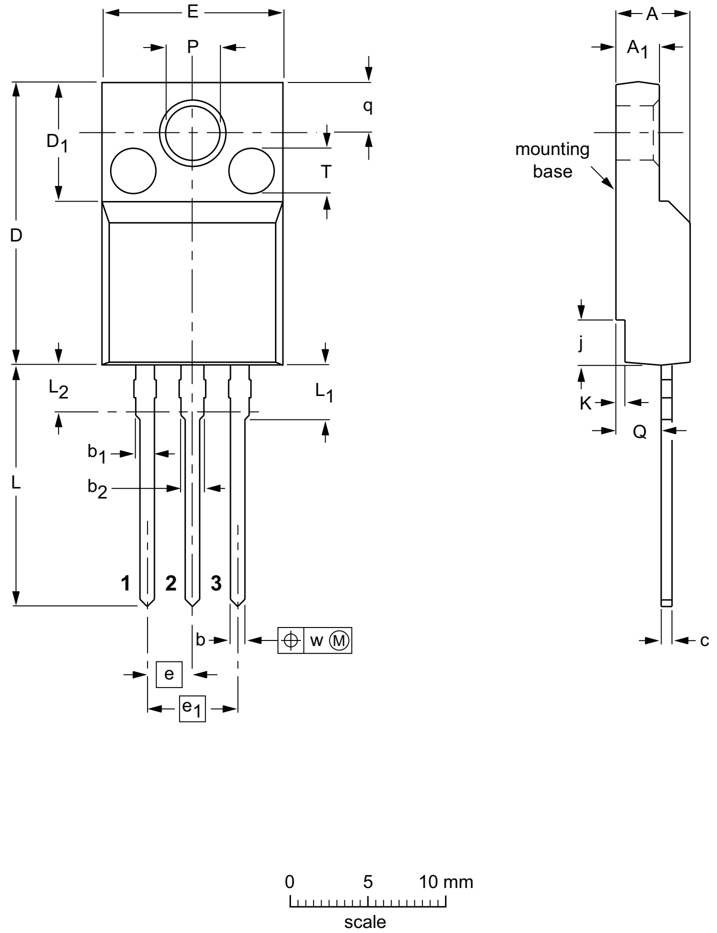
**Table 8. Isolation characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{isol(RMS)}$ | RMS isolation voltage | from all terminals to external heatsink; clean and dust free; 50 Hz ≤ f ≤ 60 Hz; RH ≤ 65 %;$T_h$ = 25 °C | | - | - | 2500 | V |
| $C_{isol}$ | isolation capacitance | from collector to external heatsink; f = 1 MHz; $T_h$ = 25 °C | | - | 10 | - | pF |

# 11. Package outline

**Plastic single-ended package; isolated heatsink mounted;**
**1 mounting hole; 3-lead TO-220 'full pack'**

**SOT186A**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | $A_1$ | b | $b_1$ | $b_2$ | c | D | $D_1$ | E | e | $e_1$ | j | K | L | $L_1$ | $L_2$(1) max. | P | Q | q | T(2) | w |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.6<br>4.0 | 2.9<br>2.5 | 0.9<br>0.7 | 1.1<br>0.9 | 1.4<br>1.0 | 0.7<br>0.4 | 15.8<br>15.2 | 6.5<br>6.3 | 10.3<br>9.7 | 2.54 | 5.08 | 2.7<br>1.7 | 0.6<br>0.4 | 14.4<br>13.5 | 3.30<br>2.79 | 3 | 3.2<br>3.0 | 2.6<br>2.3 | 3.0<br>2.6 | 2.5 | 0.4 |

**Notes**

1. Terminal dimensions within this zone are uncontrolled.
2. Both recesses are ⊠2.5 × 0.8 max. depth

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT186A | | 3-lead TO-220F | | | | ~~02-04-09~~<br>06-02-14 |

## 12. Revision history

**Table 9. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| PHE13005X v.3 | 20180426 | Product data sheet | - | PHE13005X_2 |
| Modifications: | Change from NXP version to WeEn version | | | |
| PHE13005X_2 | 2091120 | Product data sheet | - | PHE13005X_1 |
| Modifications: | Various changes to content. | | | |
| PHE13005X_1 | 20080515 | Product data sheet | - | - |

# 13. Legal information

## Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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