A Maxim Integrated Products Brand

PHY2078

125Mbps – 2.5Gbps FTTx Burst Mode Laser Driver / Postamplifier

Features

- Burst-Mode common anode laser driver with up to 80mA modulation and 90mA bias current
- 7ns output switching in Burst Mode
- Power saving mode with zero bias and modulation current between bursts
- Closed or open loop bias mode with temperature lookup table
- Temperature compensated modulation current
- Limiting amplifier with programmable low pass filter and output swing
- Device settings stored in external 2k EEPROM

Applications

- GPON
- GEPON
- BPON

Description

The PHY2078 is a combined burst mode laser driver and limiting amplifier for use within fiber optic modules for FTTx applications. Used with the PHY1095 or PHY1097 transimpedance amplifiers and a low cost serial EEPROM it forms a complete PON diplexer silicon solution.

The transmit block includes a high frequency modulator and a bias current generator. The bias current can be controlled either by a fast settling APC loop or in open loop mode which uses a temperature lookup table.

The receiver includes a limiting amplifier with programmable bandwidth. A Signal Detect/Loss Of Signal function is implemented using the input signal modulation amplitude with user selectable threshold and hysteresis.

Operating with a 3.3V supply and rated from -40 to +95°C ambient, the PHY2078 is housed in a 32pin, 5x5mm, RoHS compliant, TQFN package.

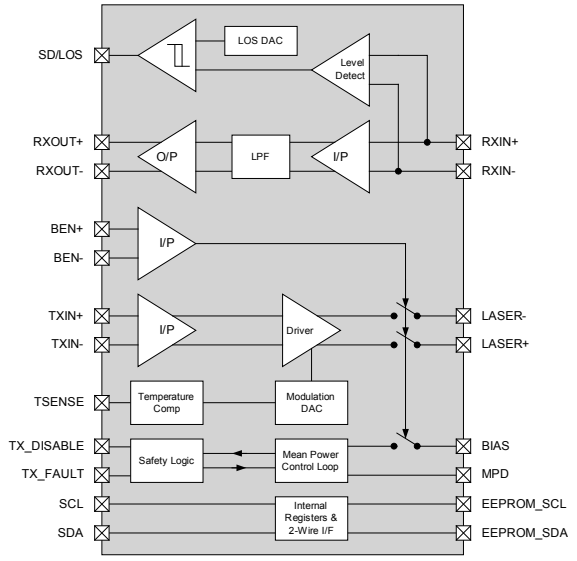


Figure 1 – Block diagram

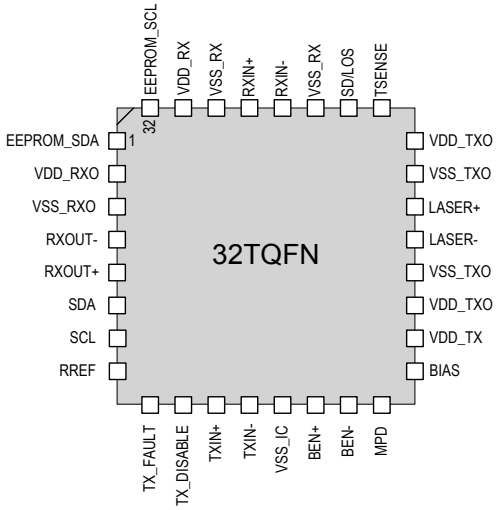


Figure 2 – Device pin out

Contents

1. Ordering Information

Part Number	Description	Package
PHY2078QT-RR	FTTx LASER driver and Post Amp	TQFN32, 5mmx5mm in Tape and Reel

2. Pin Description

Pin No	Name	Direction	Type	Description
1	EEPROM_SDA	I/O	LVTTL	EEPROM 2 wire serial interface data, internal 8kΩ pull up
2	VDD_RXO		Power	Receiver output power supply
3	VSS_RXO		Ground	Receiver output ground connection
4	RXOUT-	O/P	CML	Limiting amplifier serial data output
5	RXOUT+	O/P	CML	Limiting amplifier serial data output
6	SDA	I/O	LVTTL	2-wire serial interface data
7	SCL	I/O	LVTTL	2-wire serial interface clock
8	RREF			Internal connection, leave open circuit
9	TX_FAULT	O/P	LVTTL (Open Collector)	Laser fail alarm (requires external pull up)
10	TX_DISABLE	I/P	LVTTL	Laser enable / disable
11	TXIN+	I/P	High Speed Input	Laser driver serial input, see section 7 for interfacing details
12	TXIN-	I/P	High Speed Input	Laser driver serial input, see section 7 for interfacing details
13	VSS_IC			Internal connection, connect to ground
14	BEN+	I/P	High Speed Input	Burst enable positive, see section 7 for interfacing details
15	BEN-	I/P	High Speed Input	Burst enable negative, see section 7 for interfacing details
16	MPD	I/P	Analog	Monitor photodiode input
17	BIAS	O/P	Analog	Laser bias current output
18	VDD_TX		Power	Driver power supply
19	VDD_TXO		Power	Driver output power supply
20	VSS_TXO		Ground	Driver output ground connection
21	LASER-	O/P	High speed Output	Laser driver serial output
22	LASER+	O/P	High speed Output	Laser driver serial output
23	VSS_TXO		Ground	Driver output ground connection
24	VDD_TXO		Power	Driver output power supply
25	TSENSE	I/P	Analog	External temperature component connection

Pin No	Name	Direction	Type	Description
26	SD/LOS	O/P	LVTTL (Open Collector)	Signal Detect or Loss of signal output (requires external pull up). Polarity selected by user
27	VSS_RX		Ground	Receiver ground connection
28	RXIN-	I/P	CML	Limiting amplifier serial data input
29	RXIN+	I/P	CML	Limiting amplifier serial data input
30	VSS_RX		Power	Receiver ground connection
31	VDD_RX		Power	Receiver power supply
32	EEPROM_SCL	O/P	LVTTL	EEPROM 2-wire serial interface clock, internal 8kΩ pull up
EP	VSS_EP		Ground	Common ground / thermal pad

3. Key Specifications

3.1. Absolute Maximum Ratings

Parameter	Conditions	Min	Typ	Max	Unit
Supply voltage		-0.5		6.5	V
Voltage on any signal pin		-0.5		VDD + 0.5V	V
Storage temperature				150	°C
Max junction temperature				140	°C
Max soldering temperature	IPC/JEDEC J-STD-020C			260	°C
ESD	Human Body Model JESD-22-A114-B	2			kV

Device not guaranteed to meet specifications, permanent damage may be incurred by operating beyond these limits.

3.2. Continuous Ratings

Parameter	Conditions	Min	Typ	Max	Unit
Operating supply voltage	Continuous operation	2.97	3.3	3.63	V
Current consumption	Excluding bias & modulation current at 20mA bias & 20mA modulation		120	145	mA
Operating temperature	Case Temperature			+110	°C
	Ambient Still Air	-40	25	+95	°C

3.3. Receiver

3.3.1. Receive Limiting Amplifier

Parameter	Conditions	Min	Typ	Max	Unit
Input sensitivity	1.25Gbps, PRBS 2^7-1, BER=1x10^{-12}		6	8	mVp-p
	2.5Gbps, PRBS 2^{31}-1, BER=1x10^{-10}		7	10	mVp-p
System sensitivity	1.25Gbps, PRBS 2^7-1, BER=1x10^{-12} With PHY1095 TIA PD Responsivity = 0.8A/W, PD Capacitance = 0.5pF, Er = 10dB		-32		dBm
	2.5Gbps, PRBS 2^{31}-1, BER=1x10^{-10} With PHY1097 TIA PD Responsivity = 0.9A/W, PD Capacitance = 0.5pF, ER = 10dB		-29		dBm
Maximum differential input	TJ within spec	1200			mVp-p
Input termination impedance	Differential	80	100	120	Ω
Input common mode voltage			VDD_RX - 1.5		V
Input low frequency cutoff	High pass 3dB point for RX system		15		kHz

Parameter	Conditions	Min	Typ	Max	Unit
Differential output rise and fall times (20% - 80%)	Fast slew rate setting, 1250Mbps - 2488Mbps filter setting			100	ps
Differential output swing	CML_LEVEL = 0 CML_LEVEL = 1	700 370		900 470	mVp-p
Total jitter	Input voltage swing 30mVp-p, K28.5 pattern			200	mUIp-p
Output resistance	RXOUT+/- Single ended to VDD_RXO	40	50	60	Ω
Output return loss	Differential, f<2GHz, device powered on	10			dB
Rx 3dB frequency	125/155 Mbps setting 622 Mbps setting 1250 Mbps setting 2488 Mbps setting		120 470 940 1900		MHz

3.3.2. OMA LOS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OMA LOS assert time	t_{loss_on}				100	µs
OMA LOS de-assert time	t_{loss_off}				20	µs
Electrical hysteresis		$20\log_{10}$ (Vdeassert / Vassert) High setting Low setting		 4 3		dB
OMA LOS assert level		Set by OMA_DAC, Address D9h	10		50	mV
Squelch assert time	$t_{squelch\_on}$				100	µs
Squelch de-assert time	$t_{squelch\_off}$				20	µs

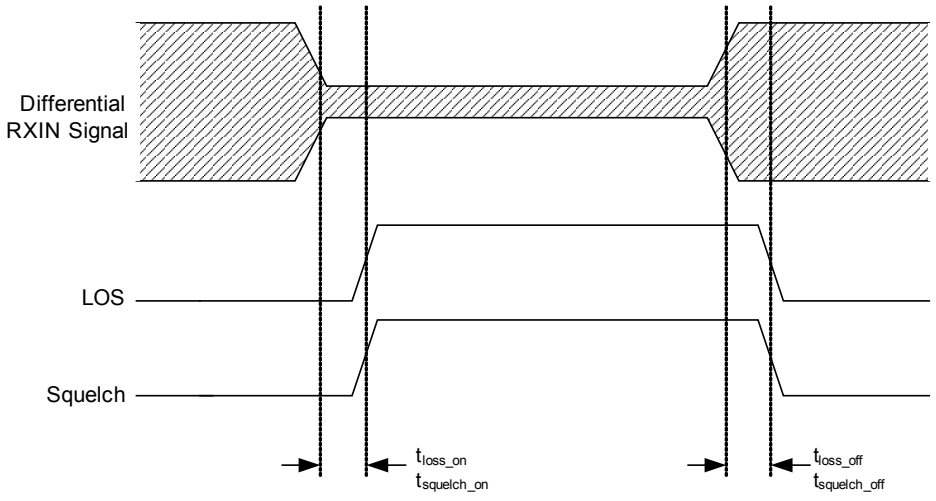


Figure 3 - OMA LOS Detection

3.4. Transmitter

3.4.1. Transmitter Inputs: TXIN+/-, BEN+/-

Parameter	Conditions	Min	Typ	Max	Unit
Input Voltage	VILmin	1.14			V
	VIHmax			VDD_TX	V
Input Swing	Vpp(diff)	0.2			Vpp

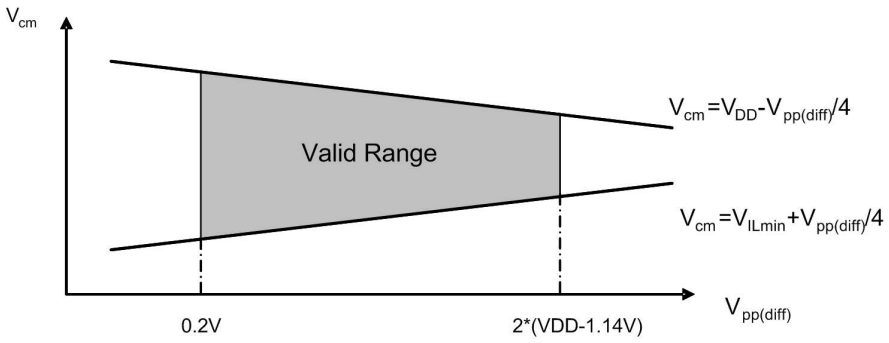


Figure 4 – Valid combinations of transmitter input voltages

3.4.2. Laser Driver

Parameter	Conditions	Min	Typ	Max	Unit
Maximum bias current		90			mA
Bias generator shutdown current	TX_DISABLE active or BEN disabled			100	μA
Maximum modulation current		80			mA
Modulation generator shutdown current	TX_DISABLE active or BEN disabled			100	μA
Electrical 20% to 80% rise / fall time	Measured using 15Ω□effective termination, Imod = 50mA, AC and DC applications		95		ps
Electrical Pulse Width Distortion	Measured using 15Ω□effective termination, Imod = 20 to 50mA			50	ps
Total jitter contribution	Measured over modulation current range			150	mUIp-p
Laser output compliance range	Allowed voltage for laser driver output pins in dynamic operation.	600		VDD_TX	mV
Bias current output compliance	Minimum allowed voltage for pin BIAS, referenced to ground	500			mV
MPD input sink current	For correct APC loop operation			2.6	mA
MPD capacitance	For correct APC loop operation			20	pF

3.4.3. Burst Timings

Parameter	Conditions	Min	Typ	Max	Unit
Burst enable/disable time (Electrical)	Assertion of BEN to 90% of desired bias + modulation current De-assert of BEN to 10% of settled bias + modulation current Target bias current > 3mA		5	12.8	ns
Burst Length	During closed loop operation MPD current must settle to 98% of final value within 60ns	100			ns
	During fast startup algorithm	400			ns
Initial mean power control settling time	From power up or negation of TX_DISABLE to 90% of desired optical power Fast settling algorithm enabled Overshoot < 10% See Section 7.5		1.2		µs

3.4.4. Fault Timing

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Time to initialize	t_{init}	From power on or application of VDD>2.97V during plug in			300	ms
Hard TX_DISABLE assert time	t_{off}	Time from rising edge of TX_DISABLE to when the optical output falls below 10% of nominal		5.5		µs
Hard TX_DISABLE negate time	t_{on}	Time from falling edge of TX_DISABLE to when the modulated optical output rises above 90% of nominal			1	ms
Hard TX_FAULT assert time	t_{fault}	Time from fault to TX_FAULT on Bias/Temperature ADC outside safe range All other fault conditions			 10 100	 ms µs
TX_DISABLE pulse width	t_{reset}	Time TX_DISABLE must be held high to reset TX_FAULT	5			µs
TX_FAULT deassert time	$t_{faultdass}$	Time to deassert TX_FAULT after TX_DISABLE			300	ms

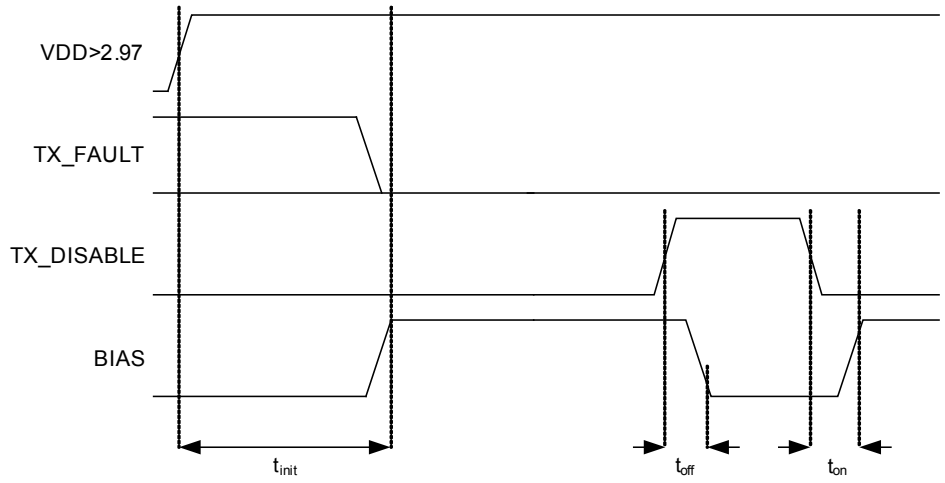


Figure 5 - Device turn on

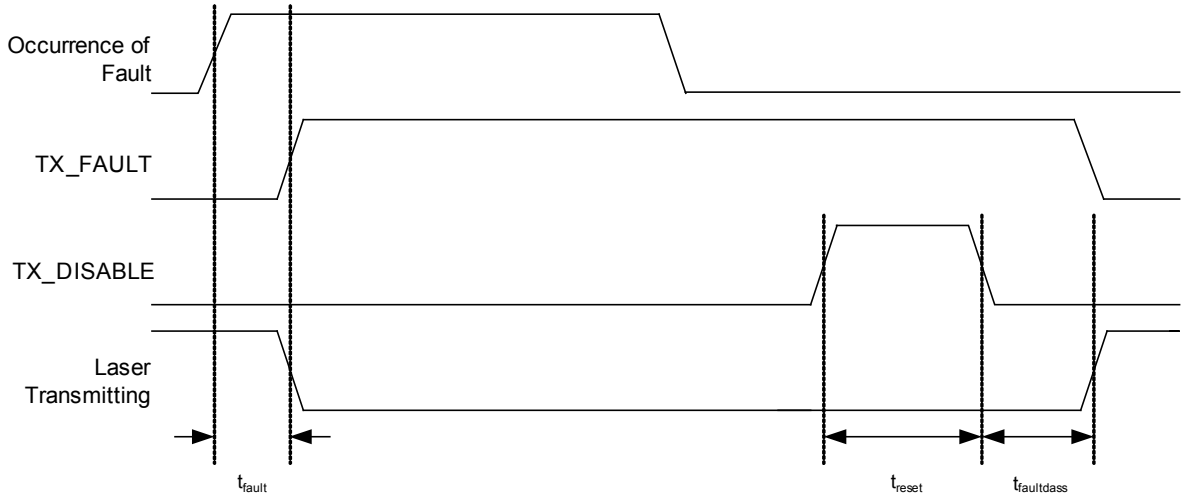


Figure 6 - Fault detection

3.4.5. Eye Safety Internal fixed limits

Parameter	Symbol	Comment	Min	Typ	Max	Unit
High supply voltage assert limit	V_{eyeHa}	Applies to VDD_TXO or VDD_TX	4.0	4.15	4.3	V
High supply voltage de-assert limit	V_{eyeHd}		3.7	3.85	4.0	V
Low supply voltage assert limit	V_{eyeLa}		2.45	2.6	2.75	V
Low supply voltage de-assert limit	V_{eyeLd}		2.7	2.8	2.95	V
High Supply Hysteresis			- 0.1			V
Low Supply Hysteresis			0.1			V
High RREF pin voltage assert limit	V_{rrefHa}			1.2		V
High RREF pin voltage de-assert limit	V_{rrefHd}			1.1		V
Low RREF pin voltage assert limit	V_{rrefLa}			0.8		V
Low RREF pin voltage de-assert limit	V_{rrefLd}			0.9		V

3.4.6. Power on Reset (PoR)

Parameter	Symbol	Comment	Min	Typ	Max	Unit
Power on reset (PoR) voltage		Reset is low input voltage			0.5	V
PoR time to reset			1.0			ms
Power on reset (PoR) exit voltage	V_{exit}		1.2			V
PoR exit delay	t_{delay}	Time before first EEPROM access	8.0			ms

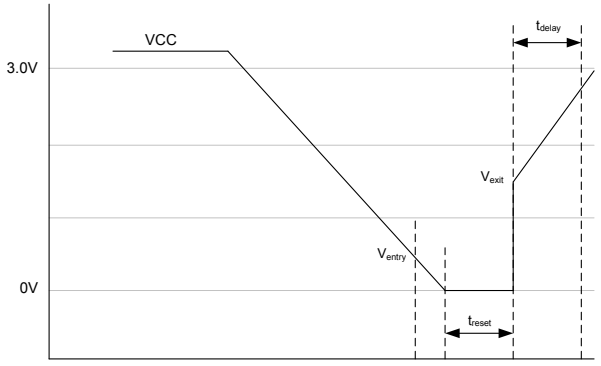


Figure 7 – PoR Timing

3.5. 2-Wire Serial Interface

3.5.1. AC Electrical Characteristics

Parameter	Symbol	Comment	Min	Typ	Max	Unit
SCL clock frequency	f_{SCL}		0		100	kHz
LOW period of the SCL clock	t_{LOW}		4.7			µs
HIGH period of the SCL clock	t_{HIGH}		4.0			µs
Set-up time for a repeated START condition	$t_{SU:STA}$		4.7			µs
Hold time (repeated) START condition	$t_{HD:STA}$		4.0			µs
Data hold time	$t_{HD:DAT}$		0		3.45	µs
Data set-up time	$t_{SU:DAT}$		250			ns
Rise time of both SDA and SCL signals	t_R				1000	ns
Fall time of both SDA and SCL signals	t_F				300	ns
Set-up time for STOP condition	$t_{SU:STO}$		4.0			µs
Bus free time between a STOP and START condition	t_{BUF}		4.7			µs
Output fall time from V_{IHmin} to V_{ILmax}	t_{of}	10pF < C_b [1] < 400pF	0		250	ns
Capacitance for each I/O pin	C_i				10	pF

1: C_b = capacitance of a single bus line in pF.

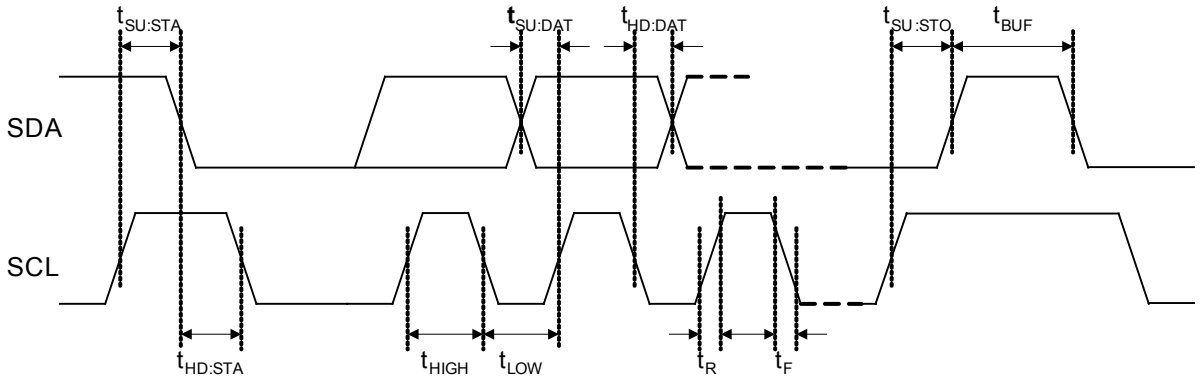


Figure 8 - SDA and SCL bus timing

3.5.2. DC Electrical Characteristics

Parameter	Symbol	Comment	Min	Typ	Max	Unit
Low level input voltage	V_{IL}		-0.5		0.3VDD	V
High level input voltage	V_{IH}		0.7VDD		VDD+0.5	V
Low level O/P voltage	V_{OL}	3 mA sink current	0		0.4	V
I/P current each I/O pin	I_i	$0.1V_{DD} < V_i < 0.9V_{DD}$	-10		10	mA
Power on reset (PoR) voltage		Reset is low input voltage			0.5	V
PoR time to reset			1.0			ms

3.5.3. LVTTL I/O Pins [1]

Parameter	Comment	Min	Typ	Max	Unit
LVTTL voltage out high	External 4.7k to 10k pullup	2.4			V
LVTTL voltage out low	External 4.7k to 10k pullup			0.4	V
LVTTL voltage in high	Internal pullup	2.0		VDD - 0.2	V
LVTTL voltage in low	Internal pullup	0		0.8	V
Internal pull-up resistance	EEPROM_SDA, EEPROM_SCL	6		10	kΩ

[1] Applies to LVTTL Pins specified on pages 3-4

4. Functional Description

4.1. Overview

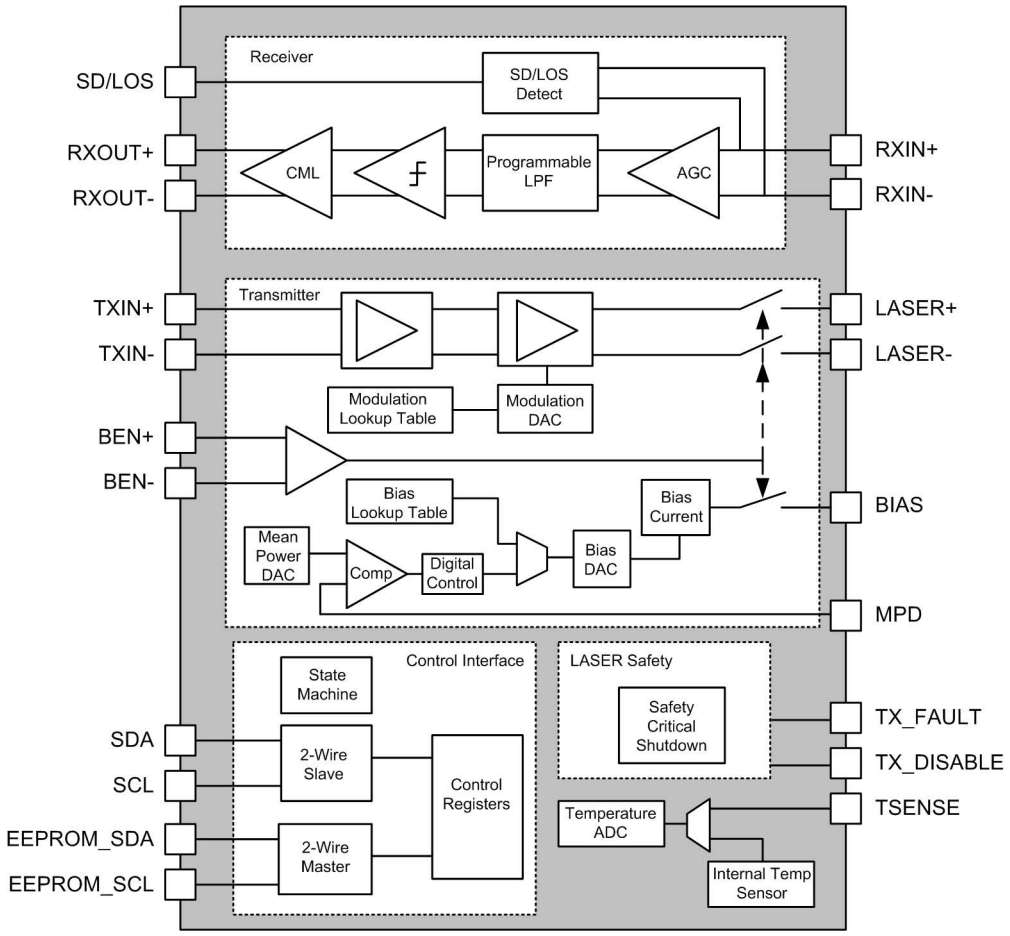


Figure 9 - PHY2078 Functional Overview

4.2. Receiver Features

The PHY2078 receiver section consists of an Automatic Gain Control (AGC) input amplifier, which is followed by a programmable low pass filter. The filtered signal is passed to a limiting stage and the receiver output is a CML driver. Offset cancellation is provided by DC-feedback.

A Signal Detect (SD)/Loss Of Signal (LOS) alarm is provided to detect if the amplitude of the AC-signal at the receiver input is below a programmable threshold. For a transimpedance amplifier with a constant gain, the LOS threshold corresponds to a particular Optical Modulation Amplitude (OMA).

4.2.1. Receiver Input Stage

The receiver input stage includes internal 50Ω single-ended termination resistors and is designed to be AC-coupled to the transimpedance amplifier.

By default the receiver is non-inverting; however, to simplify the PCB layout of differential signals the polarity of the data can be inverted by setting RX_POLARITY (C3h, RX_LIMITER, bit 1) to ‘1’.

4.2.2. Receiver Filter

The programmable low pass filter provides band limiting in the receive signal path and can be used to improve the system sensitivity when a higher bandwidth TIA is used. The bandwidth of the filter is set to 0.7 x signal data rate selected and is controlled by a 3-bit control word as follows:

Bit			Data Rate
2	1	0	
0	0	0	125/155Mbps
0	0	1	622Mbps
0	1	0	Reserved
0	1	1	1.250Gbps
1	0	0	2.488Gbps

Table 1- Receive Filter Data Rates

The 3-bit control word is set in the RATE_SELECT register (C4h, RX_FILTER, bits 2:0).

4.2.3. Receiver CML Output Stage

The CML output stage has two slew rate settings, selected by CML_SLEW (C5h, RX_DRIVER, bit 1). The switching speed can be reduced in order to minimise electromagnetic radiation by setting CML_SLEW to a ‘1’. Setting CML_SLEW to ‘0’ maximises the slew rate of the output.

The signal swing can also be adjusted. Setting CML_LEVEL to ‘0’ (C5h, RX_DRIVER, bit 0) results in a higher receiver differential output swing. Setting CML_LEVEL to ‘1’ results in a reduced output swing.

RXOUT+/- can also be disabled by setting RX_SQUELCH to a ‘1’ (C2h, RX_AGC, bit 2).

The PHY2078 can automatically disable RXOUT+/- if a LOS condition is detected. To enable this function LOS_TO_SQUELCH should be set to ‘1’ (C2h, RX_AGC, bit 3).

In both cases the output termination remains as 50Ω but a logical ‘0’ is output on RXOUT+/-.

4.2.4. Loss of Signal

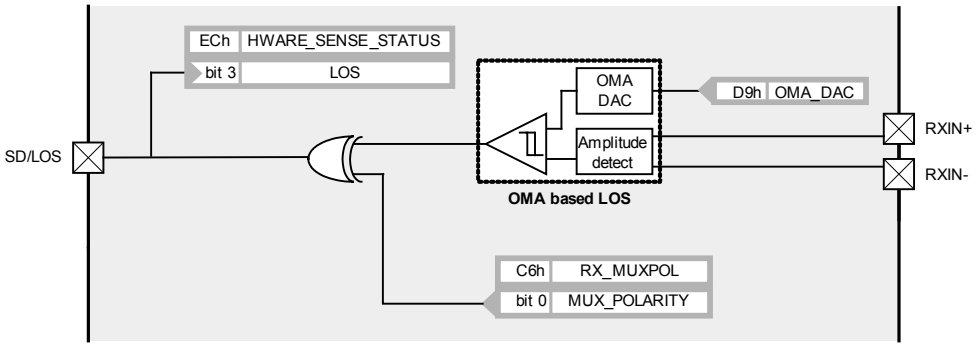


Figure 10 - LOS Detection

Signal Detect (SD) or Loss of Signal (LOS) is detected by measuring the optical modulation amplitude (OMA).

The signal amplitude measured at RXIN+/- is compared to an analog threshold level set by the OMA_DAC register (D9h, OMA_DAC). If the received signal amplitude does not exceed the threshold then the LOS pin is asserted and the LOS indicator bit is set (ECh, HWARE_SENSE_STATUS, bit 3).

The polarity of the LOS pin and register indicator bit are controlled by MUX_POLARITY (C6h, RX_MUXPOL, bit 0). If MUX_POLARITY is set to '0' then the LOS pin is set high during a loss of signal condition. Conversely, if MUX_POLARITY is set to '1' then the LOS pin is set high when a signal is detected.

LOS detection has hysteresis, the level of which can be selected by OMAHYSTSEL (C6h, RX_MUXPOL, bit 1). If OMAHYSTSEL is set to '0' then 3dB of hysteresis is used. If OMAHYSTSEL is set to '1' then 4dB of hysteresis is used.

Parameter	Comments	Step Size	DAC Range	Operational Range
OMA_DAC	OMA LOS DAC (8 bits)	250µV (±125µV)	0 to 64mV	10mV to 50mV

Table 2 - LOS DAC Characteristics

4.2.5. Voltage Reference

The PHY2078 includes a temperature stable 1V reference source which provides the bias for the internal analog circuitry. The reference voltage is set using an internal resistor RINTERNAL (CEh, DAC_PWRD, bit 5) to 1. The accuracy of the reference voltage using the internal resistor is +/-10%.

4.3. Transmitter features

The transmitter input buffer provides the necessary drive to the laser driver output stage. It includes an internal high impedance bias network and is designed to be DC or AC-coupled. For high frequency applications an external termination network must be implemented. See section 7 for more interfacing details.

The laser driver output is designed to drive lasers in the common anode configuration using either AC- or DC-coupling. For burst mode operation DC-coupling must be used.

The laser driver circuit delivers a maximum peak to peak modulation current of 80mA measured at the device output pin LASER+.

By default the transmitter is non-inverting; however, to simplify the PCB layout of differential signals the polarity of the data can be inverted by setting TX_POLARITY (CAh, TX_DBUFF, bit 0) to '1'.

4.3.1. Modulation Current Control

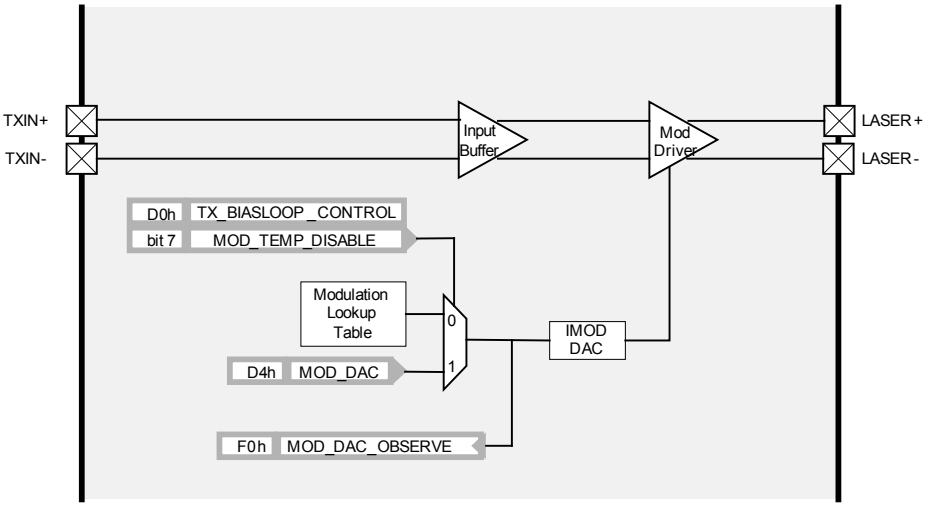


Figure 11 - Modulation Current Generation

The modulation current can be either set by a constant register value or controlled by a temperature indexed look-up table (LUT).

If MOD_TEMP_DISABLE is set to '1' (D0h, TX_BIASLOOP_CONTROL, bit 7) then the modulation DAC is set directly from a register (D4h, MOD_DAC).

If MOD_TEMP_DISABLE is set to '0' then a 64 byte LUT is used to set the modulation DAC. The LUT is indexed by the temperature ADC (E1h, TEMP_ADC_VALUE), where the index is given by:

Index = (temperature ADC x 64)/255.

The values of the LUT reside in the EEPROM, between addresses 80h (lowest temperature entry) and BFh (highest temperature entry), and are transferred at start up to on-chip registers.

The active setting for the modulation DAC can be observed by reading MOD_DAC_OBSERVE (F0h).

Parameter	Comments	Step Size	DAC Range	Operational Range
IMOD_DAC	Modulation current DAC (8 bits)	0.375mA (±187µA)	0 to 96mA	0mA to 80mA

Table 3 - Modulation DAC Characteristics

4.3.2. Bias Current Control

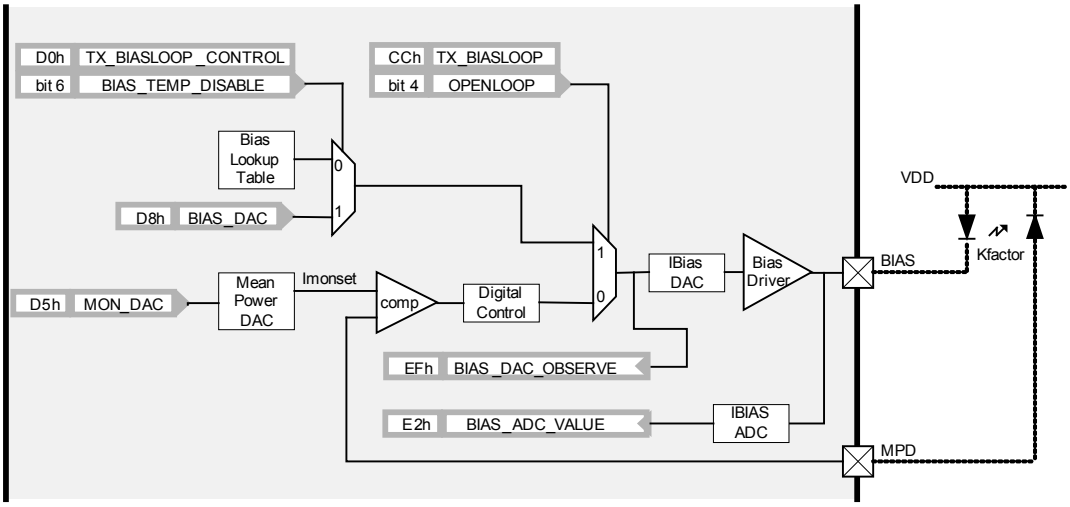


Figure 12 - Bias Current Generation

The PHY2078 can operate with open or closed loop bias control. In either mode the current setting for the bias DAC can be observed by reading BIAS_DAC_OBSERVE (EFh).

The bias current level is measured using an on-chip ADC and can be observed by reading BIAS_ADC_VALUE (E2h).

Parameter	Comments	Step Size	ADC Range	Operational Range
IBIAS_ADC	Bias current ADC (8 bits)	0.588mA (±0.294mA)	0 to 150mA	0mA to 90mA

Table 4 - Bias ADC Characteristics

Parameter	Comments	Step Size	DAC Range	Operational Range
IBIAS_DAC	Bias current DAC (8 bits)	0.392mA (±0.196mA)	0 to 100mA	0mA to 90mA

Table 5 - Bias DAC Characteristics

4.3.3. Open Loop

If OPENLOOP is set to '1' (CCh, TX_BIASLOOP, bit 4) the bias generator operates in open loop mode. The bias current can be either set by a constant register value or controlled by a temperature indexed lookup table (LUT).

If BIAS_TEMP_DISABLE is set to '1' (D0h, TX_BIASLOOP_CONTROL, bit 6) then the bias DAC is set directly from a register (D8h, BIAS_DAC).

If BIAS_TEMP_DISABLE is set to ‘0’ then a 128 byte LUT is used to set the bias DAC. The LUT is indexed by the temperature ADC (E1h), where the index is given by:

Index = (temperature ADC x 128)/255.

The values for the LUT reside in the EEPROM, between addresses 00h (lowest temperature entry) and 7Fh (highest temperature entry), and are loaded into on-chip registers at start up.

In open loop mode the MPD device pin is not used and can be left unconnected.

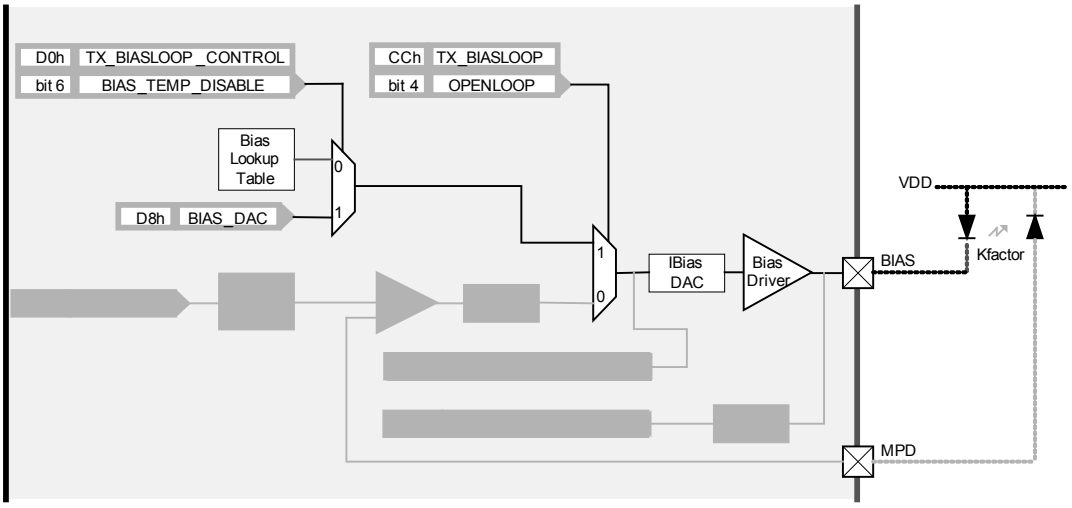


Figure 13 - Bias Current Generation, Open Loop

4.3.4. Closed Loop

If OPENLOOP is set to ‘0’ the bias generator operates in closed loop mode. The average output power of the laser is controlled by a digital mean power control loop. The feedback to the control loop is provided by a monitor photodiode connected to MPD. The current from the monitor photodiode is compared with a reference current (Imonset). This is output by the mean power DAC and controlled by MON_DAC (D5h).

In order to provide the required resolution and range the mean power DAC has three step sizes as shown in the table below.

Parameter	Comments	Step Size and Resolution	Range
Imonset	Mean power DAC (8 bits).	MON_DAC ≤ 31 = 1.042µA (±0.5µA) 32 ≤ MON_DAC ≤ 127 = 4.167µA (±2µA) MON_DAC ≥ 128 = 16.67µA (±8µA)	0 to 2.55mA

Table 6 - Mean Power DAC Characteristics

The 3dB frequency of the digital mean power control loop is controlled by the size of a prescaling counter and can be determined (in Hertz) by:

F_{3dB} = (Kfactor x 692) / (M x Imonset)

where Kfactor = laser current to monitor photodiode current coupling coefficient

Imonset = desired monitor photodiode current (A)

$M = 2^{(2 \times prescale\_size)}$

Prescale_size is set by (D0h, TX_BIASLOOP_CONTROL, bits 2:0).

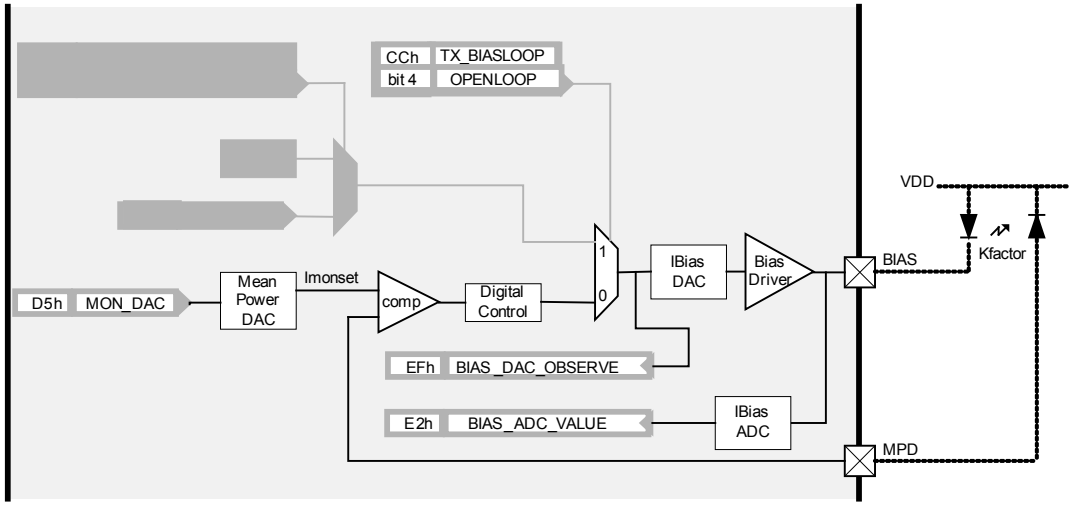


Figure 14 - Bias Current Generation, Closed Loop

4.3.5. Initial Start-up

At power up or after TX_DISABLE is de-asserted the PHY2078 can use a fast startup algorithm to quickly settle the mean power control loop to the desired bias level. The algorithm can only be invoked in closed loop, DC-coupled mode and after it has completed the low bandwidth digital mean power control loop takes over to maintain the optical output power. The details of the startup algorithm and its parameters are described in section 8.5.

4.3.6. Burst Mode and Power Saving

In burst mode operation de-asserting the BEN+/- inputs causes the mean power control loop to pause and turning off the bias current. This mode of operation saves power compared with burst laser drivers that maintain a diverted bias current during burst off. The saving can be up to 95% of the bias and modulation current during burst off periods for a system with a split ratio of 16:1. Re-asserting the BEN+/- input re-enables the modulation current and releases the mean power control loop such that the bias current from the end of the preceding burst is used as the start point for the next burst. The burst on/off timings are detailed in the electrical timings section.

The polarity of the BEN+/- inputs can be inverted using BURST_POLARITY (CAh, TX_DBUFF, bit 2).

4.3.7. Laser Driver Setup

There is a trimming network on the output driver which adjusts the time constant of the output damping on LASER+/-. It is controlled by the value in TX_DRIVER_CAP (C9h). Table 7 contains the valid register settings and the damping time constant they set, where RC = 16.8ps.

TX_DRIVE_CAP value	Time Constant
00h	0
01h	RC
02h	3RC
04h	5RC
08h	6RC
10h	7RC
20h	8RC

Table 7 - Time constant selection for the transmit output damping network

4.3.8. Performance Monitoring

As part of its main control loop the PHY2078 monitors temperature and transmit bias current via an on-chip ADC. The ADC values are reported via registers TEMP_ADC_VALUE (E1h) and BIAS_ADC_VALUE (E2h).

The user has the option of using the measured values of temperature and bias current to set alarm bits. These are generated if the values measured are above or below programmable limits. The conditions are shown in Table 8 and 9 below.

TEMP_MAX_ALARM_EN (DAh ALARM_EN bit 3)	TEMP_MIN_ALARM_EN (DAh ALARM_EN bit 2)	CONDITION	TEMP_MAX_ERROR (EAh bit7)	TEMP_MIN_ERROR (EAh bit 6)
1	X	TEMP_ADC_VALUE > TEMP_MAX (DBh)	1	0
X	X	TEMP_MIN (DCh)< TEMP_ADC_VALUE < TEMP_MAX (DBh)	0	0
X	1	TEMP_ADC_VALUE < TEMP_MIN (DCh)	0	1
0	0	X	0	0

Table 8 - Over and under temperature alarm generation

BIAS_MAX_ALARM_EN (DAh ALARM_EN bit 1)	BIAS_MIN_ALARM_EN (DAh ALARM_EN bit 0)	CONDITION	BIAS_MAX_ERROR (EAh bit 5)	BIAS_MIN_ERROR (EAh bit 4)
1	X	BIAS_ADC_VALUE > BIAS_MAX (DDh)	1	0
X	X	BIAS_MIN (DEh) < BIAS_ADC_VALUE < BIAS_MAX (DDh)	0	0
X	1	BIAS_ADC_VALUE < BIAS_MIN (DEh)	0	1
0	0	X	0	0

Table 9 - Bias current alarm generation

An out of range monitored temperature (TEMP_MAX_ERROR is set to '1' or TEMP_MIN_ERROR is set to '1') will cause a TX_FAULT condition to be raised.

An out of range monitored bias current (BIAS_MAX_ERROR is set to '1' or BIAS_MIN_ERROR is set to '1') will cause a TX_FAULT condition to be raised.

The response of the PHY2078 to an alarm condition is described in Section 4.4.

4.4. Laser Safety Features

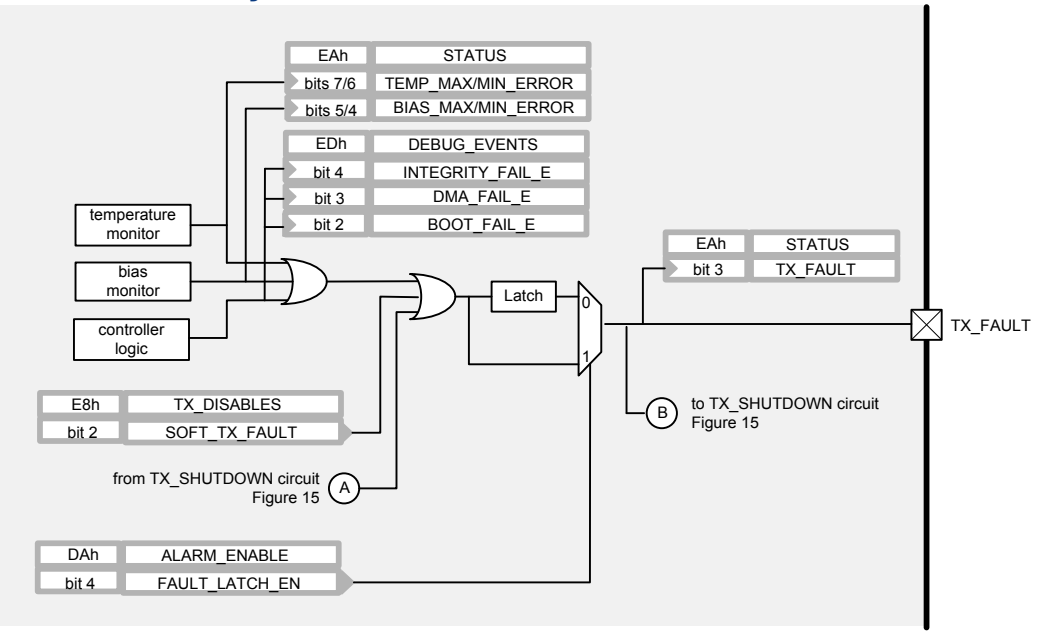


Figure 15 - Transmit Fault Generation

The laser safety circuit monitors the device for potential faults. If a fault is detected the pin TX_FAULT is asserted.

The register bit TX_FAULT (EAh, STATUS, bit 3) reflects the status of the pin TX_FAULT.

Using bias alarm requires FAULT_LATCH_ENABLE to be set to 0.

A transmit fault can be raised by the following:

1. The temperature monitor detects that the measured temperature has gone out of range (see section 4.3.8).

2. The bias current monitor detects that the measured transmit bias current has gone out of range (see section 4.3.8).

3. The internal controller logic detects that a DMA from EEPROM has failed (see section 5.1)

4. The SOFT_TX_FAULT bit (E8h, TX_DISABLES, bit 2) is set to '1'

5. The voltage reference monitoring circuit detects that the reference voltage is incorrect

6. The supply monitoring circuit detects that the power supply voltage is incorrect

If FAULT_LATCH_EN = '0' (DAh, ALARM_ENABLE, bit 4) then a transmit fault condition will cause the TX_FAULT pin to stay asserted even if the fault condition goes away. The pin will stay asserted until either the chip is power cycled or the pin TX_DISABLE is set to '1' or the register SOFT_TX_DISABLE is set to '1' (E8h, TX_DISABLES, bit 1) or FAULT_LATCH_EN is set to '1'.

If FAULT_LATCH_EN = '1' then the TX_FAULT pin is deasserted when the fault condition goes away.

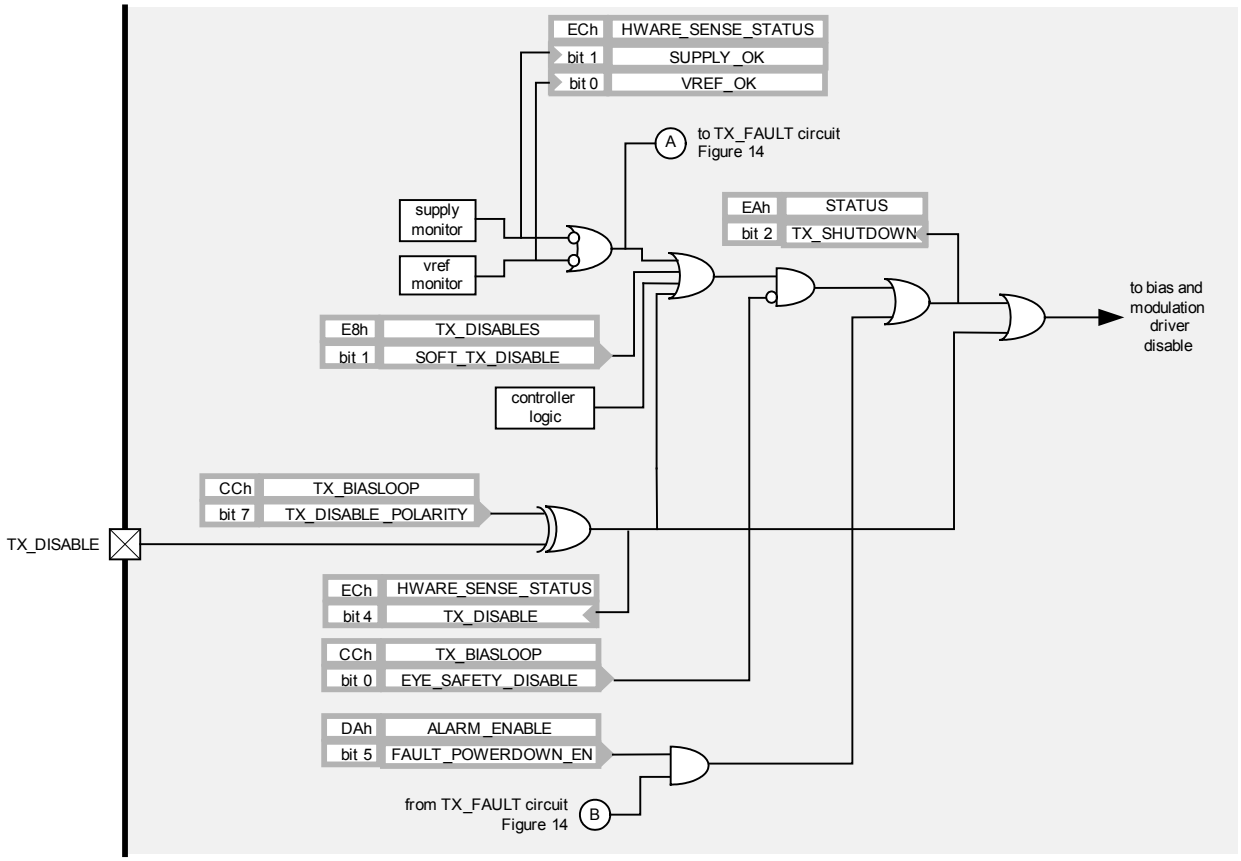


Figure 16 - Transmit Shutdown Generation

The PHY2078 contains circuitry to shutdown the transmitter bias and modulation current if a problem is detected. The conditions to cause a shutdown are:

1. The voltage reference monitoring circuit detects that the reference voltage is incorrect

2. The supply monitoring circuit detects that the power supply voltage is incorrect

3. The SOFT_TX_DISABLE bit (E8h, TX_DISABLES, bit 1) is set to ‘1’

4. The internal controller logic has not successfully completed its initialisation (see section 5.1)

5. The pin TX_DISABLE is asserted

6. TX_FAULT is active and FAULT_POWERDOWN_EN = ‘1’ (DAh ALARM_EN bit 5)

If a shutdown condition occurs the modulation and bias currents are disabled. Conditions 1-4 can be disabled from contributing to shutdown by setting EYE_SAFETY_DISABLE = ‘1’ (CCh, TX_BIASLOOP, bit 0). This feature should be used with great caution.

The polarity of the TX_DISABLE pin can be inverted by setting TX_DISABLE_POLARITY (CCh, TX_BIASLOOP, bit 7).

The register bit TX_SHUTDOWN (EAh, STATUS, bit 2) reflects the status of the shutdown circuit.

The register bit TX_DISABLE (ECh, HWARE_SENSE_STATUS, bit 4) reflects the status of the pin TX_DISABLE (after optional inversion using TX_DISABLE_POLARITY).

4.5. Temperature Measurement

The PHY2078 uses an on-chip 8 bit ADC to perform a temperature measurement once per iteration of its main control loop (approximately every 10ms). The measured ADC value can be read from register TEMP_ADC_VALUE (E1h). This measurement can be used to control the modulation and bias currents.

The temperature is determined by forcing two different currents through a diode connected transistor (base and collector shorted together) measuring the resulting voltage difference, ΔV_{BE}. This voltage is directly proportional to the temperature. If NPN_INTERNAL is set to '1' (CBh, TX_TEMPSENSE, bit 1) then an on-chip transistor is used. In this case pin TSENSE should be left unconnected. If NPN_INTERNAL is set to '0' then the ADC uses a suitable external device connected to pin TSENSE. The transistor can be any standard npn silicon transistor with a beta > 100, however Phyworks recommends using a BC847B or similar. Where accuracy improvement is needed calibration and averaging of the temperature sensor values are recommended or use of an external temperature sensor such as that in a microcontroller.

SELECT_3I (CBh, TX_TEMPSENSE, bit 0) and VTOISLOPESEL (CBh, TX_TEMPSENSE, bits 2 - 3) can be adjusted, depending on the external device used, to ensure that the PHY2078 is capable of measuring the required range of temperatures.

The temperature sensor operating range is shown in Table 10.

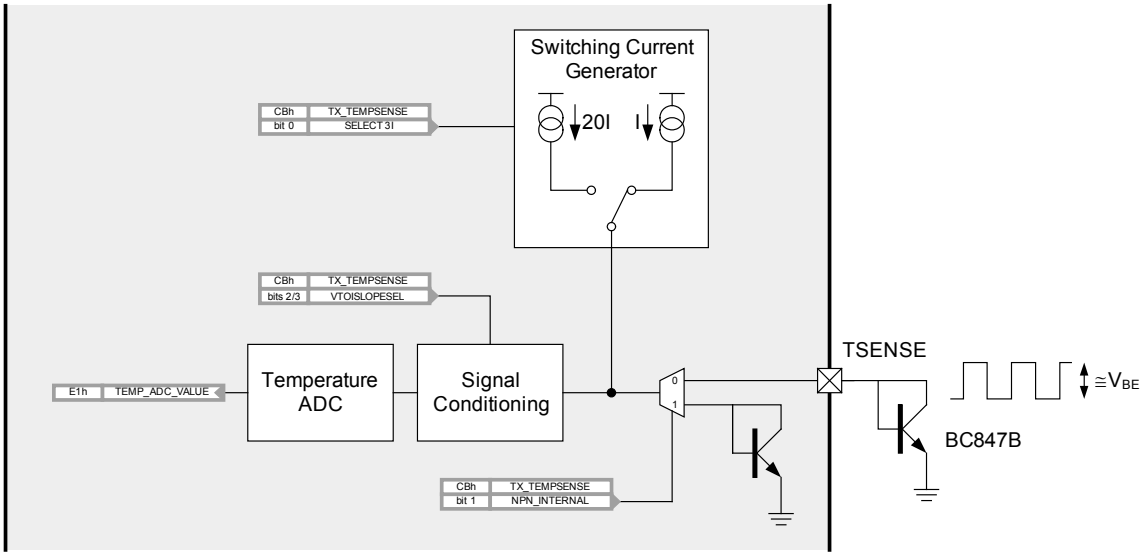


Figure 17 – Temperature sensor functional block diagram

Parameter	Comment	Symbol	Min	Typical	Max	Units
Temperature		T	-45		90	°C
ADC slope	VTOISLOPESEL = 00			0.67		°C/bit
	VTOISLOPESEL = 01			1.32		°C/bit
	VTOISLOPESEL = 10			1.63		°C/bit
	VTOISLOPESEL = 11			2.25		°C/bit
TSENSE delta input voltage	VTOISLOPESEL = 00	ΔV_{BE}	50		100	mV

Table 10 – Internal Temperature Measurement

5. Control Interface

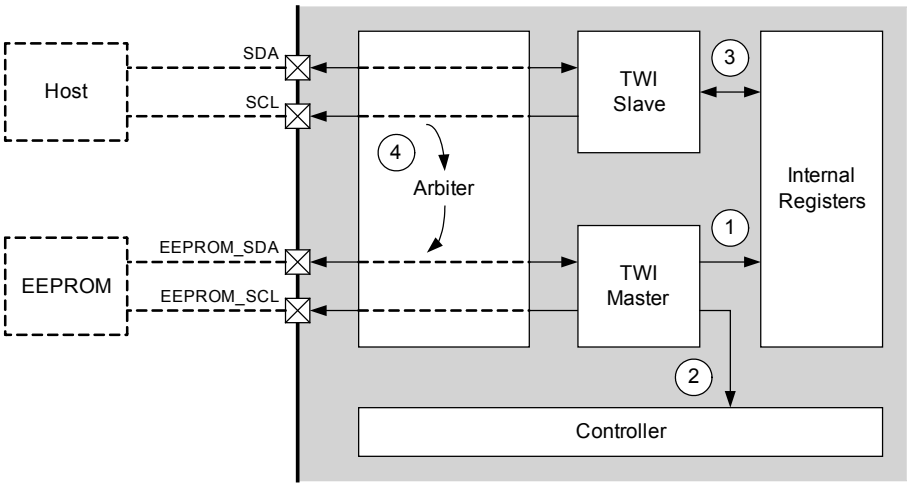


Figure 18 - Serial interfaces to internal registers

The host communicates with the PHY2078 and the EEPROM via the slave Two Wire Interface (TWI) pins of the PHY2078. Slave addresses A0h and A2h are supported, register settings for PHY2078 are stored in A2h. If a transaction arriving at the slave interface is addressed to A2h, then the PHY2078 examines the register address in order to decide how the transaction should be processed (see address map in figure 19).

- If the register is implemented in EEPROM only (addresses 00h to BFh) then the transaction is forwarded to the EEPROM via path 4 in figure 18. There is a direct combinational logic path between the slave and master interfaces which makes the PHY2078 transparent when transactions from the host are forwarded to the EEPROM.
- If the register is only implemented internally to the PHY2078 (addresses E0h to FFh) then the data is written to or read from the registers inside the PHY2078 (path 3).
- If the register is implemented both internally and EEPROM (addresses C0h to DFh) then the PHY2078 checks the INTERNAL_ACCESS register bit (E7h INTERNAL bit 1) to determine whether the host wishes to access the EEPROM or internal registers. Set INTERNAL_ACCESS is set to ‘1’ to access the internal registers and ‘0’ to access the EEPROM.

When the PHY2078 comes out of reset, the state machine uses the master two wire interface to read configuration bytes out of EEPROM. This data is used to configure the internal registers of the device (path 1).

Subsequently, during normal operation the state machine will use the master interface to periodically access look-up table and alarm threshold information stored in the EEPROM (path 2). In order to prevent collisions between state machine and host accesses to EEPROM, the host must always stop the state machine before attempting to access the EEPROM by setting an internal register bit, SM_STOP, to ‘1’ (E7h, INTERNAL, bit 0). When the host has completed its transactions with the EEPROM it must set SM_STOP to ‘0’ to allow normal operation of the state machine to resume. If the host attempts to access the EEPROM when SM_STOP is set to ‘0’ then writes are ignored and reads return a zero.

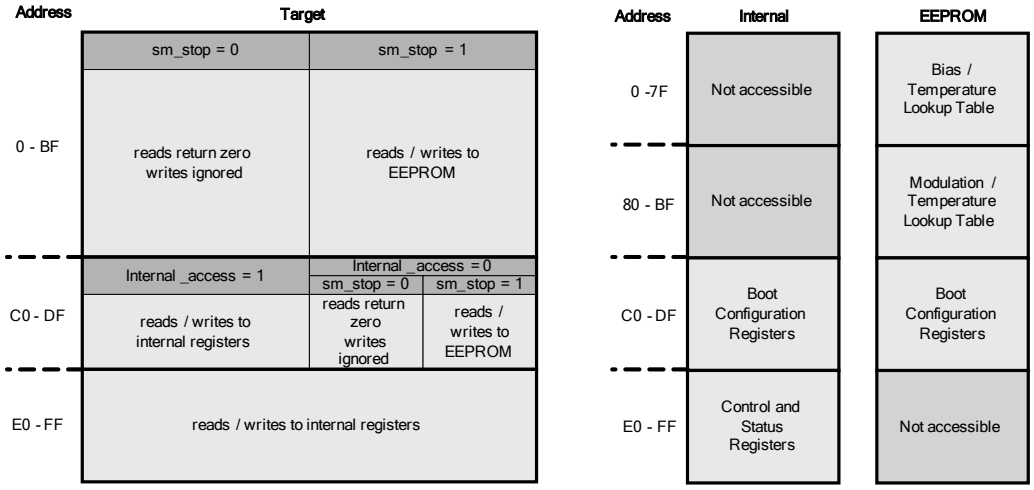


Figure 19 - PHY2078 TWI Slave Accesses

5.1. Boot Sequence

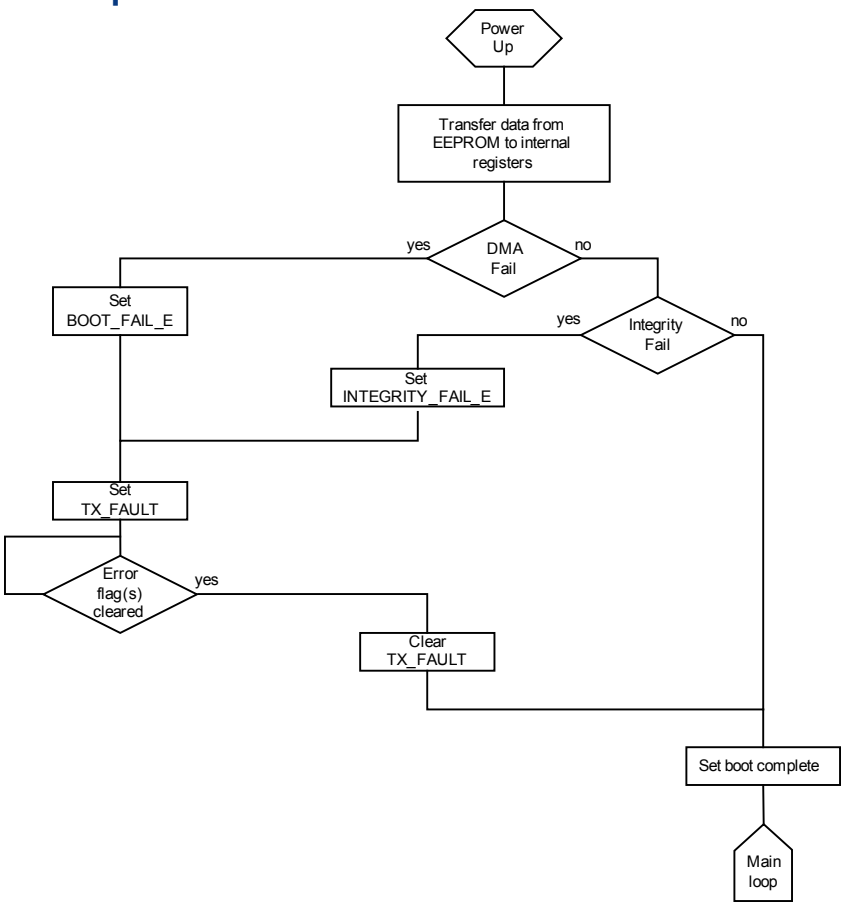


Figure 20 - PHY2078 Boot Sequence

At power up the PHY2078 attempts to read a number of bytes of configuration information from an external EEPROM into its internal registers.

If the read fails due to a problem on the TWI, such as a read not being correctly acknowledged, the state machine sets register bit BOOT_FAIL_E to ‘1’ (EDh, DEBUG_EVENTS, bit 2), raises a transmit fault condition and remains in an error state.

The first two bytes read from EEPROM, C0h and C1h, are compared against a data integrity number (C35Ah). If the compare fails, the state machine sets register bit INTEGRITY_FAIL_E to ‘1’ (EDh, DEBUG_EVENTS, bit 4), raises a transmit fault condition and remains in an error state.

In the error state the host is able to configure the internal registers of the PHY2078 using the slave TWI. When it has completed configuration the host must clear the active error(s) by writing a ‘1’ to the corresponding bit(s). When the state machine sees that the error bit(s) are cleared it clears the transmit fault condition.

The state machine sets the register BOOT_COMPLETE_E (EDh, DEBUG_EVENTS, bit 1) to indicate that the boot process is complete and then enters the main control loop.

5.2. Main Control Loop

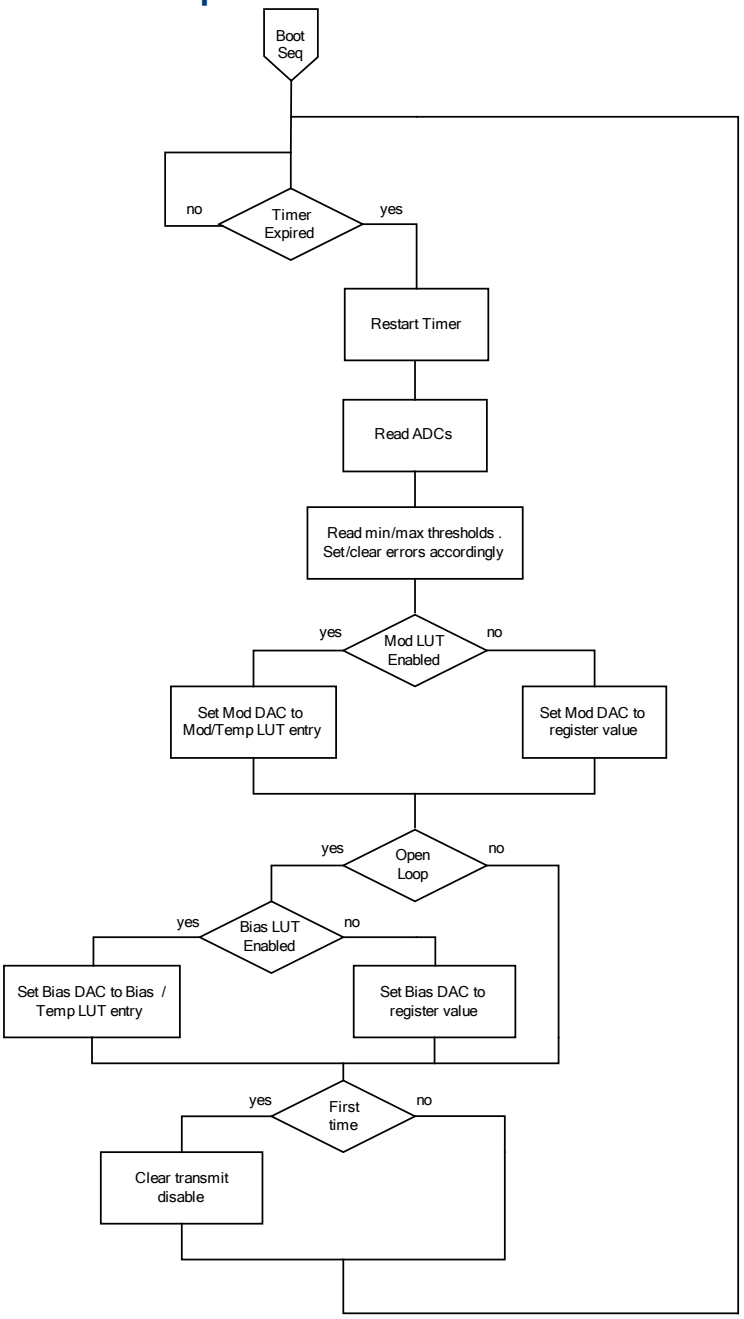


Figure 21 - PHY2078 Main Loop Function

A loop timer is implemented in the state machine to ensure that the start of each iteration of the loop is separated by 10ms.

When the timer has expired the state machine reads the on-chip ADC to obtain temperature and bias current levels, reads alarm levels out of EEPROM and sets/clears performance alarms accordingly.

The state machine then sets the modulation current and bias current.

At the end of the first iteration of the loop after boot-up the state machine clears transmit disable to enable the transmit data path.

5.3. 2-wire Serial Interface

The PHY2078 has a pair of 2-wire serial interfaces: a slave for interfacing to a host for module setup and programming, and a master for interfacing to an external EEPROM and for device configuration after reset. Both interfaces communicate using the protocol described in this section.

5.3.1. Framing and Data Transfer

The two-wire interface comprises a clock line (SCL) and a data line (SDA). When the bus is idle both are pulled high within the PHY2078 by 8kΩ pull-ups.

An individual transaction is framed by a start condition and a stop condition. A start condition occurs when a bus master pulls SDA low while the clock is high. A stop condition occurs when the bus master allows SDA to transition low-to-high when the clock is high. Within the frame, the master has exclusive control of the bus. The PHY2078 supports REPEAT START conditions whereby the master may simultaneously end one frame and start another without releasing the bus by replacing the STOP condition with a START condition.

Within a frame, the state of SDA may only change when SCL is low. A data bit is transferred on a low-to-high transition of SCL. Data is arranged in packets of 9 bits. The first 8 bits represent data to be transferred (most significant bit first). The last bit is an acknowledge bit. The recipient of the data holds SDA low during the ninth clock cycle of a data packet to acknowledge (ACK) the byte. Leaving SDA to float high on the ninth bit signals a not-acknowledged (NACK) condition. The interpretation of the acknowledge bit by the sender will depend on the type of transaction and the nature of the byte being received.

5.3.2. Device Addressing

The first byte to be sent after a START condition is an address byte. The first seven bits of the byte contain the target slave address (msb first). The eighth bit indicates the transaction type – '0' = write, '1' = read. Each slave interface on the bus is assigned a 7-bit slave address. If no slave matches the address broadcast by the master then SDA will be left to float high during the acknowledge bit and the master receives a NACK. The master must then assert a STOP condition. If a slave identifies the address then it acknowledges the master and proceeds with the transaction identified by the type bit.

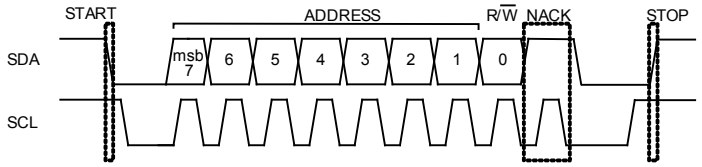


Figure 22 - Address decoding example – slave not available

5.3.3. Write Transaction

Figure 23 shows an example of a write transaction. The address byte is successfully acknowledged by the slave, and the type bit is set low to signify a write transaction. After the acknowledge the master sends a single data byte. All signalling is controlled by the master except for the SDA line during the acknowledge bits. During the acknowledge the direction of the SDA line is reversed and the slave pulls SDA low to return a '0' (ACK) to the master.

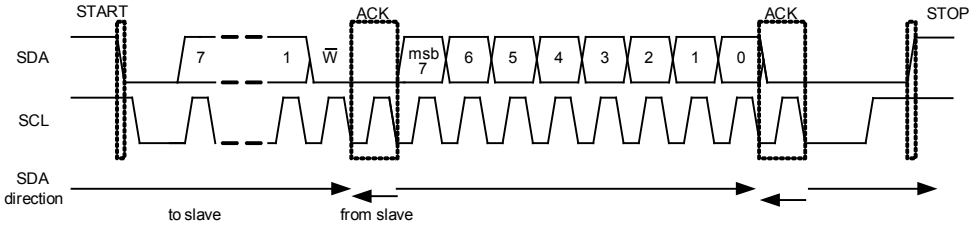


Figure 23 - Write transaction

If the slave is unable to receive data then it should return a NACK after the data byte. This will cause the master to issue a STOP and thus terminate the transaction.

The PHY2078 interprets the first data byte as a register address. This will be used to set an internal memory pointer. Subsequent data bytes within the same transaction will then be written to the memory location addressed by the pointer. The pointer is auto-incremented after each byte. There is no limit to the number of bytes which may be written in a single burst to the internal RAM of the PHY2078. If, however, the write access is destined for the EEPROM the requirements of page writes specified for the EEPROM apply.

If the slave is not ready to receive a byte then it may hold SCL low immediately after the acknowledge bit. When SCL is released the master starts to send the next byte. This is known as clock stretching. The PHY2078 slave interface will not clock stretch at up to 100 kHz SCL frequency.

5.3.4. Read Transaction

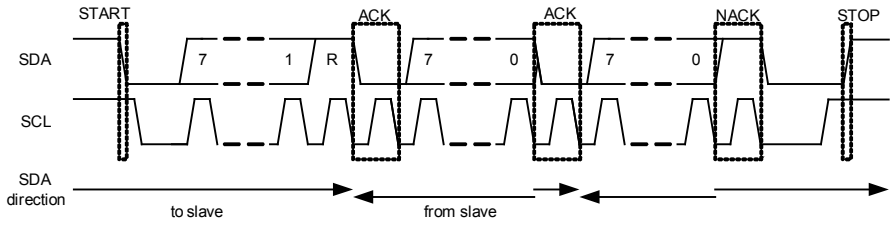


Figure 24 - Read transaction

Figure 24 shows an example of a 2 byte read transaction. The address byte is successfully acknowledged by the slave, and the type bit is set high to signify a read. After the ACK the slave returns a byte from the location identified by the internal memory pointer. This pointer is then auto-incremented. The slave then releases SDA so that the master can ACK the byte. If the slave receives an ACK then it will send another byte. The master identifies the last byte by sending a NACK to the slave. The master then issues a STOP to terminate the transaction.

Thus, to implement a random access read transaction, a write must first be issued by the master containing a slave address byte and a single data byte (the register address) as shown in Figure 23. This sets up the memory pointer. A read is then sent to retrieve data from this address (see Figure 24).

6. Register Map

Where a single power-on reset (PoR) value is shown for a range of addresses, that value applies to all bytes in the range. Note that the power on reset values may be overwritten during initialisation from the EEPROM.
For registers containing a single 8-bit field, the most significant bit of the field is stored in bit 7 of the register byte.
Note that 'reserved' or 'internal use only' register bits are specified as read only. These registers should not changed from their PoR default settings.

R Bit is read only. A write to this bit via the TWI will have no effect. The value may be changed by the device itself as part of its normal operation

R/W Bit is readable and writable via the TWI. The value will not be changed by the device itself except under a device reset.

E Bit is readable via the TWI. The bit may be set by the device itself as part of its normal operation. Once set the bit may be cleared by writing a '1' via the TWI. Writing a '0' via the TWI has no effect.

C0h	**DATA_INTEGRITY_LOWER**			Integrity check for EEPROM contents. Must be set to C3h for a boot load from EEPROM to be successful. Note, this register exists only in EEPROM and not in the internal registers of the device, therefore a write to this address when 'INTERNAL_ACCESS' is set high will be ignored and a read return zero.
Type	R/W	PoR	00h	

C1h	**DATA_INTEGRITY_UPPER**			Integrity check for EEPROM contents. Must be set to 5Ah for a boot load from EEPROM to be successful. Note, this register exists only in EEPROM and not in the internal registers of the device, therefore a write to this address when 'INTERNAL_ACCESS' is set high will be ignored and a read return zero.
Type	R/W	PoR	00h	

C2h	**RX_AGC**			This register controls functions in the AGC in the receive path of the device
Bit	Field name	Type	PoR	
7	-	R	0	reserved
6	-	R	0	reserved
5	-	R	0	reserved
4	-	R	0	reserved
3	LOS_TO_ SQUELCH	R/W	0	Setting this bit to a '1' connects the LOS function to the receiver squelch such that a LOS will automatically disable the receiver output
2	RX_SQUELCH	R/W	0	Setting this bit to a '1' causes the receiver output to be disabled
1	-	R/W	0	Internal use only. Must be set to '0'
0	-	R/W	0	Internal use only. Must be set to '0'

C3h	RX_LIMITER			This register controls functions in the limiter in the receive path of the device
Bit	Field name	Type	PoR	
7	-	R	0	reserved
6	-	R	0	reserved
5	-	R	0	reserved
4	-	R	0	reserved
3	-	R	0	reserved
2	-	R/W	0	Internal use only. Must be set to ‘0’
1	RX_POLARITY	R/W	0	Setting this bit to a ‘1’ causes the receive output polarity to be inverted
0	-	R/W	0	Internal use only. Must be set to ‘0’

C4h	RX_FILTER			This register controls functions in the filter in the receive path of the device
Bit	Field name	Type	PoR	
7	-	R	0	reserved
6	-	R	0	reserved
5	-	R	0	reserved
4	-	R	0	reserved
3	-	R/W	0	Internal use only. Must be set to ‘0’
2	RATE_SELECT(2)	R/W	0	Selects the filter rate in the receiver ’000’ = 155 Mbps ’001’ = 622 Mbps ’010’ = Reserved ‘011’ = 1250 Mbps ‘100’ = 2488 Mbps
1	RATE_SELECT(1)	R/W	0	
0	RATE_SELECT(0)	R/W	0	

C5h	RX_DRIVER			This register controls functions in the output driver in the receive path of the device
Bit	Field name	Type	PoR	
7	-	R	0	reserved
6	-	R	0	reserved
5	-	R	0	reserved
4	-	R	0	reserved
3	-	R	0	reserved
2	-	R	0	reserved
1	CML_SLEW	R/W	0	Sets the receiver output slew rate ’1’ = slow ’0’ = fast
0	CML_LEVEL	R/W	0	Sets the receiver output swing level ’1’ = low swing ’0’ = high swing

C6h	RX_MUXPOL			This register controls the loss of signal detection circuit in the receive path of the device
Bit	Field name	Type	PoR	
7	-	R	0	reserved
6	-	R	0	reserved
5	-	R	0	reserved
4	-	R	0	reserved
3	-	R	0	reserved
2	-	R	0	reserved
1	OMAHYSTSEL	R/W	0	Sets the amount of hysteresis in the LOS detection circuit '1' = 4 dB of hysteresis '0' = 3 dB of hysteresis
0	MUX_POLARITY	R/W	0	Sets the polarity of LOS output pin '1' = Pin is high when signal detect '0' = Pin is high when loss of signal

C7h	TEST0			Internal use only, must be set to 00h
Type	R/W	PoR	00h	

C8h	TEST1			Internal use only, must be set to 00h
Type	R/W	PoR	00h	

C9h	TX_DRIVER_CAP			This register allows selective snubbing capacitors to be applied to the transmit output stage. Setting the register to 0h applies no damping.
Type	R/W	PoR	00h	

CAh	TX_DBUFF			This register controls functions in the data buffer in the transmit path of the device
Bit	Field name	Type	PoR	
7	-	R	0	reserved
6	-	R	0	reserved
5	-	R	0	reserved
4	HIGH_EXT(1)	R/W	0	This register controls the pedestal current I_{ped} to allow high extinction ratios to be set with consequently reduced rise time. '00' : default, I_{ped} = 0μA, low ER, higher speed '01' : I_{ped} = 130μA '10' : I_{ped} = 390μA '11' : I_{ped} = 520μA, high ER, lower speed
3	HIGH_EXT(0)	R/W	0	
2	BURST_ POLARITY	R/W	0	Setting this bit inverts the polarity of the burst enable input pins
1	-	R/W	0	Internal use only. Must be set to '0'
0	TX_POLARITY	R/W	0	Setting this bit to a '1' causes the transmit output polarity to be inverted

CBh	TX_TEMPSENSE			This register controls functions associated with the device temperature measurement
Bit	Field name	Type	PoR	
7	-	R	0	reserved
6	-	R	0	reserved
5	-	R	0	reserved
4	-	R	0	reserved
3	VTOISLOPESEL(1)	R/W	0	This field modifies the expected slope from the temperature sensor into the ADC and should be set depending on the type of external temperature sensor
2	VTOISLOPESEL(0)	R/W	0	
1	NPN_INTERNAL	R/W	0	Setting this bit to '1' selects the internal sensor for temperature measurement. Setting to '0' selects an external sensor connected to the TSENSE input pin
0	SELECT_3I	R/W	0	Setting this bit to '1' causes the temperature sensor to operate at 3 times the default measurement current.

CCh	TX_BIASLOOP			This register controls functions in the bias current generator in the transmit path of the device
Bit	Field name	Type	PoR	
7	TX_DISABLE_ POLARITY	R/W	0	Setting this bit to a '1' inverts the polarity of the TX_DISABLE input pin
6	-	R/W	0	Internal use only. Must be set to '0'
5	-	R/W	0	Internal use only. Must be set to '0'
4	OPENLOOP	R/W	0	Sets the configuration of the transmit bias circuit '1' = open loop '0' = closed loop
3	-	R/W	0	Internal use only. Must be set to '0'
2	-	R/W	0	Internal use only. Must be set to '0'
1	-	R/W	0	Internal use only. Must be set to '0'
0	RESERVED	R/W	0	Set to '0' during operation of the device

CDh	TEST2			Internal use only, must be set to 00h
Type	R/W	PoR	00h	

CEh	DAC_PWRD			
Bit	Field name	Type	PoR	
7	-	R	0	reserved
6	-	R	0	reserved
5	RINTERNAL	R/W	0	Set to '1', an internal 10kΩ resistor is used for generating the reference voltage.
4	-	R/W	0	Internal use only, must be set to 0
3	-	R/W	0	Internal use only, must be set to 0
2	-	R/W	0	Internal use only, must be set to 0
1	-	R/W	0	Internal use only, must be set to 0
0	-	R/W	0	Internal use only, must be set to 0

CFh	TEST3			Internal use only, must be set to 00h
Type	R/W	PoR	00h	

D0h	TX_BIASLOOP_CONTROL			This register controls generation of the transmit bias current
Bit	Field name	Type	PoR	
7	MOD_TEMP_ DISABLE	R/W	0	Setting this bit to '1' disables the modulation current / temperature lookup table
6	BIAS_TEMP_ DISABLE	R/W	0	In open loop mode setting this bit to '1' disables the bias current / temperature lookup table. In closed loop mode it has no effect
5	BURST_START_ FACTOR(1)	R/W	0	These bits control the ramp rate used in the closed loop bias current fast startup algorithm. See section 8.5 for further details
4	BURST_START_ FACTOR(0)	R/W	0	
3	BIAS_STARTUP_ BYPASS	R/W	0	Setting this bit to '1' disables the fast startup algorithm used for closed loop bias current generation
2	PRESCALE_ SIZE(2)	R/W	0	These bits configure the loop bandwidth of the closed loop bias current. See the section 4.3.4 for further details
1	PRESCALE_ SIZE(1)	R/W	0	
0	PRESCALE_ SIZE(0)	R/W	0	

D1h	TX_BURST_CONTROL			This register controls the fast startup algorithm used in the generation of bias current in closed loop mode
Bit	Field name	Type	PoR	
7	-	R	0	reserved
6	-	R	0	reserved
5	-	R	0	reserved
4	-	R	0	reserved
3	BS_OPTIMISE	R/W	0	Setting this bit to '1' allows the fast startup algorithm used for closed loop bias current generation to perform an optimisation during its first binary step
2	BINARY_SEARCH_WIDTH(2)	R/W	0	These bits control the length of time that each step of the binary search sequence of the closed loop bias current fast startup algorithm take to complete. See section 8.5 for further details
1	BINARY_SEARCH_WIDTH(1)	R/W	0	
0	BINARY_SEARCH WIDTH(0)	R/W	0	

D2h	RAMP_STEP_FACTOR			This register controls the ramp rate used in the closed loop bias current fast startup algorithm. See section 8.5 for further details
Type	R/W	PoR	00h	

D3h	VREF_DAC			Reference voltage trim DAC. **Set to 71h**
Type	R/W	PoR	00h	

D4h	MOD_DAC			Sets the modulation current (via a DAC) when the Modulation / Temperature LUT is disabled (MOD_TEMP_DISABLE is set to '1').
Type	R/W	PoR	00h	

D5h	MON_DAC			Sets the target bias current level (via a DAC) when the device is in closed loop configuration (OPENLOOP is set to '0')
Type	R/W	PoR	00h	

D8h	BIAS_DAC			Sets the bias current (via a DAC) when the device is in open loop configuration (OPENLOOP is set to '1') and the Bias / Temperature LUT is disabled (BIAS_TEMP_DISABLE is set to '1')
Type	R/W	PoR	00h	

D9h	OMA_DAC			Sets the threshold level for optical measurement amplitude based LOS detection.
Type	R/W	PoR	00h	

DAh	ALARM_ENABLE			Controls the behaviour of the TX_FAULT pin and the generation of alarms based on temperature and bias current levels.
Bit	Field name	Type	PoR	
7	-	R	0	reserved
6	-	R	0	reserved
5	FAULT_POWERDOWN_EN	R/W	0	If this bit is set to '1' a TX_FAULT condition will cause the transmitter modulation and bias currents to be shutdown
4	FAULT_LATCH_EN	R/W	0	If this bit is set to a '0' the output pin TX_FAULT will remain asserted once a fault condition has been detected even if the fault condition goes away. The pin will remain asserted until either the device is reset or this bit is set to a '1'. If this bit is set to a '1' then the output pin TX_FAULT will be asserted if a fault condition is detected and will be deasserted once the condition is cleared.
3	TEMP_MAX_ALARM_EN	R/W	0	Set this bit to a '1' to enable alarm generation if the measured temperature exceeds TEMP_MAX
2	TEMP_MIN_ALARM_EN	R/W	0	Set this bit to a '1' to enable alarm generation if the measured temperature falls below TEMP_MIN
1	BIAS_MAX ALARM_EN	R/W	0	Set this bit to a '1' to enable alarm generation if the measured bias current exceeds BIAS_MAX
0	BIAS_MIN_ALARM_EN	R/W	0	Set this bit to a '1' to enable alarm generation if the measured bias current falls below BIAS_MIN

DBh	TEMP_MAX			If TEMP_MAX_ALARM_EN is set then this register sets the threshold above which a maximum temperature error is raised based on the internal ADC reading. Note, this register exists only in EEPROM and not in the internal registers of the device, therefore a write to this address when 'INTERNAL_ACCESS' is set high will be ignored and a read return zero.
Type	R/W	PoR	00h	

DCh	TEMP_MIN			If TEMP_MIN_ALARM_EN is set then this register sets the threshold below which a minimum temperature error is raised based on the internal ADC reading. Note, this register exists only in EEPROM and not in the internal registers of the device, therefore a write to this address when 'INTERNAL_ACCESS' is set high will be ignored and a read return zero.
Type	R/W	PoR	00h	

DDh	BIAS_MAX			If BIAS_MAX_ALARM_EN is set then this register sets the threshold above which a maximum bias current error is raised based on the internal ADC reading. Note, this register exists only in EEPROM and not in the internal registers of the device, therefore a write to this address when 'INTERNAL_ACCESS' is set high will be ignored and a read return zero.
Type	R/W	PoR	00h	

DEh	BIAS_MIN			If BIAS_MIN_ALARM_EN is set then this register sets the threshold below which a minimum bias current error is raised based on the internal ADC reading. Note, this register exists only in EEPROM and not in the internal registers of the device, therefore a write to this address when 'INTERNAL_ACCESS' is set high will be ignored and a read return zero.
Type	R/W	PoR	00h	

The following registers exist only in the internal registers of the device. The corresponding addresses in EEPROM are unreachable. Therefore a TWI transaction to these addresses will target the internal device registers regardless of the setting of 'INTERNAL_ACCESS'.

E0h	TEST4			Internal use only, must be set to 00h
Type	R/W	PoR	00h	

E1h	TEMP_ADC_VALUE			Indicates the current temperature value measured by the internal ADC.
Type	R	PoR	00h	

E2h	BIAS_ADC_VALUE			Indicates the current bias current value measured by the internal ADC.
Type	R	PoR	00h	

E3h	TEST5			Internal use only, must be set to 00h
Type	R/W	PoR	00h	

E4h	TEST6			Internal use only, must be set to 00h
Type	R/W	PoR	00h	

E5h	TEST7			Internal use only, must be set to 00h
Type	R/W	PoR	00h	

E6h	TEST8			Internal use only, must be set to 00h
Type	R/W	PoR	00h	

E7h	INTERNAL			This register controls the internal state machines used to generate transmit modulation and bias currents
Bit	Field name	Type	PoR	
7	-	R	0	reserved
6	-	R	0	reserved
5	-	R	0	reserved
4	-	R	0	reserved
3	BIAS_SM_RESET	R/W	0	Set this bit to a '1' to put the bias current control logic into reset. Set to '0' for normal device operation
2	MOD_SM_RESET	R/W	0	Set this bit to a '1' to put the modulation current control logic into reset. Set to '0' for normal device operation
1	INTERNAL_ ACCESS	R/W	0	Set this bit to a '1' to direct TWI accesses to addresses C0h – DFh to the internal registers of the device. If set to '0' such addresses map to the external EEPROM.
0	SM_STOP	R/W	0	Set this bit to a '1' to suspend the internal control logic and allow TWI accesses to the external EEPROM. If this bit is set to '0' and a TWI access is targeted at the EEPROM then a write will be ignored and a read will return zero.

E8h	TX_DISABLES			This register controls the transmit safety shutdown circuit. See section 4.4 for further details
Bit	Field name	Type	PoR	
7	-	R	0	reserved
6	-	R	0	reserved
5	-	R	0	reserved
4	-	R	0	reserved
3	-	R	0	reserved
2	SOFT_TX_FAULT	R/W	0	This bit allows a TX_FAULT to be declared under control of the TWI. Setting this bit to a '1' causes a TX_FAULT condition to be declared
1	SOFT_TX_ DISABLE	R/W	0	This bit allows a TX_DISABLE to be declared under control of the TWI. Setting this bit to a '1' causes a TX_DISABLE condition to be declared
0	-	R/W	0	Internal use only. Must be set to '0'

E9h	EVENTS			This register contains latched versions of the bits in the STATUS register. If a condition becomes active the bit will report a '1'. If the condition goes inactive the bit will stay at '1' until a '1' is written to the bit via the TWI
Bit	Field name	Type	PoR	
7	TEMP_MAX_ ERROR_E	E	0	Has value '1' if a maximum temperature error condition has occurred
6	TEMP_MIN_ ERROR_E	E	0	Has value '1' if a minimum temperature error condition has occurred
5	BIAS_MAX_ ERROR_E	E	0	Has value '1' if a maximum bias current error condition has occurred
4	BIAS_MIN_ ERROR_E	E	0	Has value '1' if a minimum bias current error condition has occurred
3	TX_FAULT_E	E	0	Has value '1' if the output pin TX_FAULT has been asserted
2	TX_SHUTDOWN_ E	E	0	Has value '1' if a shutdown condition has been detected
1	SM_TX_FAULT_E	E	0	Has value '1' if the internal control logic has reported a fault condition
0	SM_TX_DISABLE_ E	E	0	Has value '1' if the internal control has disabled the transmit circuitry

EAh	STATUS			This register reports the status of a number of internally monitored conditions within the device. A bit will report a '1' if the condition is active and a '0' if the condition is inactive
Bit	Field name	Type	PoR	
7	TEMP_MAX_ ERROR	R	0	Has value '1' if a maximum temperature error condition is currently being detected
6	TEMP_MIN_ ERROR	R	0	Has value '1' if a minimum temperature error condition is currently being detected
5	BIAS_MAX_ ERROR	R	0	Has value '1' if a maximum bias current error condition is currently being detected
4	BIAS_MIN_ ERROR	R	0	Has value '1' if a minimum bias current error condition is currently being detected
3	TX_FAULT	R	0	Has value '1' if the output pin TX_FAULT is currently being asserted
2	TX_SHUTDOWN	R	0	Has value '1' if a shutdown condition is currently being asserted
1	SM_TX_FAULT	R	0	Has value '1' if the internal control logic is currently reporting a fault condition
0	SM_TX_DISABLE	R	0	Has value '1' if the internal control logic is currently disabling the transmit circuitry

EBh	HWARE_SENSE_EVENTS			This register contains latched versions of the bits in the HWARE_SENSE_STATUS register. If a condition becomes active the bit will report a '1'. If the condition goes inactive the bit will stay at '1' until a '1' is written to the bit via the TWI
Bit	Field name	Type	PoR	
7	-	R	0	reserved
6	-	R	0	reserved
5	-	R	0	reserved
4	TX_DISABLE_E	E	0	Has value '1' if the input pin TX_DISABLE changes from '0' to '1'
3	LOS_E	E	0	Has value '1' if the LOS detect circuit has detected a LOS condition
2	-	R	0	reserved
1	SUPPLY_OK_E	E	0	Has value '1' if the power supply monitoring circuit detects the supply voltage has gone from correct to incorrect
0	VREF_OK_E	E	0	Has value '1' if the voltage reference monitoring circuit detects the reference voltage has gone from correct to incorrect

ECh	HWARE_SENSE_STATUS			This register reports the status of various device input pins and detection circuits
Bit	Field name	Type	PoR	
7	-	R	0	reserved
6	-	R	0	reserved
5	-	R	0	reserved
4	TX_DISABLE	E	0	Indicates the logical status of the input pin TX_DISABLE (after potential inversion according to TX_DISABLE_POLARITY)
3	LOS	E	0	Indicates the status of the LOS detect circuit. The polarity depends on MUX_POLARITY
2	-	R	0	reserved
1	SUPPLY_OK	E	0	Indicates the status of the power supply monitoring circuit. If set to '1' then the supply voltage is correct
0	VREF_OK	E	0	Indicates the status of the voltage reference monitoring circuit. If set to '1' then the reference voltage is correct

EDh	DEBUG_EVENTS			This register indicates whether certain events have occurred within the control logic of the device. If a condition occurs bit will report a '1' and will stay at '1' until a '1' is written to the bit via the TWI
Bit	Field name	Type	PoR	
7	-	R	0	reserved
6	-	R	0	reserved
5	-	R	0	reserved
4	INTEGRITY_FAIL_E	E	0	This bit is set to '1' by the device if the boot DMA from EEPROM fails its integrity check
3	DMA_FAIL_E	E	0	This bit is set to '1' by the device if a DMA from EEPROM does not complete successfully
2	BOOT_FAIL_E	E	0	This bit is set to '1 by the device if the boot DMA from EEPROM does not complete successfully
1	BOOT_COMPLETE_E	E	0	This bit is set to '1' by the device if the boot DMA from EEPROM completes successfully
0	ITERATION_E	E	0	This bit is set to '1' by the device once per iteration of the modulation state machine logic (approx every 10ms)

EFh	BIAS_DAC_OBSERVE			This register indicates the current value of the transmit bias current setting DAC
Type	R	PoR	00h	

F0h	MOD_DAC_OBSERVE			This register indicates the current value of the transmit modulation current setting DAC
Type	R/W	PoR	00h	

FFh	CHIP_ID			Contains a hardwired chip identification number
Type	R	PoR	78h	

7. Simplified Interface Models

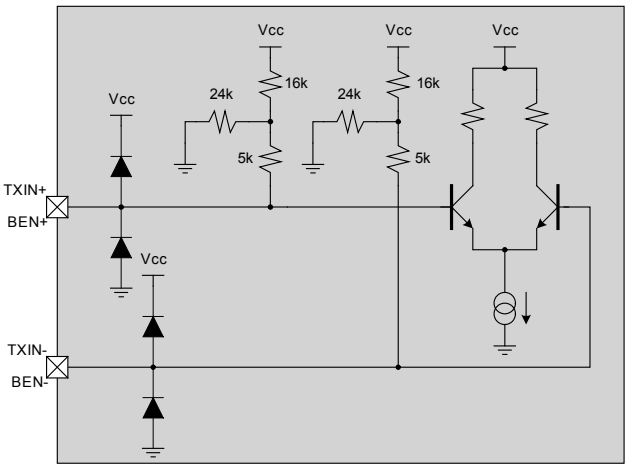


Figure 25 - Transmit input structure

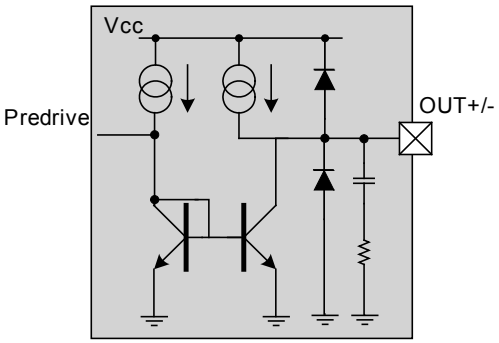


Figure 26 - Transmit output structure

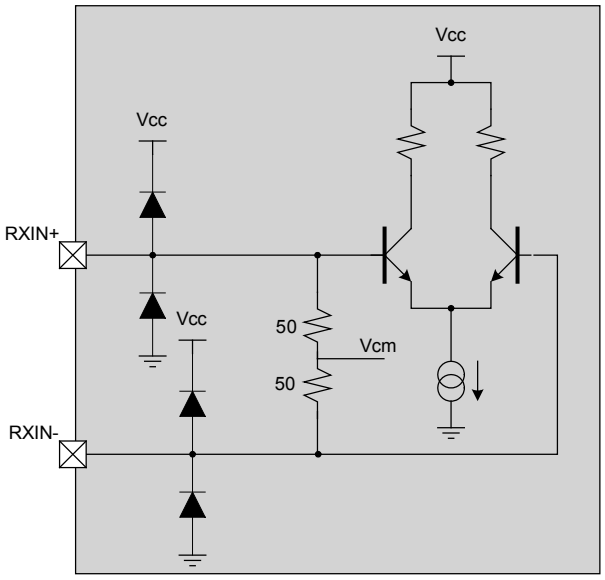


Figure 27- Receive input structure

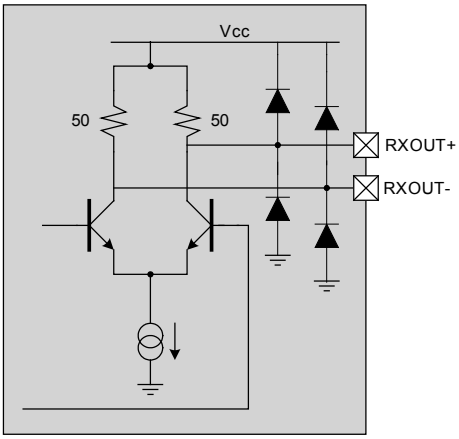


Figure 28- Receive output structure

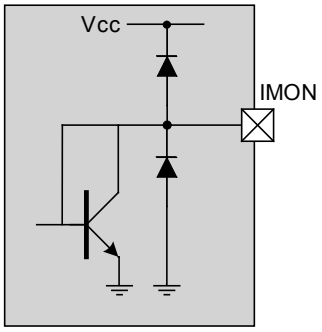


Figure 29 - MPD input structure

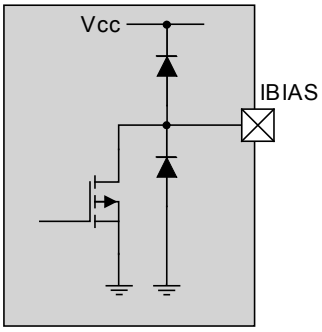


Figure 30 - Laser bias output structure

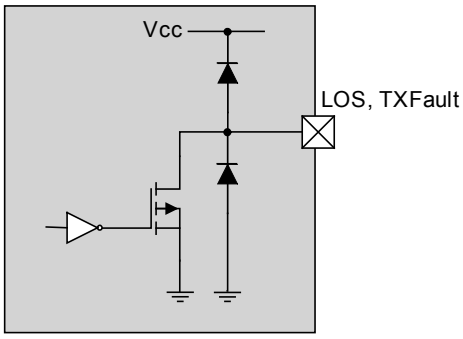


Figure 31 - LOS/TX_FAULT output

8. Applications Information

8.1. PHY2078 in an ONU application

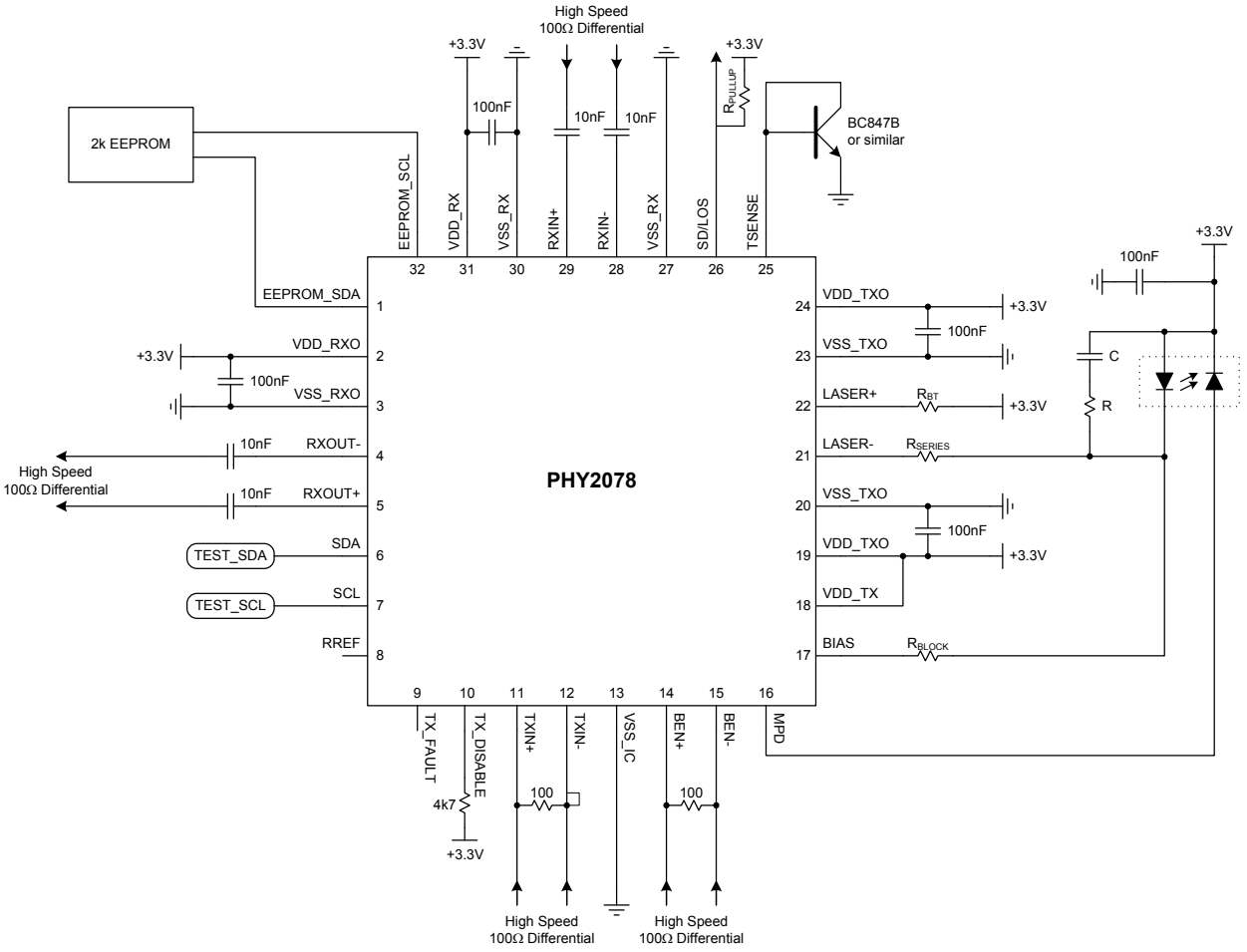


Figure 32 – Typical ONU Application Diagram

Figure 32 shows the general connectivity required with the PHY2078 to implement a Small Form Factor (SFF) type application, as used in GEPON systems.

The PHY2078 post amplifier is AC-coupled to the TIA in the ROSA. DC-coupling is required at the transmitter input and the laser output in order to support burst-mode operation. Exact implementation of the matching network varies with the actual laser used. When used in open-loop mode, no Monitor Photo Diode (MPD) will be required in conjunction with the Laser. When used in closed loop mode, the MPD is connected to the MPD pin on the PHY2078.

Module settings are stored in the EEPROM, and can be programmed using the EEPROM_SDA/SCL interface. Figure 32 shows the use of an external temperature sensor (diode-connected NPN-transistor) this should not be used when the internal temperature sensor is used.

8.1.1. Reference Design and Firmware

Checking for the latest reference design and firmware to support PHY2078 is recommended. The documents can be downloaded from the Phyworks website or by contacting Phyworks representatives.

8.2. Power Supply Connections

The PHY2078 has been designed as a low power device. In order to achieve low operating power consumption the transmitter and receiver circuitry in the PHY2078 share some common internal bias circuitry. This requires that the PHY2078 transmitter and receiver be powered up together for correct operation.

8.2.1. Power Supply Filtering

Although the Tx VDDs and Rx VDDs should be powered together and therefore, ultimately be connected at a common node, it is beneficial to separately filter the power supplies for the Tx VDD and Rx VDD supplies. Separately filtering the transmitter and receiver supplies off chip will reduce power supply noise and cross talk between the transmitter and receiver – it is generally good practice to separately filter and decouple the individual supplies on any multifunction IC.

In addition to supplying separately filtered supplies to the Tx VDDs and Rx VDDs of the PHY2078, it is recommended that any other ICs and digital circuitry connected to the PHY2078 in an application environment (e.g. SFF module) be suitably filtered and decoupled. An example of this would be to supply a filtered digital supply for an external MCU.

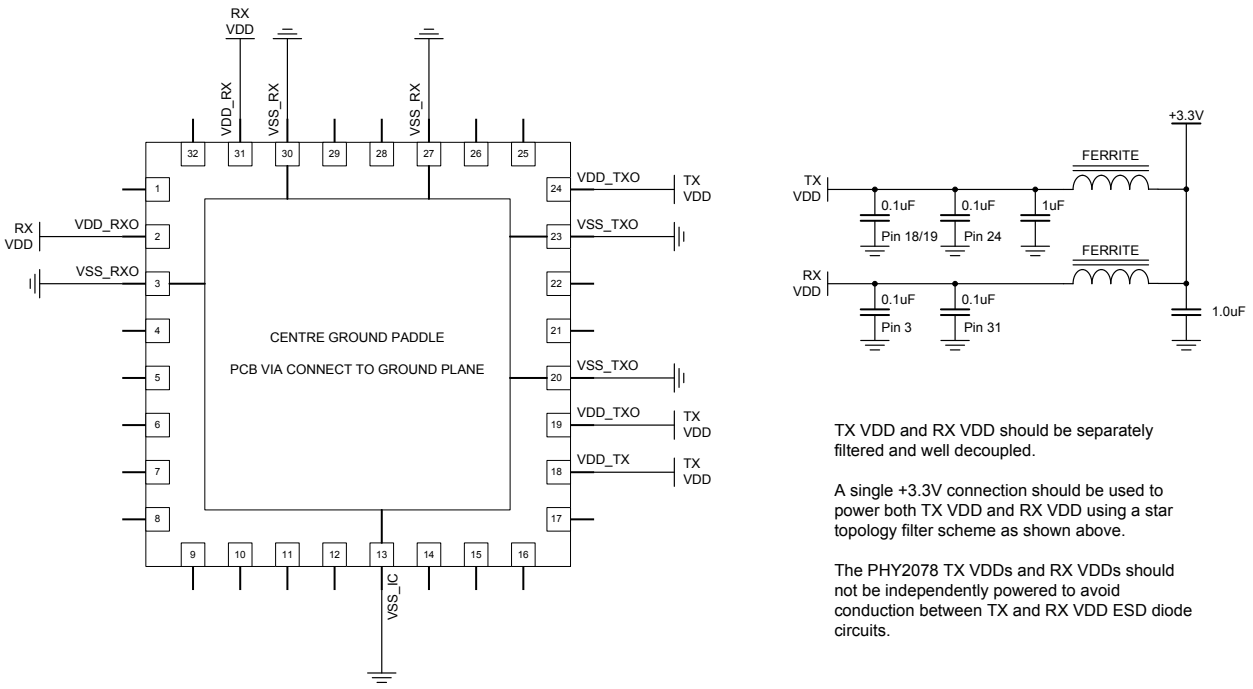


Figure 33 – Recommended power supply connections and filtering.

8.3. Burst Enable and TX Input connection options

The PHY2078 supports various modes of interfacing to the transmit data (TXIN+/-) and burst enable (BEN+/-) inputs providing the signal voltage and common-mode voltage levels are within the valid range specified in figure 4. Some common examples are shown in figures 34-36 below.

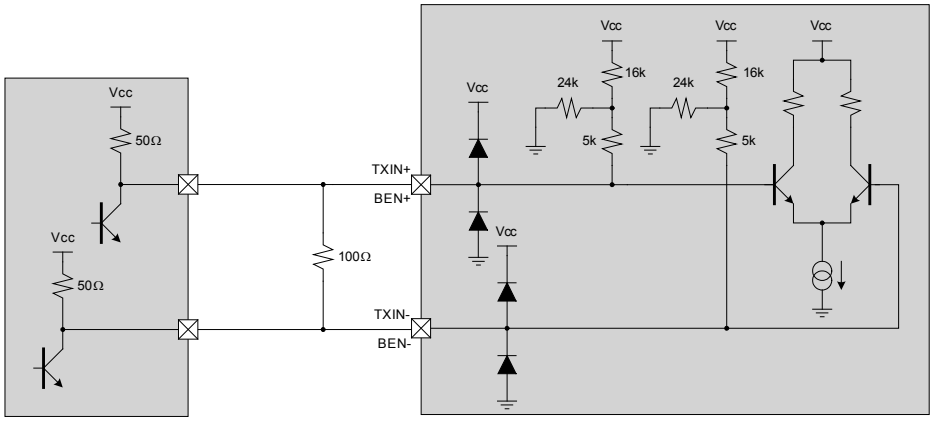


Figure 34 - DC-Coupled CML interface for TXIN and BEN

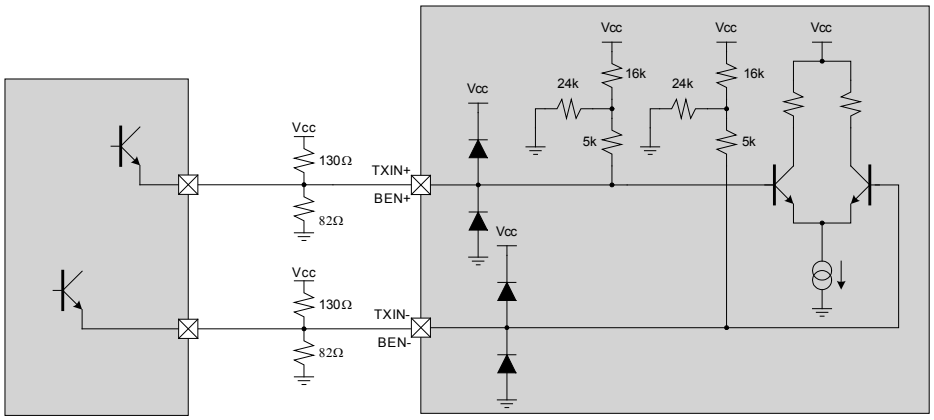


Figure 35 - DC-Coupled LVPECL interface for TXIN and BEN

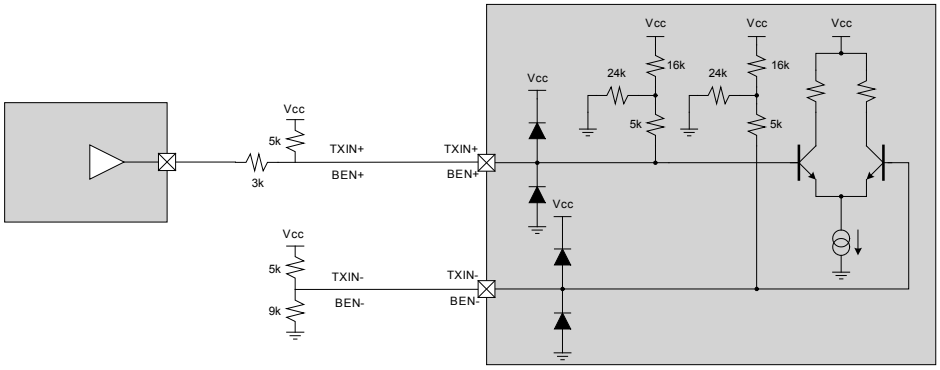


Figure 36 – Single-ended CMOS/LVTTL interface for BEN

8.4. Laser Connection – DC-Coupled

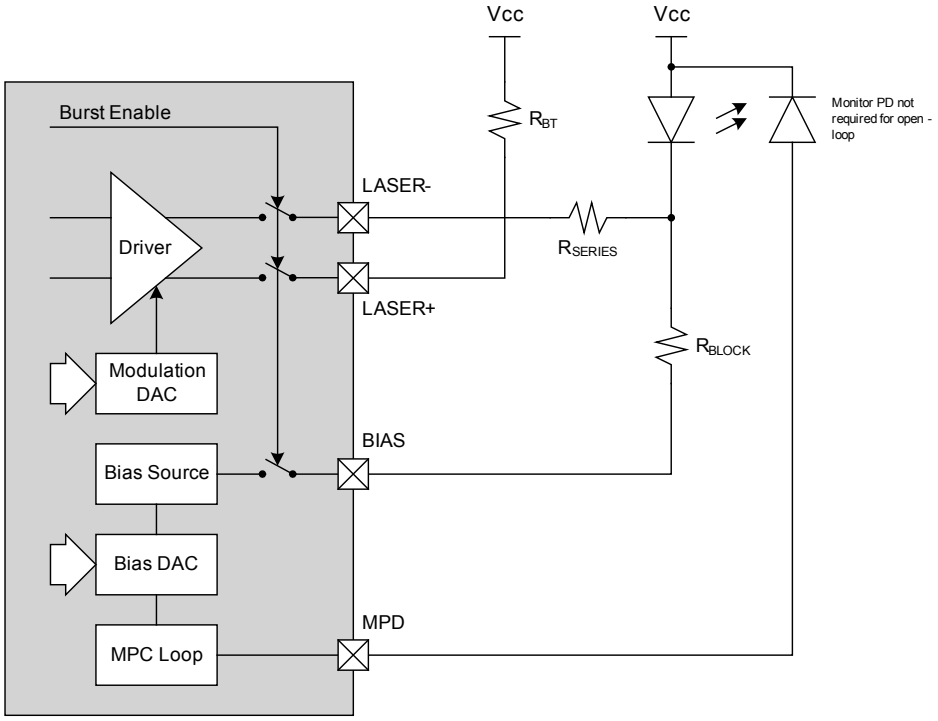


Figure 37 - DC-Coupled Laser Application Diagram

Figure 37 shows a typical DC-coupled application. DC current is provided to the output stage via a resistive network. The AC impedance to ground of the LASER+ pin should be approximately 50Ω to properly terminate that output. R_{SERIES} is used to match the laser impedance. It may also be necessary to use a RC snubbing circuit connected in parallel with the laser to reduce any ringing caused by series inductance in the packaging. A 10Ω resistor, R_{BLOCK}, is used to isolate the output stage from the capacitive loading of the BIAS pin. In this mode, the BIAS pin can sink up to 80mA of current. For burst-mode applications ferrites should not be used as they will not allow the bias to settle correctly.

8.5. Mean Power Control Loop Startup Algorithm

At power up or after TX_DISABLE is de-asserted the PHY2078 can use a fast startup algorithm to quickly settle the mean power control loop to the desired bias level. After the algorithm has completed the low bandwidth digital mean power control loop takes over to maintain the optical output power. The algorithm can only be invoked in closed loop, DC coupled mode, for AC coupled applications the startup algorithm must be disabled, and the mean power control loop will settle at a rate determined by its bandwidth.

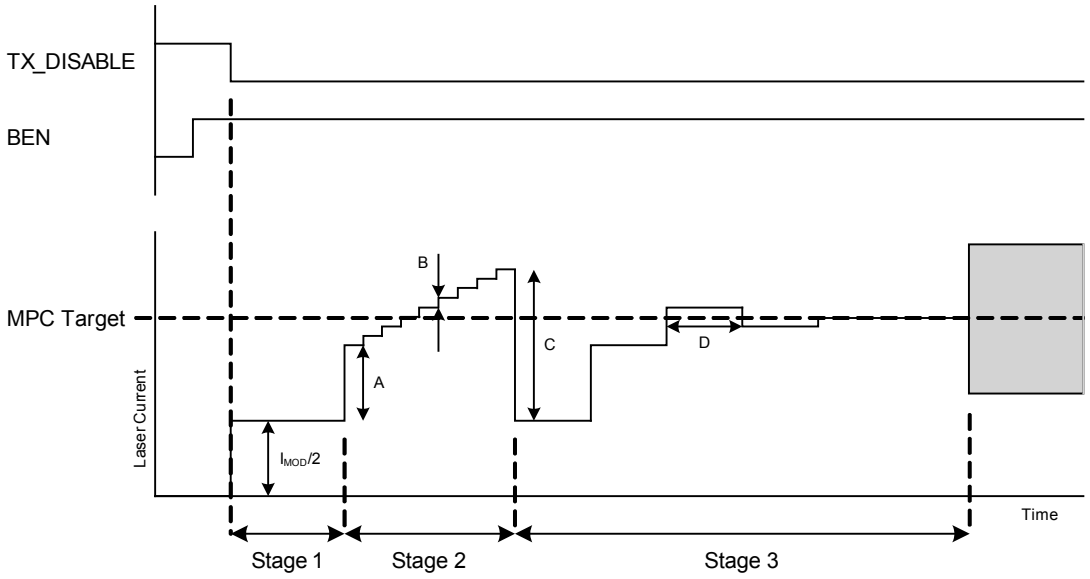


Figure 38 - Closed Loop Fast Start-up Algorithm

The fast start-up algorithm contains three stages as shown in Figure 38.

Stage 1 begins at power-up or after TX_DISABLE is de-asserted and completes when the PHY2078 has successfully loaded its operating parameters from the companion EEPROM. During this stage the data path is disabled and the modulation outputs balanced such that $I_{MOD}/2$ flows into both LASER+ and LASER-.

Stage 2 is a ramp sequence which starts with an initial step (A) approximately equal to $I_{MOD}/2$ and is followed by smaller increments (B) on each cycle of the algorithm clock (64MHz). The ramp continues until an internal comparator detects that the photodiode current has exceeded the desired reference current set by MON_DAC (D5h). The finite delay present in the system between setting a bias current and the monitor photodiode current settling means that the bias level at the end of the ramp sequence will have overshot the desired operating point.

Stage 3 is a binary search sequence used to quickly and accurately acquire the mean power level. This can take up to eight steps. Control of the bias current is transferred to the low frequency mean power control loop and the data path is enabled at the end of the binary search sequence.

There are various parameters within each of the stages which can be controlled by the user:

A = IMODCODE x 0.2662

Where A is in mA and IMODCODE is the value applied to the modulation DAC. If a modulation lookup table is used IMODCODE will be dependant on temperature, otherwise IMODECODE is equal to the value set in the MOD_DAC (D4h) register. The actual value applied to the modulation DAC is visible in MOD_DAC_OBSERVE (F0h)

B = IMODCODE x RAMP_STEP_FACTOR x 0.001512

Where B is in mA and the recommended setting for RAMP_STEP_FACTOR (D2h) is 82d.

C = IMODCODE x BURST_START_FACTOR x 0.2662

Where C is in mA and BURST_START_FACTOR (D0h, TX_BIASLOOP_CONTROL, bits 5:4) can be set between 1 and 3, but 2 is the recommended setting.

D = BINARY_SEARCH_WIDTH x $1/F_{clk}$

BINARY_SEARCH_WIDTH (D1h, TX_BURST_CONTROL_1, bits 2:0) has a valid range of 4 to 8, where 8 is the default and 4 represents fastest binary search time, see Table 11 for coding. F_{clk} is 64MHz, the frequency of the internal clock.

BINARY_SEARCH_WIDTH	Bit		
	2	1	0
8	0	0	0
7	1	1	1
6	1	1	0
5	1	0	1
4	1	0	0

Table 11 - BINARY_SEARCH_WIDTH values

At the end of stage 2 the bias current will have exceeded the desired bias level. This overshoot can be estimated using the following equation:

Max Overshoot (mA) < ($\tau_L F_{clk}$ + 1) x RAMP_STEP_FACTOR x IMODCODE x 0.001512

Where τ_L is the delay round the APC feedback loop. For most applications this is dominated by the capacitance of the monitor photodiode (C_{PD}), so $\tau_L \approx 250 \times C_{PD}$.

Overshoot can be reduced by lowering the value of RAMP_STEP_FACTOR however this reduction will be at the expense of a longer startup time.

The time taken for the algorithm to complete and the parameters used, are highly dependent on the optics used in the system. For most systems the default parameter values will be acceptable.

The foregoing description assumes that the burst enable signal is always asserted. However, the startup algorithm can be split over up to three bursts. The algorithm pauses while the burst enable signal is de-asserted and resumes when it is re-asserted. If the algorithm has not completed after three bursts, then control of the bias current is transferred to the mean power control loop using the value reached by the algorithm at the end of the third burst. The mean power control loop settles from that point at a rate determined by its bandwidth.

The fast startup algorithm can be disabled by setting BIAS_STARTUP_BYPASS (D0h, TX_BIASLOOP_CONTROL, bit 3) to '1'. If the algorithm is disabled the bias current is initialized to zero and settles to the desired level at a rate determined by the bandwidth of the digital control loop.

Fast Startup Example

For:

Imod = 30mA

IMODCODE = 80

BINARY_SEARCH_WIDTH=4

BURST_START_FACTOR=2

C_{PD} = 10pF

We get:

A = 80 x 0.2662 = 21.3mA

B = 80 x 82 x 0.001512 = 9.9mA

C = 80 x 2 x 0.2662 = 42.6mA

D = 4 / Fclk = 61ns

Max Overshoot = 11.5mA

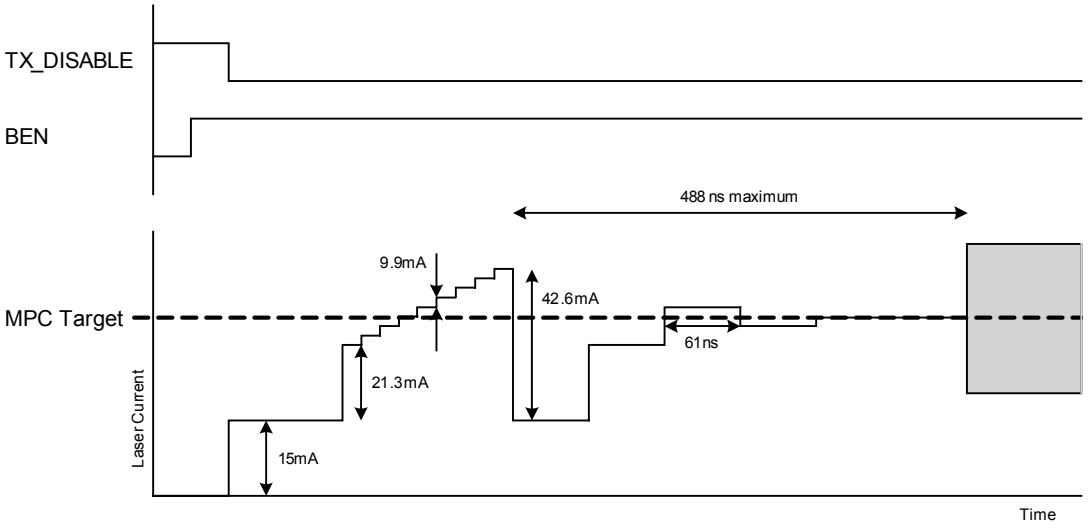
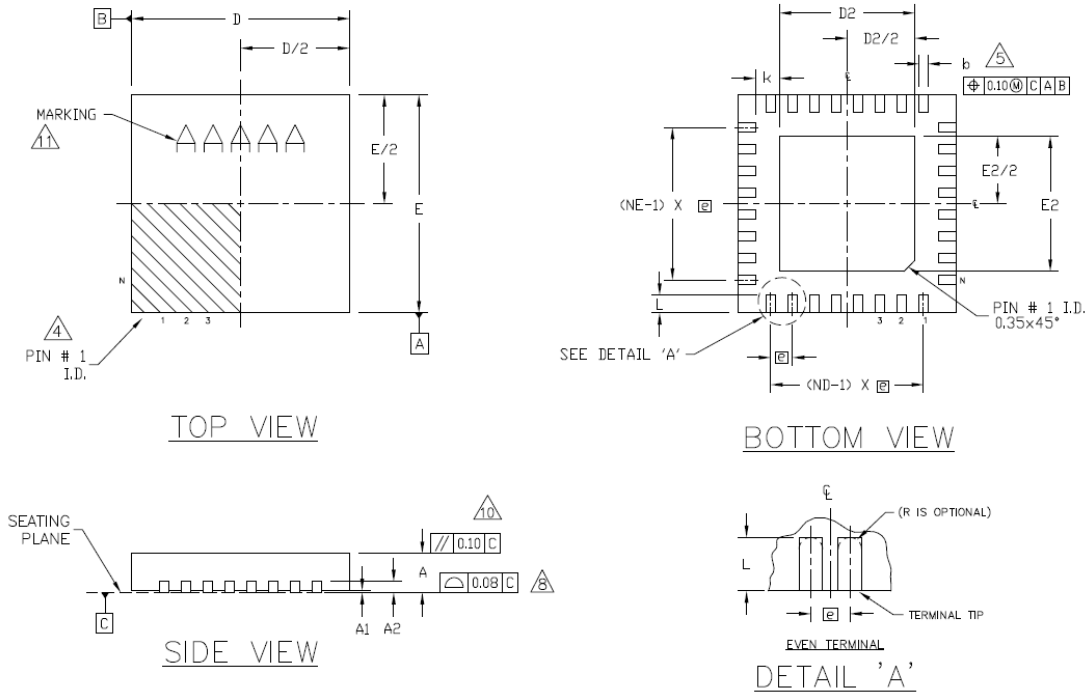


Figure 39 - Closed Loop Fast Start-up Algorithm Example

9. Packaging



PKG.	32L 5x5		
SYMBOL	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0	0.02	0.05
A2		0.20 REF	
b	0.20	0.25	0.30
D	4.90	5.00	5.10
E	4.90	5.00	5.10
e		0.50 BSC	
k	0.25	-	-
L	0.30	0.40	0.50
N		32	
ND		8	
NE		8	
D2	3.00	3.10	3.20
E2	3.00	3.10	3.20
JEDEC		WHHD-2	

Figure 40 – 32pin TQFN Package Dimensions

PACKAGING NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 MM AND 0.30 MM FROM TERMINAL TIP.

5. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
6. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
7. DRAWING CONFORMS TO JEDEC MO220.
8. WARPAGE SHALL NOT EXCEED 0.10 MM.
9. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
10. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
11. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.

For the latest package outline information and land patterns (footprints), go to www.maxim-ic.com/packages. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

	Symbol	Typical	Unit
Thermal Resistance – Junction to Ambient	θ_{Ja}	39	°C/W
Thermal Resistance – Junction to Case	θ_{Jc}	31	°C/W

Note: Refer to EIA/JEDEC standard JESD51 for test method and conditions

Table 12 - 32pin TQFN Package Thermal Data