PI2EQX4401D

2.5Gbps x1 Lane Serial PCI-Express Repeater/Equalizer with Clock Buffer & Signal Detect Feature

Features

- One high-speed PCI-Express lane
- Adjustable Transmiter De-Emphasis & Amplitude
- Adjustable Receiver Equalization
- One Spread Spectrum Reference Clock Buffer Output
- Input Signal Level Detect and Output Squelch
- 100Ω Differential CML I/O's
- Low Power (100mW per Channel)
- Stand-by Mode – Power Down State
- V_{DD} Operating Range: 1.8V ±0.1V
- Packaging (Pb-free & Green):
  — 36-pad TQFN (ZF36)

Description

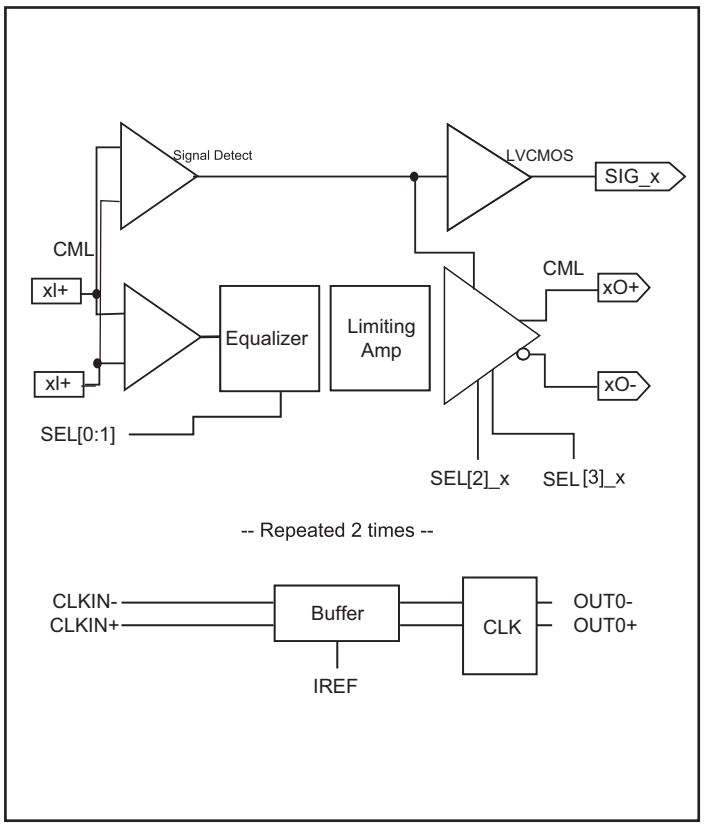
Pericom Semiconductor's PI2EQX4401D is a low power, PCI-Express compliant signal re-driver. The device provides programmable equalization, amplification, and de-emphasis by using 4 select bits, SEL[0:3], to optimize performance over a variety of physical mediums by reducing Inter-symbol interference. PI2EQX4401D supports two 100Ω Differential CML data I/O's between the Protocol ASIC to a switch fabric, across a backplane, or extends the signals across other distant data pathways on the user's platform.

The integrated equalization circuitry provides flexibility with signal integrity of the PCI-express signal before the re-driver. Whereas the integrated de-emphasis circuitry provides flexibility with signal integrity of the PCI-express signal after the Re-Driver.

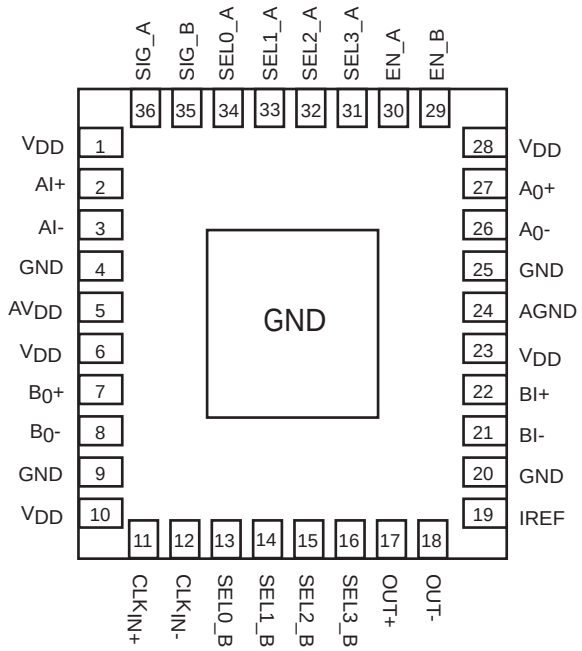
A low-level input signal detection and output squelch function is provided for both channels. Each channel operates fully independantly. When a channel is enabled (EN_x=1) and operating, that channel's input signal level (on xl+/-) determines whether the output is enabled. If the input level of the channel falls below the active threshold level (Vth-) then the output driver switches off, and the pin is pulled to VDD via a high impedance resistor.

In addition to providing signal re-conditioning, Pericom's PI2EQX4401D also provides power management Stand-by mode operated by a Bus Enable pin. A differential clock buffer is provided for test and other system requirements. This clock function is not used by the data channels.

Block Diagram



Pin Description



Pin Description

Pin #	Pin Name	I/O	Description
1, 6, 10, 23, 28	V_{DD}	PWR	1.8V Supply Voltage
2	AI+	I	Positive CML Input Channel A with internal 50Ω pull down during normal operation (EN_A=1). When EN_A=0, this pin is high-impedance.
3	AI-	I	Negative CML Input Channel A with internal 50Ω pull down during normal operation (EN_A=1). When EN_A=0, this pin is high-impedance.
4, 9, 20, 25	GND	PWR	Supply Ground
22	BI+	I	Positive CML Input Channel B with internal 50Ω pull down during normal operation (EN_B=1). When EN_B=0, this pin is high-impedance.
21	BI-	I	Negative CML Input Channel B with internal 50Ω pull down during normal operation (EN_B=1). When EN_B=0, this pin is high-impedance.
34, 33	SEL[0:1]_A	I	Selection pins for equalizer (see Amplifier Configuration Table) w/ 50KΩ internal pull up
13, 14	SEL[0:1]_B	I	
32	SEL[2]_A	I	Selection pins for amplifier (see Amplifier Configuration Table) w/ 50KΩ internal pull up
15	SEL[2]_B	I	
31	SEL[3]_A	I	Selection pins for De-Emphasis (See De-Emphasis Configuration Table) w/ 50KΩ internal pull up
16	SEL[3]_B	I	
27	AO+	O	Positive CML Output Channel A internal 50Ω pull up during normal operation and 2KΩ pull up otherwise.
26	AO-	O	Negative CML Output Channel A with internal 50Ω pull up during normal operation and 2KΩ pull up otherwise.
7	BO+	O	Positive CML Output Channel B with internal 50Ω pull up during normal operation and 2KΩ pull up otherwise.
8	BO-	O	Negative CMLOutput Channel B with internal 50Ω pull up during normal operation and 2KΩ pull up otherwise.
30, 29	EN_[A,B]	I	EN_[A:B] is the enable pin. A LVCMOS high provides normal operation. A LVCMOS low selects a low power down mode.
12	CLKIN-	I	Differential Input Reference Clock. If clock buffer is not used, then both CLKIN+, CLKIN- should be pulled high to VDD.
11	CLKIN+	I	
17, 18	OUT+, OUT-	O	Differential Reference Clock Output
5	AVDD	PWR	1.8V Analog supply voltage
24	AGND	PWR	Analog ground
19	IREF	O	External 475Ω resistor connection to set the differential output current. If the clock buffer is not used, then IREF should be unconnected (open).
36, 35	SIG_A, SIG_B	O	SIG Detector output for channel A-B. Provides a LVCMOS high output when an input signal greater than the threshold is detected

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5V to +2.5V
DC SIG Voltage	–0.5V to V_{DD} +0.5V
Current Output	-25mA to +25mA
Power Dissipation Continous	500mW
Operating Temperature	0 to +70°C

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Output Swing Control

SEL2_[A:B]	Swing
0	1x
1	1.2x

Output De-emphasis Adjustment

SEL3_[A:B]	De-emphasis
0	0dB
1	-3.5dB

Equalizer Selection

SEL0_[A:B]	SEL1_[A:B]	Compliance Channel
0	0	no equalization
0	1	[0:2.5dB] @ 1.25 GHz
1	0	[2.5:4.5dB] @ 1.25 GHz
1	1	[4.5:6.5dB] @ 1.25 GHz

Note:
1. Design target specification. Absolute values will be based on characterization.

AC/DC Electrical Characteristics (V_{DD} = 1.8 ±0.1V)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Ps	Supply Power	EN = LVCMOS Low			0.1	W
		EN = LVCMOS High			0.6	
	Latency	From input to output		2.0		ns
CML Receiver Input						
RL_{RX}	Return Loss	50 MHz to 1.25 GHz		12		dB
$V_{RX-DIFFP-P}$	Differential Input Peak-to-peak Voltage		0.175		1.200	V
$V_{RX-CM-ACP}$	AC Peak Common Mode Input Voltage				150	mV
V_{TH-}	Signal Detection Threshold	EN_x=High		120	175	mV
$Z_{RX-DIFF-DC}$	DC Differential Input Impedance		80	100	120	Ω
Z_{RX-DC}	DC Input Impedance		40	50	60	
Equalization						
J_{RS}	Residual Jitter	Total Jitter (2)			0.3	Ulp-p
		Deterministic jitter			0.2	
J_{RM}	Random Jitter	See note 2		1.5		psrms

Notes
1. K28.7 pattern is applied differentially at point A as shown in Figure 1.
2. Total jitter does not include the signal source jitter. Total jitter (TJ) = (14.1 × RJ + DJ) where RJ is random RMS jitter and DJ is maximum deterministic jitter. Signal source is a K28.5 ± pattern (00 1111 1010 11 0000 0101) for the deterministic jitter test and K28.7 (0011111000) or equivalent for random jitter test. Residual jitter is that which remains after equalizing media-induced losses of the environment of Figure 1 or its equivalent. The deterministic jitter at point B must be from media-induced loss, and not from clock source modulation. JItter is measured at 0V at point C of Figure 1.

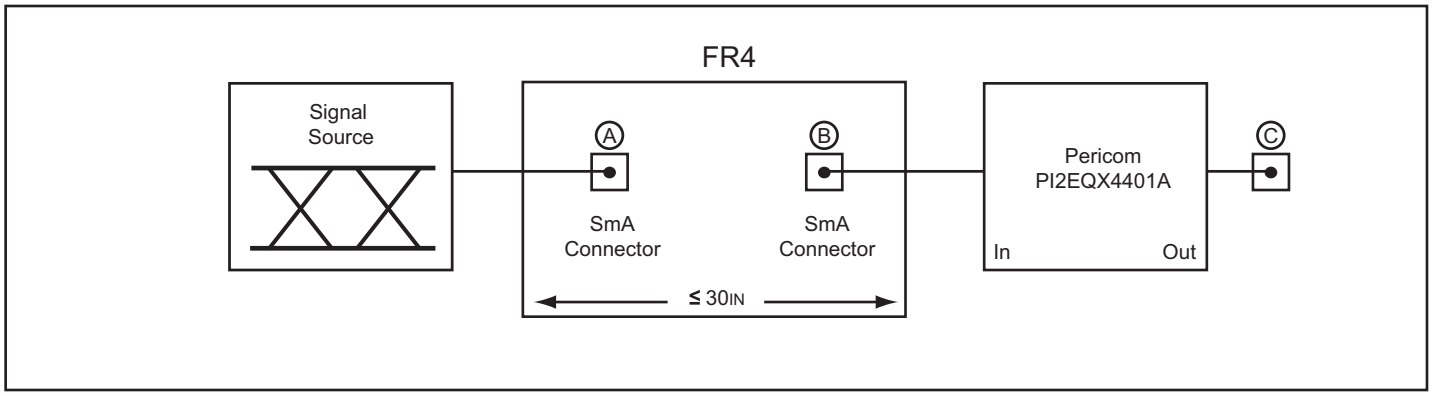


Figure 1. Test Condition Referenced in the Electrical Characteristic Table

AC/DC Electrical Characteristics (T_A = 0 to 70˚C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
CML Transmitter Output (100Ω differential)						
V_{DIFFP}	Output Voltage Swing	Differential Swing $\lvert V_{TX-D+} - V_{TX-D-} \rvert$	400		650	mVp-p
V_{TX-C}	Common-Mode Voltage	$\lvert V_{TX-D+} + V_{TX-D-} \rvert$ / 2		V_{DD}-0.3		
t_F, t_R	Transition Time	20% to 80% (3)			150	ps
Z_{OUT}	Output resistance	Single ended	40	50	60	Ω
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance		80	100	120	Ω
C_{TX}	AC Coupling Capacitor		75		200	nF
$V_{TX-DIFFP-P}$	Differential Peak-to-peak Ouput Voltage	$V_{TX-DIFFP-P} = 2 * \lvert V_{TX-D+} - V_{TX-D-} \rvert$	0.8		1.3	V
LVCMOS Control Pins						
V_{IH}	Input High Voltage		0.65 × V_{DD}		V_{DD}	V
V_{IL}	Input Low Voltage				0.35 × V_{DD}	
I_{IH}	Input High Current				250	µA
I_{IL}	Input Low Current				500	

Notes
3. Using K28.7 (0011111000) patern)
4. AC specifications are guaranteed by design and characterization

AC Switching Characteristics for Clock Buffer (V_{DD} = 1.8 ±0.1V, AV_{DD} = 1.8 ±0.1V)

Symbol	Parameters	Min	Max.	Units	Notes
T_{rise} / T_{fall}	Rise and Fall Time (measured between 0.175V to 0.525V)	125	525	ps	1
□T_{rise} / □T_{fall}	Rise and Fall Time Variation		75	ps	1
V_{HIGH}	Voltage High including overshoot	660	900	mV	1
V_{LOW}	Voltage Low including undershoot	-200		mV	1
V_{CROSS}	Absolute crossing point voltages	200	550	mV	1
□V_{CROSS}	Total Variation of Vcross over all edges		250	mV	1
T_{DC}	Duty Cycle (input duty cycle = 50%)	45	55	%	2

Notes:
1. Measurement taken from Single Ended waveform.
2. Measurement taken from Differential waveform.
3. Test configuration is R_S = 33.2Ω, Rp = 49.9Ω, and 2pF.

Configuration Test Load Board Termination

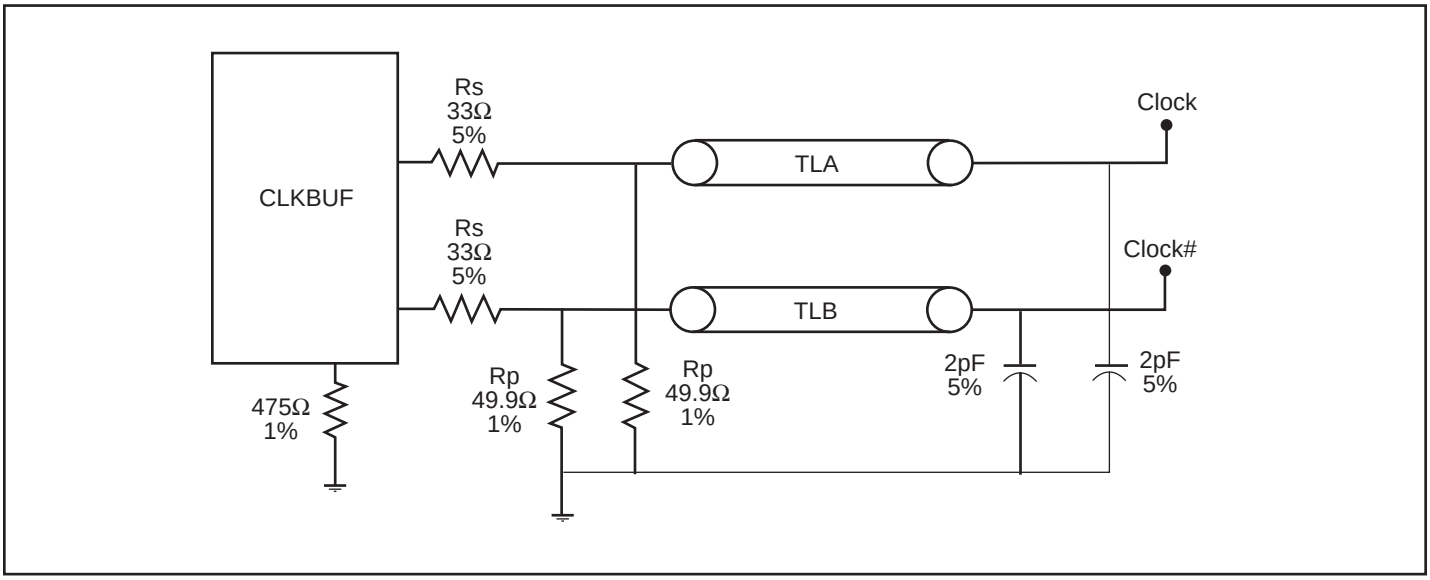


Figure 2. Configuration test load board termination

Note:
1. TLA and TLB are 3” transmission lines.