A product Line of
Diodes Incorporated

PI3DPX1203

DisplayPort 1.4 Linear ReDriver for Source, Active Cable & Sink-side Applications

Description

Diodes' PI3DPX1203 is the Displayport compliant, up to 4 channel, 8.1 Gbps Linear Redriver with Link Training transparency support. Displayport source-side and sink-side devices communicate through the AUX transaction between the source and the sink-side devices.

Input Equalization, Voltage Swing and Flat Gain control can configure with pin-strapping or I2C programing to optimized Main Link high speed signals over a variety of physical medium by reducing inter-symbol interference. Pericom's Linear Redriver technology can deliver 2 times better additive jitters performance than traditional Redrivers.

Linear Equalizer always provide very flexible component placement, cascade connection and easy adjustment after the Redriver location changes during the product development events.

Features

- Compliant with VESA DisplayPort 1.4 specification up to 10 Gbps Link Rate
- Linear ReDriver allows flexible placement with Main Link boost setting
- Ideal for DP/USB Type-C Source and Sink-side application with PD Controllers with Aux Link Training Transparent Mode support
- Linear Equalizer Increases Main Link Margin with sink-side DFE (Decision Feedback Equalizer)
- Independent Main Link channel configuration for 4-bit Equalization, 2-bit Voltage Output swing and 2-bit Flat Gain control
- Pin strap or I2C programmable for device Configuration setting
- Intra- and Inter-Channel Polarity swap support
- I2C Address selectable for configuration register access
- Power Supply Voltage: 3.3V
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.

  https://www.diodes.com/quality/product-definitions/

Applications

- Display, Monitors
- Active Adaptors, Dongles, Docking
- Notebook, DeskTop, AIO PC

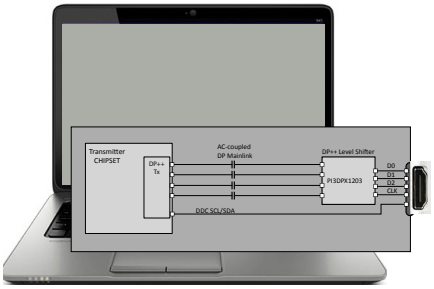


Figure 1-1. DP1.4 ReDriver in the NB PC

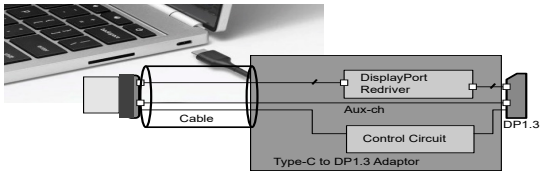


Figure 1-2. ReDriver in the DP1.4 Type-C Dongle

Ordering Information

Ordering Number	Package Code	Package Description
PI3DPX1203 ZHEX	ZH	42-pin, Very Thin Quad Flat No-Lead (TQFN), Tray Type W24
PI3DPX1203 ZHE+DRX	ZH	42-pin, Very Thin Quad Flat No-Lead (TQFN), Type W16

Notes:
1. No purposely added lead. EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See http://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free. Thermal characteristics can be found on the company web site at www.diodes.com/design/support/packaging/
3. E = Pb-free and Green
4. X suffix = Tape/Reel

2. General Information

2.1 Revision History

Date	Description of Changes
May 2016	In Functional/Application, informative data added for system design supports
July 2016	In application session, Evaluation board reference schematic removed
Apr 2017	Add Tape/Reel Package W16 in Product Brief Ordering Information
Jun 2017	Power-up sequence added in the functional description
Jan 2018	Changed for DP 1.4 8.1Gbps support. Added package marking information. In Application session, updated reference schematics and DP 1.4 CTS test report
Feb 2021	Updated Section 3 Pinout Updated Section 3.2 Pin Description Updated Section 4.1 Block Diagram Updated 5.2 I2C Operation and added 5.3 I2C Data Transfer

2.2 Related Products

Part Numbers	**Products Description**
Retimers / Jitter Cleaner	
PI3HDX2711B	HDMI 2.0 and DP++ Retimer (Jitter Cleaner)
PI3HDX711B	HDMI 1.4 and DP++ ReTimer (Jitter Cleaner)
Redrivers	
PI3DPX1203B	DisplayPort 1.4 Redriver for Source/Sink/Cable Application, Linear-type
PI3HDX1204B1	HDMI 2.0 Redriver (DP++ Level Shifter), High EQ, place near to the source-side, Limiting type
PI3HDX1204E	HDMI 2.0 Linear Redriver (DP++ Level Shifter) , Link transparent, place near to the sink-side
PI3DPX1207B	DisplayPort 1.4 Alt Type-C Redriver, 8.1 Gbps and USB3.1 10 Gbps, Link Transparent
PI3DPX1202A	Low Power DisplayPort 1.2 Redriver with built-in AUX Listener, Limiting-type
PI3HDX511F	High EQ HDMI 1.4b Redriver and DP++ Level Shifter for Sink/Source Application, Limiting-type
Active Switches & Splitters	
PI3DPX1205A	DisplayPort 1.4 Alt Type-C Mux Redriver, 8.1 Gbps and USB3.1 10 Gbps, Link Transparent
PI3HDX231	HDMI 2.0 3:1 ports Mux Redriver, Linear-type
PI3HDX414	HDMI 1.4b 1:4 Demux Redriver & Splitter for 3.4 Gbps Application, Limiting-type
PI3HDX412BD	HDMI 1.4b 1:2 Demux Redriver & Splitter for 3.4 Gbps Application, Limiting-type
PI3HDX621	HDMI 1.4 Redriver 2:1 Active Switch with built-in ARC and Fast Switching support, Limiting-type

Contents

3. Pinout

3.1 Package Pinout (Top View)

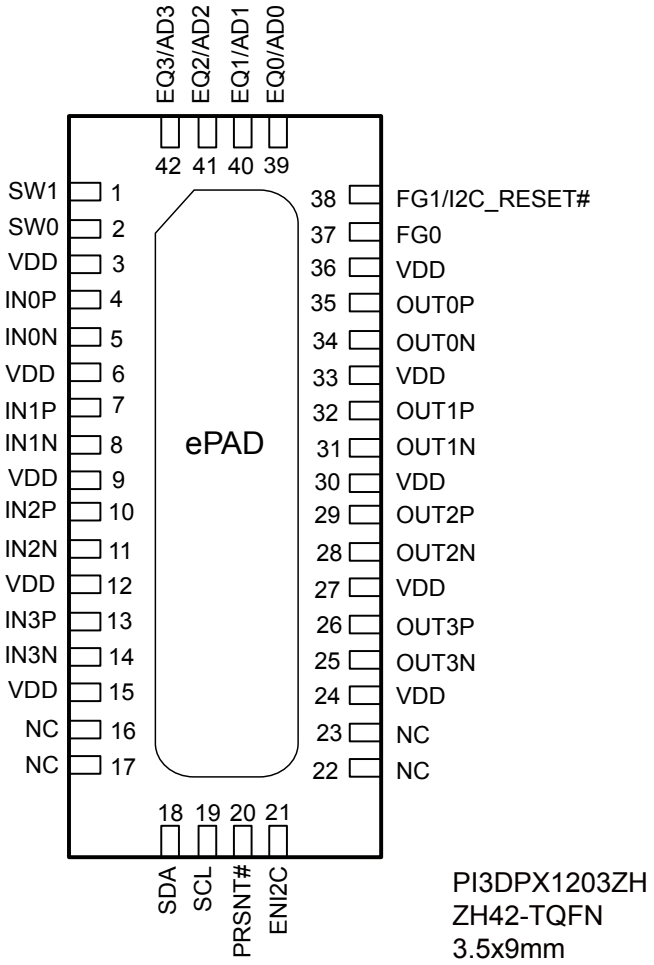


Figure 3-1. 42-TQFN package pin-out

Note: High-speed data channels support inter-channel polarity and inter-channel order swap.

3.2 Pin Description

Pin Name	Pin #	Type	Description
IN0P/N	4, 5	I	CML Inputs +/- for Channel A0 with internal 50Ω pull-up, and 200kΩ pull-up for power down mode
IN1P/N	7, 8	I	CML Inputs +/- for Channel A1 with internal 50Ω pull-up, and 200kΩ pull-up for power down mode
IN2P/N	10, 11	I	CML Inputs +/- for Channel A2 with internal 50Ω pull-up, and 200kΩ pull-up for power down mode
IN3P/N	13, 14	I	CML Inputs +/- for Channel A3 with internal 50Ω pull-up, and 200kΩ pull-up for power down mode
OUT0P/N	35, 34	O	CML Outputs +/- for Channel A0 with internal 50Ω pull-up, and 2kΩ pull-up for power down mode
OUT1P/N	32, 31	O	CML Outputs +/- for Channel A1 with internal 50Ω pull-up, and 2kΩ pull-up for power down mode
OUT2P/N	29, 28	O	CML Outputs +/- for Channel A2 with internal 50Ω pull-up, and 2kΩ pull-up for power down mode
OUT3P/N	26, 25	O	CML Outputs +/- for Channel A3 with internal 50Ω pull-up, and 2kΩ pull-up for power down mode
SDA	18	I/O	I^2C Data
SCL	19	I/O	I^2C Clock
PRSNT#	20	I	Cable Present Detect Input. This pin has internal 100kΩ pull-up. When the pin is "1", the cable does not present and enter to the lower power mode. When the pin is "0", the device is Active with normal operation.
ENI2C	21	I	I2C enable pin. When the pin is "1", register access I2C Slave mode When the pin is "0", pin-strapping control mode
SW[1:0]	1, 2	I	Swing Control 2 bits. Input with internal 100 kΩ pull-up. This pin control the output Voltage Swing Level in all channel when ENI2C is "0".
FG0	38, 37	I	Flat Gain Control 2 bits pins. Inputs with internal 100 kΩ pull-up. This pin control the output flat gain level on all channels when ENI2C is "0".
FG1/I2C_RESET#	38	I	I2C Reset pin. Active "0". All programmable registers reset to the default state. Inputs with internal 100kΩ pull up.
EQ[3:0]/ AD[3:0]	42, 41, 40, 39	I	EQ setting pins. Inputs with internal 100 kΩ pull-up. This 4-bit pins control the amount of Input Equalizer Boost in all channel, when ENI2C is "0". Or I^2C address control 4 bits with internal 100kΩ pull-up.
NC	16, 17, 22, 23	NC	No Connect
VDD	3, 6, 9, 12, 15, 24, 27, 30, 33, 36	PWR	3.3V Power Supply
GND	Center Pad	GND	Exposed Ground pad

4. Functional

4.1 Functional Block Diagram

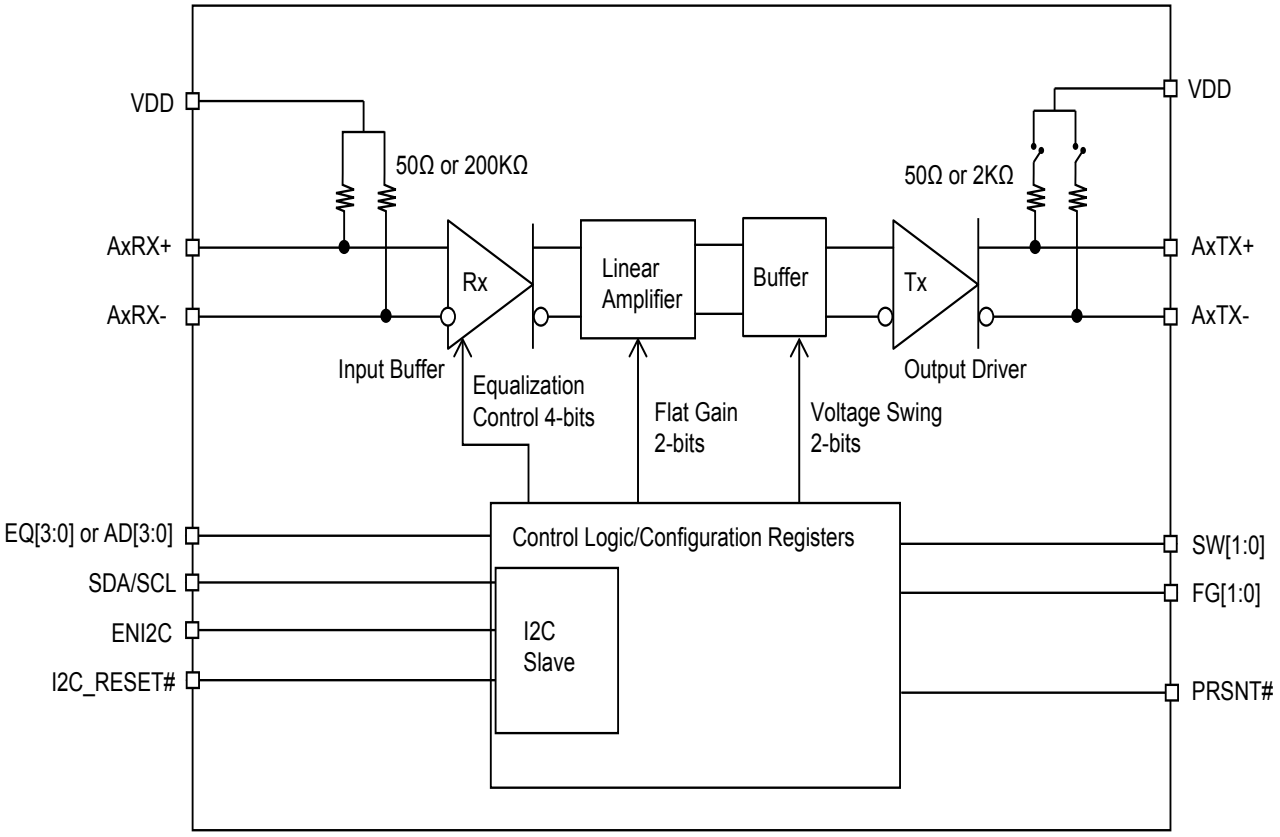


Figure 4-1. PI3DPX1203 Block Diagram

4.2 Function Description

4.2.1 Power-up Timing

After PRSNT# signal is properly set, power up timing sequence complete. PRSNT signal from controller must be low until power supply become stable.

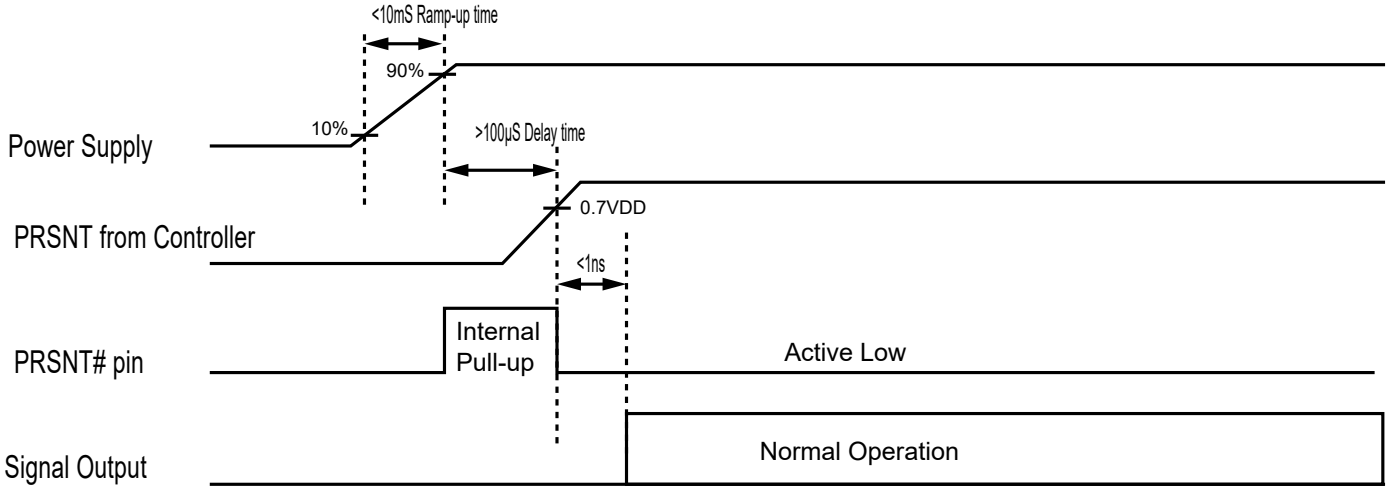


Figure 4-1 Power-up timing Sequence

4.2.2 Reset Implementation

When PRSNT# is high, the device is power-down mode and outputs are high impedance. It is critical to transition the PRSNT# , after the power supply VDD has reached the minimum recommended operation voltage. This can be achieved by the control signal GPO or by an external capacitor connected to GND.

To insure properly reset, the PRSNT# pin must be de-asserted for at least 100µS before re-asserted, and must be reprogrammed in I2C mode. When using external capacitor, the size of the cap value depends on the power-up VDD supply ramp. Larger value results in a slower ramp-up time. Consider 0.1uF capacitor is recommended as a reasonable first estimate.

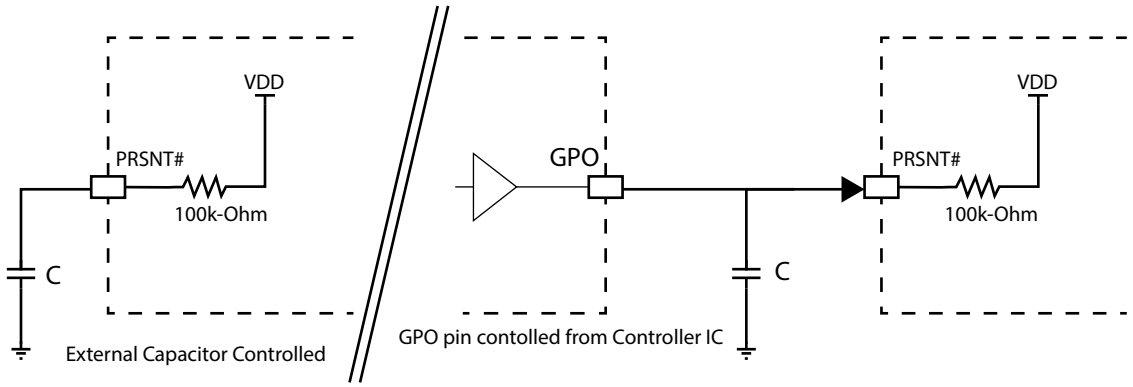


Figure 4-2 Reset Control from External Capacitor or GPO pin

4.2.3 Power-down Mode

Power-down mode can be controlled by the pin-strapping or I2C programming. When Cable Present Detection pin PRSNT# is set to HIGH, it enters into the power-down mode. Input and Output termination resistors set to 200 kΩ and 2 kΩ pull-up respectively.

PRSNT#	Description	Input Termination Resistor	Output Termination Resistor
H	Power-down mode. PRSNT# is internally pull-up 100 kΩ.	200 kΩ pull-up	2 kΩ pull-up
L	Active Low for normal operation	50 Ω pull-up	50 Ω pull-up

4.2.4 Output -1 dB Compression Setting

Swing Control 2 bits SW[1:0] can control the linearity of the output voltage, when input amplitude changes.

SW1	SW0	mVppd @ 8 Gbps
0	0	700
0	1	800
1	0	900
1	1	1000

4.2.5 Flat Gain Setting

Flat Gain Control 2 bits FG[1:0] are the selection bits for the DC value.

FG1	FG0	Gain
0	0	-4 dB
0	1	-2 dB
1	0	+0 dB
1	1	+2 dB

4.2.6 EQ Setting

Input EQ control 4 bits EQ[3:0] are the selection pins for the equalization selection of each Main Link channel.

EQ3	EQ2	EQ1	EQ0	8 Gbps Input EQ(dB)
0	0	0	0	3.3
0	0	0	1	3.8
0	0	1	0	4.3
0	0	1	1	4.8
0	1	0	0	5.4
0	1	0	1	5.8
0	1	1	0	6.3
0	1	1	1	6.8
1	0	0	0	7.2
1	0	0	1	7.7
1	0	1	0	8.1
1	0	1	1	8.5
1	1	0	0	8.9
1	1	0	1	9.2
1	1	1	0	9.6
1	1	1	1	9.9

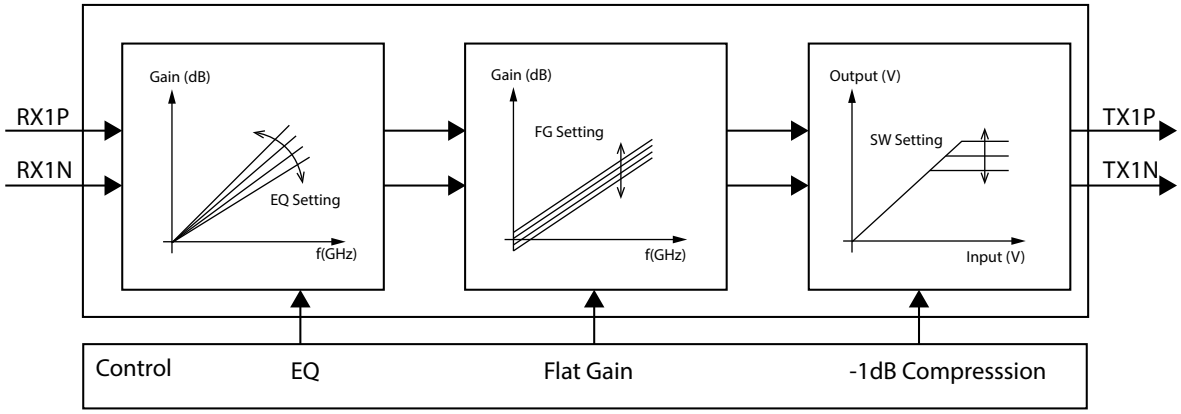


Figure 4-3 Illustration of EQ, Gain and Swing setting

5. I2C Programming

5.1 I2C Registers

I2C Address assignment								
	A6	A5	A4	A3	A2	A1	A0	R/W
Address Byte	1	1	1	AD3	AD2	AD1	AD0	1=R, 0=W

BYTE 0					
Bit	**Type**	**Power up condition**	**Description**	**Control affected**	**Comment**
7:0	Reserved				
BYTE 1					
Bit	**Type**	**Power up condition**	**Description**	**Control affected**	**Comment**
7:0	Reserved				
BYTE 2					
Bit	**Type**	**Power up condition**	**Description**	**Control affected**	**Comment**
7	R/W	0		A3 Power down	1 = Power down
6	R/W	0		A2 Power down	
5	R/W	0		A1 Power down	
4	R/W	0		A0 Power down	
3	R/W	0		Reserved	
2	R/W	0		Reserved	
1	R/W	0		Reserved	
0	R/W	0		Reserved	
BYTE 3					
Bit	**Type**	**Power up condition**	**Description**	**Control affected**	Comment
7	R/W	0	Channel A0 configuration	EQ3	Equalizer
6	R/W	0		EQ2	
5	R/W	0		EQ1	
4	R/W	0		EQ0	
3	R/W	0		FG1	Flat gain
2	R/W	0		FG0	
1	R/W	0		SW1	Swing
0	R/W	0		SW0	

BYTE 4					
Bit	**Type**	**Power up condition**	**Description**	**Control affected**	Comment
7	R/W	0	Channel A1 configuration	EQ3	Equalizer
6	R/W	0		EQ2	
5	R/W	0		EQ1	
4	R/W	0		EQ0	
3	R/W	0		FG1	Flat gain
2	R/W	0		FG0	
1	R/W	0		SW1	Swing
0	R/W	0		SW0	
BYTE 5					
Bit	**Type**	**Power up condition**	**Description**	**Control affected**	Comment
7	R/W	0	Channel A2 configuration	EQ3	Equalizer
6	R/W	0		EQ2	
5	R/W	0		EQ1	
4	R/W	0		EQ0	
3	R/W	0		FG1	Flat gain
2	R/W	0		FG0	
1	R/W	0		SW1	Swing
0	R/W	0		SW0	
BYTE 6					
Bit	**Type**	**Power up condition**	**Description**	**Control affected**	Comment
7	R/W	0	Channel A3 configuration	EQ3	Equalizer
6	R/W	0		EQ2	
5	R/W	0		EQ1	
4	R/W	0		EQ0	
3	R/W	0		FG1	Flat gain
2	R/W	0		FG0	
1	R/W	0		SW1	Swing
0	R/W	0		SW0	
BYTE 7					
Bit	**Type**	**Power up condition**	**Description**	**Control affected**	Comment
7:0	Reserved				

5.2 I2C Operation

The integrated I2C interface operates as a slave device. Standard mode (100Kbps) is supported with 7-bit addressing. The data byte format is 8-bit bytes, and supports the format of indexing to be compatible with other bus devices. In the Slave mode (ENI2C = HIGH), the device supports Read/Write. The bytes must be accessed in sequential order from the lowest to the highest byte with the ability to stop after any complete byte has been transferred.
Address bits A0 to A1 are programmable to support multiple chips environment.

5.3 I2C Data Transfer

Start & Stop Conditions

A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition, as shown in the figure below

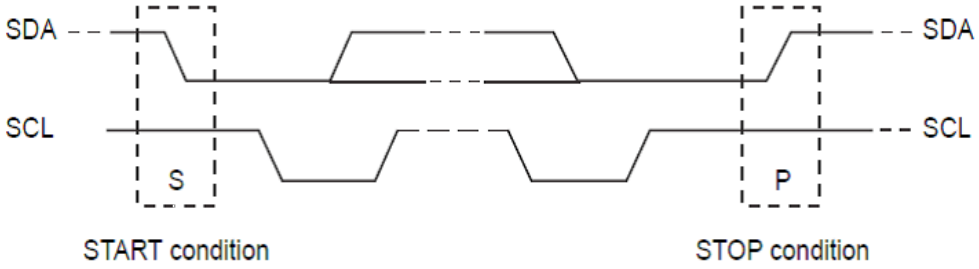


Figure 5-1. I2C START and STOP conditions

6. Electrical Specification

6.1 Absolute Maximum Ratings

Storage Temperature	–65 °C to +150 °C
Supply Voltage to Ground Potential	–0.5 V to +4.6 V
DC SIG Voltage	–0.5 V to V_{DD} + 0.5 V
Output Current	–25 mA to +25 mA
Power Dissipation Continuous	1.63 W
ESD, HBM	–2 kV to +2 kV
Maximum junction Temperature	125 °C

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

6.2 Recommended Operating Conditions(1)

Parameter(1)	Min.	Typ.	Max	Units
Power supply voltage (VDD to GND)	3.0	3.3	3.6	V
Supply Noise Tolerance (from 100KHz to 10MHz)		100		mVp-p
Ambient Temperature	-40	25	85	°C

(1) Typical parameters are measured at VCC = 3.3 ± 0.3V, TA = 25°C. They are for reference purposes, and are not production-tested

6.3 Power Consumption

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
VDD	Power supply voltage		3.0	3.3	3.6	V
IDD	Power supply current	SW[1:0]=11, VDD = 3.6 V		260	360	mA
IDDQ	Standby current	All other control pins are open		2.0	4.2	mA

6.4 AC/DC Characteristics

6.4.1 LVCMOS I/O DC Specifications

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
VIH	DC input logic HIGH		VDD/2 + 0.7		VDD + 0.3	V
VIL	DC input logic LOW		-0.3		VDD/2 - 0.7	V
VOH	At IOH = -200 µA		VDD + 0.2			V
VOL	At IOL = -200 µA				0.2	V
Vhys	Hysteresis of Schmitt trigger input		0.8			V

6.4.2 Main Link Differential

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$V_{RX-DIF-Fp-p}$	Peak to peak differential input voltage	For HBR		200(1)		mV
V_{ODO}	Differential overshoot voltage				15% *VDD	V
V_{ODU}	Differential undershoot voltage				25% *VDD	V
I_{OFF}	Single end standby current				10	μA
I_{SC}	Output short current				60	mA
G_P	Peaking gain: Compensation at 4 GHz, relative to 100 MHz, 100 mVp-p sine wave input	EQ[3:0] = 1111 EQ[3:0] = 1000 EQ[3:0] = 0000		9.9 7.2 3.3		dB
		Variation around typical	-3		+3	dB
G_F	Flat gain: 100 MHz, EQ[3:0] = 1000, SW[1:0] = 10	FG[1:0] = 11 FG[1:0] = 10 FG[1:0] = 01 FG[1:0] = 00		2 0 -2 -4		dB
		Variation around typical	-3		+3	dB
V_{1dB_100M}	-1 dB compression point of output swing at 100 MHz	SW[1:0] = 11 SW[1:0] = 10 SW[1:0] = 01 SW[1:0] = 00		1370 1280 1040 920		mVppd
C_{RX}	RX AC coupling capacitance			220		nF
S11	Input return loss(2)	10 MHz to 4.1 GHz differential		-13.0		dB
		1 GHz to 4.1 GHz common mode		-5.0		
S22	Output return loss(2)	10 MHz to 4.1 GHz differential		-15		dB
		1 GHz to 4.1 GHz common mode		-6.0		
R_{IN}	DC single-ended input impedance			50		Ω
	DC Differential Input Impedance			100		
R_{OUT}	DC single-ended output impedance			50		Ω
	DC Differential output Impedance			100		
Z_{RX-HIZ}	DC input impedance during reset or power down			200		kΩ
t_{PD}	Latency	From input to output		0.5		ns

Note:
(1) Please refer more data in the VIN/VOUT plot. VOUT changes withe EQ and FG setting. Both the Redriver and the Sink device system should be carefully designed to ensure sink-device compliance.

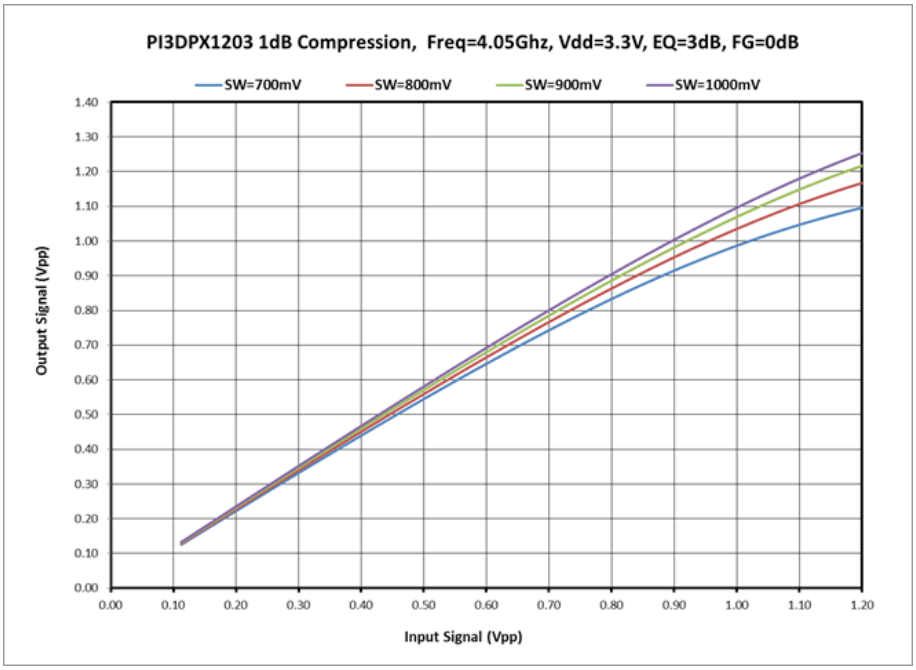


Figure 6-1. -1dB Compression(Voltage Sweep) between 0 to 600mV Inputs @ 8Gbps

(2) Measured using a vector-network analyzer (VNA) with -15dBm power level applied to the adjacent input. The VNA detects the signal at the output of the victim channel. All other inputs and outputs are terminated with 50Ω.

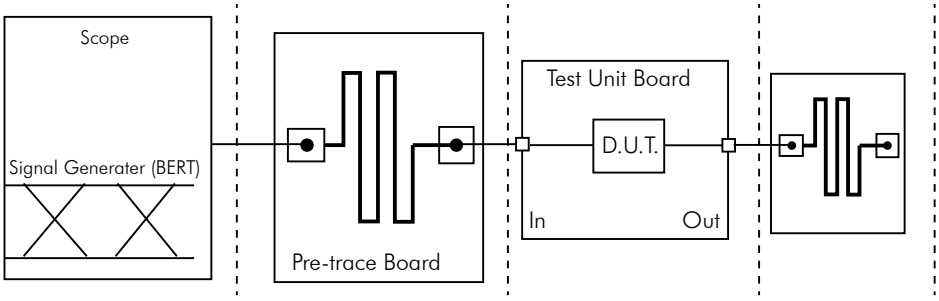


Figure 6-2. AC Electrical Measurement Test Setup

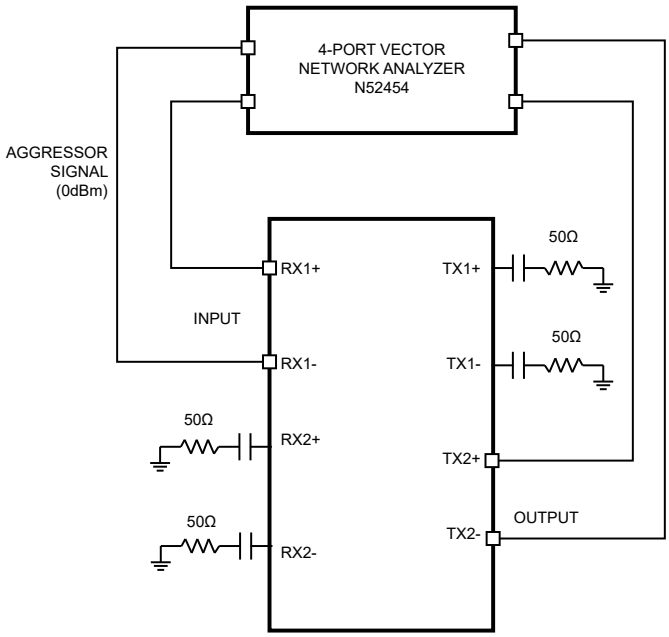


Figure 6-3. Channel-isolation test configuration

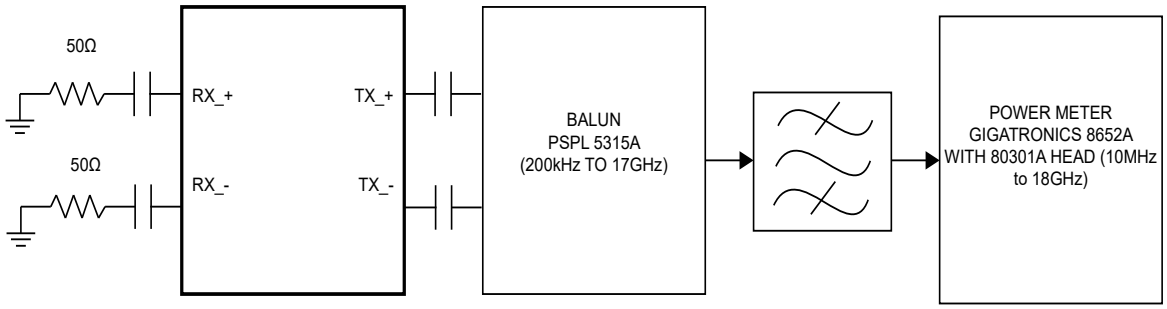
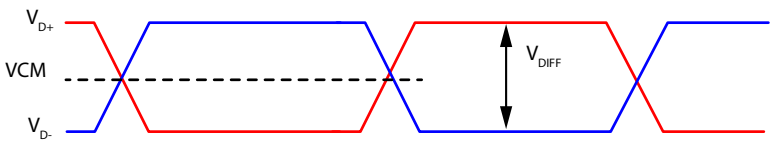


Figure 6-4. Noise test configuration

Common Mode Voltage
V_{CM} = (|VD+ + VD-| / 2)
V_{CMP} = (max |VD+ + VD-| / 2)



V_D + -V_D-

Symmetric Differential Swing
$V_{DIFFp-p}$ = (2 * max |V_{D+} - V_{D-}|)

Asymmetric Differential Swing
$V_{DIFFp-p}$ = (max |V_{D+} - V_{D-}| {V_{D+} > V_{D-}}
+ max |V_{D+} - V_{D-}| {V_{D+} < V_{D-}})

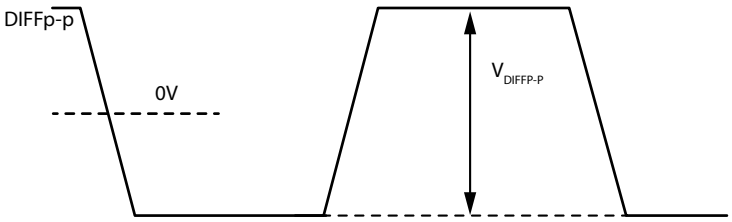


Figure 6-5. Definition of Differential Voltage and Differential Voltage Peak-to-Peak

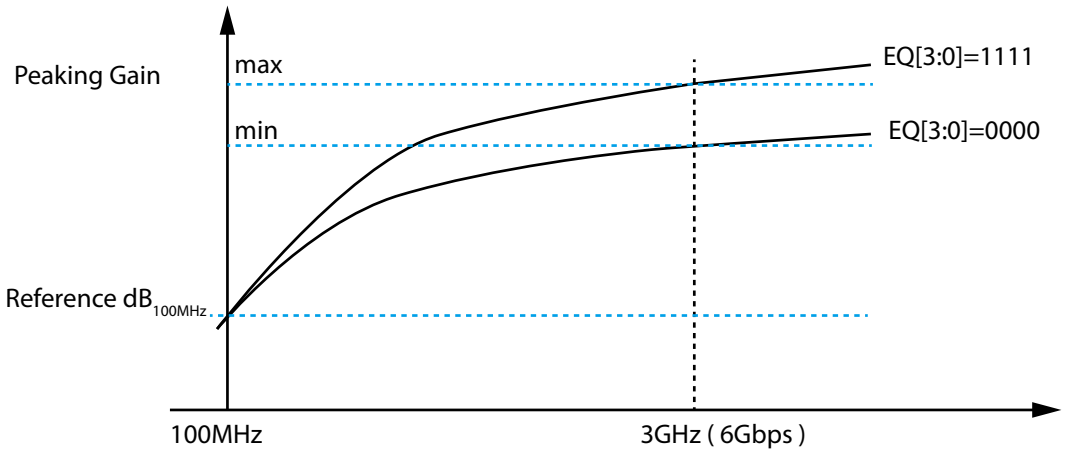


Figure 6-6. Definition of Peaking Gain relative to 100MHz, 100mVp-p sine wave input

6.4.3 SCL/SDA Specification for I2C BUS

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
SDA and SCL I/O for I2C-bus						
VDD	Nominal Bus Voltage		3.0		3.6	V
V_{IH}	DC input logic HIGH		$V_{DD}/2 + 0.7$		$V_{DD} + 0.3$	V
V_{IL}	DC input logic LOW		-0.3		$V_{DD}/2 - 0.7$	V
V_{OL}	DC output logic LOW	I_{OL} = 3mA			0.4	V
t_{OF}	Output fall time from VIHmin to VILmax with bus cap. 10-400pF				250	ns
AC/DC Specifications - SCL/SDA for I2C BUS						
I_{PU}	Current Through Pull-Up Resistor or Current Source	High Power specification	3.0		3.6	mA
Ileak-bus	Input leakage per bus segment		-200		200	uA
Ileak-pin	Input leakage per device pin			-15		uA
CI	Capacitance for SDA/SCL				10	pF
f_{SCLK}	Bus Operation Frequency			100		KHz
tBUF	"Bus Free Time Between Stop and Start condition"		1.3			us
tHD:STA	Hold time after (Repeated) Start condition. After this period, the first clock is generated.	At Ipull-up, Max	0.6			us
tSU:STA	Repeated start condition setup time		0.6			us
tSU:STO	Stop condition setup time		0.6			us
tHD:DAT	Data hold time		0			ns
tSU:DAT	Data setup time		100			ns
tLOW	Clock Low period		1.3			us
tHIGH	Clock High period		0.6		50	us
tF	Clock/Data fall time				300	ns
tR	Clock/Data rise time				300	ns
tPOR	"Time in which a device must be operation after power-on reset"				500	ms

Note:
(1) Recommended value.
(2) Recommended maximum capacitance load per bus segment is 400pF.
(3) Compliant to I2C physical layer specification.
(4) Ensured by Design. Parameter not tested in production.

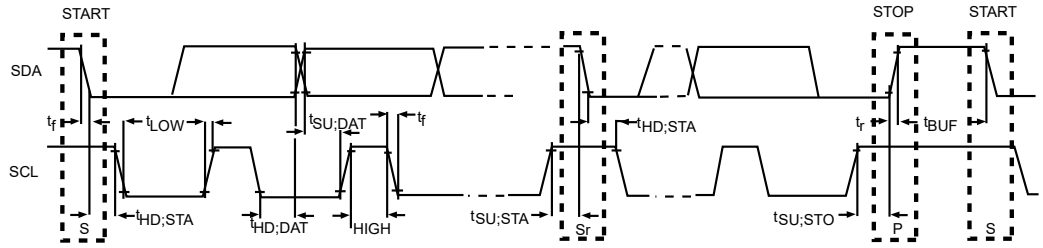


Figure 6-1 I2C Timing Diagram

6.5 Function Control vs. Output Signals (Informative)

6.5.1 Output Swing and Gain Information

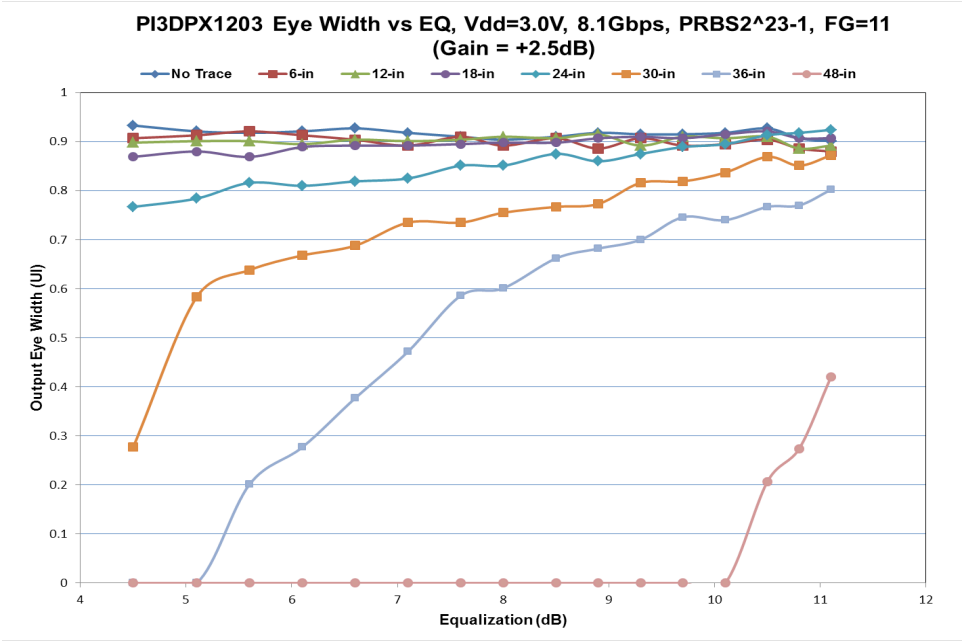


Figure 6-7. Eye Width vs EQ, Output Swing =1000mV, Gain=+2.5dB (Vin =800mVdiff)

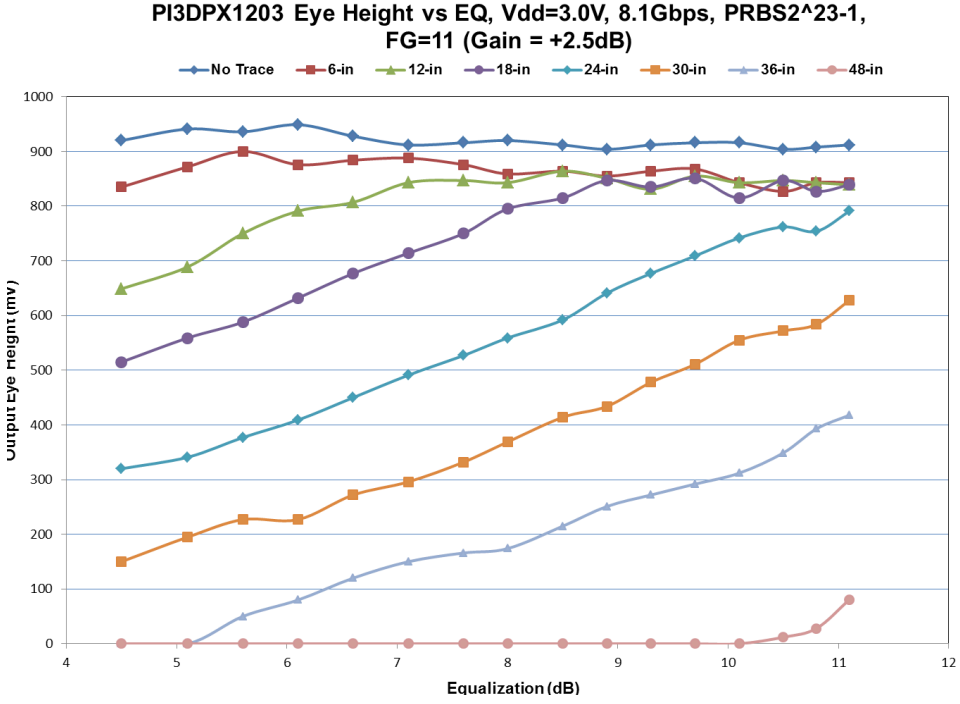


Figure 6-8. Eye Height vs EQ, Output Swing =1000mV, Gain=+2.5dB (Vin =800mVdiff)

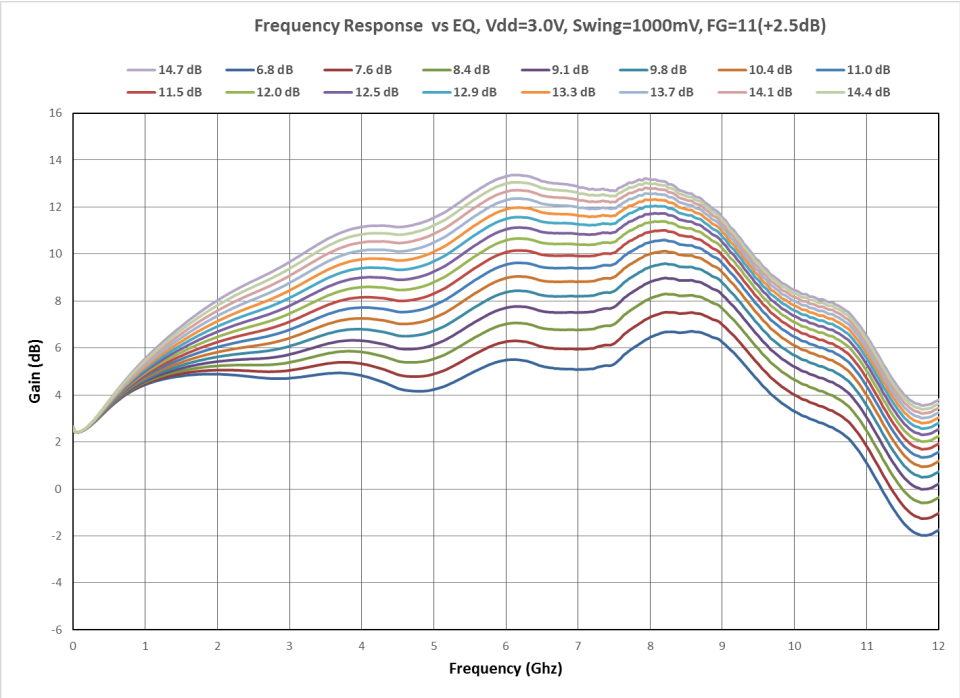


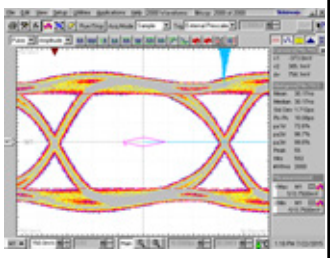
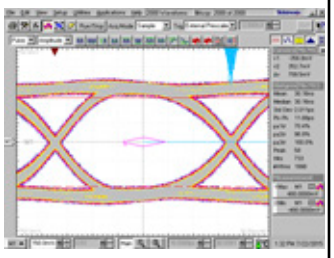
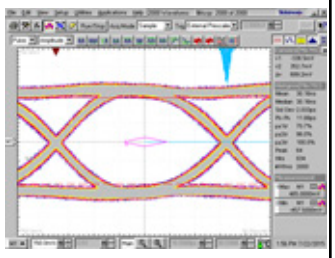
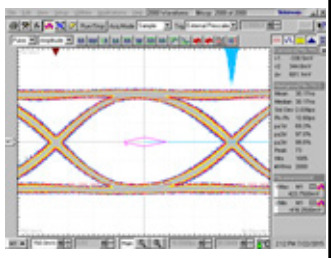
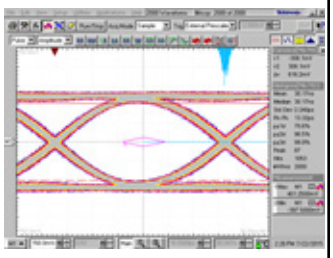
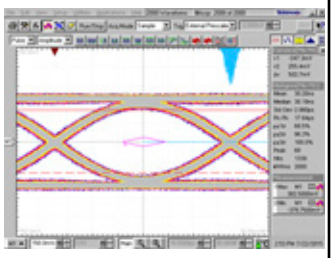
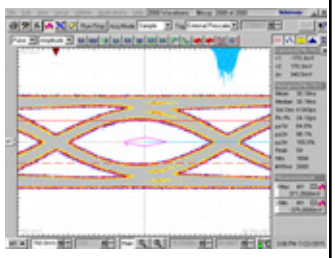
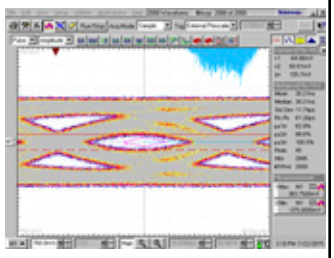
Figure 6-9. Frequency response vs EQ

Freq Response vs EQ, FG=11(+2.5dB), OutputSwing=1000mV, Vdd=3.0V, 25C
Input Power=-15dBm, No Input Trace

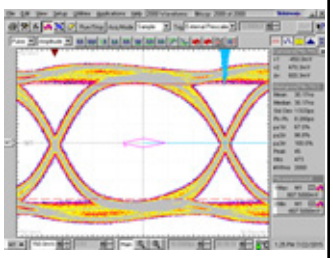
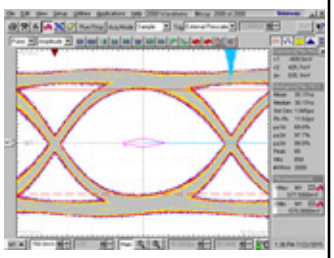
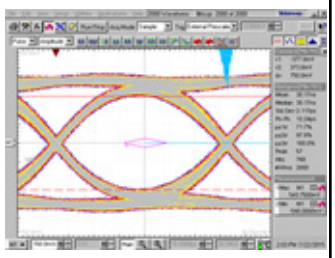
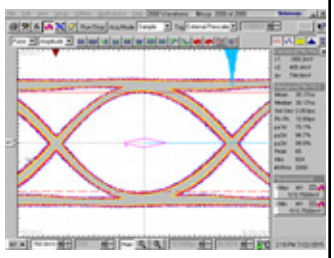
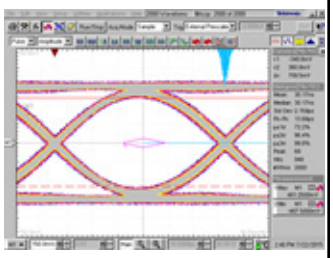
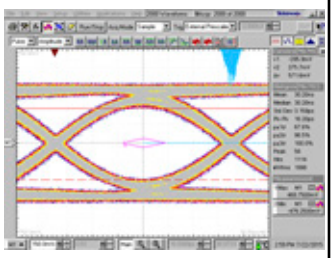
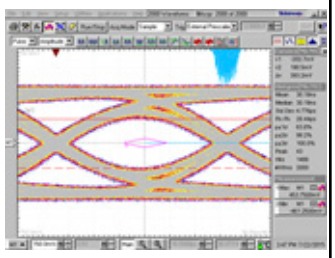
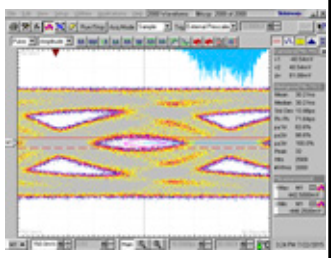
6.6 Output Eye diagram, Trace length and EQ

Condition: Output Eye Opening with Input Equalization, 8.1 Gbps, Vdd=3.0V, 25C , Using PRBS 2^23-1 pattern, Input Swing=800mVd, Output Swing= 1000mV

Output Eye waveform at FG 0.5dB

No Trace, FG = 0.5dB	FG=10(+0.5dB) 6-in	FG=10(+0.5dB) 12-in	FG=10(+0.5dB) 18-in
			
EQ=0000(4.5dB)	EQ=0000(4.5dB)	EQ=0100(6.6dB)	EQ=0110(7.6dB)
FG=10(+0.5dB) 24-in	FG=10(+0.5dB) 30-in	FG=10(0.5dB) 36-in	FG=10(+0.5dB) 48-in
			
EQ=1010(9.3dB)	EQ=1101(10.5dB)	EQ=1101(10.5dB)	EQ=1111(11.1dB)

Output Eye waveform at FG 2.5dB

FG=11 (+2.5dB) No Trace	FG=11 (+2.5dB), 6-in	FG=11 (+2.5dB), 12-in	FG=11 (+2.5dB) 18-in
			
EQ=0000(4.5dB)	EQ=0000(4.5dB)	EQ=0010(5.6dB)	EQ=0111(8.0dB)
FG=11 (+2.5dB) 24-in	FG=11 (+2.5dB) 30-in	FG=11 (+2.5dB) 36-in	FG=11 (+2.5dB) 48-in
			
EQ=1011(9.7dB)	EQ=1101(10.5dB)	EQ=1110(10.8dB)	EQ=1111(11.1dB)

Note:
(1) Trace card insertion loss profile is shown below.

Frequency	3 GHz	6 GHz	Units
6 inch Input Trace	-1.43	-4	dB
12 inch Input Trace	-6.1	-11	dB
18 inch Input Trace	-8.34	-15	dB
30 inch Input Trace	-10.14	-18	dB
36 inch Input Trace	-12.13	-22	dB
48 inch Input Trace	-16.42	-29	dB

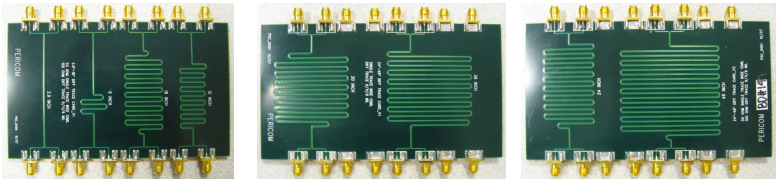


Figure 6-2 Trace board photo

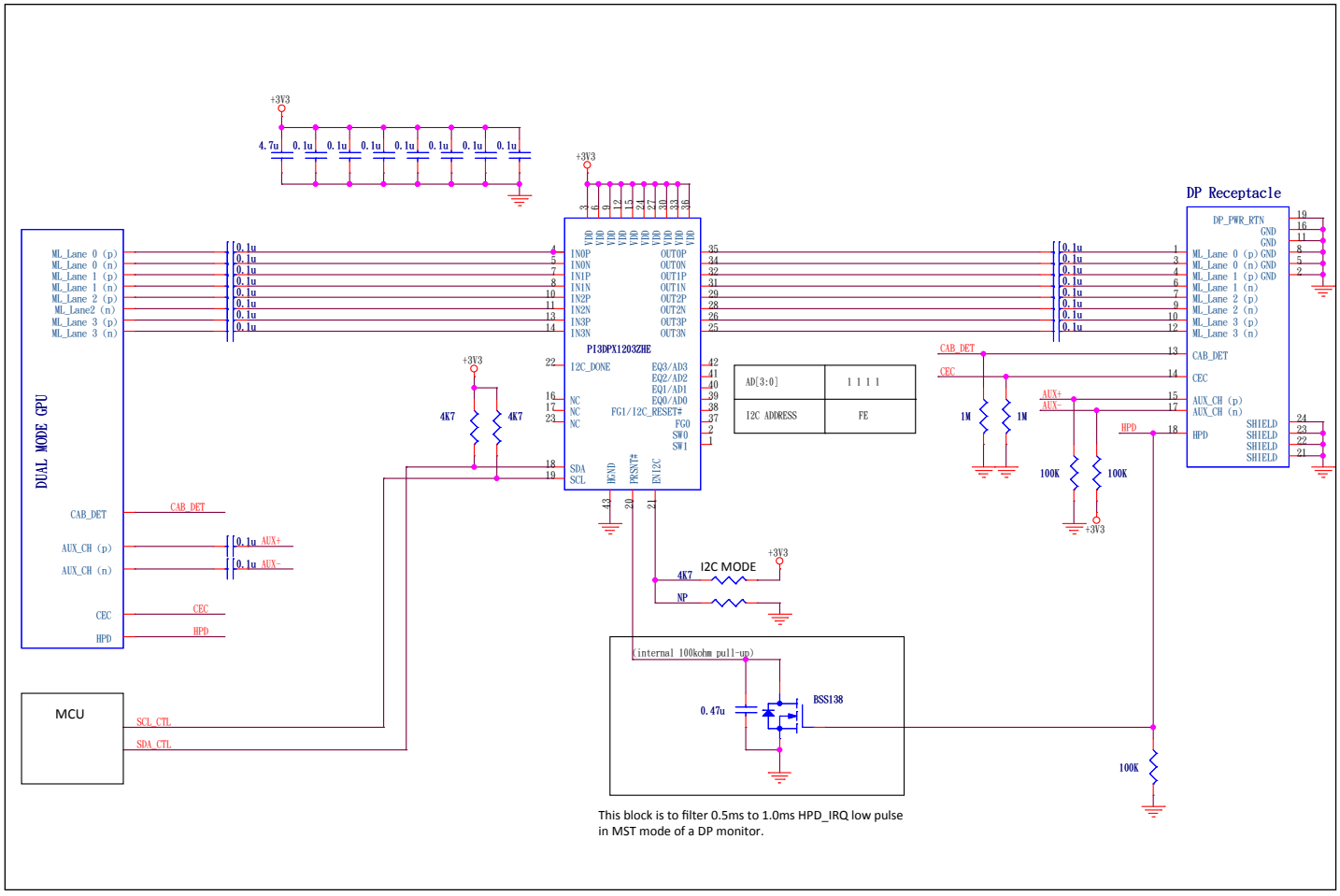
6.7 IDD with different mode settings at VDD = 3.3V [Informative]

Test Conditions			IDD (mA)		
Control Setting	Gain (dB)	Swing(mV)	-40C	25C	90C
FG/SW=0000	-3.5	700	199	216	226
FG/SW=0001	-3.5	800	217	233	243
FG/SW=0010	-3.5	900	234	250	260
FG/SW=0011	-3.5	1000	251	267	276
FG/SW=0100	-2.5	700	199	215	225
FG/SW=0101	-2.5	800	217	232	242
FG/SW=0110	-2.5	900	234	249	259
FG/SW=0111	-2.5	1000	251	266	276
FG/SW=1000	+0.5	700	199	215	224
FG/SW=1001	+0.5	800	216	232	241
FG/SW=1010	+0.5	900	233	249	258
FG/SW=1011	+0.5	1000	250	265	274
FG/SW=1100	+2.5	700	198	214	223
FG/SW=1101	+2.5	800	215	231	240
FG/SW=1110	+2.5	900	232	247	256
FG/SW=1111	+2.5	1000	249	264	273

7. Application/Implementation

7.1 Reference Schematic

- Determine the loss profile between a transmitter and a receiver.
- Based upon the loss profile and signal swing, determine the optimal equalization settings.
- Select appropriate voltage output swing.
- If required, select the correct differential pair polarity.
- To set voltage logic levels on configuration pins, use a 5-kΩ pullup for high level, tie pin to GND for low level,and place a 5-kΩ pullup and 5-kΩ pulldown for HiZ.



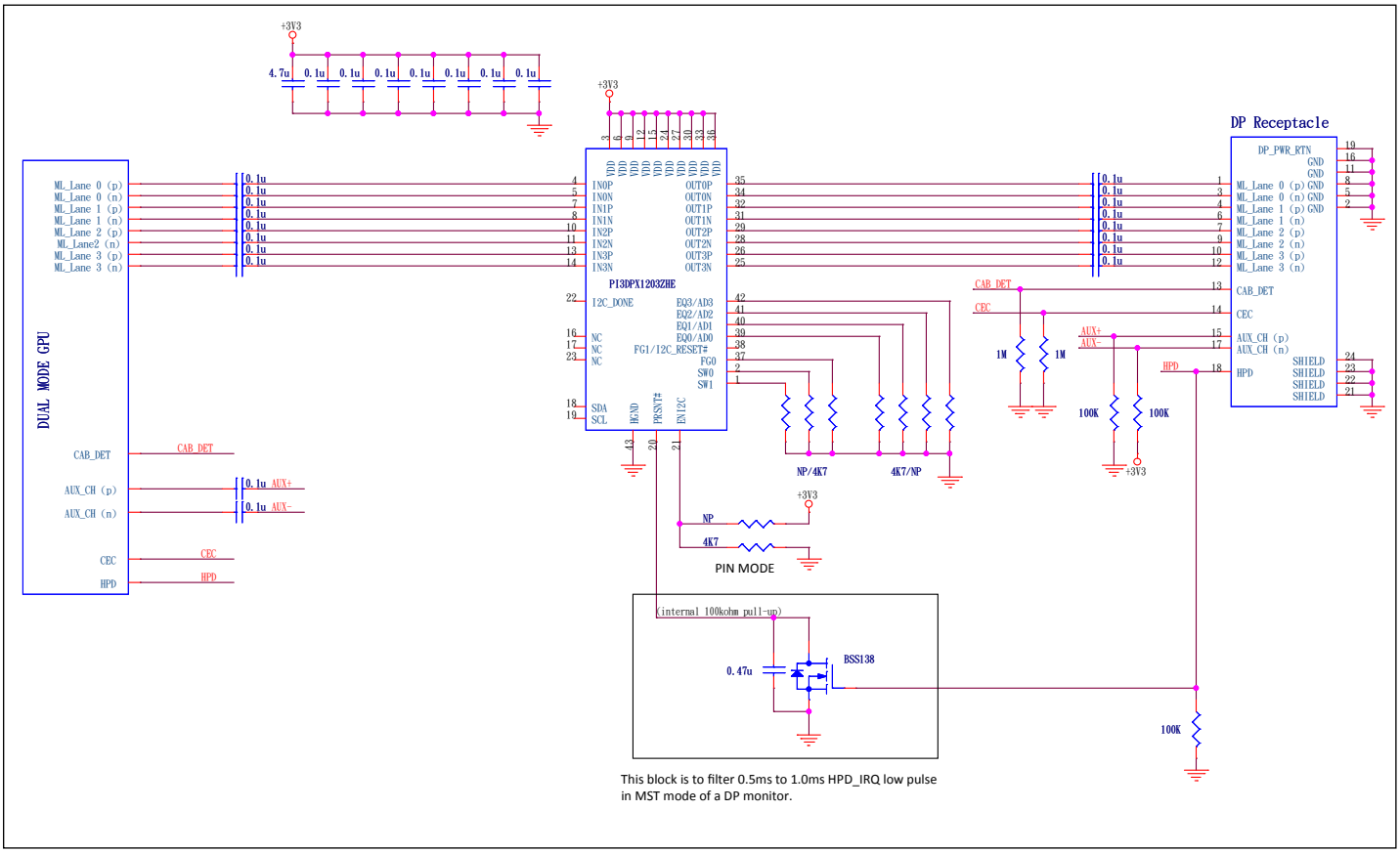
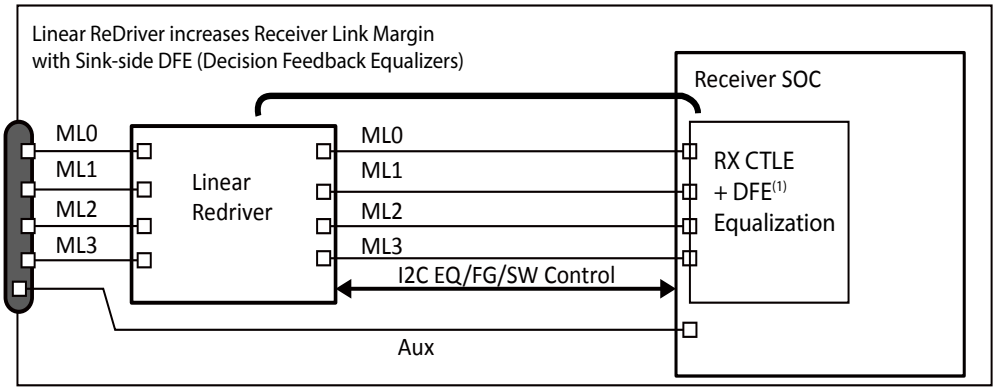


Figure 7-1 Source-side Application Circuit

7.2 Sink-side Application

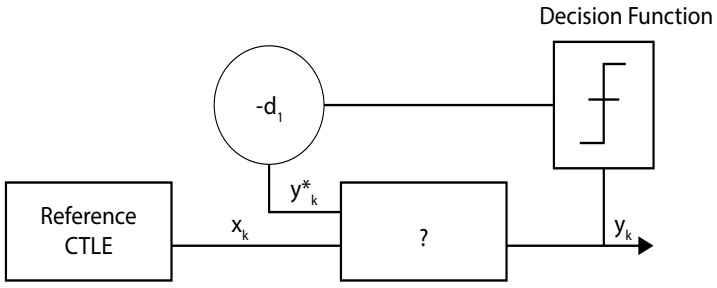


Note
(1) The HBR3 receiver equalizer includes a CTLE cascaded with a one-tap adaptive DFE with a feedback coefficient limited to < 50mV. The DFE behavior is described below.

$$y_k = x_k - d_1 * \text{sgn}(y_k - 1)$$

where:

y_k is the DFE differential output voltage
y^*_k is the decision function output voltage
x_k is the differential input voltage after CTLE
d_1 is the feedback coefficient
k is the UI sample



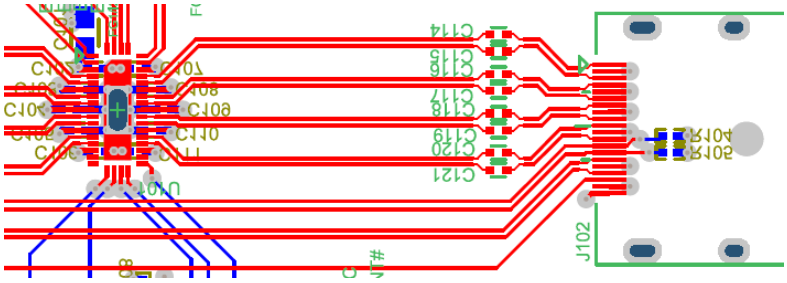
Reference HBR3 Receiver Equalizer DFE

7.3 Layout Guidelines

As transmission data rate increases rapidly, any flaws and/or mis-matches on PCB layout are amplified in terms of signal integrity. Lay-out guideline for high-speed transmission is highlighted in this application note.

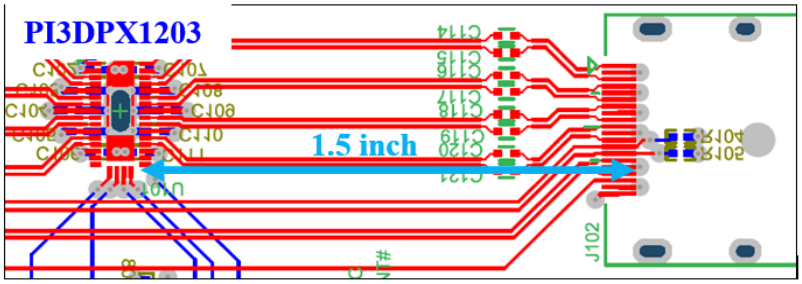
7.3.1 AC coupling Capacitor

Below is an example of placing AC coupling capacitors on high-speed channels.



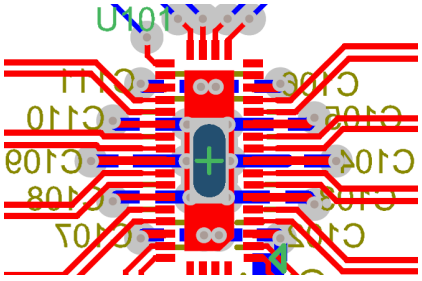
7.3.2 Location

To wisely use the equalization selections offered by PI3DPX1203, it is recommended to place PI3DPX1203 at the end of the entire path. In short, PI3DPX1203 should be located close to the output DP connector in a source application. Below is the PI3DPX1203 placement on its evaluation board.



7.3.3 Thermal Pad GND Via Recommendation

To wisely use the equalization selections offered by PI3DPX1203, it is recommended to place PI3DPX1203 at the end of the entire path. In short, PI3DPX1203 should be located close to the output DP connector in a source application. Below is the PI3DPX1203 placement on its evaluation board .



Several GND vias are the “must” requirement in thermal pad. The recommended Via size is 12/24 mil.

7.3.4 General Power and Ground Guideline

To provide a clean power supply for Pericom high-speed device, few recommendations are listed below:

- Power (VDD) and ground (GND) pins should be connected to corresponding power planes of the printed circuit board directly without passing through any resistor.
- The thickness of the PCB dielectric layer should be minimized such that the VDD and GND planes create low inductance paths.
- One low-ESR 0.1uF decoupling capacitor should be mounted at each VDD pin or should supply bypassing for at most two VDD pins. Capacitors of smaller body size, i.e. 0402 package, is more preferable as the insertion loss is lower. The capacitor should be placed next to the VDD pin.
- One capacitor with capacitance in the range of 4.7uF to 10uF should be incorporated in the power supply decoupling design as well. It can be either tantalum or an ultra-low ESR ceramic.
- A ferrite bead for isolating the power supply for Pericom high-speed device from the power supplies for other parts on the printed circuit board should be implemented.
- Several thermal ground vias must be required on the thermal pad. 25-mil or less pad size and 14-mil or less finished hole are recommended.

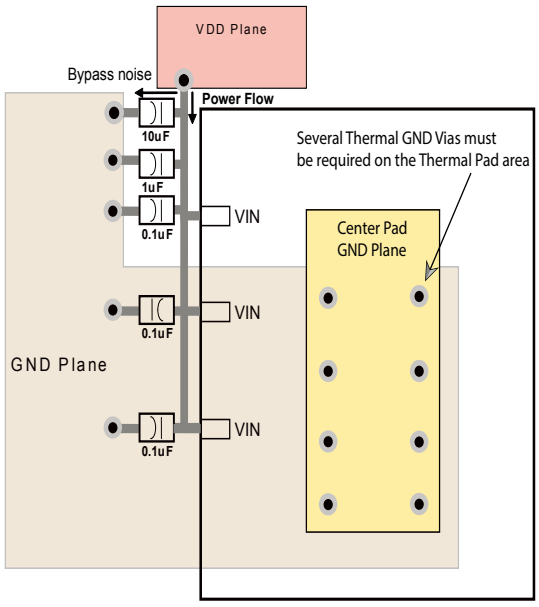


Figure 7-1 Decoupling Capacitor Placement Diagram

7.3.5 High-speed signal Routing

Good-designed layout is essential to prevent signal reflection:

- For 90Ω differential impedance, width-spacing-width micro-strip of 6-7-6 mils is recommended; for 100Ω differential impedance, width-spacing-width micro-strip of 5-7-5 mils is recommended.
- Differential impedance tolerance is targeted at ±15%.

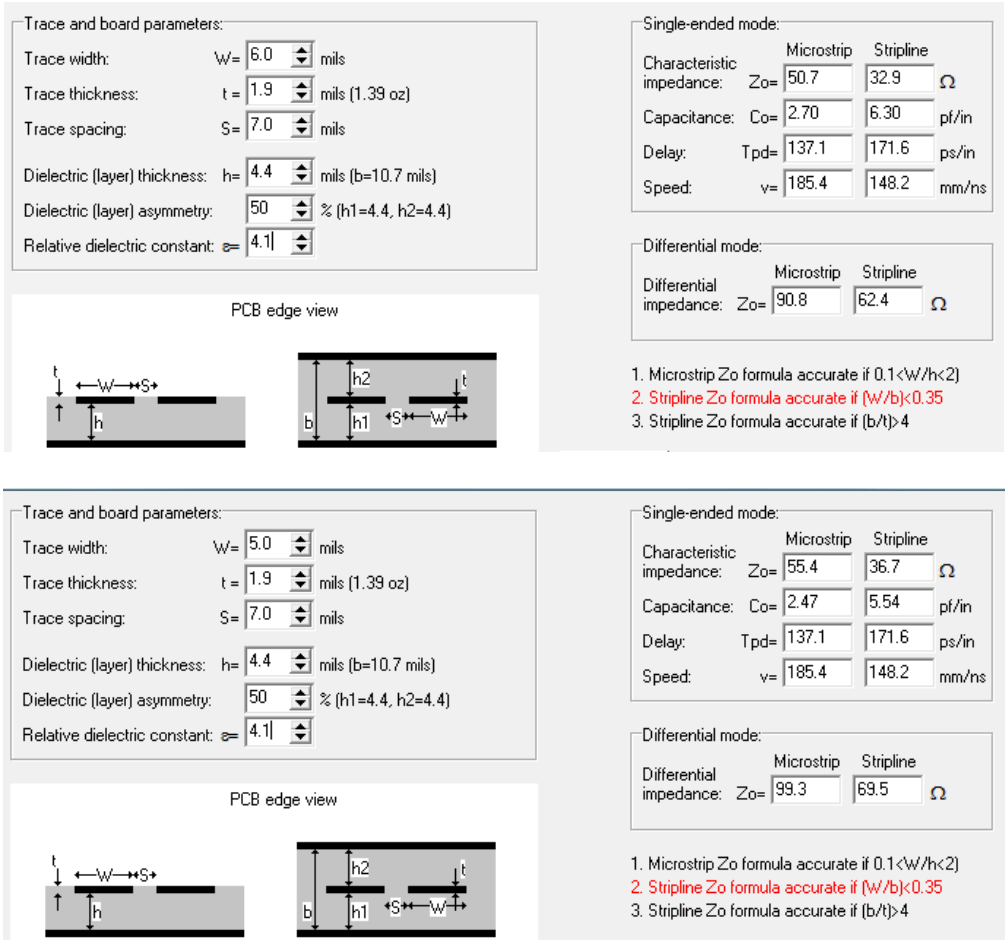


Figure 7-2 Trace Width and Clearance of Micro-strip and Strip-line

- For micro-strip, using 1/2oz Cu is fine. For strip-line in 6+ PCB layers, 1oz Cu is more preferable.

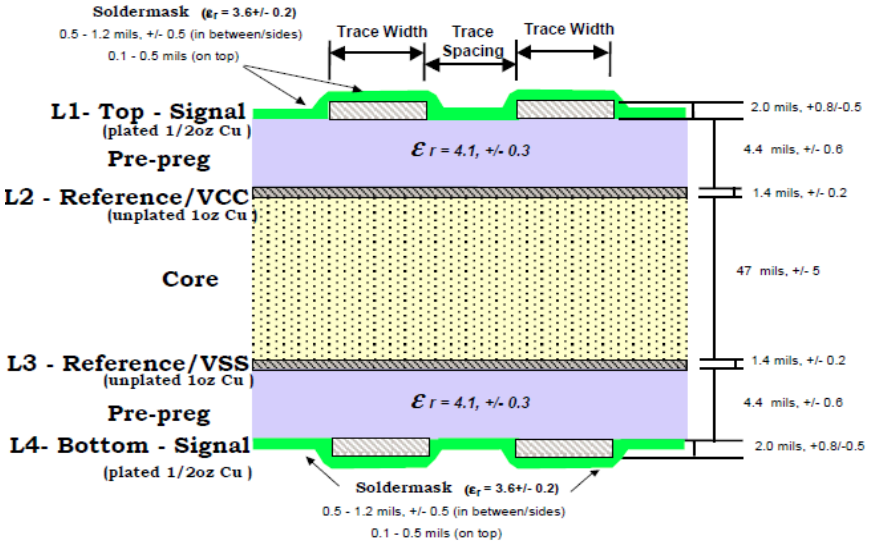


Figure 7-3 4-Layer PCB Stack-up Example

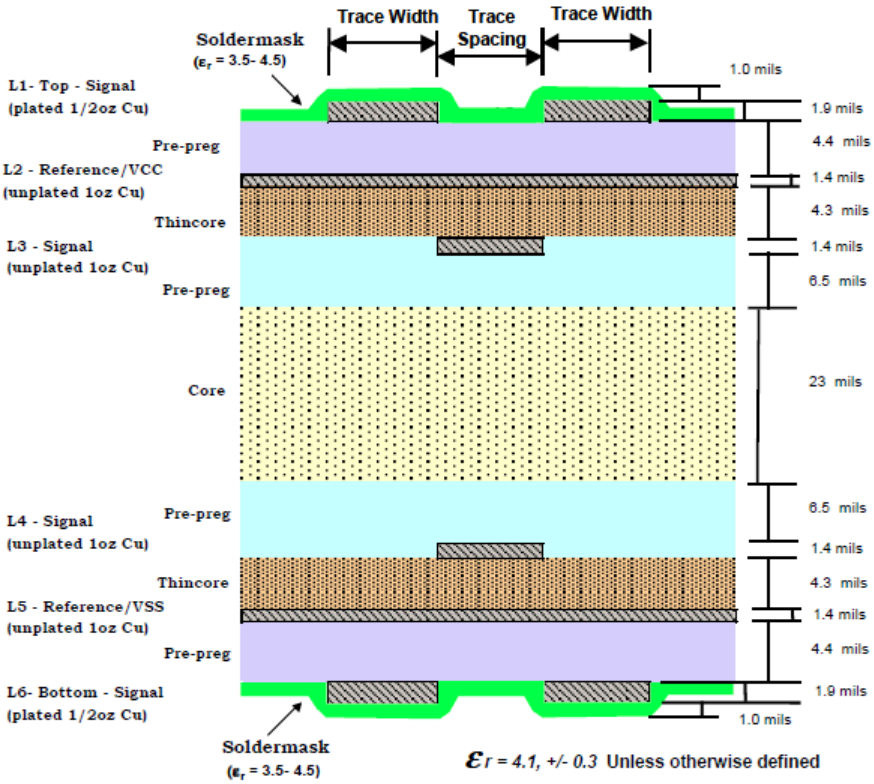


Figure 7-4 6-Layer PCB Stack-up Example

- Ground referencing is highly recommended. If unavoidable, stitching capacitors of 0.1uF should be placed when reference plane is changed.

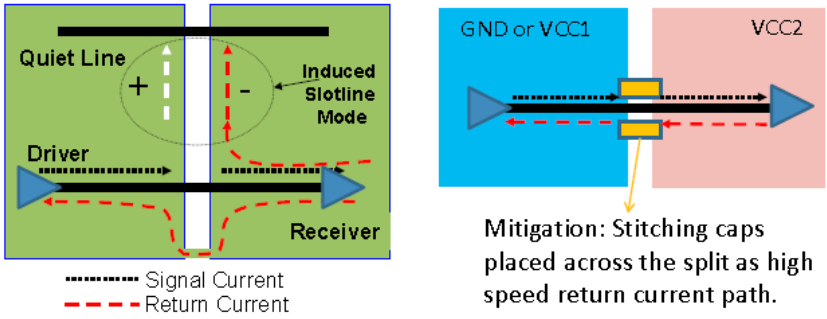


Figure 7-5 Stitching Capacitor Placement

- To keep the reference unchanged, stitching vias must be used when changing layers.
- Differential pair should maintain symmetrical routing whenever possible. The intra-pair skew of micro-strip should be less than 5 mils.

- To keep the reference unchanged, stitching vias must be used when changing layers.
- Differential pair should maintain symmetrical routing whenever possible. The intra-pair skew of micro-strip should be less than 5 mils.

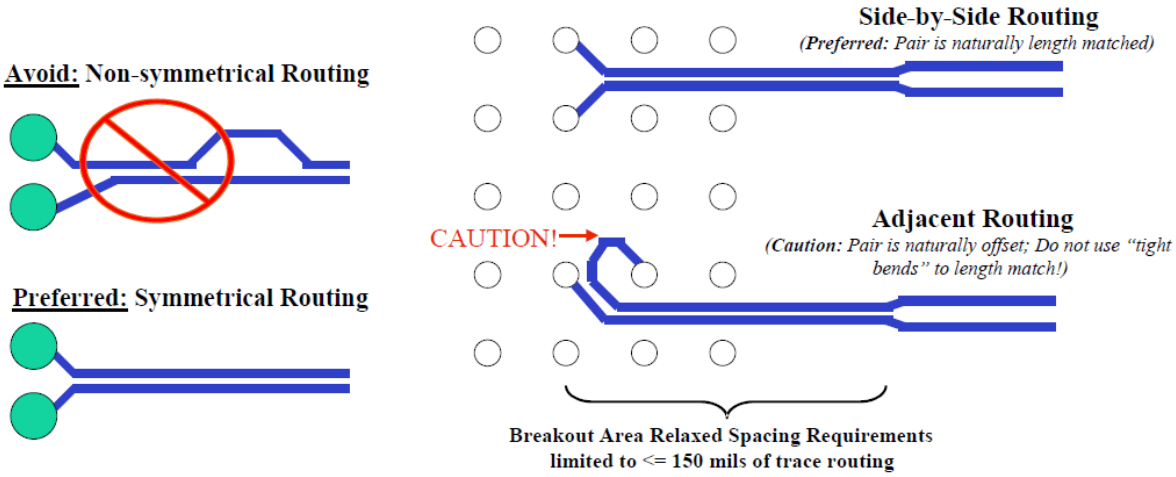


Figure 7-6 Layout Guidance of Matched Differential Pair

- For minimal crosstalk, inter-pair spacing between two differential micro-strip pairs should be at least 20 mils or 4 times the dielectric thickness of the PCB.
- Wider trace width of each differential pair is recommended in order to minimize the loss, especially for long routing. More consistent PCB impedance can be achieved by a PCB vendor if trace is wider.
- Differential signals should be routed away from noise sources and other switching signals on the printed circuit board.
- To minimize signal loss and jitter, tight bend is not recommended. All angles α should be at least 135 degrees. The inner air gap A should be at least 4 times the dielectric thickness of the PCB.

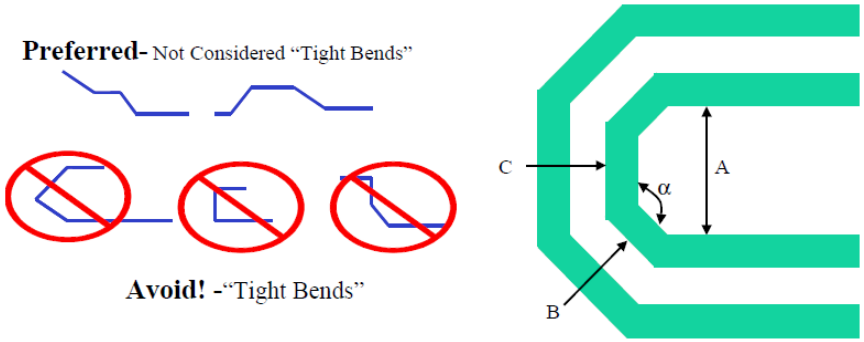


Figure 7-7 Layout Guidance of Bends

- Stub creation should be avoided when placing shunt components on a differential pair.

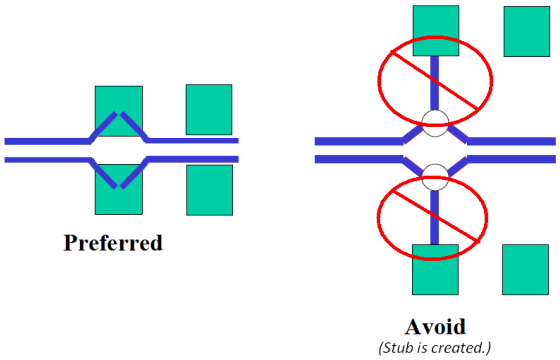


Figure 7-8 Layout Guidance of Shunt Component

- Placement of series components on a differential pair should be symmetrical.

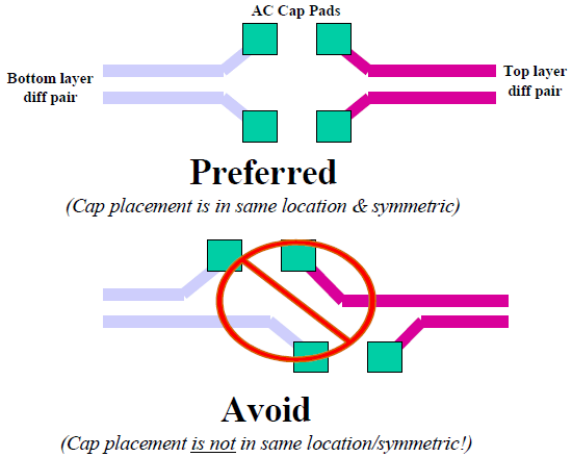


Figure 7-9 Layout Guidance of Series Component

- Stitching vias or test points must be used sparingly and placed symmetrically on a differential pair.

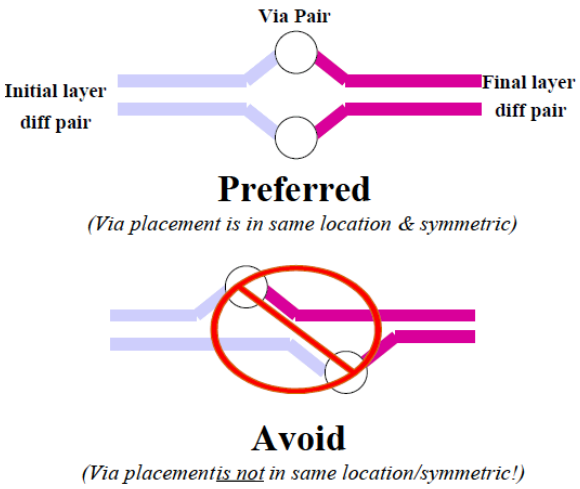


Figure 7-10 Layout Guidance of Stitching Via

7.4 DP 1.4 CTS Test Report

Internal DisplayPort test setup is shown below for the reference.

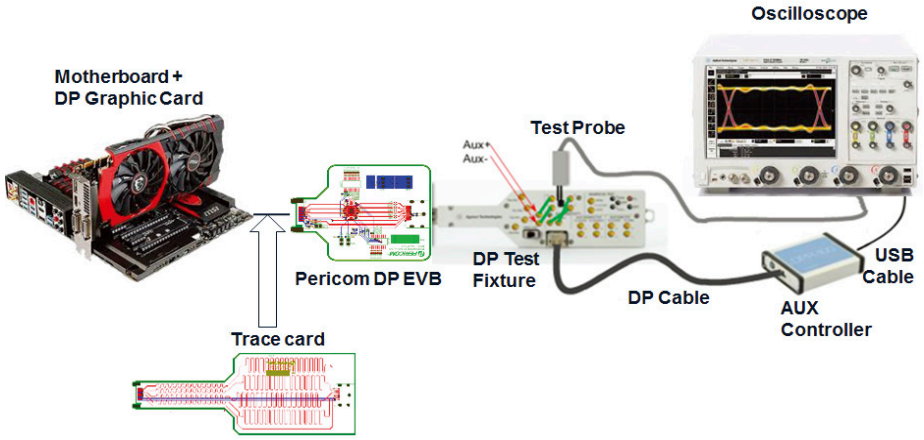


Figure 7-11 Displayport test set-up

Below is application-side trace card insertion loss information.

DP FR4 trace	0 in	6 in	12 in	18 in	24 in	30 in	36 in
Insertion loss @ 8.1Gbps	-8.15 dB	-11.52 dB	-14.88 dB	-17.60 dB	-19.94 dB	-22.92 dB	-28.62 dB

PI3DPX1203 DP1.4 CTS Report

Overall Result: PASS

Test Configuration Details	
Device Description	
Test Specification	1.4
Lane	4 Lanes
SSC	Disabled
Test Session Details	
DisplayPort Test Controller	UnigrafDPTC
Fixture Type	Other
Infiniium SW Version	05.70.00901
Infiniium Model Number	DSOX92504A
Infiniium Serial Number	MY54410104
Application SW Version	3.52.0001
Debug Mode Used	No
Compliance Limits (official)	DisplayPort Compliance Test Specification Version 1.4 Official Test Limit

Summary of Results

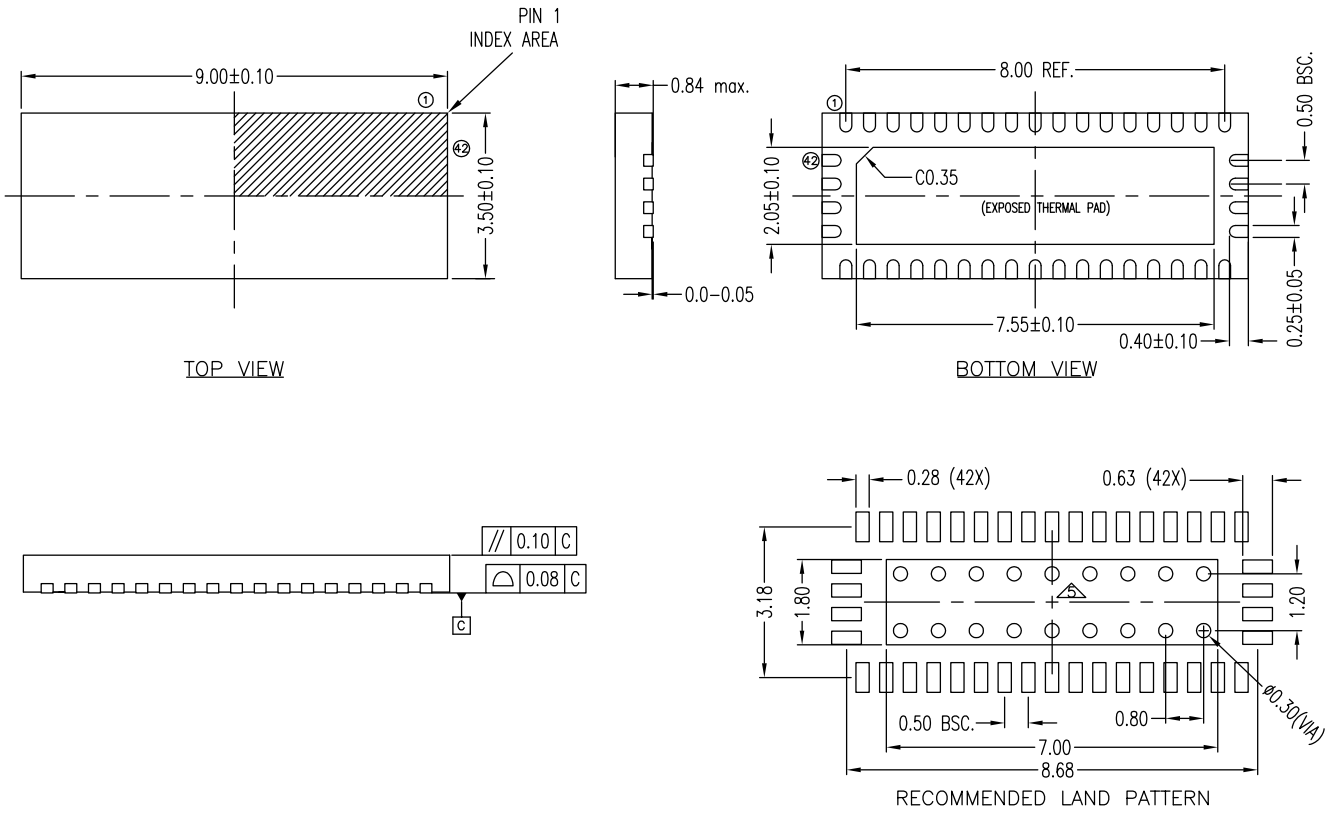
Test Statistics	
Failed	0
Passed	15
Total	15

Margin Thresholds	
Warning	< 2 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Worst Actual	Worst Margin	Pass Limits
✓	0	2	3.1 Lane 3 - Eye Diagram Test (TP3_EQ) (HBR2 and HBR3) - HBR2CPAT	0.000	50.0 %	-500 m <= VALUE <= 500 m
✓	0	1	3.1 Lane 3 - Eye Diagram Test with No Cable Model (TP3_EQ) (HBR2 and HBR3) - HBR2CPAT	0.000	50.0 %	-500 m <= VALUE <= 500 m
✓	0	2	3.12 Lane 3 - Total Jitter Test (TP3_EQ) (High Bit Rate 3) - HBR2CPAT	566.000 mUI	12.9 %	VALUE <= 650.000 mUI
✓	0	1	3.12 Lane 3 - Total Jitter Test with No Cable Model (TP3_EQ) (High Bit Rate 3) - HBR2CPAT	626.600 mUI	3.6 %	VALUE <= 650.000 mUI
✓	0	10	3.3 Lane 3 - Peak to Peak Voltage Test - PLTPAT	874 mV	36.7 %	VALUE <= 1.380 V
✓	0	1	3.2 Lane 3 - Non Pre-Emphasis Level Test (Swing 2/Swing 0) - PLTPAT	5.3748 dB	10.3 %	5.2000 dB <= VALUE <= 6.9000 dB
✓	0	1	3.2 Lane 3 - Non Pre-Emphasis Level Test (Swing 2/Swing 1) - PLTPAT	3.0294 dB	24.8 %	1.6000 dB <= VALUE <= 3.5000 dB
✓	0	4	3.3 Lane 3 - Pre-Emphasis Level Test (Pre-emphasis 0) - PLTPAT	-3.536 dB	151E+01 %	VALUE <= 250 mdB
✓	0	3	3.3 Lane 3 - Pre-Emphasis Level Delta Test (Pre-emphasis 1 to Pre-emphasis 0) - PLTPAT	2.021 dB	**1.1 %**	VALUE >= 2.000 dB
✓	0	1	3.3 Lane 3 - Non-Transition Voltage Range Measurement (Swing 2) - PLTPAT	1.007	42.2 %	VALUE >= 708 m
✓	0	2	3.3 Lane 3 - Pre-Emphasis Level Delta Test (Pre-emphasis 2 to Pre-emphasis 1) - PLTPAT	2.304 dB	44.0 %	VALUE >= 1.600 dB
✓	0	1	3.3 Lane 3 - Non-Transition Voltage Range Measurement (Swing 1) - PLTPAT	1.037	46.5 %	VALUE >= 708 m
✓	0	1	3.3 Lane 3 - Pre-Emphasis Level Delta Test (Pre-emphasis 3 to Pre-emphasis 2) - PLTPAT	1.874 dB	17.1 %	VALUE >= 1.600 dB
✓	0	1	3.3 Lane 3 - Non-Transition Voltage Range Measurement (Swing 0) - PLTPAT	1.026	20.7 %	VALUE >= 850 m
✓	0	1	3.2 Lane 3 - Non Pre-Emphasis Level Test (Swing 3/Swing 2) - PLTPAT	1.8652 dB	25.4 %	1.0000 dB <= VALUE <= 4.4000 dB

8. Mechanical / Packaging

8.1 Packaging Mechanical



NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO-220
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
5. THERMAL PAD SOLDERING AREA (MESH STENCIL IS RECOMMENDED).

DIODES INCORPORATED / PERICOM ENABLING SERIAL CONNECTIVITY	DATE: 07/28/16
DESCRIPTION: 42-Contact, Very Thin Quad Flat No-Lead (TQFN)	
PACKAGE CODE: ZH (ZH42)	
DOCUMENT CONTROL #: PD-2035	REVISION: F

8.2 Part Marking Information

Our standard product mark follows our standard part number ordering information, except for those products with a speed letter code. The speed letter code mark is placed after the package code letter, rather than after the device number as it is ordered. After electrical test screening and speed binning has been completed, we then perform an "add mark" operation which places the speed code letter at the end of the complete part number.

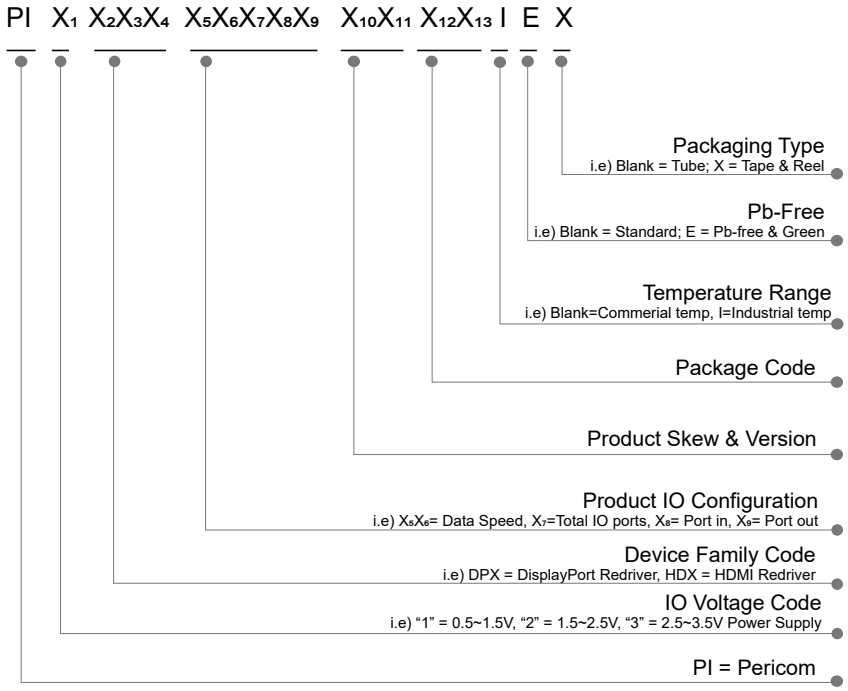


Figure 8-1 Part naming information

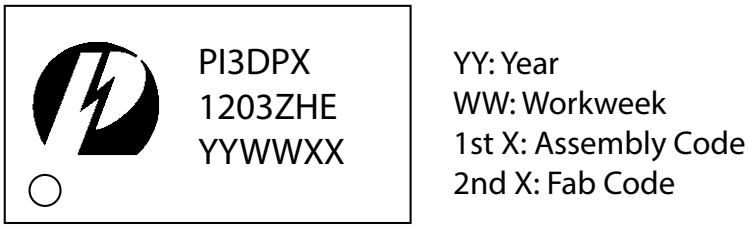


Figure 8-2 Part marking information

8.3 Tape & Reel Materials and Design

Carrier Tape

The Pocketed Carrier Tape is made of Conductive Polystyrene plus Carbon material (or equivalent). The surface resistivity is 106Ohm/sq. maximum. Pocket tapes are designed so that the component remains in position for automatic handling after cover tape is removed. Each pocket has a hole in the center for automated sensing if the pocket is occupied or not, thus facilitating device removal. Sprocket holes along the edge of the center tape enable direct feeding into automated board assembly equipment. See Figures 3 and 4 for carrier tape dimensions.

Cover Tape

Cover tape is made of Anti-static Transparent Polyester film.The surface resistivity is 107Ohm/Sq. Minimum to 1011Ohm sq. maximum. The cover tape is heat-sealed to the edges of the carrier tape to encase the devices in the pockets. The force to peel back the cover tape from the carrier tape shall be a MEAN value of 20 to 80gm (2N to 0.8N).

Reel

The device loading orientation is in compliance with EIA-481, current version. The loaded carrier tape is wound onto either a 13-inch reel, or 7-inch reel. The reel is made of Antistatic High-Impact Polystyrene. The surface resistivity 10^{7}Ohm/sq. minimum to 10^{11}Ohm/sq. max.

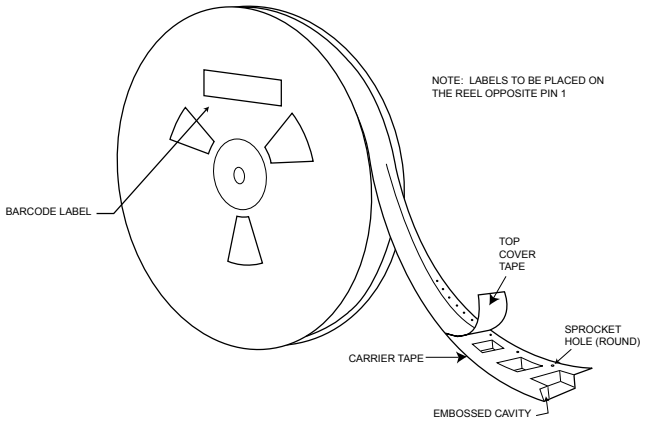


Figure 8-3 Tape & Reel label information

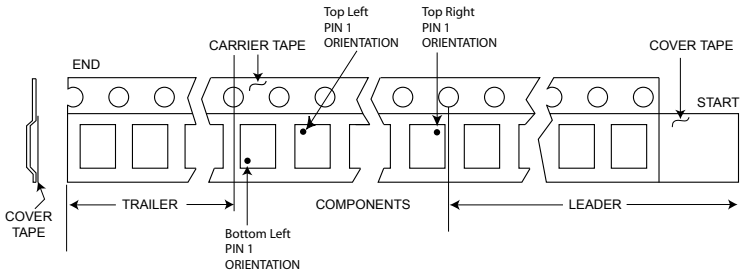


Figure 8-4 Tape leader and trailer pin 1 orientations

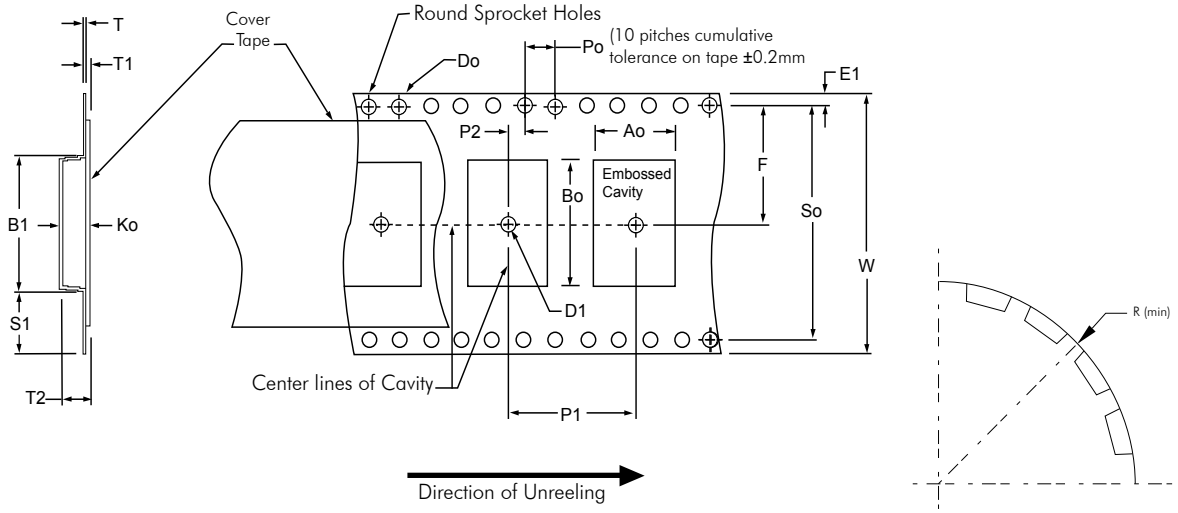


Figure 8-5 Standard embossed carrier tape dimensions

Table 8-1. Constant Dimensions

Tape Size	D0	D1 (Min)	E1	P0	P2	R (See Note 2)	S1 (Min)	T (Max)	T1 (Max)
8mm	1.5 +0.1 -0.0	1.0	1.75 ± 0.1	4.0 ± 0.1	2.0 ± 0.05	25	0.6	0.6	0.1
12mm		1.5				30			
16mm					2.0 ± 0.1				
24mm									
32mm		2.0				50	N/A (See Note 3)		
44mm					2.0 ± 0.15				

Table 8-2. Variable Dimensions

Tape Size	P_1	B_1 (Max)	E_2 (Min)	F	So	T_2 (Max.)	W (Max)	A_0, B_0, & K_0
8mm	Specific per package type. Refer to FR-0221 (Tape and Reel Packing Information) or visit www.pericom.com/pdf/gen/tapereel.pdf	4.35	6.25	3.5 ± 0.05	N/A (see note 4)	2.5	8.3	See Note 1
12mm		8.2	10.25	5.5 ± 0.05		6.5	12.3	
16mm		12.1	14.25	7.5 ± 0.1		8.0	16.3	
24mm		20.1	22.25	11.5 ± 0.1		12.0	24.3	
32mm		23.0	N/A	14.2 ± 0.1	28.4± 0.1		32.3	
44mm		35.0	N/A	20.2 ± 0.15	40.4 ± 0.1	16.0	44.3	

NOTES:
1. A0, B0, and K0 are determined by component size. The cavity must restrict lateral movement of component to 0.5mm maximum for 8mm and 12mm wide tape and to 1.0mm maximum for 16,24,32, and 44mm wide carrier. The maximum component rotation within the cavity must be limited to 20o maximum for 8 and 12 mm carrier tapes and 10o maximum for 16 through 44mm.
2. Tape and components will pass around reel with radius "R" without damage.
3. S1 does not apply to carrier width ≥32mm because carrier has sprocket holes on both sides of carrier where Do≥S1.
4. So does not exist for carrier ≤32mm because carrier does not have sprocket hole on both side of carrier.

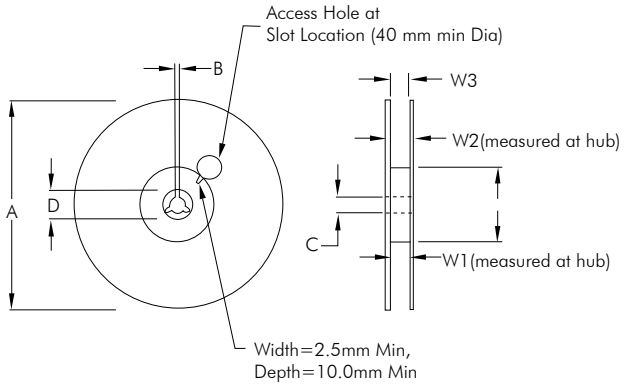


Table 8-3. Reel dimensions by tape size

Tape Size	A	N (Min) See Note A	W1	W2(Max)	W3	B (Min)	C	D (Min)
8mm	178 ±2.0mm or 330±2.0mm	60 ±2.0mm or 100±2.0mm	8.4 +1.5/-0.0 mm	14.4 mm	Shall Accommodate Tape Width Without Interference	1.5mm	13.0 +0.5/-0.2 mm	20.2mm
12mm			12.4 +2.0/-0.0 mm	18.4 mm				
16mm	330 ±2.0mm	100 ±2.0mm	16.4 +2.0/-0.0 mm	22.4 mm				
24mm			24.4 +2.0/-0.0 mm	30.4 mm				
32mm			32.4 +2.0/-0.0 mm	38.4 mm				
44mm			44.4 +2.0/-0.0 mm	50.4 mm				

NOTE:
A. If reel diameter A=178 ±2.0mm, then the corresponding hub diameter (N(min) will by 60 ±2.0mm. If reel diameter A=330±2.0mm, then the corresponding hub diameter (N(min)) will by 100±2.0mm.