A product Line of
Diodes Incorporated

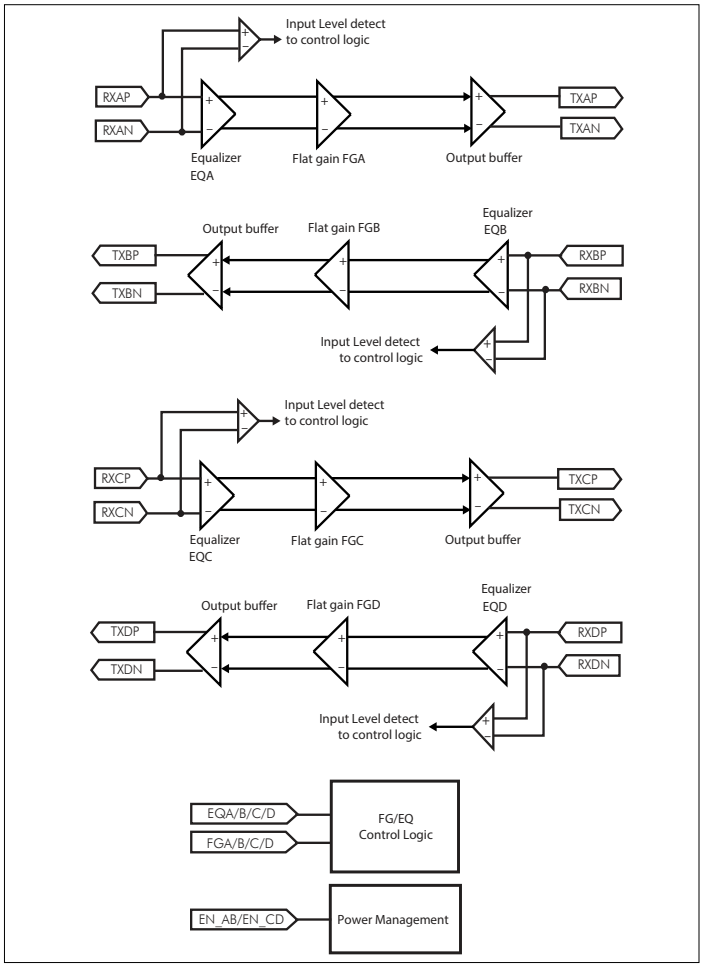
PI3EQX1004B1

2-Port USB3.1 Gen-2 10Gbps ReDriver

Features

- 5 & 10Gbps serial link with linear equalizer
- USB3.1 and USB3.0 Compatible
- Full Compliancy to USB3.1 Super Speed Standard
- Four 10Gbps differential signal pairs
- Pin Adjustable Receiver Equalization
- Pin Adjustable Flat Gain
- 100Ω Differential CML I/O's
- Automatic Receiver Detect
- Auto "Slumber" mode for adaptive power management
- Single Supply Voltage: 3.3V
- Packaging:
  - 42-pin, TQFN 3.5 x 9mm (ZH42)

Block Diagram



Description

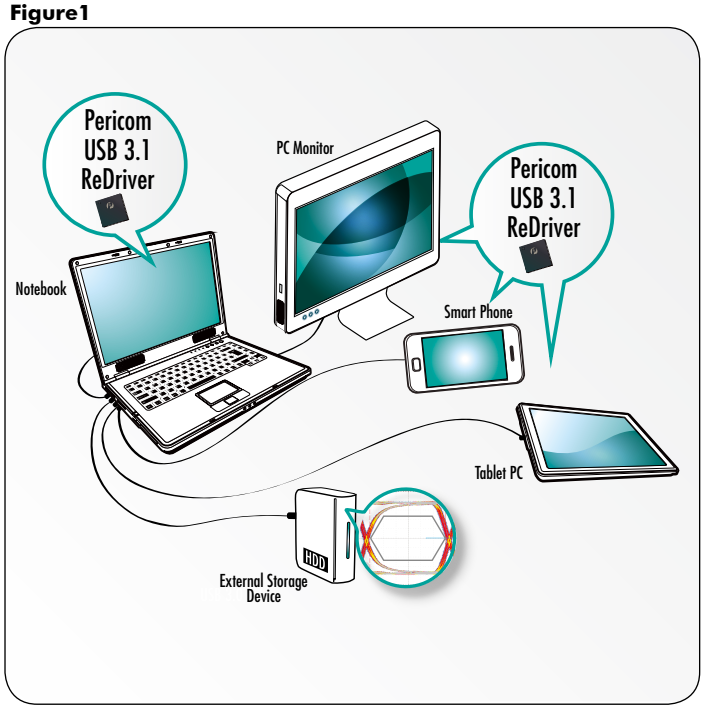
The PI3EQX1004B1 is a low power, high performance 10.0 Gbps 2-Port USB 3.1 linear ReDriver™ designed specifically for the USB 3.1 protocol.

The device provides programmable equalization, and flat gain to optimize performance over a variety of physical mediums by reducing Inter-Symbol Interference. PI3EQX1004B1 supports two 100Ω Differential CML data I/O's between the Protocol ASIC to a switch fabric, over cable, or to extend the signals across other distant data pathways on the user's platform.

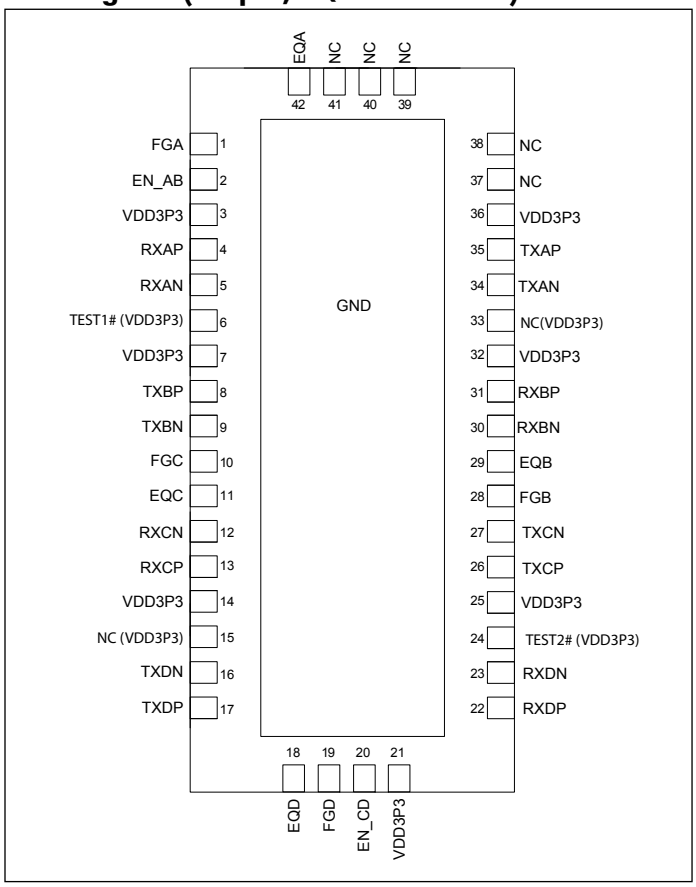
The integrated equalization circuitry provides flexibility with signal integrity of the signal before the ReDriver. Each channel operates fully independently. The channels' input signal level determines whether the output is active.

The PI3EQX1004B1 also includes an automatic receiver detect function. The receiver detection loop will be active again if the corresponding channel's signal detector is idle for longer than 7.3ms. The channel will then move to Unplug Mode if load not detected, or it will return to Low Power Mode (Slumber Mode) due to inactivity.

Figure1



Pin Diagram (42-pin, TQFN 3.5x9mm) ZH42



Pin Description (42-pin, TQFN 3.5x9mm)

Pin #	Pin Name	Type	Description
3, 7, 14, 21, 25, 32, 36	VDD	Power	3.3V power supply, +/-0.3V
1, 28 10, 19	FGA, FGB FGC, FGD	Input	The DC flat gain selection. 4-level input pins. With internal 100kΩ pull-up resistor and 200kΩ pull-down resistor.
42, 29 11, 18	EQA, EQB EQC, EQD	Input	The EQ selection. 4-level input pins. With internal 100kΩ pull-up resistor and 200kΩ pull-down resistor.
4, 5 31, 30 13, 12 22, 23	RXAP, RXAN RXBP, RXBN RXCP, RXCN RXDP, RXDN	Input	CML input terminals. With selectable input termination between 50Ω to VDD, 67kΩ to VbiasRx or 67kΩ to GND.
35, 34 8, 9 26, 27 17, 16	TXAP, TXAN TXBP, TXBN TXCP, TXCN TXDP, TXDN	Output	CML output terminals. With selectable output termination between 50Ω to VDD, 6kΩ to VDD, 6kΩ to VbiasTx or Hi-Z.
2 20	EN_AB EN_CD	Input	Channel Enable. With internal 300kΩ pull-up resistor. "High" – Channel is in normal operation. "Low" – Channel is in power down mode.
Center Pad	GND	GND	Supply Ground
6 24	Test1# Test2#	Input	Connect to VDD is recommended
15, 33	NC	NC	NC pin connect to VDD is recommended
37, 38, 39, 40, 41	NC	NC	NC

Power Management

Notebooks, netbooks, and other power sensitive consumer devices require judicious use of power in order to maximize battery life. In order to minimize the power consumption of our devices, Diodes has added an additional adaptive power management feature. When a signal detector is idle for longer than 1.3ms, the corresponding channel will move to low power mode ONLY. (It means both channels will move to low power mode individually).

In the low power mode, the signal detector will still be monitoring the input channel. If a channel is in low power mode and the input signal is detected, the corresponding channel will wake-up immediately. If a channel is in low power mode and the signal detector is idle longer than 6ms, the receiver detection loop will be active again. If load is not detected, then the Channel will move to Device Unplug Mode and monitor the load continuously. If load is detected, it will return to Low Power Mode and receiver detection will be active again per 6ms.

Operating Modes

Mode	R_{IN}	R_{OUT}
PD	67kΩ to GND	HIZ
Unplug Mode	67kΩ to VbiasRx	6kΩ to VbiasTx
Deep Slumber Mode	50Ω to Vdd	6kΩ to VbiasTx
Slumber Mode	50Ω to Vdd	6kΩ to Vdd
Active Mode	50Ω to Vdd	50Ω to Vdd

Equalization Setting:

EQA/B/C/D are the selection pins for the equalization selection

	Equalizer setting (dB)	
EQA/B/C/D	*@2.5GHz*	*@5GHz*
0 (Tie 0Ω to GND)	6.7	12.4
R (Tie Rext to GND)	3.5	8.0
F (Leave Open)	5.3	10.6
1 (Tie 0Ω to VDD)	8.4	14.6

Flat Gain Setting:

FGA/B/C/D are the selection pins for the DC gain

	Flat Gain Settings
FGA/B/C/D	*dB*
0 (Tie 0Ω to GND)	-1.6
R (Tie Rext to GND)	-0.5
F (Leave Open)	1.0
1 (Tie 0Ω to VDD)	2.7

Channel Enable Setting:

EN_AB/EN_CD are the channel enable pins for channels A&B and C&D respectively

	Channel Enable Setting
EN	*Setting*
0	Disabled
1	Enabled (Default)

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5V to +3.8V
DC SIG Voltage	–0.5V to V_{DD} +0.5V
Output Current	–25mA to +25mA
ESD, Human Body Model	-2kV to +2kV
Power Dissipation Continuous	1.2W
Max Junction Temperature	125°C

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Control pin Specifications (VDD = 3.3 ± 0.3V TA = 0 to 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Units
2-level control pins					
V_{IH}	DC input logic High	VDD*0.65			V
V_{IL}	DC input logic Low			VDD*0.35	V
I_{IH}	Input High current			25	uA
I_{IL}	Input Low current	-25			uA
4-level control pins					
V_{IH}	DC input logic "High"	0.92*VDD	VDD		V
V_{IF}	DC input logic "Float"	0.59*VDD	0.67*VDD	0.75*VDD	V
V_{IR}	DC input logic "With Rext to GND"	0.25*VDD	0.33*VDD	0.41*VDD	V
V_{IL}	DC input logic "Low"		GND	0.08*VDD	V
I_{IH}	Input High current			50	uA
I_{IL}	Input Low current	-50			uA
Rext	External resistor connects to GND (±5%)	64.6	68	71.4	kΩ

AC/DC Electrical Characteristics (VDD = 3.3 ± 0.3V TA = 0 to 70°C)

Power and Latency						
Symbol	**Parameter**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Units**
$V_{dd-3.3}$	Supply voltage		3.0	3.3	3.6	V
I_{active}	Active mode current consumption	EN_AB & EN_CD = 1, 10Gbps, compliance test pattern		260	334	mA
$I_{slumber}$	Slumber mode current consumption	EN_AB & EN_CD = 1, no input signal longer than $T_{slumber}$		32	38	mA
$I_{DeepSlumber}$	Deep slumber mode current consumption	EN_AB & EN_CD = 1 no input signal longer than $T_{DeepSlumber}$		0.8	1.2	
I_{unplug}	Unplug mode current consumption	EN_AB & EN_CD = 1, no output load is detected		0.6	0.9	
I_{pd}	Power down mode current consumption	EN_AB & EN_CD = 0		20	100	µA
t_{pd}	Latency	From input to output			2	ns

AC/DC Electrical Characteristics Cont.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
CML Receiver Input (100Ω differential)						
Receiver Electrical Specification						
$C_{rxparasitic}$	The parasitic capacitor for RX				1.0	pF
$R_{RX-DIFF-DC}$	DC Differential Input Impedance		72		120	Ω
$R_{RX-SINGLE\_DC}$	DC single ended input impedance	DC impedance limits are need to guarantee RxDet. Measured with respect to GND over a voltage of 500mV max	18		30	
$Z_{RX-HIZ-DC-PD}$	DC input CM input impedance for V>0 during reset or power down	(Vcm=0 to 500mV)	25			kΩ
$C_{ac\_coupling}$	AC coupling capacitance		75		265	nF
$V_{RX-CM-AC-P}$	Common mode peak voltage	AC up to 5GHz			150	mVpeak
$V_{RX-CM-DC-Active-Idle-Delta-P}$	Common mode peak voltage $\lvert Avg_{uo}(\lvert V_{TX-D+} + V_{TX-D-}\rvert)/2\text{-}Avg_{u1}(\lvert V_{TX-D+} + V_{TX-D-}\rvert)/2\rvert$	Between U0 and U1. AC up to 5GHz			200	mVpeak
Transmitter Electrical Specification						
$V_{TX-DIFF-PP}$	Ouput differential p-p voltage swing	Differential Swing $\lvert V_{TX-D+}\text{-}V_{TX-D-}\rvert$			1.2	Vppd
$R_{TX-DIFF-DC}$	DC Differential TX Impedance		72		120	Ω
$V_{TX-RCV-DET}$	The amount of voltage change allowed during RxDet				600	mV
$C_{ac\_coupling}$	AC coupling capacitance		75		265	nF
$T_{TX-EYE(10Gbps)}$	Transmitter eye, Include all jittter	At the silicon pad. 10Gbps	0.646			UI
$T_{TX-EYE(5Gbps)}$	Transmitter eye, Include all jittter	At the silicon pad. 5Gbps	0.625			UI
$T_{TX-DJ-DD(10Gbps)}$	Transmitter deterministic jittter	At the silicon pad. 10Gbps			0.17	UI
$T_{TX-DJ-DD(5Gbps)}$	Transmitter deterministic jittter	At the silicon pad. 5Gbps			0.205	UI
$C_{txparasitic}$	The parasitic capacitor for TX				1.1	pF
$R_{TX-DC-CM}$	Common mode DC output Impedance		18		30	Ω
$V_{TX-DC-CM}$	The instantaneous allowed DC common mode voltage at the connector side of the AC coupling capacitors	$\lvert V_{TX-D+}+V_{TX-D-}\rvert/2$	0		2.2	V
V_{TX-C}	Common-Mode Voltage	$\lvert V_{TX-D+}+V_{TX-D-}\rvert/2$	VDD-2V		VDD	V
$V_{TX-CM-AC-PP-Active}$	Active mode TX AC common mode voltage	$V_{TX-D+}+V_{TX-D-}$ for both time and amplitude			100	mVpp
$V_{TX-CM-DC-Active\_Idle-Delta}$	Common mode delta voltage $\lvert Avg_{uo}(\lvert V_{TEX-D+} + V_{TX-D-}\rvert)/2\text{-}Avg_{u1}(\lvert V_{TX-D+} + V_{TX-D-}\rvert)/2\rvert$	Between U0 to U1			200	mV-peak

AC/DC Electrical Characteristics Cont.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$V_{TX\text{-}Idle\text{-}Diff\text{-}AC\text{-}pp}$	Idle mode AC common mode delta voltage|$V_{TX\text{-}D+}$-$V_{TX\text{-}D\text{-}}$|	Between Tx+ and Tx- in idle mode. Use the HPF to remove DC components. =1/ LPF. No AC and DC signals are applied to Rx terminals .			10	mVppd
$V_{TX\text{-}Idle\text{-}Diff\text{-}DC}$	Idle mode DC common mode delta voltage|$V_{TX\text{-}D+}$-$V_{TX\text{-}D\text{-}}$|	Between Tx+ and Tx- in idle mode. Use the LPF to remove DC components. =1/ HPF. No AC and DC signals are applied to Rx terminals.			10	mV
Channel Performance						
G_p	Peaking gain (Compensation at 5GHz, relative to 100MHz, 100$mV_{p\text{-}p}$ sine wave input)	EQx=0 EQx=R EQx=F EQx=1		12.4 8.0 10.6 14.6		dB
		Variation around typical	-3		+3	dB
G_F	Flat gain (100MHz, EQx=F)	FQx=0 FQx=R FQx=F FQx=1		-1.6 -0.5 1.0 2.7		dB
		Variation around typical	-3		+3	dB
V_{SW_100M}	-1dB compression point output swing (at 100MHz)			1000		mVppd
V_{SW_5G}	-1dB compression point output swing (at 5GHz)			850		mVppd
DDNEXT	Differential near-end crosstalk[1]	100MHz to 5GHz, Figure2		-40		dB
$V_{noise\text{-}input}$	Input-referred noise	100MHz to 5GHz, FGx=1, EQx=R, Figure 3		0.6		mV_{RMS}
		100MHz to 5GHz, FGx=1, EQx=1, Figure 3		0.5		
$V_{noise\text{-}output}$	Output-referred noise[2]	100MHz to 5GHz, FGx=1, EQx=R, Figure 3		0.8		mV_{RMS}
		100MHz to 5GHz, FGx=1, EQx=1, Figure 3		1		
Signal and Frequency Detectors						
V_{th_upm}	Unplug mode detector threshold	Threshold of LFPS when the input impedance of the redriver is 67kohm to VbiasRx only. Used in the unplug mode.	200		800	mVppd
V_{th_dsm}	Deep slumber mode detector threshold	LFPS signal threshold in Deep slumber mode	100		600	mVppd

AC/DC Electrical Characteristics Cont.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{th_am}	Active mode detector threshold	Signal threshold in Active and slumber mode	45		175	mVppd
F_{th}	LFPS frequency detector	Detect the frequency of the input CLK pattern	100		400	MHz

Note:

1. Measured using a vector-network analyzer (VNA) with -15dBm power level applied to the adjacent input. The VNA detects the signal at the output of the victim channel. All other inputs and outputs are terminated with 50Ω.
2. Guaranteed by design and characterization.

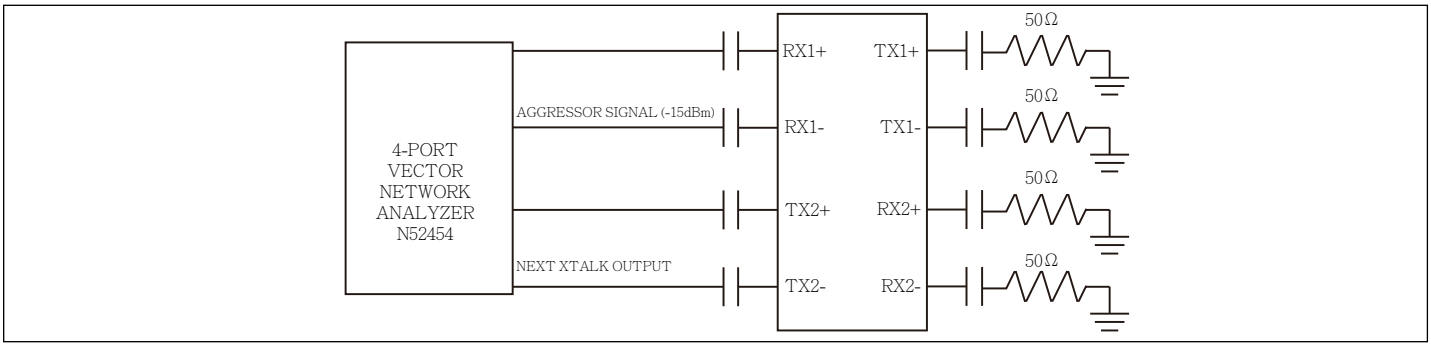


Figure2. Channel-isolation test configuration

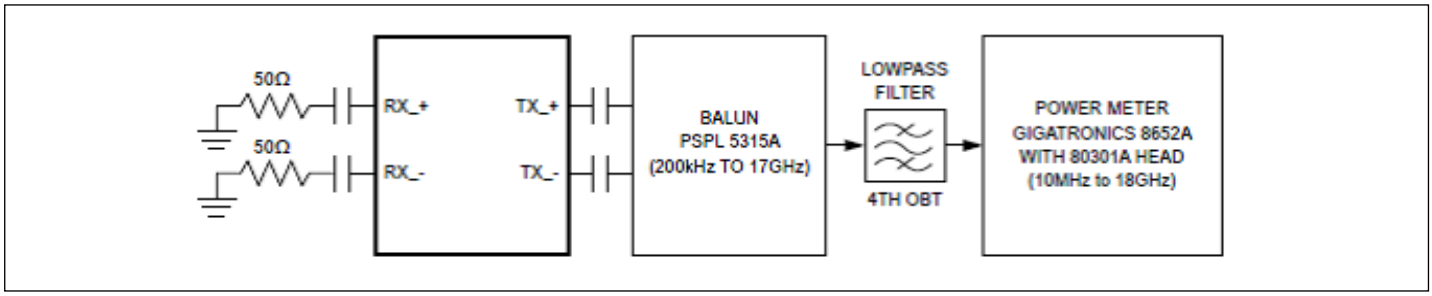


Figure3. Noise test configuration

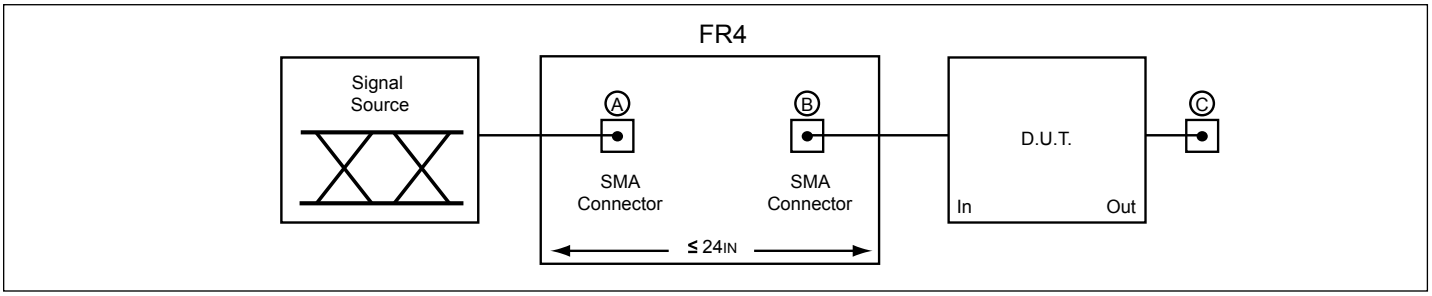
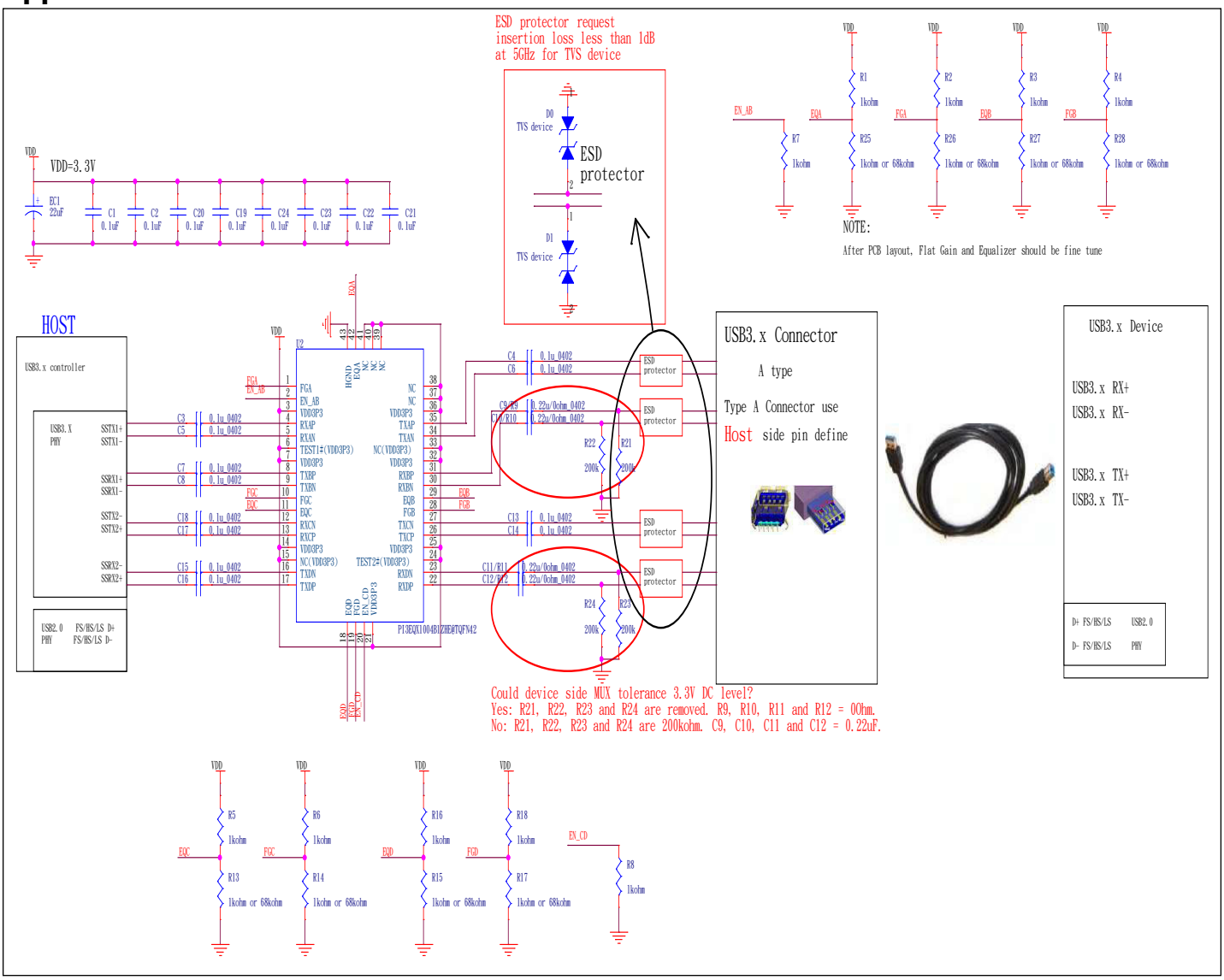


Figure4. Test Condition Referenced in the Electrical Characteristic Table

Application Schematics

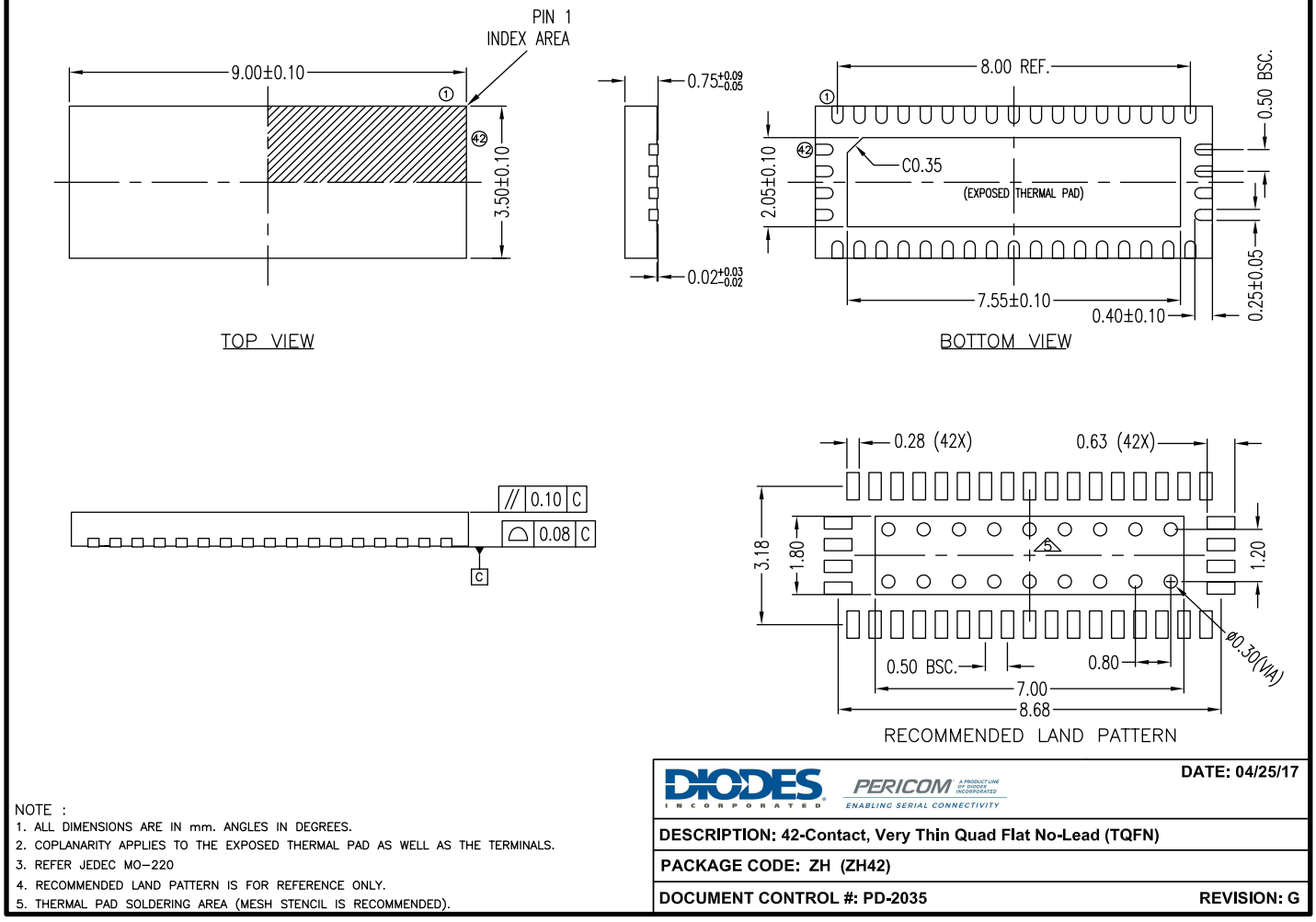


Part Marking

ZH Package

YY: Year
WW: Workweek
1st X: Assembly Code
2nd X: Fab Code

Packaging Mechanical: 42-TQFN (ZH)



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For latest package info.

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Ordering Number	Package Code	Package Description
PI3EQX1004B1ZHEX	ZH	42-contact, Very Thin Quad Flat No-Lead (TQFN)

Notes:

1. EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.
2. See http://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free. Thermal characteristics can be found on the company web site at www.diodes.com/design/support/packaging/
3. E = Pb-free and Green
4. X suffix = Tape/Reel