

## Low Voltage Dual SPDT 0.8Ω Analog Switch

### Features

- CMOS Technology for Bus and Analog Applications
- Low On-Resistance: 0.8Ω at 3.0V
- Wide V<sub>CC</sub> Range: 1.65V to 5.5V
- Rail-to-Rail Signal Range
- Control Input Overvoltage Tolerance: 5.5V(Min)
- Fast Transition Speed: 12ns at 5.0V
- High Bandwidth: 150 MHz
- Extended Industrial Temperature Range: -40 °C to 85 °C
- Packaging (Pb-free & Green): 10-Pin MSOP

### Applications

- Cell Phones
- PDAs
- Portable Instrumentation
- Battery powered Communications
- Computer Peripherals

### Pin Description

Pin No	Name	Description
2, 4	<sub>1</sub> B <sub>x</sub>	Data Port (Normally open)
3	GND	Ground
7, 9	<sub>0</sub> B <sub>x</sub>	Data Port (Normally closed)
6, 10	A <sub>x</sub>	Common Output / Data Port
8	V <sub>CC</sub>	Positive Power Supply
1, 5	S <sub>x</sub>	Logic Control

### Logic Function Table

Logic Input (S <sub>x</sub> )	Function
0	<sub>0</sub> B <sub>x</sub> Connected to A <sub>x</sub>
1	<sub>1</sub> B <sub>x</sub> Connected to A <sub>x</sub>

Note: X= 0 or 1

### Description

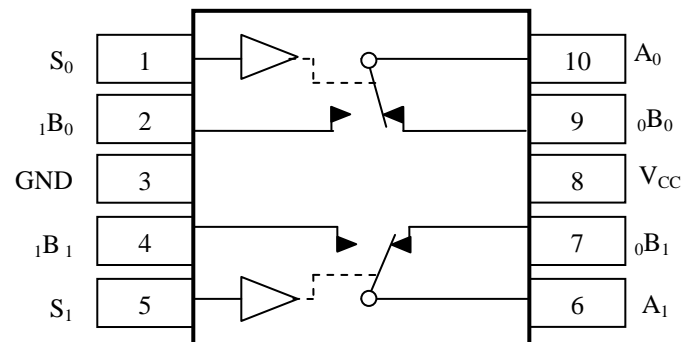
The PI5A23159 is a dual high-bandwidth, fast single-pole double-throw (SPDT) CMOS switch. It can be used as an analog switch or as a low-delay bus switch. The device features ultra low RON of 0.8Ω typical at 3.0V VCC and will operate over the wide VCC range of 1.65V to 5.5V.

The PI5A23159 features very low quiescent current even when the control voltage is lower than the VCC supply. This feature services the mobile handset applications very well by allowing direct interface with baseband processor general purpose I/Os.

Break-before-make switching prevents both switches being enabled simultaneously. This eliminates signal disruption during switching.

The control input, S, is independent of supply voltage.

### Pin Assignment



## Maximum Ratings

Storage Temperature.....	-65 °C to +150 °C
Ambient Temperature with Power Applied.....	-40 °C to +85 °C
Supply Voltage $V_{CC}$ .....	-0.5V to +7.0V
DC Switch Voltage $V_S$ .....	-0.5V to +7.0V
DC Input Voltage $V_{IN}$ .....	-0.5V to +7.0V
DC Output Current $V_{OUT}$ .....	128mA
DC $V_{CC}$ or Ground Current $I_{CC} / I_{GND}$ .....	±100mA
Junction Temperature under Bias ( $T_J$ ) .....	150 °C
Junction Lead Temperature ( $T_L$ ) (Soldering, 10 seconds) .....	260 °C
ESD (HBM) .....	.5KV
Power Dissipation (PD) @ +85 °C .....	MSOP10 350mW

**Note:**

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{CC}$	Operating Voltage	-	1.65	-	5.5	V
$V_{IN}$	Control Input Voltage	-	0	-	$V_{CC}$	V
$V_S$	Switch Input Voltage	-	0	-	5.5	V
$V_{OUT}$	Output Voltage	-	0	-	$V_{CC}$	V
$T_A$	Operating Temperature	-	-40	25	85	°C
$t_r, t_f$	Input Rise and Fall Time	Control Input $V_{CC} = 2.7V$ to $3.6V$	0	-	10	ns/V
		Control Input $V_{CC} = 4.5V$ to $5.5V$	0	-	5	ns/V

**Note:** Control input must be held HIGH or LOW; it must not float.

## DC Electrical Characteristics

(T<sub>A</sub> = -40 °C to 85 °C, unless otherwise noted.)

Symbol	Parameter	Test Conditions	Supply Voltage	Min.	Typ.	Max.	Units		
V <sub>IAR</sub>	Analog Input Signal Range	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V		
R <sub>ON</sub>	ON Resistance <sup>(1)</sup>	I <sub>AX</sub> =100mA, V <sub>nBx</sub> =0V	V <sub>CC</sub> =4.5V	-	0.7	-	Ω		
		I <sub>AX</sub> =100mA, V <sub>nBx</sub> =2.4V		-	0.6	-			
		I <sub>AX</sub> =100mA, V <sub>nBx</sub> =4.5V		-	0.8	-			
		R <sub>ON</sub>	ON Resistance <sup>(1)</sup>	I <sub>AX</sub> =100mA, V <sub>nBx</sub> =0V	V <sub>CC</sub> =3.0V	-	0.8	-	Ω
				I <sub>AX</sub> =100mA, V <sub>nBx</sub> =3.0V		-	0.9	-	
		R <sub>ON</sub>	ON Resistance <sup>(1)</sup>	I <sub>AX</sub> =100mA, V <sub>nBx</sub> =0V	V <sub>CC</sub> =2.3V	-	1.0	-	Ω
				I <sub>AX</sub> =100mA, V <sub>nBx</sub> =2.3V		-	1.2	-	
		R <sub>ON</sub>	ON Resistance <sup>(1)</sup>	I <sub>AX</sub> =100mA, V <sub>nBx</sub> =0V	V <sub>CC</sub> =1.65V	-	1.3	-	Ω
I <sub>AX</sub> =100mA, V <sub>nBx</sub> =1.65V	-			2.0		-			
ΔR <sub>ON</sub>	ON Resistance Match Between Channels <sup>(1,2,3)</sup>	I <sub>AX</sub> =100mA, V <sub>nBx</sub> =3.15V	V <sub>CC</sub> =4.5V	-	0.01	0.12	Ω		
		I <sub>AX</sub> =100mA, V <sub>nBx</sub> =2.1V	V <sub>CC</sub> =3.0V	-	0.02	-			
		I <sub>AX</sub> =100mA, V <sub>nBx</sub> =1.6V	V <sub>CC</sub> =2.3V	-	0.03	-			
		I <sub>AX</sub> =100mA, V <sub>nBx</sub> =1.15V	V <sub>CC</sub> =1.65V	-	0.03	-			
R <sub>ONF</sub>	ON Resistance Flatness <sup>(1,2,4)</sup>	I <sub>AX</sub> =100mA, V <sub>nBx</sub> =0V,2.4V,4.5V	V <sub>CC</sub> =4.5V	-	0.2	0.4	Ω		
		I <sub>AX</sub> =100mA, V <sub>nBx</sub> =0V,1.5V,3.3V	V <sub>CC</sub> =3.3V	-	0.2	0.4			
		I <sub>AX</sub> =100mA, V <sub>nBx</sub> =0V,1.1V,2.5V	V <sub>CC</sub> =2.5V	-	0.4	1.4			
		I <sub>AX</sub> =100mA, V <sub>nBx</sub> =0V,0.7V,1.8V	V <sub>CC</sub> =1.8V	-	1.0	-			
V <sub>IH</sub>	Input High Voltage	Logic High Level	V <sub>CC</sub> =1.65V	0.9	-	-	V		
			V <sub>CC</sub> =2.3V	1.0	-	-			
			V <sub>CC</sub> =3.0V	1.1	-	-			
			V <sub>CC</sub> =4.2V	1.2	-	-			
			V <sub>CC</sub> =5.5V	1.3	-	-			
V <sub>IL</sub>	Input Low Voltage	Logic Low Level	V <sub>CC</sub> =1.65V	-	-	0.6	V		
			V <sub>CC</sub> =2.3V	-	-	0.6			
			V <sub>CC</sub> =3.0V	-	-	0.6			
			V <sub>CC</sub> =4.2V	-	-	0.8			
			V <sub>CC</sub> =5.5V	-	-	0.8			
I <sub>OFF(Bn)</sub>	Source Off Leakage Current	V <sub>AX</sub> =1V/4.5V, V <sub>nBx</sub> =1V/4.5V	V <sub>CC</sub> =3.0V	-20	-	+20	nA		
I <sub>ON(A, Bn)</sub>	Channel On Leakage Current	-	V <sub>CC</sub> =1.65V to 5.5V	-40	-	+40	nA		
I <sub>CC</sub>	Quiescent Supply Current	All Channels ON or OFF, V <sub>nBx</sub> =V <sub>CC</sub> and GND, I <sub>OUT</sub> =0A	V <sub>CC</sub> =3.6V	-	0.002	0.1	μA		
			V <sub>CC</sub> =5.5V	-	0.002	0.1			
I <sub>CCT</sub>	Increase in I <sub>CC</sub> per Input	Channel Input at 2.7V	V <sub>CC</sub> =4.3V	-	0.2	10.0	μA		

### Notes:

1. Measured by voltage drop between A and B pins at the indicated current through the device. ON resistance is determined by the lower of the voltages on two ports (Ax or nBx) x= 0 or 1, n= 0 or 1.
2. Parameter is characterized but not tested in production.
3. ΔR<sub>ON</sub> = R<sub>ON</sub> max – R<sub>ON</sub> min. measured at identical V<sub>CC</sub>, temperature and voltage levels.
4. Flatness is defined as difference between maximum and minimum value of ON resistance over the specified range of conditions.

## Capacitance<sup>(1)</sup>

Symbol	Parameter	Test Conditions	Supply Voltage	Temp ( °C )	Min.	Typ.	Max.	Units
C <sub>IN</sub>	Control Input	f = 1 MHz	V <sub>CC</sub> = 5.0V	T <sub>A</sub> = 25 °C	-	3.5	-	pF
C <sub>IO-B</sub>	For Bn Port, Switch OFF				-	15.0	-	
C <sub>IOA-ON</sub>	For An Port, Switch ON				-	34.0	-	

### Notes:

1. Capacitance is characterized but not tested in production

**Switch and AC Characteristics** <sup>(1)</sup>

Parameter	Description	Test Conditions	Supply Voltage	Min	Typ	Max	Units
$t_{\text{BBM}}$	Break Before Make Time	See Figure 2	$V_{\text{CC}} = 2.7\text{V to } 3.6\text{V}$	-	10	-	ns
			$V_{\text{CC}} = 4.5\text{V to } 5.5\text{V}$	-	6	-	
$t_{\text{ON}}$	Turn on Time	See Figure 1	$V_{\text{CC}} = 2.7\text{V to } 3.6\text{V}$	-	16	-	
			$V_{\text{CC}} = 4.5\text{V to } 5.5\text{V}$	-	12	-	
$t_{\text{OFF}}$	Turn off Time	See Figure 1	$V_{\text{CC}} = 2.7\text{V to } 3.6\text{V}$	-	8	-	
			$V_{\text{CC}} = 4.5\text{V to } 5.5\text{V}$	-	5	-	
Q	Charge Injection	$C_{\text{L}} = 1\text{nF}$ , $V_{\text{GEN}} = 0\text{V}$ , $R_{\text{GEN}} = 0\Omega$ . See Figure 3	$V_{\text{CC}} = 5.0\text{V}$	-	35	-	pC
			$V_{\text{CC}} = 3.3\text{V}$	-	25	-	
OIRR	Off Isolation <sup>(2)</sup>	$R_{\text{L}} = 50\Omega$ , $V_{\text{GEN}} = 0\text{V}$ , $R_{\text{GEN}} = 0\Omega$ , $f = 1\text{MHz}$ . See Figure 4	$V_{\text{CC}} = 1.65\text{V to } 5.5\text{V}$	-	-70	-	dB
$X_{\text{TALK}}$	Crosstalk Isolation	$f = 1\text{MHz}$ , See Figure 5	$V_{\text{CC}} = 1.65\text{V to } 5.5\text{V}$	-	-70	-	
$f_{3\text{dB}}$	-3dB Bandwidth	See Figure 8	$V_{\text{CC}} = 1.65\text{V to } 5.5\text{V}$	-	150	-	MHz
$T_{\text{HD}}$	Total Harmonic Distortion	$R_{\text{L}} = 600\Omega$ , $V_{\text{IN}} = 0.5\text{Vpp}$ , $f = 20\text{Hz to } 20\text{kHz}$ See Figure 9	$V_{\text{CC}} = 2.7\text{V to } 4.2\text{V}$	-	0.015	-	%

**Notes:**

1. Guaranteed by design.
2. Off Isolation =  $20 \text{Log}_{10} [V_{\text{nBx}} / V_{\text{Ax}}]$  and is measured in dB.

### Test Circuits and Timing Diagrams

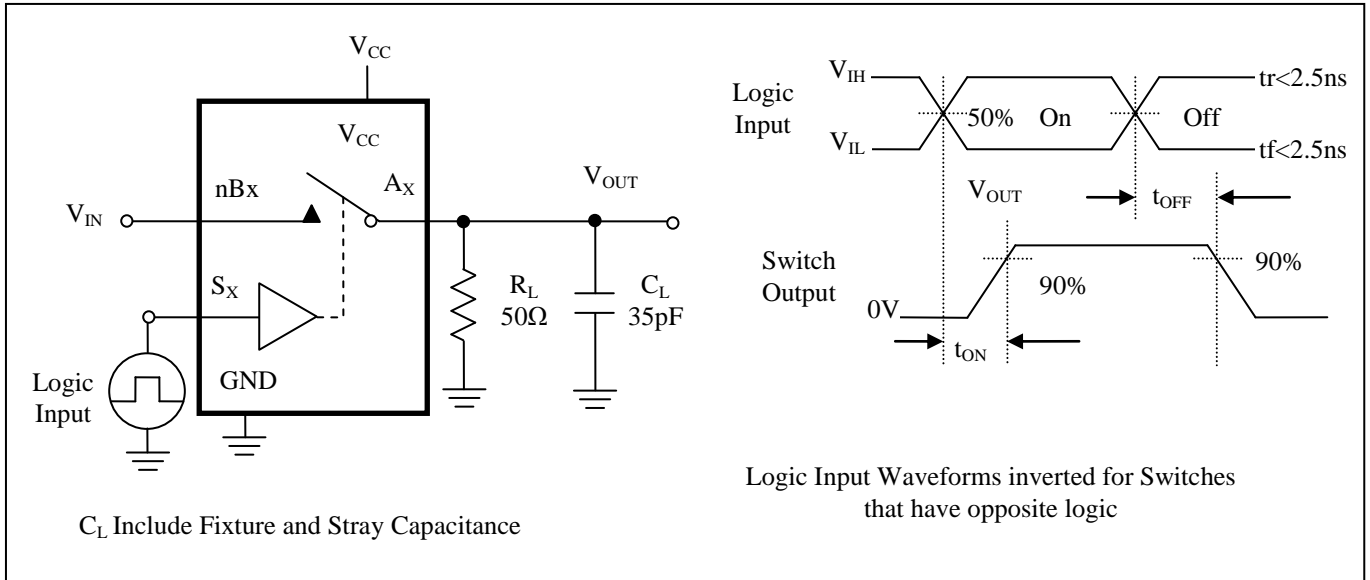


Figure 1. Turn ON/OFF Timing

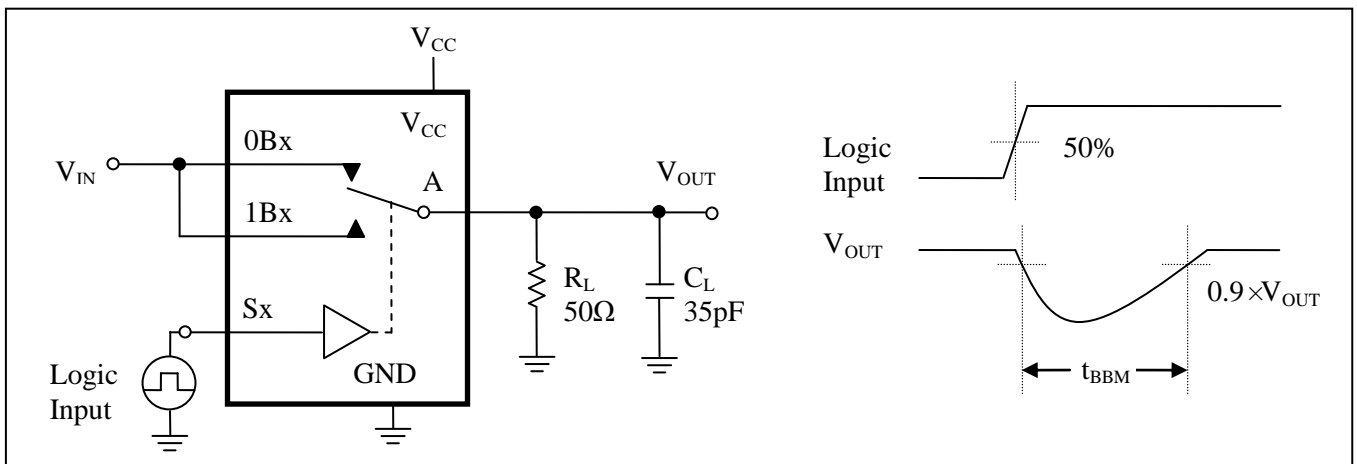


Figure 2. Break Before Make Interval Timing

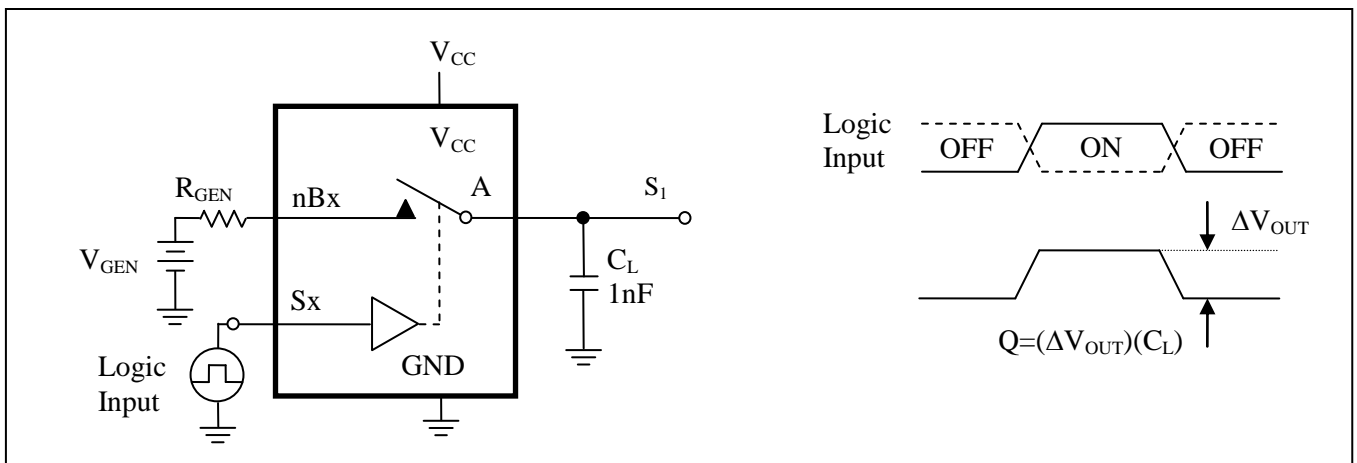
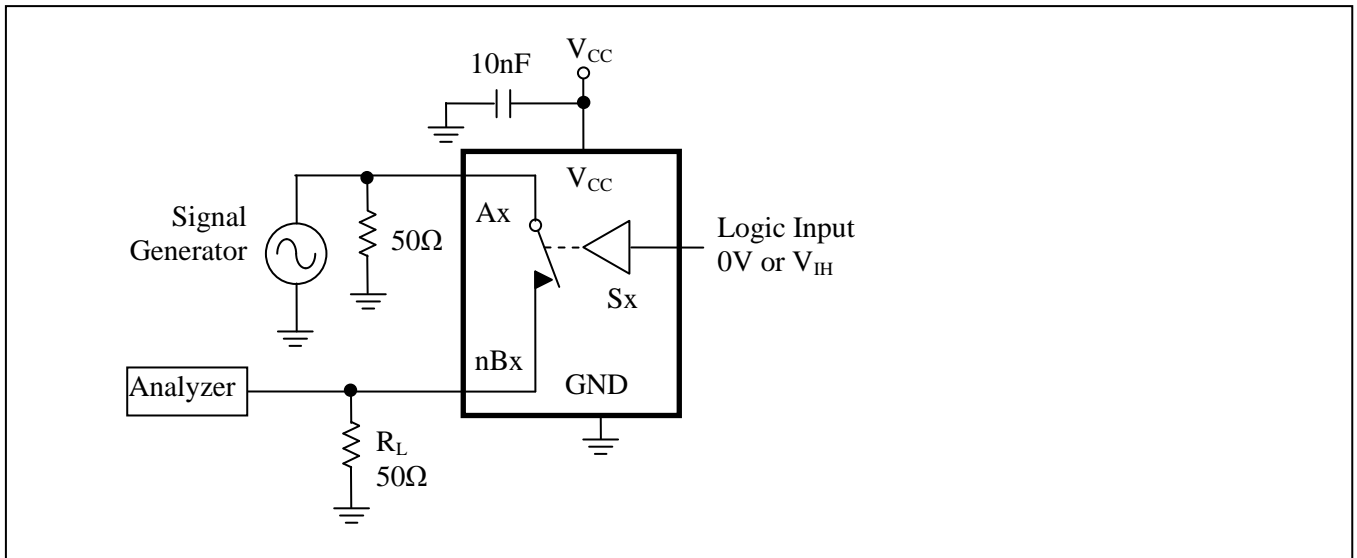
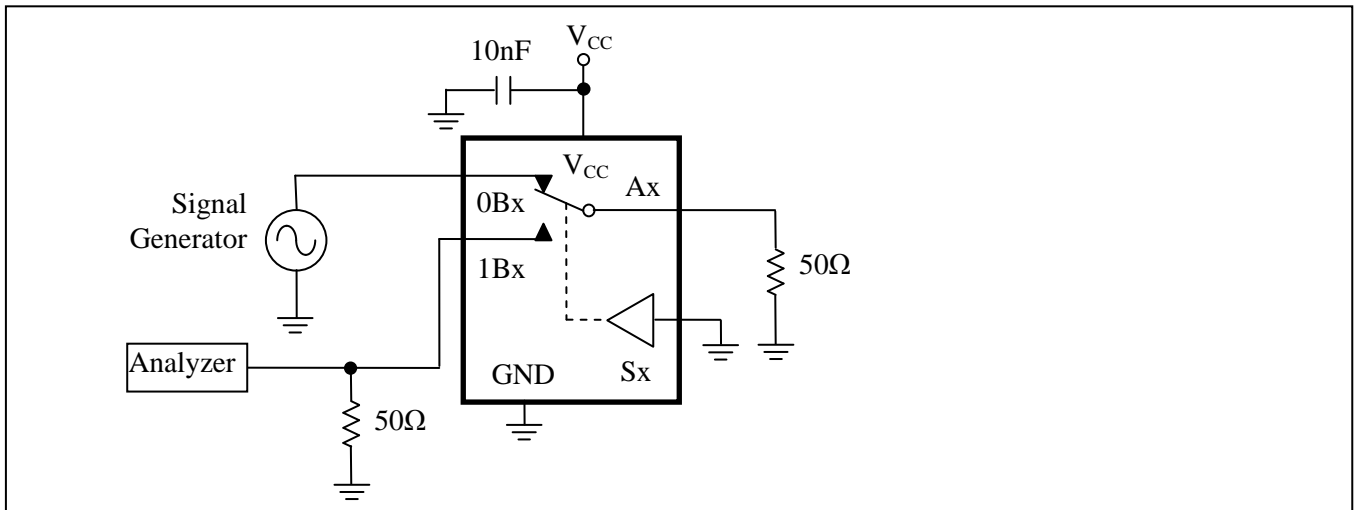


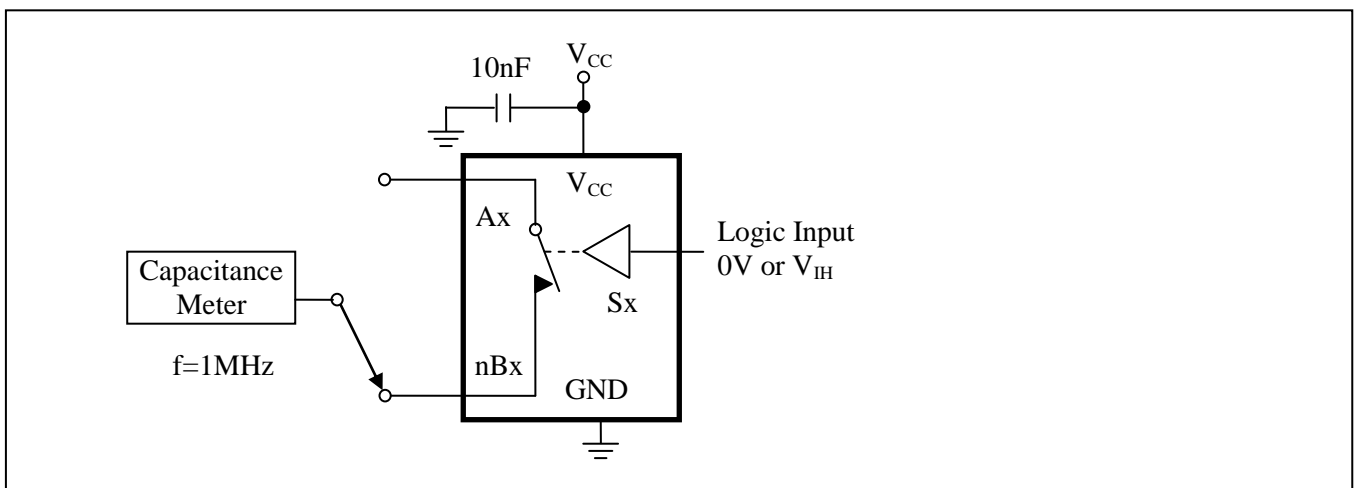
Figure 3. Charge Injection Test



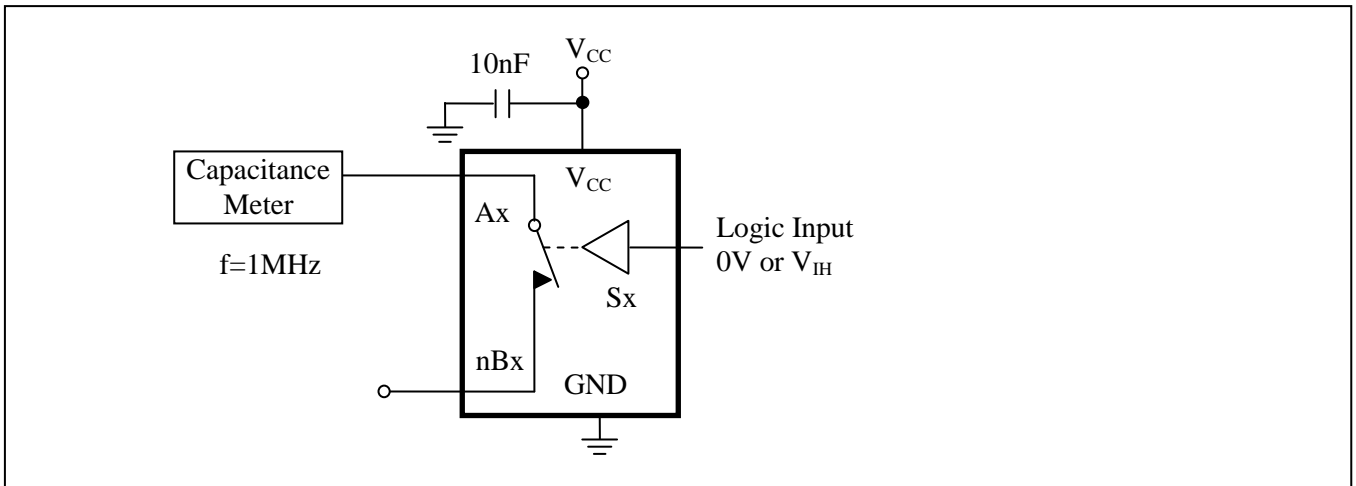
**Figure 4. Off Isolation**



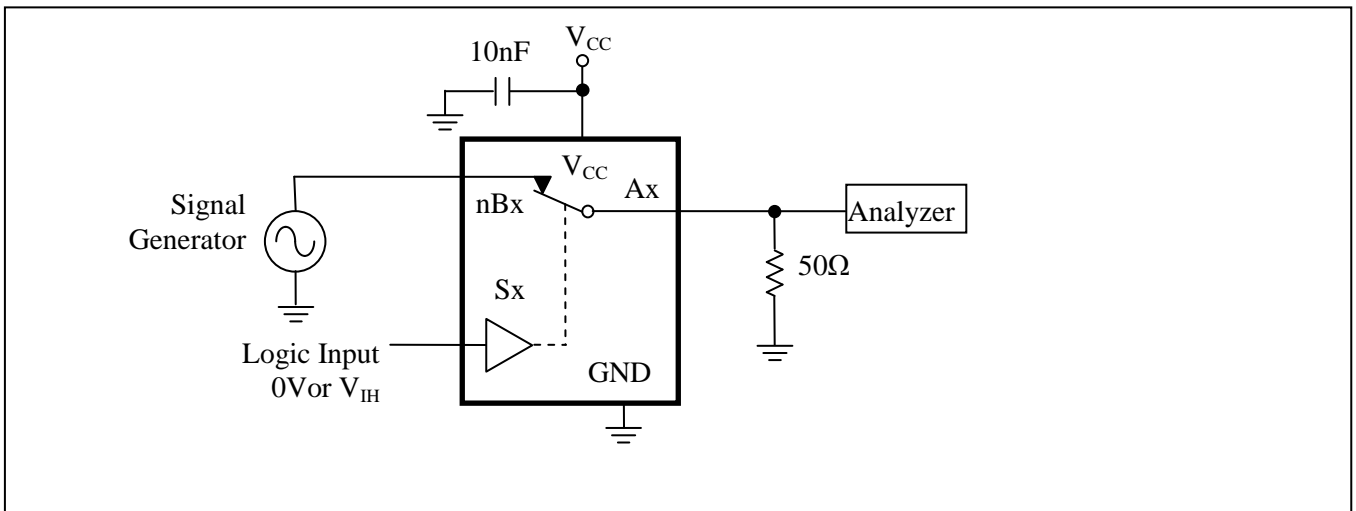
**Figure 5. Crosstalk**



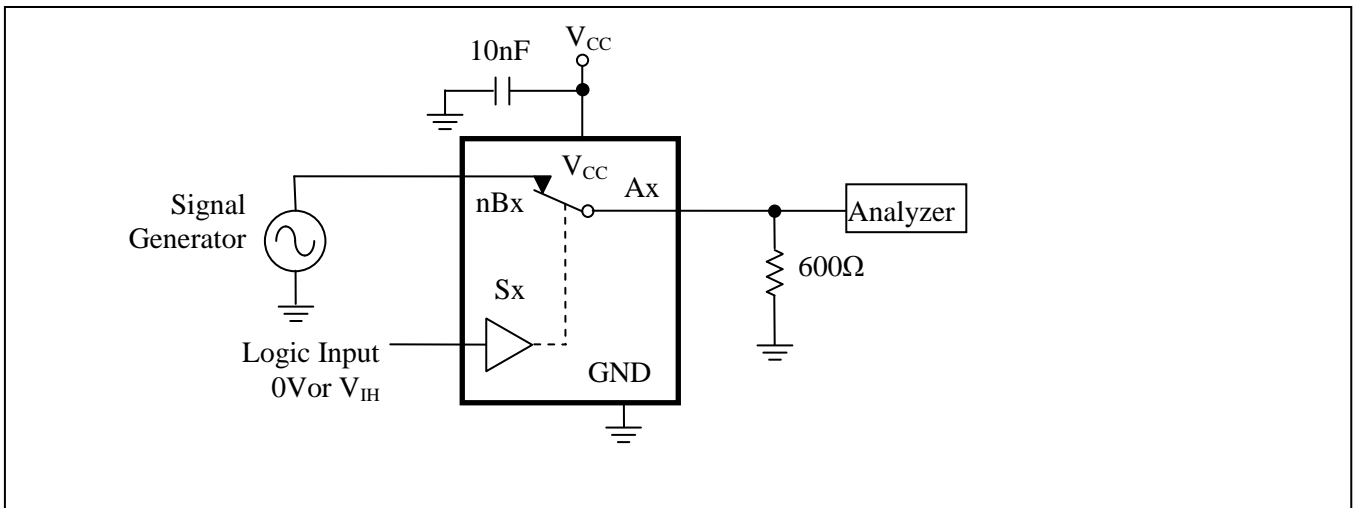
**Figure 6. Channel Off Capacitance**



**Figure 7. Channel On Capacitance**



**Figure 8. Bandwidth**



**Figure 9. Harmonic Distortion**