PI6C2409-1H

Zero-Delay Clock Buffer

Features

- Maximum rated frequency: 133 MHz
- Low cycle-to-cycle jitter
- Input to output delay, less than 200ps
- Internal feedback allows outputs to be synchronized to the clock input
- Spread spectrum compatible
- Operates at 3.3V V_{DD}
- Space-saving Package: (Pb-free & Green available)
  - 16-Pin TSSOP (L)
  - 16-Pin SOIC (W)

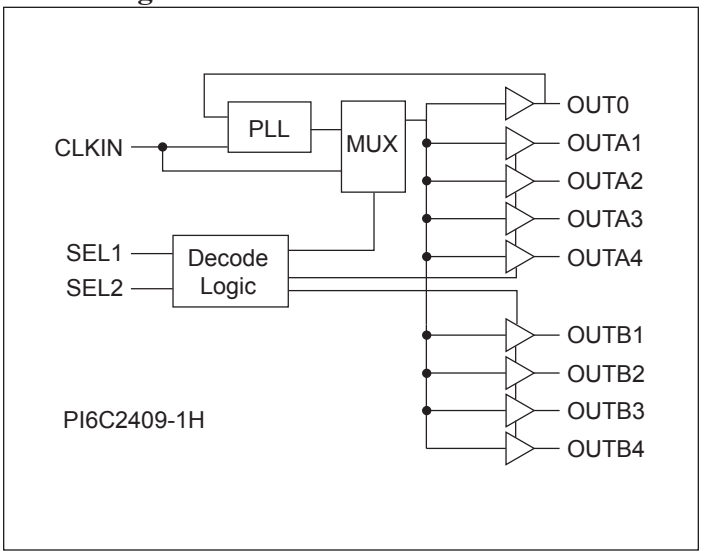
Description

The PI6C2409-1H is a PLL based, zero-delay buffer, with the ability to distribute nine outputs of up to 133 MHz at 3.3V. All the outputs are distributed from a single clock input CLKIN and output OUT0 performs zero delay by connecting a feedback to PLL.

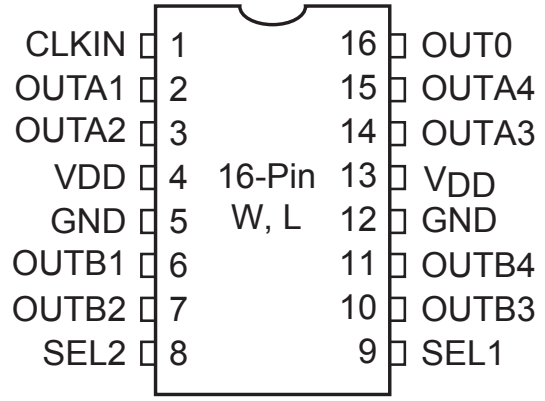
PI6C2409-1H has two banks of four outputs that can be controlled by the selection inputs, SEL1 & SEL2. It also has a power sparing feature: when input SEL1 is 0 and SEL2 is 1, PLL is turned off and all outputs are referenced from CLKIN. PI6C2409-1H is available in high drive and industrial environment versions.

An internal feedback on OUT0 is used to synchronize the outputs to the input; the relationship between loading of this signal and the outputs determines the input-output delay. PI6C2409-1H are characterized for both commercial and industrial operation

Block Diagram



Pin Configuration



Input Select Decoding

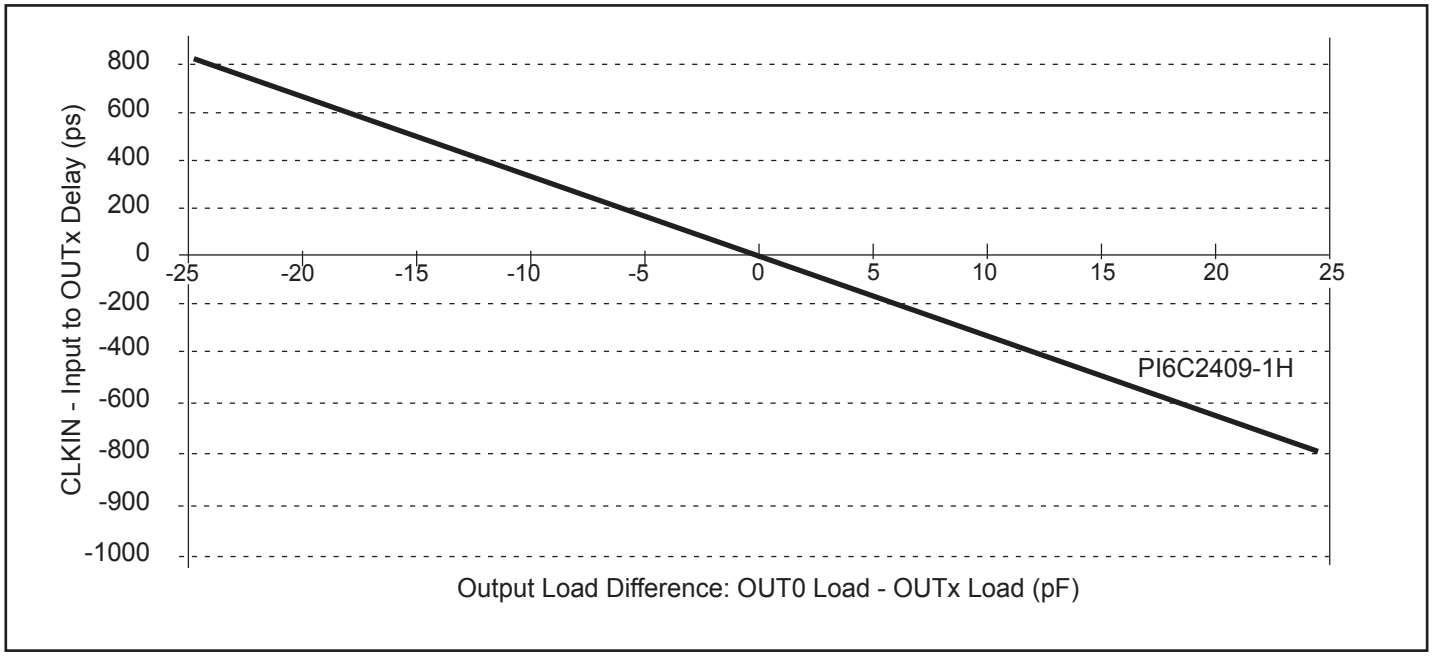
SEL2	SEL1	OUTA [1-4]	OUTB [1-4]	Output Source (OUT0)	PLL
0	0	3-State	3-State	PLL	ON
0	1	PLL	3-State	PLL	ON
1	0	CLKIN	CLKIN	CLKIN	OFF
1	1	PLL	PLL	PLL	ON

Pin Description

Pin	Signal	Description
1	CLKIN	Input clock reference frequency (weak pull-down)
2, 3, 14, 15	OUTA[1-4]	Clock outputs, Bank A
4, 13	VDD	3.3V supply
5, 12	GND	Ground
6, 7, 10 ,11	OUTB[1-4]	Clock outputs, Bank B
8	SEL2	Select input, bit 2 (weak pull-up)
9	SEL1	Select input, bit 1 (weak pull-up)
16	OUT0	Clock Output , internal PLL feedback

Zero-Delay and Skew Control

CLKIN Input to OUTx Delay vs. Difference in Loading between OUT0 pin and OUTx pins



The relationship between loading of the OUT0 signal and other outputs determines the input-output delay. Zero delay is achieved when all outputs, including feedback, are loaded equally.

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature..... –65°C to +150°C
Supply Voltage to Ground Potential.....–0.5V to +4.6V
DC Input Voltage ..... –0.5V to V_{DD} +0.5V
ESD Protection (Input)..... 2000 V min (HBM)

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Conditions (V_{CC} = 3.3V ±0.3V)

Parameter	Description	Min.	Max.	Units
V_{DD}	Supply Voltage	3.0	3.6	V
T_A	Commercial Operating Temperature	0	70	ºC
	Industrial Operating Temperature	-40	85	
C_L	Load Capacitance, below 100 MHz		30	pF
	Load Capacitance, from 100 MHz to 133 MHz	-	15	
C_{IN}	Input Capacitance	-	7	

DC Electrical Characteristics for Industrial Temperature Devices

Parameters	Description	Test Conditions	Min.	Max.	Units
V_{IL}	Input LOW Voltage			0.8	V
V_{IH}	Input HIGH Voltage		2.0		
I_{IL}	Input LOW Current	V_{IN} = 0V		50.0	µA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}		125	
V_{OL}	Output LOW Voltage	I_{OL} = 12mA		0.4	V
V_{OH}	Output HIGH Voltage	I_{OH} = –12mA	2.4		
I_{DD}	Bypass, PLL OFF	SEL1 = 0, SEL2 = 1		1.0	mA
	Supply Current	Unloaded outputs 100 MHz, Select inputs at V_{DD} or GND		62	
		Unloaded outputs 66 MHz, CLKIN		44	

AC Electrical Characteristics for Industrial Temperature Devices

Parameters	Name	Test Conditions	Min.	Typ.	Max.	Units
F_O	Output Frequency	30pF load	10.0		100	MHz
		10pF load			133	
t_{DC}	Duty Cycle(1)	Measured at $V_{DD}/2$, F_{OUT} = 66.67 MHz	40.0	50	60.0	%
	Duty Cycle(1)	Measured at $V_{DD}/2V$, F_{OUT} <50MHz	45.0		55.0	
t_R	Rise Time(1)	Measured between 0.8V and 2.0V			1.5	ns
t_F	Fall Time(1)	Measured between 0.8V and 2.0V			1.5	
$t_{SK(O)}$	Output to Output Skew(1)	All outputs equally loaded			250	ps
t_0	Delay, CLKIN Rising Edge to OUT0 Rising Edge(1)	Measured at $V_{DD}/2$		0	±350	
$t_{SK(D)}$	Device-to-Device Skew(1)	Measured at $V_{DD}/2$ on OUT0 pins of devices		0	700	
t_{SLEW}	Output Slew Rate(1)	Measured between 0.8V & 2.0V on –1H device using Test Crt #2	1			V/ns
t_{JIT}	Cycle-to-Cycle Jitter(1)	Measured at 66.67 MHz, loaded 30pF load			250	ps
t_{LOCK}	PLL Lock Time(1)	Stable power supply, valid clocks presented on CLKIN pin			1.0	ms

Note:

1. See Switching Waveforms on page 6.

DC Electrical Characteristics for Commercial Temperature Devices

Parameters	Description	Test Conditions	Min.	Max.	Units
V_{IL}	Input LOW Voltage	-	-	0.8	V
V_{IH}	Input HIGH Voltage	-	2.0	-	
I_{IL}	Input LOW Current	V_{IN} = 0V	-	50	µA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}	-	125	
V_{OL}	Output LOW Voltage	I_{OL} = 12mA	-	0.4	V
V_{OH}	Output HIGH Voltage	I_{OH} = –12mA	2.4	-	
I_{DD}	Bypass, PLL off	SEL1 = 0 SEL2 = 1	-	1.0	mA
	Supply Current	Unloaded outputs, 66.67 MHz, Select inputs at V_{DD} or GND	-	39	
		Unloaded outputs 100 MHz Select Inputs @ V_{DD} or GND	-	54	

AC Electrical Characteristics for Commercial Temperature Devices

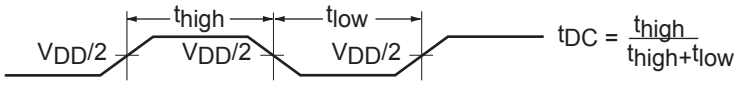
Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
F_O	Output Frequency	30pF load	10.0		100	MHz
		10pF load			133	
t_{DC}	Duty Cycle(1)	Measured at $V_{DD}/2$, F_O = 66.67 MHz	40.0	50	60.0	%
	Duty Cycle(1)	Measured at $V_{DD}/2V$, F_O <50 MHz	45.0		55.0	
t_R	Rise Time(1)	Measured between 0.8V and 2.0V			1.5	ns
t_F	Fall Time(1)				1.5	
$t_{SK(O)}$	Output to Output Skew(1)	All outputs equally loaded			250	ps
t_0	Delay, CLKIN Rising Edge to OUT0 Rising Edge(1)	Measured at $V_{DD}/2$		0	±350	
$t_{SK(D)}$	Device-to-Device Skew(1)	Measured at $V_{DD}/2$ on OUT0 pins of devices		0	700	
t_{SLEW}	Output Slew Rate(1)	Measured between 0.8V & 2.0V on –1H device using Test Crt #2	1			V/ns
t_{JIT}	Cycle-to-Cycle Jitter(1)	Measured at 66.67 MHz, loaded 30pF load			200	ps
t_{LOCK}	PLL Lock Time(1)	Stable power supply, valid clocks presented on CLKIN pin			1.0	ms

Note:

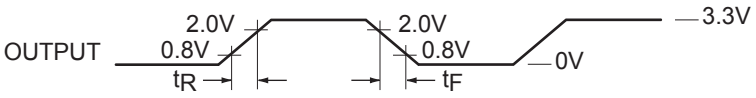
1. See Switching Waveforms on page 6.

Switching Waveforms

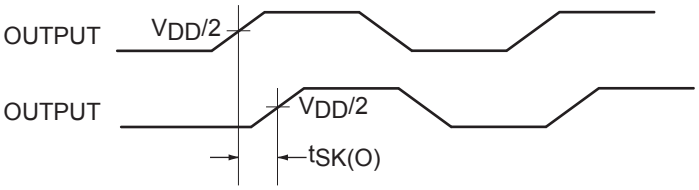
Duty Cycle Timing



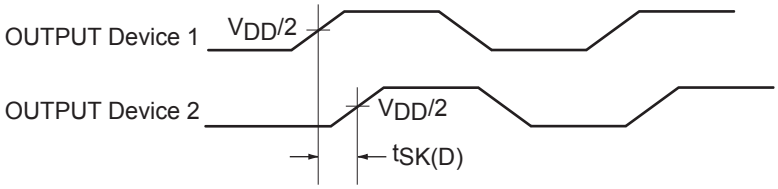
All Outputs Rise/Fall Time



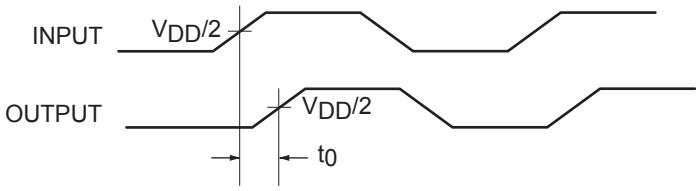
Output-Output Skew

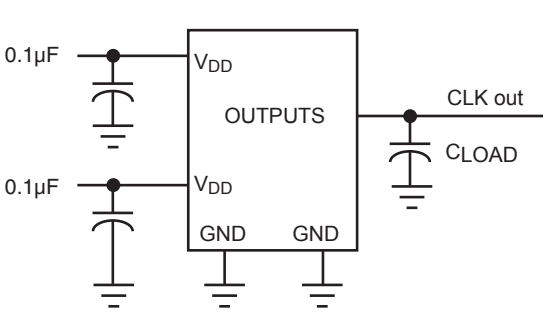


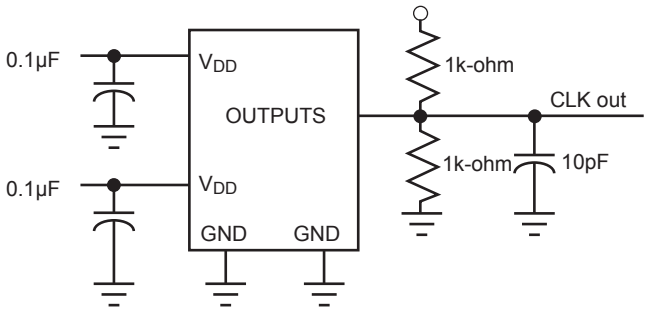
Device-Device Skew



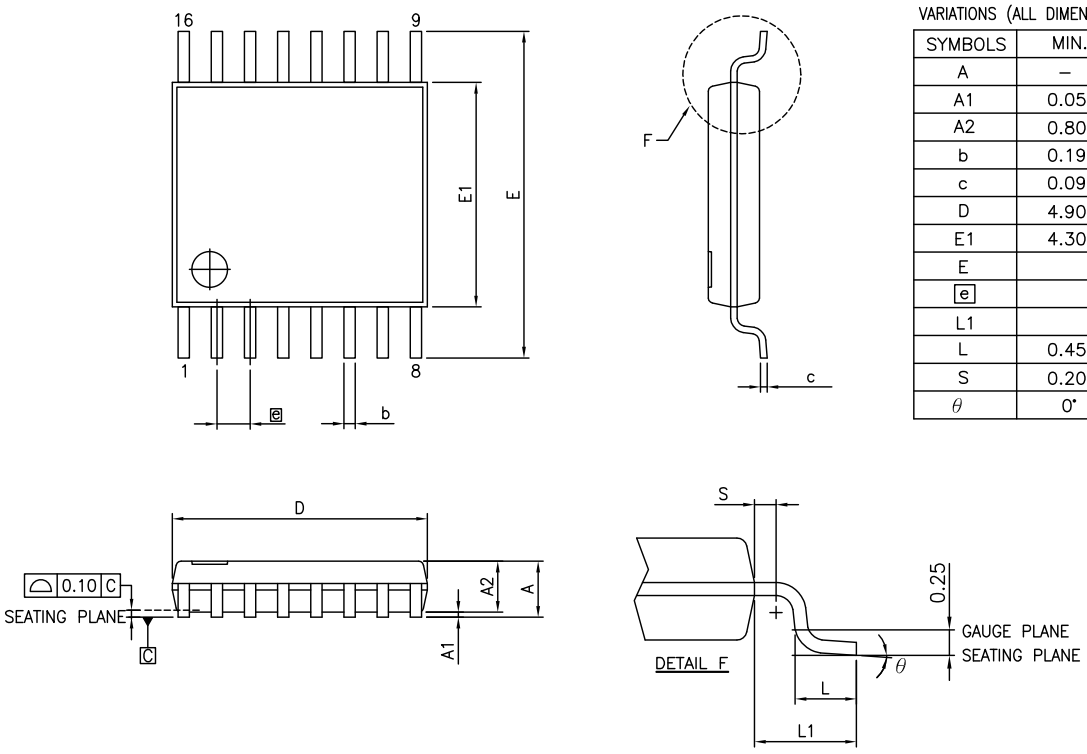
Input-Output Propagation Delay







Packaging Mechanical: 16-Pin TSSOP (L)



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	–	1.05
b	0.19	–	0.30
c	0.09	–	0.20
D	4.90	5.00	5.10
E1	4.30	4.40	4.50
E		6.40 BSC	
e		0.65 BSC	
L1		1.00 REF	
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°

Notes:
1. Refer JEDEC MO-153F/AB
2. Controlling dimensions in millimeters
3. Package outline exclusive of mold flash and metal burr

PERICOM Enabling Serial Connectivity

DATE: 05/03/12

DESCRIPTION: 16-Pin, 173mil Wide TSSOP

PACKAGE CODE: L

DOCUMENT CONTROL #: PD-1310 **REVISION: F**

12-0372