Lead-free Green

PI7C9X2G606PR

PCI EXPRESS GEN 2 PACKET SWITCH

6Port-6Lane PCI Express Gen 2 Switch

Green Package Family

DATASHEET

REVISION 7

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A Product Line of Diodes Incorporated

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REVISION HISTORY

Date	Revision Number	Description
12/31/13	0.1	Preliminary Datasheet
07/21/14	0.2	Updated Section 3 Pin Description Updated Section 4 Pin Assignments Updated Section 6.1.3 EEPROM Space Address Map Updated Section 6.1.4 Mapping EEPROM Contents to Configuration Registers Updated Section 7.2 Transparent Mode Configuration Registers Updated Section 1 Features
07/29/14	0.3	Update Section 5.1 Physical Layer Circuit
09/26/14	0.4	Added Section 6.2.1 SMBus Operation Added Section 6.2.2 SMBus Commands Supported Added Section 6.3 I^2C Slave Interface Added Section 8 Clock Sheme Updated Section 1 Feature Updated Section 3.4 Miscellaneous Signals Updated Section 4.1 Pin List of 196-Pin LBGA Updated Section 6 EEPROM Interface & System Management BUS/ I^2C BUS Updated Section 6.1.4 Mapping EEPROM Contents to Configuration Registers Updated Section 6.2 SMBus Interface Updated Section 7 Register Description
10/15/14	1.0	Remove “Preliminary”
10/21/14	1.1	Updated Section 6.2 SMBUS Interface Updated Section 6.3 I2C Slave Interface Updated Section 7.2 Transparent Mode Configuration Registers
11/13/14	1.2	Updated Section 3.4 Miscellaneous Signals Updated Section 6.1 EEPROM Interface Updated Section 6.2 SMBUS Interface Updated Section 6.3 I2C Slave Interface Updated Section 7.2 Transparent Mode Configuration Registers Updated Section 8 Clock Scheme
12/10/14	1.3	Added Section 5 Mode Selection and Port-lane Mapping Updated Section 1 Features Updated Section 3.1 PCI Express Interface Signals (31 BALLS) Updated Section 3.2 Port Specific Signals (10 BALLS) Updated Section 3.4 Miscellaneous Signals (71 BALLS) Updated Section 4.1 PIN LIST of 196-Pin LBGA Updated Figure 4 1 PI7C9X2G606PR Ball Assignment Updated Section 7.1 EEPROM Interface Updated Section 7.2 SMBus Interface Updated Section 8.2 Transparent Mode Configuration Registers Updated Section 9 Clock Scheme
8/24/15	1.3	Updated Section 3.2 Port Specific Signals (10 Balls) Update Section 5.1 Physical Layer Circuit Updated Section 6.1 EEPROM Interface Updated Section 7.2.5 REVISION ID REGISTER Updated Section 8 Clock Scheme Updated Section 10.2 DC Specifications
09/15/15	1.4	Updated Table 11-1 Absolute Maximum Ratings
12/18/15	1.5	Updated Section 3 Pin Description Updated Table 7-5 SMBUS Block Write Portion Updated Figurate 7-11/7-13 I2C Read Command Packet Updated Section 8.2.48 XPIP_CSR0 Register Updated Section 8.2.59 XPIP_CSR5 Register Updated Section 8.2.60 TL_CSR Register Updated Section 8.2.77 PCI Express Capabilities Register Updated Section 8.2.84 Slot Capabilities Register Updated Section 8.2.109 Port VC Capability Register 1 Updated Section 8.2.144 Power Saving Disable Register Updated Table 11-1 Absolution Maximum Ratings

Date	Revision Number	Description
		Updated Table 11-2 DC Electrical Characteristics
03/03/16	1.6	Added Section 11 Power Sequence
04/07/16	1.7	Updated Section 3.4 MISCELLANEOUS SIGNALS (71 BALLS)
08/25/16	1.8	Updated Section 1 Features Updated Section 3-2 Port Specific Signals (19 balls) Updated Section 5-3 Port-Lane Mapping Updated Section 8.2.17 Memory Base Address Register – OFFSET 20h Updated Section 8.2.59 XPIP_CSR5 – OFFSET 88h Updated Section 8.2.63 Operation Mode – OFFSET 98h Updated Section 8.2.81 Link Capabilities Register – OFFSET CCh Updated Section 8.2.83 Link Status Register – OFFSET D0h Updated Section 8.2.140 SMBUS Control Register – OFFSET 344h (Upstream Port Only)
09/19/17	2-2	Updated Section 3.2 Port Specific Signals (10 Balls) Updated Section 3.3 EEPROM and SMBUS/I2C Signals (6 balls) Updated Section 7.1.4 Mapping EEPROM Contents to Configuration Registers U[dated Section 8.2 Transparent Mode Configuration Registers Updated Section 12.1 Absolute Maximum Ratings Updated Table 12 2 DC Electrical Characteristics Added Section 12.4 Operating Ambient Temperature Added Table 12.8 Power Consumption Added Section 13 Thermal Data Updated Section 14 Package Information Updated Section 15 Ordering Information Revision numbering system changed to whole number
01/12/18	3	Updated Section 6.7 Transaction Ordering Updated Section 7 EEPROM Interface and System Management/I2C Bus Updated Section 8.2 TRANSPARENT MODE CONFIGURATION REGISTERS Updated Section Table 9-1 DC Electrical Characteristics Updated Section Table 12-1 Absolute Maximum Ratings Updated Section 15 Ordering Information Added Figure 14-2 Part Marking
08/14/19	4	Updated Section 1 Features Updated Section 7.1.1 Auto Mode EEPROM Access Updated Section 7.1.2 EEPROM Normal Mode At Reset Updated Section 10 POWER MANAGEMENT Updated Section 12.1 Absolute Maximum Ratings
10/25/19	5	Updated Section 1 Features Updated Section 15 Ordering Information Updated Figure 14-2 Part Marking
03/26/20	6	Updated Section 15 Ordering Information Updated Section 6.1 Physical Layer Circuit
12/11/20	7	For Datasheet Status Change

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1 Features

- 6-lane PCI Express Gen 2 Switch with 6 PCI Express ports
- Supports “Cut-through”(Default) as well as “Store and Forward” mode for packet switching
- Peer-to-peer switching between any two downstream ports
- 150 ns typical latency for packet routed through Switch without blocking
- Strapped pins configurable with optional EEPROM, SMBus or I2C Bus
- SMBus interface support
- I2C Slave interface support
- Compliant with System Management (SM) Bus, Version 2.0
- Compliant with I2C Bus Specification, Version 2.1
- Compliant with *PCI Express Base Specification Revision 2.1*
- Compliant with *PCI Express CEM Specification Revision 2.0*
- Compliant with *PCI-to-PCI Bridge Architecture Specification Revision 1.2*
- Compliant with *Advanced Configuration Power Interface (ACPI) Specification*
- Reliability, Availability and Serviceability
  - Supports Data Poisoning and End-to-End CRC
  - Advanced Error Reporting and Logging
- Advanced Power Saving
  - Empty downstream ports are set to idle state to minimize power consumption
- Link Power Management
  - Supports L0, L0s, L1, L2, L2/$L3_{Ready}$ and L3 link power states
  - Active state power management for L0s and L1 states
- Device State Power Management
  - Supports D0, $D3_{Hot}$ and $D3_{Cold}$ device power states
- Port Arbitration: Round Robin (RR), Weighted RR and Time-based Weighted RR
- Extended Virtual Channel capability
  - Two Virtual Channels (VC) and Eight Traffic Class (TC) support
  - Disabled VCs’ buffer is assigned to enabled VCs for resource sharing
  - Independent TC/VC mapping for each port
  - Provides VC arbitration selections: Strict Priority, Round Robin (RR) and Programmable Weighted RR
- Supports Isochronous Traffic
  - Isochronous traffic class mapped to VC1 only
  - Strict time based credit policing
- Supports up to 512-byte maximum payload size
- Programmable driver current and de-emphasis level at each individual port
- Support Address Translation (AT) and Access Control Service (ACS)
- Support OBFF and LTR
- Support Serial Hot Plug Controller
- Low Power Dissipation: 0.6 W typical in L0 normal mode
- Industrial Temperature Range -40° to 85°C
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. “Green” Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.
  https://www.diodes.com/quality/product-definitions/
- 196-pin LBGA 15mm x 15mm package

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated’s definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

2 GENERAL DESCRIPTION

Similar to the role of PCI/PCIX Bridge in PCI/PCIX bus architecture, the function of PCI Express (PCIE) Switch is to expand the connectivity to allow more end devices to be reached by host controllers in PCIE serial interconnect architecture. The 6-lane PCIe Switch is in 6-port type configuration. It provides users the flexibility to expand or fan-out the PCI Express lanes based on their application needs.

In the PCI Express Architecture, the PCIE Switch forwards posted and non-posted requests and completion packets in either downstream or upstream direction concurrently as if a virtual PCI Bridge is in operation on each port. By visualizing the port as a virtual Bridge, the Switch can be logically viewed as two-level cascaded multiple virtual PCI-to-PCI Bridges, where one upstream-port Bridge sits on all downstream-port Bridges. Similar to a PCI Bridge during enumeration, each port is given a unique bus number, device number, and function number by the initiating software. The bus number, device number, and function number are combined to form a destination ID for each specific port. In addition to that, the memory-map and IO address ranges are exclusively allocated to each port as well. After the software enumeration is finished, the packets are routed to the dedicated port based on the embedded address or destination ID. To ensure the packet integrity during forwarding, the Switch is not allowed to split the packets to multiple small packets or merge the received packets into a large transmit packet. Also, the IDs of the requesters and completers are kept unchanged along the path between ingress and egress port.

The Switch employs the architecture of Combined Input and Output Queue (CIOQ) in implementation. The main reason for choosing CIOQ is that the required memory bandwidth of input queue equals to the bandwidth of ingress port rather than increasing proportionally with port numbers as an output queue Switch does. The CIOQ at each ingress port contains separate dedicated queues to store packets. The packets are arbitrated to the egress port based on the PCIe transaction-ordering rule. For the packets without ordering information, they are permitted to pass over each other in case that the addressed egress port is available to accept them. As to the packets required to follow the ordering rule, the Head-Of-Line (HOL) issue becomes unavoidable for packets destined to different egress ports since the operation of producer-consumer model has to be retained; otherwise the system might occur hang-up problem. On the other hand, the Switch places replay buffer at each egress port to defer the packets before sending it out. This can assure the maximum throughput being achieved and therefore the Switch works efficiently. Another advantage of implementing CIOQ in PCIe Switch is that the credit announcement to the counterpart is simplified and streamlined because of the credit-based flow control protocol. The protocol requires that each ingress port maintains the credits independently without checking other ports' credit availability, which is otherwise required by pure output queue architecture.

The Switch supports two virtual channels (VC0, VC1) and eight traffic classes (TC0 ~ TC7) at each port. The ingress port independently assigns packets into the preferred virtual channel while the egress port outputs the packet based on the predefined port and VC arbitration algorithm. For instance, the isochronous packet is given a special traffic class number other than TC0 and mapped into VC1 accordingly. By employing the strict time based credit policy for port arbitration and assigning higher priority to VC1 than VC0, the Switch can therefore guarantee the time-sensitive packet is not blocked by regular traffic to assure the quality of service. In addition, some data-centric applications only carry TC0/VC0 traffic. As a result, there are no packets that would consume VC1 bandwidth. In order to improve the efficiency of buffer usage, the unused VC1 queues can be reassigned to VC0 and enable each of the ingress ports to handle more data traffic bursts. This virtual channel resource relocation feature enhances the performance of the PCIe Switch further.

The Switch provides the advanced feature of Access Control Service (ACS). This feature regulates which components are allowed to communicate with each other within the PCIe multiple-point fabric, and allows the system to have more control over packet routing in the Switch. As a result, peer-to-peer traffic can be facilitated more accurately and efficiently. When the system also implements Address Translation Service (ATS), the peer-to-peer requests with translated address can be routed directly by enabling the corresponding option in ACS to avoid possible performance bottleneck associated with re-direction, which introduces extra latency and may increase link and RC congestion.

3 PIN DESCRIPTION

3.1 PCI EXPRESS INTERFACE SIGNALS (31 BALLS)

NAME	PIN	TYPE	DESCRIPTION
REFCLKP REFCLKN	N8 P8	I	**Reference Clock Input Pairs:** Connect to 100MHz differential clock.
PERP[7:4, 1:0]	A3, A5, A10, A12, P5, P3	I	**PCI Express Data Serial Input Pairs:** Differential data receive signals in six ports. Please refer to Section 5 for Mapping of the Lanes to transmission and receive pairs and configuration of Port-Lane.
PERN[7:4, 1:0]	B3, B5, B10, B12, N5, N3	I	
PETP[7:4, 1:0]	A4, A6, A9, A11, P6, P4	O	**PCI Express Data Serial Output Pairs:** Differential data transmit signals in six ports. Please refer to Section 5 for Mapping of the Lanes to transmission and receive pairs and configuration of Port-Lane.
PETN[7:4, 1:0]	B4, B6, B9, B11, N6, N4	O	
PERST_L	H13	I	**System Reset (Active LOW):** When PERST_L is asserted, the internal states of whole chip except sticky logics are initialized. Please refer to Table 11-2 for PERST_L Spec.
REXT[1:0]	A8, P7	I	**External Reference Resistor:** Connect an external resistor (1.43K Ohm +/- 1%) to REXT_GND to provide a reference to both the bias currents and impedance calibration circuitry.
REXTGND[1:0]	B8, N7	I	**External Reference Resistor Ground:** Connect to an external resistor to REXT.

3.2 PORT SPECIFIC SIGNALS (10 BALLS)

NAME	PIN	TYPE	DESCRIPTION
LNKSTS[7:4, 1:0]	C2, *A14, *B14, B1, *M13, P14	O	**Link Status:** These signals indicate the link status of each port . When continuously asserts, the device is in the condition of link down. When continuously deasserts, the link is up and operates at 5GT/s. When blinking, asserts and deasserts with 0.2-second intervals, the link is up and operates at 2.5GT/s. These signals are valid when LNKSTS_DIS is set to low and GPIO[4:0] are set to "01011b". LNKSTS[x] is correspondent to Lane x, where x=0,1,4,5,6,7. **Debug Mode Disable (DBG_DIS):** During system initialization, LNKSTS[1] acts as the DBG_DIS pin. When tied high, it is in the normal mode. When tied low, it is in the debug mode. This pin has internal pull-up resistor. If no board trace is connected to this pin, the internal pull-up resistor of this pin is enough. However, if pin is connected to a board trace and not driven, it is recommended that an external 5.1K- ohm pull-up resistor be used. **LNKSTS Disable (LNKSTS_DIS):** During system initialization, LNKSTS[5] acts as the LNKSTS_DIS to select enable or disable LNKSTS pins output link status. When tied high, it is disabled LNKSTS outputs. When tied low, it is enabled LNKSTS outputs. This pin has internal pull-up resistor. **LED_DEBUG_MODE (LED_DEBUG):** During system initialization, LNKSTS[6] acts as the LED_DEBUG to select enable or disable LNKSTS pins output link status. When tied high, it is disabled LNKSTS outputs. When tied low, it is enabled LNKSTS outputs. This pin has internal pull-up resistor.

NAME	PIN	TYPE	DESCRIPTION
UPS_PORTSEL[3:0]	G2, H2, F1, F3	I	**Upstream Port Selection:** These signals decide which port will be the upstream port. These pins have internal pull-down resistors. If no board trace is connected to these pins, the internal pull-down resistors of these pins are enough. However, if pins are connected to a board trace and not driven, it is recommended that external 330-ohm pull-down resistors be used. Please refer to Section 5 for Port-Lane Mapping.

3.3 EEPROM and SMBUS/I2C SIGNALS (9 BALLS)

NAME	PIN	TYPE	DESCRIPTION
EECK	J14	I/O	**EEPROM Clock:** Clock signal to 4-wire EEPROM interface.
EEDI	K14	O	**EEPROM Data Input:** Pericom 2G606PR outputs data to the Data Input pin of Serial EEPROM.
EEDO	H14	I	**EEPROM Data Output:** Pericom 2G606PR inputs data from the Data Output pin of Serial EEPROM.
EECS_L	*J13	I/O	**EEPROM Chip Select (Active Low):** Pericom 2G606PR asserts this signal to enable Serial EEPROM. **EEPROM Bypass Mode (EEPROM_BYPASS_L):** During system initialization, EECS_L acts as the EEPROM_BYPASS_L pin. When tied low, eeprom function is disabled. When tied high, eeprom function is enabled. The pin has internal pull-up resistor. If no board trace is connected to this pin, the internal pull-up resistor of this pin is enough. However, if pin is connected to a board trace and not driven, it is recommended that an external 5.1K-ohm pull-up resistor be used.
SCL_I2C	F14	OD	**SMBUS/I2C Serial Clock:** System management or I2C Bus Clock. This pin requires an external 5.1K-ohm pull-up resistor.
SDA_I2C	F12	OD	**SMBUS/I2C Serial Data:** Bi-Directional System Management or I2C Bus Data. This pin requires an external 5.1K-ohm pull-up resistor.
I2C_ADDR[2:0]	G14, F11, G13	I	**SMBUS/I2C Slave Address Bit [2:0]:** These pins are used to configure the value of the three least significant bits of the PI7C2G606PR 7-bit Slave address.

3.4 MISCELLANEOUS SIGNALS (71 BALLS)

NAME	PIN	TYPE	DESCRIPTION
SHCL_I2C	F13	OD	**I2C Clock Signal of Serial Hot Plug Controller:** It is connected to SCL pin of all I2C IO expanders.
SHDA_I2C	E14	OD	**I2C Data Signal of Serial Hot Plug Controller:** It is connected to SDA pin of all I2C IO expanders.
SHPCINT_L	C14	I	**Interrupt Input (Active Low) of Serial Hot Plug Controller:** It is connected to INT# output pin of all I2C IO expanders. When asserted, it notifies Hot Plug Controller to access the port registers of all I/O expanders for touching changed status to de-assert INT#.
GPIO[7:0]	J1, J4, F2, E1, E2, E3, D1, D2	I/O	**General Purpose Input and Output:** These eight general-purpose pins are programmed as either input-only or bi-directional pins by writing the GPIO output enable control register. **Port-Lane Configuration Selection:** GPIO[1:0] are used for Port-Lane Configuration Selection. GPIO[1:0]=00b… 5Port-5Lane GPIO[1:0]=01b… 6Port-6Lane (default) GPIO[1:0]=10b… 5Port-6Lane **Debug Mode Selection:** In debug mode, GPIO[4:0] are used for Debug Mode Selection.

NAME	PIN	TYPE	DESCRIPTION
DBO[4:0]	*F1, *F3, *L14, *L12, *N1	O	**Debugout Pins:** These signals will output internal debug status. Please connect to test pin header for debug used. **Operation Mode Selection (OPMode_Sel):** During system initialization, DBO[2:0] acts as the OPMode_Sel[2:0] pins. When tied low, it is in the normal mode. These pins have internal pull-down resistors. If no board trace is connected to these pins, the internal pull-down resistors of these pins are enough. However, if pins are connected to a board trace and not driven, it is recommended that external 330-ohm pull-down resistors be used. DBO[4] shares with UPS_PORTSEL[1] DBO[3] shares with UPS_PORTSEL[0]
SMBUS_EN_L	L1	I	**System Manage Bus Enable:** Select either SMBUS or I2C protocol. When tied high, I2C protocol is selected. When tied low, SMBUS protocol is chosen. The pin has internal pull-up resistor. If no board trace is connected to this pin, the internal pull-up resistor of this pin is enough. However, if pin is connected to a board trace and not driven, it is recommended that an external 5.1K-ohm pull-up resistor be used.
STRAP_TEST_H	L2, M14, N13, N14	I	**STRAP_TEST_HIGH Signals:** Must be pulled or tied High to VDD
TEST	H12	I	**Test Signal:** This pin is used for internal test purpose and can be left unconnected. The pin has internal pull-down resistor to make chip operate under normal mode. If no board trace is connected to this pin, the internal pull-down resistor of this pin is enough. However, if pin is connected to a board trace and not driven, it is recommended that an external 330-ohm pull-down resistor be used.
TCK	E13	I	**Test Clock:** Used to clock state information and data into and out of the chip during boundary scan. When JTAG boundary scan function is not implemented, this pin should be left open (NC).
TDI	D12	I	**Test Data Input:** Used (in conjunction with TCK) to shift data and instructions into the TAP in a serial bit stream. When JTAG boundary scan function is not implemented, this pin should be left open (NC).
TDO	E12	O	**Test Data Output:** Used (in conjunction with TCK) to shift data out of the Test Access Port (TAP) in a serial bit stream. When JTAG boundary scan function is not implemented, this pin should be left open (NC).
TMS	D14	I	**Test Mode Select:** Used to control the state of the Test Access Port controller. When JTAG boundary scan function is not implemented, this pin should be pulled low through a 330-Ohm pull-down resistor.
TRST_L	C13	I	**Test Reset (Active LOW):** Active LOW signal to reset the TAP controller into an initialized state. When JTAG boundary scan function is not implemented, this pin should be pulled low through a 330-Ohm pull-down resistor.
NC	A1, A2, A7, A13, B2, B7, B13, C1, C3, C4, C7, C12, D3, D13, F4, G1, H1, J2, J3, J11, J12, K1, K2, K3, K12, K13, L3, L13, M1, M2, M3, M4, M8, M12, N2, N9, N10, N11, N12, P1, P2, P9, P10, P11, P12, P13		**No Connection:** leaves these pins floating.

3.5 POWER PINS (75 BALLS)

NAME	PIN	TYPE	DESCRIPTION
VDDC	D5, D6, D9, D10, E4, E11, G4, G11, H4, H11, K4, K11, L5, L6, L9, L10	P	**VDDC Supply (1.0V):** Used as digital core power pins.

NAME	PIN	TYPE	DESCRIPTION
VDDR	D4, D11, L4, L11	P	**VDDR Supply (2.5V):** Used as digital I/O power pins.
AVDD	D7, D8, L7, L8	P	**AVDD Supply (1.0V):** Used as PCI Express analog power pins.
AVDDH	C8, G3, G12, M7	P	**AVDDH Supply (2.5V):** Used as PCI Express analog high voltage power pins.
AGND	C5, C6, C9, C10, C11, H3, M5, M6, M9, M10, M11	P	**Analog Ground:** Used as analog ground pins.
DGND	E5, E6, E7, E8, E9, E10, F5, F6, F7, F8, F9, F10, G5, G6, G7, G8, G9, G10, H5, H6, H7, H8, H9, H10, J5, J6, J7, J8, J9, J10, K5, K6, K7, K8, K9, K10	P	**Digital Ground:** Used as digital ground pins.

4 PIN ASSIGNMENTS

4.1 PIN LIST of 196-PIN LBGA

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
A1	NC	D8	AVDD	H1	NC	L8	AVDD
A2	NC	D9	VDDC	H2	UPS_PORTSEL[2]	L9	VDDC
A3	PERP[7]	D10	VDDC	H3	AGND	L10	VDDC
A4	PETP[7]	D11	VDDR	H4	VDDC	L11	VDDR
A5	PERP[6]	D12	TDI	H5	DGND	L12	DBO[1]
A6	PETP[6]	D13	NC	H6	DGND	L13	NC
A7	NC	D14	TMS	H7	DGND	L14	DBO[2]
A8	REXT[1]	E1	GPIO[4]	H8	DGND	M1	NC
A9	PETP[5]	E2	GPIO[3]	H9	DGND	M2	NC
A10	PERP[5]	E3	GPIO[2]	H10	DGND	M3	NC
A11	PETP[4]	E4	VDDC	H11	VDDC	M4	NC
A12	PERP[4]	E5	DGND	H12	TEST	M5	AGND
A13	NC	E6	DGND	H13	PERST_L	M6	AGND
A14	LNKSTS[6]/LED_DEBUG	E7	DGND	H14	EEDO	M7	AVDDH
B1	LNKSTS[4]	E8	DGND	J1	GPIO[7]	M8	NC
B2	NC	E9	DGND	J2	NC	M9	AGND
B3	PERN[7]	E10	DGND	J3	NC	M10	AGND
B4	PETN[7]	E11	VDDC	J4	GPIO[6]	M11	AGND
B5	PERN[6]	E12	TDO	J5	DGND	M12	NC
B6	PETN[6]	E13	TCK	J6	DGND	M13	LNKSTS[1]/DBG_DIS
B7	NC	E14	SHDA_I2C	J7	DGND	M14	STRAP_TEST_H
B8	REXTGND[1]	F1	UPS_PORTSEL[1]/DBO[4]	J8	DGND	N1	DBO[0]
B9	PETN[5]	F2	GPIO[5]	J9	DGND	N2	NC
B10	PERN[5]	F3	UPS_PORTSEL[0]/DBO[3]	J10	DGND	N3	PERN[0]
B11	PETN[4]	F4	NC	J11	NC	N4	PETN[0]
B12	PERN[4]	F5	DGND	J12	NC	N5	PERN[1]
B13	NC	F6	DGND	J13	EECS_L	N6	PETN[1]
B14	LNKSTS[5]/LNKSTS_DIS	F7	DGND	J14	EECK	N7	REXTGND[0]
C1	NC	F8	DGND	K1	NC	N8	REFCLKP
C2	LNKSTS[7]	F9	DGND	K2	NC	N9	NC
C3	NC	F10	DGND	K3	NC	N10	NC
C4	NC	F11	I2C_ADDR[1]	K4	VDDC	N11	NC
C5	AGND	F12	SDA_I2C	K5	DGND	N12	NC
C6	AGND	F13	SHCL_I2C	K6	DGND	N13	STRAP_TEST_H
C7	NC	F14	SCL_I2C	K7	DGND	N14	STRAP_TEST_H
C8	AVDDH	G1	NC	K8	DGND	P1	NC
C9	AGND	G2	UPS_PORTSEL[3]	K9	DGND	P2	NC
C10	AGND	G3	AVDDH	K10	DGND	P3	PERP[0]
C11	AGND	G4	VDDC	K11	VDDC	P4	PETP[0]
C12	NC	G5	DGND	K12	NC	P5	PERP[1]
C13	TRST_L	G6	DGND	K13	NC	P6	PETP[1]
C14	SHPCINT_L	G7	DGND	K14	EEDI	P7	REXT[0]
D1	GPIO[1]	G8	DGND	L1	SMBUS_EN_L	P8	REFCLKN
D2	GPIO[0]	G9	DGND	L2	STRAP_TEST_H	P9	NC
D3	NC	G10	DGND	L3	NC	P10	NC
D4	VDDR	G11	VDDC	L4	VDDR	P11	NC
D5	VDDC	G12	AVDDH	L5	VDDC	P12	NC
D6	VDDC	G13	I2C_ADDR[0]	L6	VDDC	P13	NC
D7	AVDD	G14	I2C_ADDR[2]	L7	AVDD	P14	LNKSTS[0]

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	NC	NC	PERP [7]	PETP [7]	PERP [6]	PETP [6]	NC	REXT [1]	PETP [5]	PERP [5]	PETP [4]	PERP [4]	NC	LNK STS[6]	A
B	LNK STS[4]	NC	PERN [7]	PETN [7]	PERN [6]	PETN [6]	NC	REXT GND [1]	PETN [5]	PERN [5]	PETN [4]	PERN [4]	NC	LNK STS[5]/ LNTST S_DIS	B
C	NC	LNK STS[7]	NC	NC	AGND	AGND	NC	AVDD H	AGND	AGND	AGND	NC	TRST_ L	SHPC INT_L	C
D	GPIO [1]	GPIO [0]	NC	VDDR	VDDC	VDDC	AVDD	AVDD	VDDC	VDDC	VDDR	TDI	NC	TMS	D
E	GPIO [4]	GPIO [3]	GPIO [2]	VDDC	DGND	DGND	DGND	DGND	DGND	DGND	VDDC	TDO	TCK	SHDA _I2C	E
F	UPS_ PORT SEL[1]/ DBO[4]	GPIO [5]	UPS_ PORT SEL[0]/ DBO[3]	NC	DGND	DGND	DGND	DGND	DGND	DGND	I2C_ ADDR [1]	SDA _I2C	SHCL _I2C	SCL _I2C	F
G	NC	UPS_ PORT SEL[3]	AVDD H	VDDC	DGND	DGND	DGND	DGND	DGND	DGND	VDDC	AVDD H	I2C_ ADDR [0]	I2C_ ADDR [2]	G
H	NC	UPS_ PORT SEL[2]	AGND	VDDC	DGND	DGND	DGND	DGND	DGND	DGND	VDDC	TEST	PERST _L	EEDO	H
J	GPIO [7]	NC	NC	GPIO [6]	DGND	DGND	DGND	DGND	DGND	DGND	NC	NC	EECS _L	EECK	J
K	NC	NC	NC	VDDC	DGND	DGND	DGND	DGND	DGND	DGND	VDDC	NC	NC	EEDI	K
L	SMBU S_EN_ L	STRAP _TEST_ H	NC	VDDR	VDDC	VDDC	AVDD	AVDD	VDDC	VDDC	VDDR	DBO[1]	NC	DBO[2]	L
M	NC	NC	NC	NC	AGND	AGND	AVDD H	NC	AGND	AGND	AGND	NC	LNK STS[1]/ DBG_D IS	STRAP _TEST_ H	M
N	DBO[0]	NC	PERN [0]	PETN [0]	PERN [1]	PETN [1]	REXT GND [0]	REFC LKP	NC	NC	NC	NC	STRAP _TEST_ H	STRAP _TEST_ H	N
P	NC	NC	PERP [0]	PETP [0]	PERP [1]	PETP [1]	REXT [0]	REFC LKN	NC	NC	NC	NC	NC	LNK STS[0]	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Figure 4-1 PI7C9X2G606PR Ball Assignment (Transparent Top View)

5 MODE SELECTION AND PORT-LANE MAPPING

5.1 MODE SELECTION

PI7C9X2G606PR can be configured into 5 Port-6 Lane, 6 Port-6 Lane and 5 Port-5 Lane modes by setting GPIO[1:0].

GPIO[1]	GPIO[0]	Functional Mode
0	0	505 mode, 5Port-5Lane Configuration
0	1	606 mode, 6Port-6Lane Configuration (default)
1	0	506 mode, 5Port-6Lane Configuration
1	1	Reserved

5.2 LANE MAPPING

The table below shows the mapping of the lanes to the transmission and receives pairs.

Lane	TX Pair	RX Pair
Lane 0	PETP[0]PETN[0]	PERP[0]PERN[0]
Lane 1	PETP[1]PETN[1]	PERP[1]PERN[1]
Lane 4	PETP[4]PETN[4]	PERP[4]PERN[4]
Lane 5	PTTP[5]PETN[5]	PERP[5]PERN[5]
Lane 6	PETP[6]PETN[6]	PERP[6]PERN[6]
Lane 7	PETP[7]PETN[7]	PERP[7]PERN[7]

5.3 PORT-LANE MAPPING

The table below shows the mapping of the lanes to ports in different functional modes via UPS_PORTSEL[3:0] settings.

GPIO[1:0]	Functional Mode											
	505	505	505	505	505	506	606	606	606	606	606	606
UPS_PORTSEL[3:0]	0000	0001	0101	0111	1001	0000	0000	0001	0101	0111	1001	0100
Lane 0	P0	P1	P2	P3	P4	P0	P0	P1	P2	P3	P4	P5
Lane 1	-	-	-	-	-	P0	P5	P5	P5	P5	P5	P0
Lane 4	P1	P0	P1	P1	P1	P1	P1	P0	P1	P1	P1	P1
Lane 5	P2	P2	P0	P2	P2	P2	P2	P2	P0	P2	P2	P2
Lane 6	P3	P3	P3	P0	P3	P3	P3	P3	P3	P0	P3	P3
Lane 7	P4	P4	P4	P4	P0	P4	P4	P4	P4	P4	P0	P4

Notes:
P0: upstream port
P1~P5: downstream ports

6 FUNCTIONAL DESCRIPTION

Multiple virtual PCI-to-PCI Bridges (VPPB), connected by a virtual PCI bus, reside in the Switch. Each VPPB contains the complete PCIe architecture layers that consist of the physical, data link, and transaction layer. The packets entering the Switch via one of VPPBs are first converted from serial bit-stream into parallel bus signals in physical layer, stripped off the link-related header by data link layer, and then relayed up to the transaction layer to extract out the transaction header. According to the address or ID embedded in the transaction header, the entire transaction packets are forwarded to the destination VPPB for formatting as a serial-type PCIe packet through the transmit circuits in the data link layer and physical layer. The following sections describe these function elements for processing PCIe packets within the Switch.

6.1 PHYSICAL LAYER CIRCUIT

The physical layer circuit design is based on the **P**HY **I**nterface for **P**CI **E**xpress Architecture (PIPE). It contains Physical Media Attachment (PMA) and Physical Coding Sub-layer (PCS) blocks. PMA includes Serializer/ Deserializer (SERDES), PLL[1], Clock Recovery module, receiver detection circuits, beacon transmitter, electrical idle detector, and input/output buffers. PCS consists of framer, 8B/10B encoder/decoder, receiver elastic buffer, and PIPE PHY control/status circuitries. To provide the flexibility for port configuration, each lane has its own control and status signals for MAC to access individually.

In order to meet the needs of different application, the drive amplitude, de-emphasis and equalization of each transmitting channels can be adjusted using EEPROM, SMBus or I2C individually. De-emphasis of -3.5 db is implemented by the transmitters when full swing signaling is used, while an offset can be individually applied to each channel.

6.1.1 RECEIVER DETECTION

The physical layer circuits implement receiver detection, which detects the presence of an attached 50 ohm to ground termination as per PCI Express Specification. The detect circuits determine if the voltage levels of the receiver have crossed the internal threshold after a configurable time determined by the Receiver Detection Threshold field in the PHY Parameter 2 Register (offset 7Ch, bit[6:4]) as listed in Table 6-1, which can be configured by EEPROM, SMBus or I2C settings.

Table 6-1 Receiver Detection Threshold Settings

Receiver Detection Threshold	Threshold
000	1.0 us
001	2.0 us
010	4.0 us (Recommended)
011	5.0 us
100	10 us
101	20 us
110	40 us
111	50 us

[1] Multiple lanes could share the PLL.

6.1.2 RECEIVER SIGNAL DETECTION

Receiver signal idling is detected with levels above a programmable threshold specified by Receiver Signal Detect field in the PHY Parameter 2 Register (Offset 7Ch, bit[21:20]) as listed in Table 6-2, which can be configured on a per-port basis via EEPROM, SMBus or I2C settings.

Table 6-2 Receiver Signal Detect Threshold

Receiver Signal Detect	Min (mV ppd)	Max (mV ppd)
00	50	80
01 (Recommended)	65	175
10	75	200
11	120	240

6.1.3 RECEIVER EQUALIZATION

The receiver implements programmable equalizer via the Receiver Equalization field in the PHY Parameter 2 Register (Offset 7Ch, bit [25:22]) as listed in Table 6-3, which can be configured on a per-port basis via EEPROM, SMBus or I2C settings.

Table 6-3 Receiver Equalization Settings

Receiver Equalization	Equalization
0000	Off
0010	Low
0110 (Recommended)	Medium
1110	High

6.1.4 TRANSMITTER SWING

The PCI Express transmitters support implementations of both full voltage swing and half (low) voltage swing. In full swing signaling mode, the transmitters implement de-emphasis, while in half swing mode, the transmitters do not. The Transmitter Swing field in the PHY Parameter 2 Register (offset 7Ch, Bit[30]) is used for the selection of full swing signaling or half swing signaling, which can be configured on a per-port basis via EEPROM, SMBus or I2C settings.

Table 6-4 Transmitter Swing Settings

Transmitter Swing	Mode	De-emphasis
0	Full Voltage Swing	Implemented
1	Half Voltage Swing	Not implemented

6.1.5 DRIVE AMPLITUDE AND DE-EMPHASIS SETTINGS

Depending on the operation condition (voltage swing and de-emphasis condition), one of the Drive Amplitude Base Level fields in the Switch Operation Register (offset 74h) and one of the Drive De-Emphasis Base Level fields in the PHY Parameter 1 Register (offset 78h) are active for configuration of the amplitude and de-emphasis.

The final drive amplitude and drive de-emphasis are the summation of the base level value and the offset value. The offset value for drive amplitude is 25 mV pd, and 6.25 mV pd for drive de-emphasis.

The driver output waveform is the synthesis of amplitude and de-emphasis as shown in Figure 6-1. The driver amplitude without de-emphasis is specified as a peak differential voltage level (mVpd), and the driver de-emphasis modifies the driver amplitude.

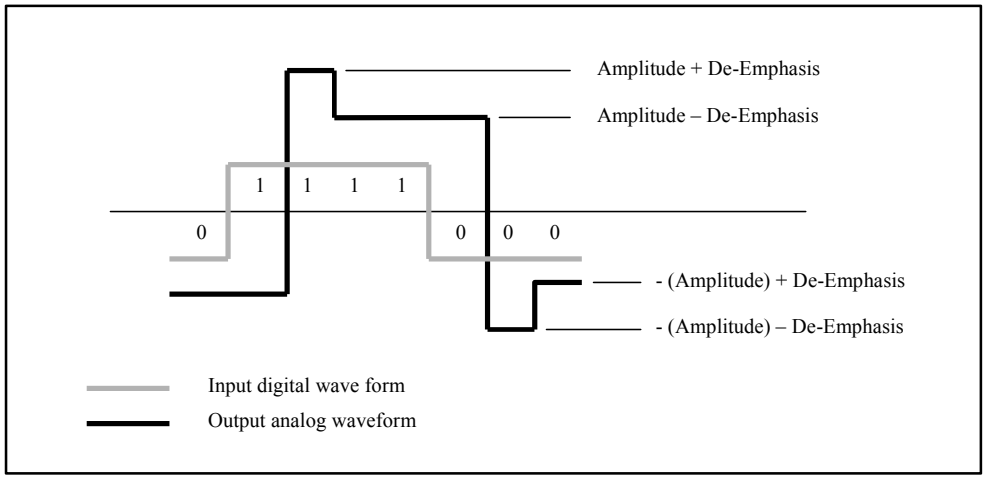


Figure 6-1 Driver Output Waveform

6.1.5.1 DRIVE AMPLITUDE

Only one of the Drive Amplitude Level field in the Switch Operation Register (offset 74h, bit[20:16], bit[25:21] and bit[30:26]) listed in

Table 6-5 is active depending on the de-emphasis and swing condition. The settings and the corresponding values of the amplitude level are listed in
Table 6-6, which can be configured by EEPROM, SMBus or I2C settings.

Table 6-5 Drive Amplitude Base Level Registers

Active Register	De-Emphasis Condition	Swing Condition
Drive Amplitude Level (3P5 Nom)	-3.5 db	Full
Drive Amplitude Level (6P0 Nom)	-6.0 db	Full
Drive Amplitude Level (Half)	N/A	Half

Table 6-6 Drive Amplitude Base Level Settings

Setting	Amplitude (mV pd)	Setting	Amplitude (mV pd)	Setting	Amplitude (mV pd)
00000	0	00111	175	01110	350
00001	25	01000	200	01111	375
00010	50	01001	225	10000	400
00011	75	01010	250	10001	425
00100	100	01011	275	10010	450
00101	125	01100	300	10011	475
00110	150	01101	325	Others	Reserved

Note:
1. Nominal levels. Actual levels will vary with temperature, voltage and board effects.
2. The maximum nominal amplitude of the output driver is 475 mV pd. Combined values of driver amplitude and de-emphasis greater than 475 mV pd should be avoided.
3. At higher amplitudes, actual swings will be less than the theoretical value due to process variations and environment factors, such as voltage overhead compression, package losses, board losses, and other effects.

6.1.5.2 DRIVE DE-EMPHASIS

The Drive De-Emphasis Level field in the PHY Parameter 1 Register (Offset 78h, bit[20:16]) listed in Table 6-7 controls the de-emphasis base level. The settings and the corresponding values of the de-emphasis level are listed in Table 6-8, which can be configured by EEPROM, SMBus or I2C settings.

Table 6-7 Drive De-Emphasis Base Level Register

Register	De-Emphasis Condition
C_EMP_POST_GEN1_3P5_NOM	-3.5 db
C_EMP_POST_GEN2_3P5_NOM	-3.5 db
C_EMP_POST_GEN2_6P0_NOM	-6.0 db

Table 6-8 Drive De-Emphasis Base Level Settings

Setting	De-Emphasis (mV pd)	Setting	De-Emphasis (mV pd)	Setting	De-Emphasis (mV pd)
00000	0.0	01011	69.0	10110	137.5
00001	6.0	01100	75.0	10111	144.0
00010	12.5	01101	81.0	11000	150.0
00011	19.0	01110	87.0	11001	156.0
00100	25.0	01111	94.0	11010	162.5
00101	31.0	10000	100.0	11011	169.0
00110	37.5	10001	106.0	11100	175.0
00111	44.0	10010	112.5	11101	181.0
01000	50.0	10011	119.0	11110	187.5
01001	56.0	10100	125.0	11111	194.0
01010	62.5	10101	131.0	-	-

Note:
1. Nominal levels. Actual levels will vary with temperature, voltage and board effects.
2. The maximum nominal amplitude of the output driver is 475 mV pd. Combined values of driver amplitude and de-emphasis greater than 475 mV pd should be avoided.
3. At higher amplitudes, actual swings will be less than the theoretical value due to process variations and environment factors, such as voltage overhead compression, package losses, board losses, and other effects.

6.1.6 TRANSMITTER ELECTRICAL IDLE LATENCY

After the last character of the PCI Express transmission, the output current is reduced, and a differential voltage of less than 20 mV with common mode of VTX-CM-DC is established within 20 UI. This delay time is programmable via Transmitter PHY Latency field in the PHY Parameter 2 Register (Offset 7Ch, bit[3:0]), which can be configured by EEPROM settings.

6.2 DATA LINK LAYER (DLL)

The Data Link Layer (DLL) provides a reliable data transmission between two PCI Express points. An ACK/NACK protocol is employed to guarantee the integrity of the packets delivered. Each Transaction Layer Packet (TLP) is protected by a 32-bit LCRC for error detection. The DLL receiver performs LCRC calculation to determine if the incoming packet is corrupted in the serial link. If an LCRC error is found, the DLL transmitter would issue a NACK data link layer packet (DLLP) to the opposite end to request a re-transmission, otherwise an ACK DLLP would be sent out to acknowledge on reception of a good TLP.

In the transmitter, a retry buffer is implemented to store the transmitted TLPs whose corresponding ACK/NACK DLLP have not been received yet. When an ACK is received, the TLPs with sequence number equals to and smaller than that carried in the ACK would be flushed out from the buffer. If a NACK is received or no ACK/NACK is returned from the link partner after the replay timer expires, then a replay mechanism built in DLL transmitter is

triggered to re-transmit the corresponding packet that receives NACK or time-out and any other TLP transmitted after that packet.

Meanwhile, the DLL is also responsible for the initialization, updating, and monitoring of the flow-control credit. All of the flow control information is carried by DLLP to the other end of the link. Unlike TLP, DLLP is guarded by 16-bit CRC to detect if data corruption occurs.

In addition, the Media Access Control (MAC) block, which is consisted of LTSSM, multiple lanes de-skew, scrambler/de-scrambler, clock correction from inserting skip order-set, and PIPE-related control/status circuits, is implemented to interface physical layer with data link layer.

6.3 TRANSACTION LAYER RECEIVE BLOCK (TLP DECAPSULATION)

The receiving end of the transaction layer performs header information retrieval and TC/VC mapping (see section 5.5), and it validates the correctness of the transaction type and format. If the TLP is found to contain an illegal header or the indicated packet length mismatches with the actual packet length, then a Malformed TLP is reported as an error associated with the receiving port. To ensure end-to-end data integrity, a 32-bit ECRC is checked against the TLP at the receiver if the digest bit is set in header.

6.4 ROUTING

The transaction layer implements three types of routing protocols: ID-based, address-based, and implicit routing. For configuration reads, configuration writes, transaction completion, and user-defined messages, the packets are routed by their destination ID constituted of bus number, device number, and function number. Address routing is employed to forward I/O or memory transactions to the destination port, which is located within the address range indicated by the address field carried in the packet header. The packet header indicates the packet types including memory read, memory write, IO read, IO write, Message Signaling Interrupt (MSI) and user-defined message. Implicit routing is mainly used to forward system message transactions such as virtual interrupt line, power management, and so on. The message type embedded in the packet header determines the routing mechanism.
If the incoming packet cannot be forwarded to any other port due to a miss to hit the defined address range or targeted ID, this is considered as Unsupported Request (UR) packet, which is similar to a master abort event in PCI protocol.

6.5 TC/VC MAPPING

The 3-bit TC field defined in the header identifies the traffic class of the incoming packets. To enable the differential service, a TC/VC mapping table at destination port that is pre-programmed by system software or EEPROM pre-load is utilized to cast the TC labeled packets into the desired virtual channel. Note that TC0 traffic is mapped into VC0 channel by default. After the TC/VC mapping, the receive block dispatches the incoming request, completion, or data into the appropriate VC0 and VC1 queues.

6.6 QUEUE

In PCI Express, it defines six different packet types to represent request, completion, and data. They are respectively Posted Request Header (PH), Posted Request Data payload (PD), Non-Posted Request Header (NPH), Non-Posted Data Payload (NPD), Completion Header (CPLH) and Completion Data payload (CPLD). Each packet with different type would be put into a separate queue in order to facilitate the following ordering processor. Since NPD usually contains one DW, it can be merged with the corresponding NPH into a common queue named NPHD. Except NPHD, each virtual channel (VC0 or VC1) has its own corresponding packet header and data queue. When

only VC0 is needed in some applications, VC1 can be disabled and its resources assigned to VC0 by asserting VC1_EN (Virtual Channel 1 Enable) to low.

6.6.1 PH

PH queue provides TLP header spaces for posted memory writes and various message request headers. Each header space occupies sixteen bytes to accommodate 3 DW or 4 DW headers. There are two PH queues for VC0 and VC1 respectively.

6.6.2 PD

PD queue is used for storing posted request data. If the received TLP is of the posted request type and is determined to have payload coming with the header, the payload data would be put into PD queue. There are two PD queues for VC0 and VC1 respectively.

6.6.3 NPHD

NPHD queue provides TLP header spaces for non-posted request packets, which include memory read, IO read, IO write, configuration read, and configuration write. Each header space takes twenty bytes to accommodate a 3-DW header, s 4-DW header, s 3-WD header with 1-DW data, and a 4-DW header with 1-DW data. There is only one NPHD queue for VC0, since non-posted request cannot be mapped into VC1.

6.6.4 CPLH

CPLH queue provides TLP header space for completion packets. Each header space takes twelve bytes to accommodate a 3-DW header. Please note that there are no 4-DW completion headers. There are two CPLH queues for VC0 and VC1 respectively.

6.6.5 CPLD

CPLD queue is used for storing completion data. If the received TLP is of the completion type and is determined to have payload coming with the header, the payload data would be put into CPLD queue. There are two CPLD queues for VC0 and VC1 respectively.

6.7 TRANSACTION ORDERING

Within a VPPB, a set of ordering rules is defined to regulate the transactions on the PCI Express Switch including Memory, IO, Configuration and Messages, in order to avoid deadlocks and to support the Producer-Consumer model. The ordering rules defined in table 6-9 apply within a single Traffic Class (TC). There is no ordering requirement among transactions within different TC labels. Since the transactions with the same TC label are not allowed to map into different virtual channels, it implies no ordering relationship between the traffic in VC0 and VC1.

Table 6-9 Summary of PCI Express Ordering Rules

Row Pass Column	Posted Request	Read Request	Non-posted Write Request	Read Completion	Non-posted Write Completion
Posted Request	Yes/No[1]	Yes[5]	Yes[5]	Yes[5]	Yes[5]
Read Request	No[2]	Yes	Yes	Yes	Yes
Non-posted Write Request	No[2]	Yes	Yes	Yes	Yes
Read Completion	Yes/No[3]	Yes	Yes	Yes	Yes
Non-Posted Write Completion	Yes[4]	Yes	Yes	Yes	Yes

1. When the Relaxed Ordering Attribute bit is cleared, the Posted Request transactions including memory write and message request must complete on the egress bus of VPPB in the order in which they are received on the ingress bus of VPPB. If the Relaxed Ordering Attribute bit is set, the Posted Request is permitted to pass over other Posted Requests occurring before it.

2. A Read Request transmitting in the same direction as a previously queued Posted Request transaction must push the posted write data ahead of it. The Posted Request transaction must complete on the egress bus before the Read Request can be attempted on the egress bus. The Read transaction can go to the same location as the Posted data. Therefore, if the Read transaction were to pass the Posted transaction, it would return stale data.

3. When the Relaxed Ordering Attribute bit is cleared, a Read completion must ‘‘pull’’ ahead of previously queued posted data transmitting in the same direction. In this case, the read data transmits in the same direction as the posted data, and the requestor of the read transaction is on the same side of the VPPB as the completer of the posted transaction. The posted transaction must deliver to the completer before the read data is returned to the requestor. If the Relaxed Ordering Attribute bit is set, then a read completion is permitted to pass a previously queued Memory Write or Message Request.

4. Non-Posted Write Completions are permitted to pass a previous Memory Write or Message Request transaction. Such transactions are actually transmitting in the opposite directions and hence have no ordering relationship.

5. Posted Request transactions must be given opportunities to pass Non-posted Read and Write Requests as well as Completions. Otherwise, deadlocks may occur when some older bridges, which do not support delayed transactions are mixed with PCIe Switch in the same system. A fairness algorithm is used to arbitrate between the Posted Write queue and the Non-posted transaction queue.

6.8 PORT ARBITRATION

Among multiple ingress ports, the port arbitration built in the egress port determines which incoming packets to be forwarded to the output port. The arbitration algorithm contains hardware fixed Round Robin, 128-phase Weighted Round-Robin and programmable 128-phase time-based WRR. The port arbitration is held within the same VC channel. It means that each port has two port arbitration circuitries for VC0 and VC1 respectively. At the upstream ports, in addition to the inter-port packets, the intra-port packet such as configurations completion would also join the arbitration loop to get the service from Virtual Channel 0.

6.9 VC ARBITRATION

After port arbitration, VC arbitration is executed among different VC channels within the same source. Three arbitration algorithms are provided to choose the appropriate VC: Strict Priority, Round Robin or Weighted Round Robin.

6.10 FLOW CONTROL

PCI Express employs Credit-Based Flow Control mechanism to make buffer utilization more efficient. The transaction layer transmitter ensures that it does not transmit a TLP to an opposite receiver unless the receiver has enough buffer space to accept the TLP. The transaction layer receiver has the responsibility to advertise the free buffer space to an opposite transmitter to avoid packet stale. In this Switch, each port has its own separate queues for different traffic types and the credits are sent to data link layer on the fly. The data link layer compares the current available credits with the monitored ones and reports the updated credit to the counterpart. If no new credit is acquired, the credit reported is scheduled for every 30 us to prevent the link from entering retrain. On the other hand, the receiver at each egress port gets the usable credits from the opposite end in a link. The output port broadcasts them to all the other ingress ports to get packet transmission.

6.11 TRANSATION LAYER TRANSMIT BLOCK (TLP ENCAPSULATION)

The transmit portion of transaction layer performs the following functions. They construct the all types of forwarded TLP generated from VC arbiter, respond with the completion packets when the local resource (i.e. configuration register) is accessed, and regenerate the message that terminates at receiver to RC if acting as an upstream port.

7 EEPROM INTERFACE AND SYSTEM MANAGEMENT BUS/I2C BUS

The EEPROM interface consists of four pins: EESK (EEPROM clock), EEDI (EEPROM serial data input), EEDO (EEPROM serial data output) and EECS (EEPROM chip select). The Switch may control a Microchip 25LC128 or compatible SPI EEPROM parts. The EEPROM is used to initialize a number of registers before enumeration. This is accomplished after PERST_L is de-asserted, at which time the data from the EEPROM is loaded. The EEPROM interface is organized into a 16-bit base, and the Switch supplies an 8-bit EEPROM word address.

The System Management Bus/I2C Bus interface consists of two pins: SCL_I2C (SMBUS/I2C Serial Clock input) and SDA_I2C (SMBUS/I2C Serial Data input/output).

7.1 EEPROM INTERFACE

7.1.1 AUTO MODE EEPROM ACCESS

The Switch may access the EEPROM in a WORD format by utilizing the auto mode through a hardware sequencer. The EEPROM start-control, address, and read/write commands can be accessed through the configuration register. Before each access, the software should check the Autoload Status bit before issuing the next start.

7.1.2 EEPROM NORMAL MODE AT RESET

During a reset, the Switch will automatically load the information/data from the EEPROM if the automatic load condition is met. The first offset in the EEPROM contains a signature. If the signature is recognized, the autoload initiates right after the reset.

During the autoload, the Bridge will read sequential words from the EEPROM and write to the appropriate registers. Before the Bridge registers can be accessed through the host, the autoload condition should be verified by reading bit [4] offset A0h (EEPROM Autoload Status). The host access is allowed only after the status of this bit is set to '1' which indicates that the autoload initialization sequence is complete.

7.1.3 EEPROM SPACE ADDRESS MAP

15 – 8	7 – 0	BYTE OFFSET
EEPROM Signature (1516h)		00h
Vendor ID		02h
Device ID		04h
Miscellaneous Parameter 0 for Port 0~5		06h
Subsystem Vender ID		08h
Subsystem ID		0Ah
Miscellaneous Parameter 1 for Port 0~5		0Ch
PHY TX Margin Parameter for Port 0~5		0Eh
PHY Parameter 0 for Port 0~5		10h
PHY Parameter 1 for Port 0~5		12h
PHY parameter 2/3 for Port 0~5		14h
XPIP_CSR4[15:0] for Port 0~5		16h
XPIP_CSR4[31:16] for Port 0~5		18h
XPIP_CSR5[15:0] for Port 0~5		1Ah
BUFFER_CTRL[4:0] for Port 0~5	XPIP_CSR5[23:16] for Port 0~5	1Ch
MAC_CTR/PHY Parameter 3 for Port 0~5		1Eh
XPIP_CSR2[14:12][10:0]/Deskew mode select for Port 0		20h
XPIP_CSR2[14:12][10:0]/Deskew mode select for Port 1		22h

15 – 8	7 – 0	BYTE OFFSET
XPIP_CSR2[14:12][10:0]/Deskew mode select for Port 2		24h
XPIP_CSR2[14:12][10:0]/Deskew mode select for Port 3		26h
XPIP_CSR2[14:12][10:0]/Deskew mode select for Port 4		28h
XPIP_CSR2[14:12][10:0]/Deskew mode select for Port 5		2Ah
Reserved		2Ch – 2Eh
PHY Parameter2[30:16] for Port 0		30h
PHY Parameter2[30:16] for Port 1		32h
PHY Parameter2[30:16] for Port 2		34h
PHY Parameter2[30:16] for Port 3		36h
PHY Parameter2[30:16] for Port 4		38h
PHY Parameter2[30:16] for Port 5		3Ah
Reserved		3Ch – 3Eh
PHY Parameter 2[12:8]/PHY Parameter 3[6:0]/Selectable De-emphasis/XPIP_CSR2[11]/TL_CSR[9:8] for Port 0		40h
PHY Parameter 2[12:8]/PHY Parameter 3[6:0]/Selectable De-emphasis/XPIP_CSR2[11]/TL_CSR[9:8] for Port 1		42h
PHY Parameter 2[12:8]/PHY Parameter 3[6:0]/Selectable De-emphasis/XPIP_CSR2[11]/TL_CSR[9:8] for Port 2		44h
PHY Parameter 2[12:8]/PHY Parameter 3[6:0]/Selectable De-emphasis/XPIP_CSR2[11]/TL_CSR[9:8] for Port 3		46h
PHY Parameter 2[12:8]/PHY Parameter 3[6:0]/Selectable De-emphasis/XPIP_CSR2[11]/TL_CSR[9:8] for Port 4		48h
PHY Parameter 2[12:8]/PHY Parameter 3[6:0]/Selectable De-emphasis/XPIP_CSR2[11]/TL_CSR[9:8] for Port 5		4Ah
Reserved		4Ch – 4Eh
PM Data for Port 0	PM Capability for Port 0	50h
PM Data for Port 1	PM Capability for Port 1	52h
PM Data for Port 2	PM Capability for Port 2	54h
PM Data for Port 3	PM Capability for Port 3	56h
PM Data for Port 4	PM Capability for Port 4	58h
PM Data for Port 5	PM Capability for Port 5	5Ah
Reserved		5Ch – 5Eh
TC/VC Map for Port 0 (VC0)	Slot Clock / LPVC Count / Port Num, Port 0	60h
TC/VC Map for Port 1 (VC0)	Slot Implemented / Slot Clock / LPVC Count / Port Num, Port 1	62h
TC/VC Map for Port 2 (VC0)	Slot Implemented / Slot Clock / LPVC Count / Port Num, Port 2	64h
TC/VC Map for Port 3 (VC0)	Slot Implemented / Slot Clock / LPVC Count / Port Num, Port 3	66h
TC/VC Map for Port 4 (VC0)	Slot Implemented / Slot Clock / LPVC Count / Port Num, Port 4	68h
TC/VC Map for Port 5 (VC0)	Slot Implemented / Slot Clock / LPVC Count / Port Num, Port 5	6Ah
Reserved		6Ch – 6Eh
Power Budgeting Capability Register for Port 0		70h
Power Budgeting Capability Register for Port 1		72h
Power Budgeting Capability Register for Port 2		74h
Power Budgeting Capability Register for Port 3		76h
Power Budgeting Capability Register for Port 4		78h
Power Budgeting Capability Register for Port 5		7Ah
Reserved		7Ch – 7Eh
XPIP_CSR5[31:24] for Port 0	PM Control Para/Rx Polarity/VGA Decode for Port 0	80h
XPIP_CSR5[31:24] for Port 1	PM Control Para/Rx Polarity/VGA Decode for Port 1	82h
XPIP_CSR5[31:24] for Port 2	PM Control Para/Rx Polarity/VGA Decode for Port 2	84h
XPIP_CSR5[31:24] for Port 3	PM Control Para/Rx Polarity/VGA Decode for Port 3	86h
XPIP_CSR5[31:24] for Port 4	PM Control Para/Rx Polarity/VGA Decode for Port 4	88h
XPIP_CSR5[31:24] for Port 5	PM Control Para/Rx Polarity/VGA Decode for Port 5	8Ah
Reserved		8Ch – 90h
Slot Capability 0 for Port 1		92h

15 – 8	7 – 0	BYTE OFFSET
Slot Capability 0 for Port 2		94h
Slot Capability 0 for Port 3		96h
Slot Capability 0 for Port 4		98h
Slot Capability 0 for Port 5		9Ah
Reserved		9Ch – A0h
Slot Capability 1 for Port 1		A2h
Slot Capability 1 for Port 2		A4h
Slot Capability 1 for Port 3		A6h
Slot Capability 1 for Port 4		A8h
Slot Capability 1 for Port 5		AAh
Reserved		ACh - AEh
XPIP_CSR3[15:0] for Port 0		B0h
XPIP_CSR3[15:0] for Port 1		B2h
XPIP_CSR3[15:0] for Port 2		B4h
XPIP_CSR3[15:0] for Port 3		B6h
XPIP_CSR3[15:0] for Port 4		B8h
XPIP_CSR3[15:0] for Port 5		BAh
Reserved		BCh - BEh
XPIP_CSR3[31:16] for Port 0		C0h
XPIP_CSR3[31:16] for Port 1		C2h
XPIP_CSR3[31:16] for Port 2		C4h
XPIP_CSR3[31:16] for Port 3		C6h
XPIP_CSR3[31:16] for Port 4		C8h
XPIP_CSR3[31:16] for Port 5		CAh
Reserved		CCh - CEh
REV_TS_CTR/Replay Time-out Counter for Port 0		D0h
REV_TS_CTR /Replay Time-out Counter for Port 1		D2h
REV_TS_CTR /Replay Time-out Counter for Port 2		D4h
REV_TS_CTR /Replay Time-out Counter for Port 3		D6h
REV_TS_CTR /Replay Time-out Counter for Port 4		D8h
REV_TS_CTR /Replay Time-out Counter for Port 5		DAh
Reserved		DCh - DEh
Acknowledge Latency Timer for Port 0		E0h
Acknowledge Latency Timer for Port 1		E2h
Acknowledge Latency Timer for Port 2		E4h
Acknowledge Latency Timer for Port 3		E6h
Acknowledge Latency Timer for Port 4		E8h
Acknowledge Latency Timer for Port 5		EAh
Reserved		ECh - EEh
XPIP_CSR6[23:16][11:10]/Device Specific PM Cap for Port 0		F0h
XPIP_CSR6[23:16][11:10]/Device Specific PM Cap for Port 1		F2h
XPIP_CSR6[23:16][11:10]/Device Specific PM Cap for Port 2		F4h
XPIP_CSR6[23:16][11:10]/Device Specific PM Cap for Port 3		F6h
XPIP_CSR6[23:16][11:10]/Device Specific PM Cap for Port 4		F8h
XPIP_CSR6[23:16][11:10]/Device Specific PM Cap for Port 5		FAh
Reserved		FCh - FEh
TC/VC Map for Port 0 (VC1)	VC1 MAX Time Slot for Port 0	100h
TC/VC Map for Port 1 (VC1)	VC1 MAX Time Slot for Port 1	102h
TC/VC Map for Port 2 (VC1)	VC1 MAX Time Slot for Port 2	104h
TC/VC Map for Port 3 (VC1)	VC1 MAX Time Slot for Port 3	106h
TC/VC Map for Port 4 (VC1)	VC1 MAX Time Slot for Port 4	108h
TC/VC Map for Port 5 (VC1)	VC1 MAX Time Slot for Port 5	10Ah
Reserved		10Ch – 10Eh
LTSSM_CSR for Port 0	Reserved	110h
LTSSM CSR for Port 1	Reserved	112h
LTSSM CSR for Port 2	Reserved	114h
LTSSM CSR for Port 3	Reserved	116h
LTSSM CSR for Port 4	Reserved	118h
LTSSM CSR for Port 5	Reserved	11Ah
Reserved		11Ch – 11Eh
Hotplug_CSR for Port 0		120h
Hotplug_CSR for Port 1		122h
Hotplug_CSR for Port 2		124h
Hotplug_CSR for Port 3		126h

15 – 8	7 – 0	BYTE OFFSET
Hotplug_CSR for Port 4		128h
Hotplug_CSR for Port 5		12Ah
Reserved		12Ch~12Eh
MAC_CSR1 for Port 0		130h
MAC_CSR1 for Port 1		132h
MAC_CSR1 for Port 2		134h
MAC_CSR1 for Port 3		136h
MAC_CSR1 for Port 4		138h
MAC_CSR1 for Port 5		13Ah
Reserved		13Ch~13Eh
CPLD Flow Control Enable		140h
X1 CPLD Flow Control Threshold		142h
X2 CPLD Flow Control Threshold		144h
X4 CPLD Flow Control Threshold		146h
Reserved		14Ch~14Eh
Power Saving Disable for Port0		150h
Power Saving Disable for Port1		152h
Power Saving Disable for Port4		154h
Power Saving Disable for Port5		156h
Power Saving Disable for Port7		158h
Power Saving Disable for Port9		15Ah
Reserved		15Ch~15Eh

7.1.4 MAPPING EEPROM CONTENTS TO CONFIGURATION REGISTERS

ADDRESS	PCI CFG OFFSET	DESCRIPTION
00h		**EEPROM signature** – 1516h
02h	**00h ~ 01h**	**Vendor ID**
04h	**02h ~ 03h**	**Device ID**
06h	**144h (Port 0~5)** 144h: Bit [0]	**Extended VC Count for Port 0~5** ▪ Bit [0]: it represents the supported VC count other than the default VC
	CCh (Port 0~5) CCh: Bit [14:12] CCh: Bit [17:15] CCh: Bit[18]	**Link Capability for Port 0~5** ▪ Bit [3:1]: it represents L0s Exit Latency for all ports ▪ Bit [6:4]: it represents L1 Exit Latency for all ports ▪ Bit [7]: clock pm capability for all ports
	74h (Port 0) 74h: Bit [5] 74h: Bit [6] 74h: Bit [0] 74h: Bit [2:1] 74h: Bit [3] 74h: Bit [4] 74h: Bit [7]	**Switch Mode Operation for Port 0** ▪ Bit [8]: no ordering on packets for different egress port mode ▪ Bit [9]: no ordering on different tag of completion mode ▪ Bit [10]: store and forward ▪ Bit [12:11]: cut-through threshold ▪ Bit [13]: port arbitrator mode ▪ Bit [14]: credit Update mode ▪ Bit [15]: non-post store and forward only mode
08h	**B4h ~ B5h**	**Subsystem Vender ID**
0Ah	**B6h ~ B7h**	**Subsystem ID**
0Ch	**C4h (Port 0~5)** C4h: Bit [1:0]	**Max_Payload_Size Support for Port 0~5** ▪ Bit [1:0]: indicate the maximum payload size that the device can support for the TLP
	CCh (Port 0~5) CCh: Bit[11:10]	**ASPM Support for Port 0~5** ▪ Bit [3:2] : indicate the level of ASPM supported on the PCIe link
	C4h (Port 0~5) C4h: Bit[15]	**Role_Base Error Reporting for Port 0~5** ▪ Bit [4] : indicate implement the role-base error reporting
	70h (Port 0~5) 70h: Bit [14]	**MSI Capability Disable for Port 0~5** ▪ Bit [5] : disable MSI capability
	74h (Port 0~5) 74h: Bit [15]	**Compliance Pattern Parity Control Disable for Port 0~5** ▪ Bit [6] : disable compliance pattern parity

ADDRESS	PCI CFG OFFSET	DESCRIPTION
	70h (Port 0~5) 70h: Bit [13]	**Power Management Capability Disable for Port 0~5** ▪ Bit [7] : disable power management capability
	8Ch (Port 0~5) 8Ch: Bit[5]	**ORDER RULE5 Enable for port 0~5** Bit[8]: capability for post packet pass non-post packet
	CCh (Port 1~5) CCh: Bit [21]	**Link Bandwidth Notification Capability for port 1~5** Bit [9]: link bandwidth notification capability
	8Ch(Port 0~5) 8Ch: Bit [6]	**Ordering Frozen for Port 0~5** ▪ Bit [10]: freeze the ordering feature
	8Ch (Port 0~5) 8Ch: Bit[0]	**TX SOF Latency Mode for Port 0~5** ▪ Bit [11]: set to zero to shorten latency
	CCh (Port 0~5) CCh: Bit [19]	**Surprise Down Capability Enable for Port 0~5** ▪ Bit [12]: enable surprise down capability
	8Ch (Port 0~5) 8Ch: Bit[1]	**Power Management's Data Select Register R/W Capability for Port 0~5** ▪ Bit [13]: enable Data Select Register R/W
	E4h (Port 0~5) E4h: Bit[12]	**Flow Control Update Type LTR Capability Enable for Port 0~5** ▪ Bit [14]: LTR capability enable
	8Ch (Port 0~5) 8Ch: Bit[3]	**4KB Boundary Check Enable for Port 0~5** ▪ Bit [15]: enable 4KB boundary check
0Eh	**94h (Port 0~5)** 94h: Bit[4:0] 94h: Bit[9:5] 94h: Bit[14:10]	**PHY TX Margin Parameter for Port 0~5** ▪ Bit[4:0]: C_DRV_LVL_3P5_MGN2 ▪ Bit[9:5]: C_DRV_LVL_6P0_MGN2 ▪ Bit[14:10]: C_DRV_LVL_HALF_MGN2
	E4h (Port 0~5) E4h: Bit [18]	**OBFF Capability Enable for Port 0~5** ▪ Bit [15]: enable OBFF capability
10h	**74h (Port 0~5)** 74h: Bit[20:16] 74h: Bit[25:21] 74h: Bit[30:26]	**PHY Parameter 0 for Port 0~5** ▪ Bit [4:0]: C_DRV_LVL_3P5_NOM ▪ Bit [9:5]: C_DRV_LVL_6P0_NOM ▪ Bit [14:10]: C_DRV_LVL_HALF_NOM
	8Ch (Port0~5) 8Ch: Bit[31]	**TL_CSR[31] for Port 0~5** ▪ Bit [15]: P35_GEN2_MODE
12h	**7Ah (Port 0~5)** 7Ah: Bit[4:0] 7Ah: Bit[9:5] 7Ah: Bit[14:10]	**PHY Parameter 1 for Port 0~5** ▪ Bit [4:0]: C_EMP_POST_GEN1_3P5_NOM ▪ Bit [9:5]: C_EMP_POST_GEN2_3P5_NOM ▪ Bit [14:10]: C_EMP_POST_GEN2_6P0_NOM
	3Ch (Port 1~5) 3Ch: Bit [8]	**Interrupt pin for Port 1~5** ▪ Bit [15]: set when INTA is requested for interrupt resource
14h	**7Ch (Port 0~5)** 7Ch: Bit[3:0] 7Ch: Bit[6:4]	**PHY Parameter 2 for Port 0~5** ▪ Bit [3:0]: C_TX_PHY_LATENCY ▪ Bit [6:4]: C_REC_DETECT_USEC
	90h (Port 0~5) 90h: Bit[19:15]	**PHY Parameter 3 for Port 0~5** ▪ Bit [11:7]: C_EMP_POST_HALF_DELTA
	8Ch (Port 0~5) 8Ch: Bit[2] 8Ch: Bit[7] 8Ch: bit[12]	**TL_CSR[2]|[7] for Port 0~5** ▪ Bit [12]: request abort select ▪ Bit [13]: grant fail to idle in port arbiter ▪ Bit [14]: ARB_VCFLG_SEL
16h	**84h (Port 0~5)** 84h: Bit[15:0]	**XPIP_CSR4[15:0] for Port 0~5** ▪ Bit[15:0]: XPIP_CSR4[15:0]
18h	**84h (Port 0~5)** 84h: Bit[31:16]	**XPIP_CSR4[31:16] for Port 0~5** ▪ Bit[15:0]: XPIP_CSR4[31:16]
1Ah	**88h (Port 0~5)** 88h: Bit[15:0]	**XPIP_CSR5[15:0] for Port 0~5** ▪ Bit[15:0]: XPIP_CSR5[15:0]
1Ch	**88h (Port 0~5)** 88h: Bit[23:16]	**XPIP_CSR5[23:16] for Port 0~5** ▪ Bit[7:0]: XPIP_CSR5[23:16]

ADDRESS	PCI CFG OFFSET	DESCRIPTION
	98h (Port 0~5) 98h: Bit[23:16]	**BUFFER_CTRL[7:0] for Port 0~5** ▪ Bit[15:8]: reference clock Buffer control
1Eh	**90h (Port 0~5)** 90h: Bit[21:20] 90h: Bit[23:22] 90h: Bit[25:24] 90h: Bit[27:26] 90h: Bit[29:28] 90h: Bit[31:30] **8Ch (Port 0~5)** 8Ch: Bit[29:26]	**PHY Parameter 3 for Port 0~5** ▪ Bit [1:0]: C_DRV_LVL_3P5_DELTA ▪ Bit [3:2]: C_DRV_LVL_6P0_DELTA ▪ Bit [5:4]: C_DRV_LVL_HALF_DELTA ▪ Bit [7:6]: C_EMP_POST_GEN1_3P5_DELTA ▪ Bit [9:8]: C_EMP_POST_GEN2_3P5_DELTA ▪ Bit [11:10]: C_EMP_POST_GEN2_6P0_DELTA **MAC Control Parameter for Port 0~5** ▪ Bit[15:12]: MAC_CTR
20h	**78h (Port 0)** 78h: Bit[7:0] **68h (Port 0)** 68h: Bit[14:13] **78h (Port 0)** 78h: Bit[9:8] 78h: Bit[10] 78h: Bit[13:12] 78h: Bit[14]	**FTS Number for Port 0** ▪ Bit [7:0]: FTS number at receiver side **Deskew Mode Select for Port 0** ▪ Bit [9:8]: deskew mode select **XPIP_CSR2[14:8] for Port 0** ▪ Bit [11:10]: scrambler control ▪ Bit [12]: L0s ▪ Bit[14:13]: change speed select ▪ Bit[15]: change speed enable
22h	**78h (Port 1)** 78h: Bit[7:0] **68h (Port 1)** 68h: Bit[14:13] **78h (Port 1)** 78h: Bit[9:8] 78h: Bit[10] 78h: Bit[13:12] 78h: Bit[14]	**FTS Number for Port 1** ▪ Bit [7:0]: FTS number at receiver side **Deskew Mode Select for Port 1** ▪ Bit [9:8]: deskew mode select **XPIP_CSR2[14:8] for Port 1** ▪ Bit [11:10]: scrambler control ▪ Bit [12]: L0s ▪ Bit[14:13]: change speed select ▪ Bit[15]: change speed enable
24h	**78h (Port 2)** 78h: Bit[7:0] **68h (Port 2)** 68h: Bit[14:13] **78h (Port 2)** 78h: Bit[9:8] 78h: Bit[10] 78h: Bit[13:12] 78h: Bit[14]	**FTS Number for Port 2** ▪ Bit [7:0]: FTS number at receiver side **Deskew Mode Select for Port 2** ▪ Bit [9:8]: deskew mode select **XPIP_CSR2[14:8] for Port 2** ▪ Bit [11:10]: scrambler control ▪ Bit [12]: L0s ▪ Bit[14:13]: change speed select ▪ Bit[15]: change speed enable
26h	**78h (Port 3)** 78h: Bit[7:0] **68h (Port 3)** 68h: Bit[14:13] **78h (Port 3)** 78h: Bit[9:8] 78h: Bit[10] 78h: Bit[13:12] 78h: Bit[14]	**FTS Number for Port 3** ▪ Bit [7:0]: FTS number at receiver side **Deskew Mode Select for Port 3** ▪ Bit [9:8]: deskew mode select **XPIP_CSR2[14:8] for Port 3** ▪ Bit [11:10]: scrambler control ▪ Bit [12]: L0s ▪ Bit[14:13]: change speed select ▪ Bit[15]: change speed enable
28h	**78h (Port 4)** 78h: Bit[7:0] **68h (Port 4)** 68h: Bit[14:13] **78h (Port 4)** 78h: Bit[9:8] 78h: Bit[10] 78h: Bit[13:12]	**FTS Number for Port 4** ▪ Bit [7:0]: FTS number at receiver side **Deskew Mode Select for Port 4** ▪ Bit [9:8]: deskew mode select **XPIP_CSR2[14:8] for Port 4** ▪ Bit [11:10]: scrambler control ▪ Bit [12]: L0s ▪ Bit[14:13]: change speed select

ADDRESS	PCI CFG OFFSET	DESCRIPTION
	78h: Bit[14]	▪ Bit[15]: change speed enable
2Ah	**78h (Port 5)** 78h: Bit[7:0] **68h (Port 5)** 68h: Bit[14:13] **78h (Port 5)** 78h: Bit[9:8] 78h: Bit[10] 78h: Bit[13:12] 78h: Bit[14]	**FTS Number for Port 5** ▪ Bit [7:0]: FTS number at receiver side **Deskew Mode Select for Port 5** ▪ Bit [9:8]: deskew mode select **XPIP_CSR2[14:8] for Port 5** ▪ Bit [11:10]: scrambler control ▪ Bit [12]: L0s ▪ Bit[14:13]: change speed select ▪ Bit[15]: change speed enable
30h	**7Ch (Port 0)** 7Ch: Bit[30:16]	**PHY Parameter 2[30:16] for Port 0** ▪ Bit [14:0]: PHY parameter 2
32h	**7Ch (Port 1)** 7Ch: Bit[30:16]	**PHY Parameter 2[30:16] for Port 1** ▪ Bit [14:0]: PHY parameter 2
34h	**7Ch (Port 2)** 7Ch: Bit[30:16]	**PHY Parameter 2[30:16] for Port 2** ▪ Bit [14:0]: PHY parameter 2
36h	**7Ch (Port 3)** 7Ch: Bit[30:16]	**PHY Parameter 2[30:16] for Port 3** ▪ Bit [14:0]: PHY parameter 2
38h	**7Ch (Port 4)** 7Ch: Bit[30:16]	**PHY Parameter 2[30:16] for Port 4** ▪ Bit [14:0]: PHY parameter 4
3Ah	**7Ch (Port 5)** 7Ch: Bit[30:16]	**PHY Parameter 2[30:16] for Port 5** ▪ Bit [14:0]: PHY parameter 5
40h	**7Ch (Port 0)** 7Ch: Bit[12:8] **90h (Port 0)** 90h: Bit[6:0] **78h (Port 0)** 78h: Bit[11] **8Ch (Port 0)** 8Ch: Bit[9:8]	**PHY Parameter 2[12:8] for Port 0** ▪ Bit [4:0]: PHY parameter 2 **PHY Parameter 3[6:0] for Port 0** ▪ Bit [11:5]: PHY parameter 3 **Compliance to Detect for Port 0** ▪ Bit [13]: compliance to detect **TL_CSR[9:8] for Port 0** ▪ Bit[15:14]: DO_CHG_DATA_CNT_SEL
42h	**7Ch (Port 1)** 7Ch: Bit[12:8] **90h (Port 1)** 90h: Bit[6:0] **F0h (Port 1)** F0h: Bit[6] **78h (Port 1)** 78h: Bit[11] **8Ch (Port 1)** 8Ch: Bit[9:8]	**PHY Parameter 2[12:8] for Port 1** ▪ Bit [4:0]: PHY parameter 2 **PHY Parameter 3[6:0] for Port 1** ▪ Bit [11:5]: PHY parameter 3 **Selectable De-emphasis for Port 1** ▪ Bit [12]: selectable De-emphasis **Compliance to Detect for Port 1** ▪ Bit [13]: compliance to detect **TL_CSR[9:8] for Port 1** ▪ Bit[15:14]: DO_CHG_DATA_CNT_SEL
44h	**7Ch (Port 2)** 7Ch: Bit[12:8] **90h (Port 2)** 90h: Bit[6:0] **F0h (Port 2)** F0h: Bit[6] **78h (Port 2)** 78h: Bit[11] **8Ch (Port 2)** 8Ch: Bit[9:8]	**PHY Parameter 2[12:8] for Port 2** ▪ Bit [4:0]: PHY parameter 2 **PHY Parameter 3[6:0] for Port 2** ▪ Bit [11:5]: PHY parameter 3 **Selectable De-emphasis for Port 2** ▪ Bit [12]: selectable De-emphasis **Compliance to Detect for Port 2** ▪ Bit [13]: compliance to detect **TL_CSR[9:8] for Port 2** ▪ Bit[15:14]: DO_CHG_DATA_CNT_SEL
46h	**7Ch (Port 3)** 7Ch: Bit[12:8] **90h (Port 3)**	**PHY Parameter 2[12:8] for Port 3** ▪ Bit [4:0]: PHY parameter 2 **PHY Parameter 3[6:0] for Port 3**

ADDRESS	PCI CFG OFFSET	DESCRIPTION
	90h: Bit[6:0]	▪ Bit [11:5]: PHY parameter 3
	F0h (Port 3) F0h: Bit[6]	**Selectable De-emphasis for Port 3** ▪ Bit [12]: selectable De-emphasis
	78h (Port 3) 78h: Bit[11]	**Compliance to Detect for Port 3** ▪ Bit [13]: compliance to detect
	8Ch (Port 3) 8Ch: Bit[9:8]	**TL_CSR[9:8] for Port 3** ▪ Bit[15:14]: DO_CHG_DATA_CNT_SEL
48h	**7Ch (Port 4)** 7Ch: Bit[12:8]	**PHY Parameter 2[12:8] for Port 4** ▪ Bit [4:0]: PHY parameter 2
	90h (Port 4) 90h: Bit[6:0]	**PHY Parameter 3[6:0] for Port 4** ▪ Bit [11:5]: PHY parameter 3
	F0h (Port 4) F0h: Bit[6]	**Selectable De-emphasis for Port 4** ▪ Bit [12]: selectable De-emphasis
	78h (Port 4) 78h: Bit[11]	**Compliance to Detect for Port 4** ▪ Bit [13]: compliance to detect
	8Ch (Port 4) 8Ch: Bit[9:8]	**TL_CSR[9:8] for Port 4** ▪ Bit[15:14]: DO_CHG_DATA_CNT_SEL
4Ah	**7Ch (Port 5)** 7Ch: Bit[12:8]	**PHY Parameter 2[12:8] for Port 5** ▪ Bit [4:0]: PHY parameter 2
	90h (Port 5) 90h: Bit[6:0]	**PHY Parameter 3[6:0] for Port 5** ▪ Bit [11:5]: PHY parameter 3
	F0h (Port 5) F0h: Bit[6]	**Selectable De-emphasis for Port 5** ▪ Bit [12]: selectable De-emphasis
	78h (Port 5) 78h: Bit[11]	**Compliance to Detect for Port 5** ▪ Bit [13]: compliance to detect
	8Ch (Port 5) 8Ch: Bit[9:8]	**TL_CSR[9:8] for Port 5** ▪ Bit[15:14]: DO_CHG_DATA_CNT_SEL
50h	**44h (Port 0)** 44h: Bit [3]	**No_Soft_Reset for Port 0** ▪ Bit [0]: No_Soft_Reset
	40h (Port 0) 40h: Bit [24:22] 40h: Bit [25] 40h: Bit [26] 40h: Bit [29:28]	**Power Management Capability for Port 0** ▪ Bit [3:1]: AUX Current ▪ Bit [4]: read only as 1 to indicate Bridge supports the D1 power management state ▪ Bit [5]: read only as 1 to indicate Bridge supports the D2 power management state ▪ Bit [7:6]: PME Support for D2 and D1 states
51h	**44h (Port 0)** 44h: Bit [31:24]	**Power Management Data for Port 0** ▪ Bit [15:8]: read only as Data register
52h	**44h (Port 1)** 44h: Bit [3]	**No_Soft_Reset for Port 1** ▪ Bit [0]: No_Soft_Reset
	40h (Port 1) 40h: Bit [24:22] 40h: Bit [25] 40h: Bit [26] 40h: Bit [29:28]	**Power Management Capability for Port 1** ▪ Bit [3:1]: AUX Current ▪ Bit [4]: read only as 1 to indicate Bridge supports the D1 power management state ▪ Bit [5]: read only as 1 to indicate Bridge supports the D2 power management state ▪ Bit [7:6]: PME Support for D2 and D1 states
53h	**44h (Port 1)** 44h: Bit [31:24]	**Power Management Data for Port 1** ▪ Bit [15:8]: read only as Data register

ADDRESS	PCI CFG OFFSET	DESCRIPTION
54h	**44h (Port 2)** 44h: Bit [3] **40h (Port 2)** 40h: Bit [24:22] 40h: Bit [25] 40h: Bit [26] 40h: Bit [29:28]	**No_Soft_Reset for Port 2** ▪ Bit [0]: No_Soft_Reset **Power Management Capability for Port 2** ▪ Bit [3:1]: AUX Current ▪ Bit [4]: read only as 1 to indicate Bridge supports the D1 power management state ▪ Bit [5]: read only as 1 to indicate Bridge supports the D2 power management state ▪ Bit [7:6]: PME Support for D2 and D1 states
55h	**44h (Port 2)** 44h: Bit [31:24]	**Power Management Data for Port 2** ▪ Bit [15:8]: read only as Data register
56h	**44h (Port 3)** 44h: Bit [3] **40h (Port 3)** 40h: Bit [24:22] 40h: Bit [25] 40h: Bit [26] 40h: Bit [29:28]	**No_Soft_Reset for Port 3** ▪ Bit [0]: No_Soft_Reset **Power Management Capability for Port 3** ▪ Bit [3:1]: AUX Current ▪ Bit [4]: read only as 1 to indicate Bridge supports the D1 power management state ▪ Bit [5]: read only as 1 to indicate Bridge supports the D2 power management state ▪ Bit [7:6]: PME Support for D2 and D1 states
57h	**44h (Port 3)** 44h: Bit [31:24]	**Power Management Data for Port 3** ▪ Bit [15:8]: read only as Data register
58h	**44h (Port 4)** 44h: Bit [3] **40h (Port 4)** 40h: Bit [24:22] 40h: Bit [25] 40h: Bit [26] 40h: Bit [29:28]	**No_Soft_Reset for Port 4** ▪ Bit [0]: No_Soft_Reset **Power Management Capability for Port 4** ▪ Bit [3:1]: AUX Current ▪ Bit [4]: read only as 1 to indicate Bridge supports the D1 power management state ▪ Bit [5]: read only as 1 to indicate Bridge supports the D2 power management state ▪ Bit [7:6]: PME Support for D2 and D1 states
59h	**44h (Port 4)** 44h: Bit [31:24]	**Power Management Data for Port 4** ▪ Bit [15:8]: read only as Data register
5Ah	**44h (Port 5)** 44h: Bit [3] **40h (Port 5)** 40h: Bit [24:22] 40h: Bit [25] 40h: Bit [26] 40h: Bit [29:28]	**No_Soft_Reset for Port 5** ▪ Bit [0]: No_Soft_Reset **Power Management Capability for Port 5** ▪ Bit [3:1]: AUX Current ▪ Bit [4]: read only as 1 to indicate Bridge supports the D1 power management state ▪ Bit [5]: read only as 1 to indicate Bridge supports the D2 power management state ▪ Bit [7:6]: PME Support for D2 and D1 states
5Bh	**44h (Port5)** 44h: Bit [31:24]	**Power Management Data for Port 5** ▪ Bit [15:8]: read only as Data register
60h	**D0h (Port 0)** D0h: Bit [28] **40h (Port 0)** 40h: Bit[21] **144h (Port 0)** 144h: Bit [4] **CCh (Port 0)** CCh: Bit [26:24]	**Slot Clock Configuration for Port 0** ▪ Bit [1]: when set, the component uses the clock provided on the connector **Device Specific Initialization for Port 0** ▪ Bit [2]: when set, the DSI is required **LPVC Count for Port 0** ▪ Bit [3]: when set, the VC1 is allocated to LPVC of Egress Port 0 **Port Number for Port 0** ▪ Bit [6:4]: it represents the logic port numbering for physical Port 0
	154h (Port 0) 154h: Bit [7:1]	**VC0 TC/VC Map for Port 0** ▪ Bit [15:9]: when set, it indicates the corresponding TC is mapped into VC0

ADDRESS	PCI CFG OFFSET	DESCRIPTION
62h	**C0h (Port1)** C0h: Bit [24]	**PCIe Capability Slot Implemented for Port 1** ▪ Bit [0]: when set, the slot is implemented for Port 1
	D0h (Port 1) D0h: Bit [28]	**Slot Clock Configuration for Port 1** ▪ Bit [1]: when set, the component uses the clock provided on the connector
	40h (Port 1) 40h: Bit[21]	**Device Specific Initialization for Port 1** ▪ Bit [2]: when set, the DSI is required
	144h (Port 1) 144h: Bit [4]	**LPVC Count for Port 1** ▪ Bit [3]: when set, the VC1 is allocated to LPVC of Egress Port 1
	CCh (Port 1) CCh: Bit [26:24]	**Port Number for Port 1** ▪ Bit [6:4]: it represents the logic port numbering for physical Port 1
	154h (Port 1) 154h: Bit [7:1]	**VC0 TC/VC Map for Port 1** ▪ Bit [15:9]: when set, it indicates the corresponding TC is mapped into VC0
64h	**C0h (Port 2)** C0h: Bit [24]	**PCIe Capability Slot Implemented for Port 2** ▪ Bit [0]: when set, the slot is implemented for Port 3
	D0h (Port 2) D0h: Bit [28]	**Slot Clock Configuration for Port 2** ▪ Bit [1]: when set, the component uses the clock provided on the connector
	40h (Port 2) 40h: Bit[21]	**Device Specific Initialization for Port 2** ▪ Bit [2]: when set, the DSI is required
	144h (Port 2) 144h: Bit [4]	**LPVC Count for Port 2** ▪ Bit [3]: when set, the VC1 is allocated to LPVC of Egress Port 3
	CCh (Port 2) CCh: Bit [26:24]	**Port Number for Port 2** ▪ Bit [6:4]: it represents the logic port numbering for physical Port 2
	154h (Port 2) 154h: Bit [7:1]	**VC0 TC/VC Map for Port 2** ▪ Bit [15:9]: when set, it indicates the corresponding TC is mapped into VC0
66h	**C0h (Port 3)** C0h: Bit [24]	**PCIe Capability Slot Implemented for Port 3** ▪ Bit [0]: when set, the slot is implemented for Port 3
	D0h (Port 3) D0h: Bit [28]	**Slot Clock Configuration for Port 3** ▪ Bit [1]: when set, the component uses the clock provided on the connector
	40h (Port 3) 40h: Bit[21]	**Device Specific Initialization for Port 3** ▪ Bit [2]: when set, the DSI is required
	144h (Port 3) 144h: Bit [4]	**LPVC Count for Port 3** ▪ Bit [3]: when set, the VC1 is allocated to LPVC of Egress Port 3
	CCh (Port 3) CCh: Bit [26:24]	**Port Number for Port 3** ▪ Bit [6:4]: it represents the logic port numbering for physical Port 3
	154h (Port 3) 154h: Bit [7:1]	**VC0 TC/VC Map for Port 3** ▪ Bit [15:9]: When set, it indicates the corresponding TC is mapped into VC0

ADDRESS	PCI CFG OFFSET	DESCRIPTION
68h	**C0h (Port 4)** C0h: Bit [24]	**PCIe Capability Slot Implemented for Port 4** ▪ Bit [0]: when set, the slot is implemented for Port 4
	D0h (Port 4) D0h: Bit [28]	**Slot Clock Configuration for Port 4** ▪ Bit [1]: when set, the component uses the clock provided on the connector
	40h (Port 4) 40h: Bit[21]	**Device Specific Initialization for Port 4** ▪ Bit [2]: when set, the DSI is required
	144h (Port 4) 144h: Bit [4]	**LPVC Count for Port 4** ▪ Bit [3]: when set, the VC1 is allocated to LPVC of Egress Port 4
	CCh (Port 4) CCh: Bit [26:24]	**Port Number for Port 4** ▪ Bit [6:4]: it represents the logic port numbering for physical Port 4
	154h (Port 4) 154h: Bit [7:1]	**VC0 TC/VC Map for Port 4** ▪ Bit [15:9]: When set, it indicates the corresponding TC is mapped into VC0
6Ah	**C0h (Port 5)** C0h: Bit [24]	**PCIe Capability Slot Implemented for Port 5** ▪ Bit [0]: when set, the slot is implemented for Port 5
	D0h (Port 5) D0h: Bit [28]	**Slot Clock Configuration for Port 5** ▪ Bit [1]: when set, the component uses the clock provided on the connector
	40h (Port 5) 40h: Bit[21]	**Device Specific Initialization for Port 5** ▪ Bit [2]: when set, the DSI is required
	144h (Port 5) 144h: Bit [4]	**LPVC Count for Port 5** ▪ Bit [3]: when set, the VC1 is allocated to LPVC of Egress Port 5
	CCh (Port 5) CCh: Bit [26:24]	**Port Number for Port 5** ▪ Bit [6:4]: it represents the logic port numbering for physical Port 5
	154h (Port53) 154h: Bit [7:1]	**VC0 TC/VC Map for Port 5** ▪ Bit [15:9]: When set, it indicates the corresponding TC is mapped into VC0
70h	**214h (Port 0)** 214h: Bit [7:0] 214h: Bit [9:8] 214h: Bit [14:13]	**Power Budgeting Data Register for Port 0** ▪ Bit [7:0]: base power ▪ Bit [9:8]: data scale ▪ Bit [11:10]: PM state
	218h (Port 0) 218h: Bit [0]	**Power Budget Capability Register for Port 0** ▪ Bit [15]: system allocated
72h	**214h (Port 1)** 214h: Bit [7:0] 214h: Bit [9:8] 214h: Bit [14:13]	**Power Budgeting Data Register for Port 1** ▪ Bit [7:0]: base power ▪ Bit [9:8]: data scale ▪ Bit [11:10]: PM state
	218h (Port 1) 218h: Bit [0]	**Power Budget Capability Register for Port 1** ▪ Bit [15]: system allocated
74h	**214h (Port 2)** 214h: Bit [7:0] 214h: Bit [9:8] 214h: Bit [14:13]	**Power Budgeting Data Register for Port 2** ▪ Bit [7:0]: base power ▪ Bit [9:8]: data scale ▪ Bit [11:10]: PM state
	218h (Port 2) 218h: Bit [0]	**Power Budget Capability Register for Port 2** ▪ Bit [15]: system allocated
76h	**214h (Port 3)** 214h: Bit [7:0] 214h: Bit [9:8] 214h: Bit [14:13]	**Power Budgeting Data Register for Port 3** ▪ Bit [7:0]: base power ▪ Bit [9:8]: data scale ▪ Bit [11:10]: PM state
	218h (Port 3) 218h: Bit [0]	**Power Budget Capability Register for Port 3** ▪ Bit [15]: system allocated

ADDRESS	PCI CFG OFFSET	DESCRIPTION
78h	**214h (Port 4)** 214h: Bit [7:0] 214h: Bit [9:8] 214h: Bit [14:13] **218h (Port 4)** 218h: Bit [0]	**Power Budgeting Data Register for Port 4** ▪ Bit [7:0]: base power ▪ Bit [9:8]: data scale ▪ Bit [11:10]: PM state **Power Budget Capability Register for Port 4** ▪ Bit [15]: system allocated
7Ah	**214h (Port 5)** 214h: Bit [7:0] 214h: Bit [9:8] 214h: Bit [14:13] **218h (Port 5)** 218h: Bit [0]	**Power Budgeting Data Register for Port 5** ▪ Bit [7:0]: base power ▪ Bit [9:8]: data scale ▪ Bit [11:10]: PM state **Power Budget Capability Register for Port 5** ▪ Bit [15]: system allocated
80h	**74h (Port 0)** 74h: Bit [14] 74h: Bit [13:8] **70h (Port 0)** 70h: Bit[31] **88h (Port 0)** 88h: Bit[31:24]	**PM Control Parameter for Port 0** ▪ Bit [6] : disable Rx polarity capability ▪ Bit [5:4] : L0s enable ▪ Bit [3:2] : L1 delay count select ▪ Bit [1:0] : D3 enters L1 **VGA Decode Enable for Port 0** ▪ Bit [7] : enable VGA decode **XPIP_CSR5[31:24] for Port 0** ▪ Bit[15:8]: XPIP_CSR5[31:24]
82h	**74h (Port 1)** 74h: Bit [14] 74h: Bit [13:8] **70h (Port 1)** 70h: Bit[31] **88h (Port 1)** 88h: Bit[31:24]	**PM Control Parameter for Port 1** ▪ Bit [6] : disable Rx polarity capability ▪ Bit [5:4] : L0s enable ▪ Bit [3:2] : L1 delay count select ▪ Bit [1:0] : D3 enters L1 **VGA Decode Enable for Port 1** ▪ Bit [7] : enable VGA decode **XPIP_CSR5[31:24] for Port 1** ▪ Bit[15:8]: XPIP_CSR5[31:24]
84h	**74h (Port 2)** 74h: Bit [14] 74h: Bit [13:8] **70h (Port 2)** 70h: Bit[31] **88h (Port 2)** 88h: Bit[31:24]	**PM Control Parameter for Port 2** ▪ Bit [6] : disable Rx polarity capability ▪ Bit [5:4] : L0s enable ▪ Bit [3:2] : L1 delay count select ▪ Bit [1:0] : D3 enters L1 **VGA Decode Enable for Port 2** ▪ Bit [7] : enable VGA decode **XPIP_CSR5[31:24] for Port 2** ▪ Bit[15:8]: XPIP_CSR5[31:24]
86h	**74h (Port 3)** 74h: Bit [14] 74h: Bit [13:8] **70h (Port 3)** 70h: Bit[31] **88h (Port 3)** 88h: Bit[31:24]	**PM Control Parameter for Port 3** ▪ Bit [6] : disable Rx polarity capability ▪ Bit [5:4] : L0s enable ▪ Bit [3:2] : L1 delay count select ▪ Bit [1:0] : D3 enters L1 **VGA Decode Enable for Port 3** ▪ Bit [7] : enable VGA decode **XPIP_CSR5[31:24] for Port 3** ▪ Bit[15:8]: XPIP_CSR5[31:24]

ADDRESS	PCI CFG OFFSET	DESCRIPTION
88h	**74h (Port 4)** 74h: Bit [14] 74h: Bit [13:8] **70h (Port 4)** 70h: Bit[31] **88h (Port 4)** 88h: Bit[31:24]	**PM Control Parameter for Port 4** ▪ Bit [6] : disable Rx polarity capability ▪ Bit [5:4] : L0s enable ▪ Bit [3:2] : L1 delay count select ▪ Bit [1:0] : D3 enters L1 **VGA Decode Enable for Port 4** ▪ Bit [7] : enable VGA decode **XPIP_CSR5[31:24] for Port 4** ▪ Bit[15:8]: XPIP_CSR5[31:24]
8Ah	**74h (Port 5)** 74h: Bit [14] 74h: Bit [13:8] **70h (Port 5)** 70h: Bit[31] **88h (Port 5)** 88h: Bit[31:24]	**PM Control Parameter for Port 5** ▪ Bit [6] : disable Rx polarity capability ▪ Bit [5:4] : L0s enable ▪ Bit [3:2] : L1 delay count select ▪ Bit [1:0] : D3 enters L1 **VGA Decode Enable for Port 5** ▪ Bit [7] : enable VGA decode **XPIP_CSR5[31:24] for Port 5** ▪ Bit[15:8]: XPIP_CSR5[31:24]
92h	**D4h (Port 1)** D4h: Bit [15:0]	**Slot Capability 0 of Port 1** ▪ Bit [15:0]: Mapping to the low word of slot capability register
94h	**D4h (Port 2)** D4h: Bit [15:0]	**Slot Capability 0 of Port 2** ▪ Bit [15:0]: Mapping to the low word of slot capability register
96h	**D4h (Port 3)** D4h: Bit [15:0]	**Slot Capability 0 of Port 3** ▪ Bit [15:0]: Mapping to the low word of slot capability register
98h	**D4h (Port 4)** D4h: Bit [15:0]	**Slot Capability 0 of Port 4** ▪ Bit [15:0]: Mapping to the low word of slot capability register
9Ah	**D4h (Port 5)** D4h: Bit [15:0]	**Slot Capability 0 of Port 5** ▪ Bit [15:0]: Mapping to the low word of slot capability register
A2h	**D4h (Port 1)** D4h: Bit [31:16]	**Slot Capability 1 of Port 1** ▪ Bit [15:0]: Mapping to the high word of slot capability register
A4h	**D4h (Port 2)** D4h: Bit [31:16]	**Slot Capability 1 of Port 2** ▪ Bit [15:0]: Mapping to the high word of slot capability register
A6h	**D4h (Port 3)** D4h: Bit [31:16]	**Slot Capability 1 of Port 3** ▪ Bit [15:0]: Mapping to the high word of slot capability register
A8h	**D4h (Port 4)** D4h: Bit [31:16]	**Slot Capability 1 of Port 4** ▪ Bit [15:0]: Mapping to the high word of slot capability register
AAh	**D4h (Port 5)** D4h: Bit [31:16]	**Slot Capability 1 of Port 5** ▪ Bit [15:0]: Mapping to the high word of slot capability register
B0h	**80h (Port 0)** 80h: Bit[15:0]	**XPIP_CSR3[15:0] for Port 0** ▪ Bit[15:0]: XPIP_CSR3[15:0]
B2h	**80h (Port 1)** 80h: Bit[15:0]	**XPIP_CSR3[15:0] for Port 1** ▪ Bit[15:0]: XPIP_CSR3[15:0]
B4h	**80h (Port 2)** 80h: Bit[15:0]	**XPIP_CSR3[15:0] for Port 2** ▪ Bit[15:0]: XPIP_CSR3[15:0]
B6h	**80h (Port 3)** 80h: Bit[15:0]	**XPIP_CSR3[15:0] for Port 3** ▪ Bit[15:0]: XPIP_CSR3[15:0]
B8h	**80h (Port 4)** 80h: Bit[15:0]	**XPIP_CSR3[15:0] for Port 4** ▪ Bit[15:0]: XPIP_CSR3[15:0]
BAh	**80h (Port 5)** 80h: Bit[15:0]	**XPIP_CSR3[15:0] for Port 5** ▪ Bit[15:0]: XPIP_CSR3[15:0]
C0h	**80h (Port 0)** 80h: Bit[31:16]	**XPIP_CSR3[31:16] for Port 0** ▪ Bit[15:0]: XPIP_CSR3[31:16]
C2h	**80h (Port 1)** 80h: Bit[31:16]	**XPIP_CSR3[31:16] for Port 1** ▪ Bit[15:0]: XPIP_CSR3[31:16]
C4h	**80h (Port 2)** 80h: Bit[31:16]	**XPIP_CSR3[31:16] for Port 2** ▪ Bit[15:0]: XPIP_CSR3[31:16]
C6h	**80h (Port 3)** 80h: Bit[31:16]	**XPIP_CSR3[31:16] for Port 3** ▪ Bit[15:0]: XPIP_CSR3[31:16]
C8h	**80h (Port 4)** 80h: Bit[31:16]	**XPIP_CSR3[31:16] for Port 4** ▪ Bit[15:0]: XPIP_CSR3[31:16]
CAh	**80h (Port 5)** 80h: Bit[31:16]	**XPIP_CSR3[31:16] for Port 5** ▪ Bit[15:0]: XPIP_CSR3[31:16]

ADDRESS	PCI CFG OFFSET	DESCRIPTION
D0h	**70h (Port 0)** 70h: Bit [11:0] 70h: Bit [12] **8Ch (Port 0)** 8Ch: Bit[25:24]	**Replay Time-out Counter for Port 0** ▪ Bit [11:0]: replay time-out counter ▪ Bit [12]: enable user replay time-out timer **REV_TS_CTR for Port 0** ▪ Bit[14:13] REV_TS_CTR
D2h	**70h (Port 1)** 70h: Bit [11:0] 70h: Bit[12] **8Ch (Port 1)** 8Ch: Bit[25:24]	**Replay Time-out Counter for Port 1** ▪ Bit [11:0]: relay time-out counter ▪ Bit [12]: enable user replay time-out timer **REV_TS_CTR for Port 1** ▪ Bit[14:13] REV_TS_CTR
D4h	**70h (Port 2)** 70h: Bit [11:0] 70h: Bit[12] **8Ch (Port 2)** 8Ch: Bit[25:24]	**Replay Time-out Counter for Port 2** ▪ Bit [11:0]: relay time-out counter ▪ Bit [12]: enable user replay time-out timer **REV_TS_CTR for Port 2** ▪ Bit[14:13] REV_TS_CTR
D6h	**70h (Port 3)** 70h: Bit [11:0] 70h: Bit[12] **8Ch (Port 3)** 8Ch: Bit[25:24]	**Replay Time-out Counter for Port 3** ▪ Bit [11:0]: relay time-out counter ▪ Bit [12]: enable user replay time-out timer **REV_TS_CTR for Port 3** ▪ Bit[14:13] REV_TS_CTR
D8h	**70h (Port 4)** 70h: Bit [11:0] 70h: Bit[12] **8Ch (Port 4)** 8Ch: Bit[25:24]	**Replay Time-out Counter for Port 4** ▪ Bit [11:0]: relay time-out counter ▪ Bit [12]: enable user replay time-out timer **REV_TS_CTR for Port 4** ▪ Bit[14:13] REV_TS_CTR
DAh	**70h (Port 5)** 70h: Bit [11:0] 70h: Bit[12] **8Ch (Port 5)** 8Ch: Bit[25:24]	**Replay Time-out Counter for Port 5** ▪ Bit [11:0]: relay time-out counter ▪ Bit [12]: enable user replay time-out timer **REV_TS_CTR for Port 5** ▪ Bit[14:13] REV_TS_CTR
E0h	**70h (Port 0)** 70h: Bit [29:16] 70h: Bit [30]	**Acknowledge Latency Timer for Port 0** ▪ Bit [13:0]: acknowledge latency timer ▪ Bit [14]: enable user acknowledge latency timer
E2h	**70h (Port 1)** 70h: Bit [29:16] 70h: Bit [30]	**Acknowledge Latency Timer for Port 1** ▪ Bit [13:0]: acknowledge latency timer ▪ Bit [14]: enable user acknowledge latency timer
E4h	**70h (Port 2)** 70h: Bit [29:16] 70h: Bit [30]	**Acknowledge Latency Timer for Port 2** ▪ Bit [13:0]: acknowledge latency timer ▪ Bit [14]: enable user acknowledge latency timer
E6h	**70h (Port 3)** 70h: Bit [29:16] 70h: Bit [30]	**Acknowledge Latency Timer for Port 3** ▪ Bit [13:0]: acknowledge latency timer ▪ Bit [14]: enable user acknowledge latency timer
E8h	**70h (Port 4)** 70h: Bit [29:16] 70h: Bit [30]	**Acknowledge Latency Timer for Port 4** ▪ Bit [13:0]: acknowledge latency timer ▪ Bit [14]: enable user acknowledge latency timer
EAh	**70h (Port 5)** 70h: Bit [29:16] 70h: Bit [30]	**Acknowledge Latency Timer for Port 5** ▪ Bit [13:0]: acknowledge latency timer ▪ Bit [14]: enable user acknowledge latency timer
F0h	**8Ch (Port 0)** 8Ch: Bit[23:16] 8Ch: Bit[10] **8Ch (Port 0)** 8Ch: Bit[11]	**XPIP_CSR6[23:16][10] for Port 0** ▪ Bit[7:0]: XPIP_CSR6[7:0] ▪ Bit[12]: port disable **XPIP_CSR[11] for Port 0** ▪ Bit[14]: reset sel

ADDRESS	PCI CFG OFFSET	DESCRIPTION
F2h	**8Ch (Port 1)** 8Ch: Bit[23:16] 8Ch: Bit[10] **9Ch (Port 1)** 9Ch: Bit[0] **8Ch (Port 1)** 8Ch: Bit[11]	**XPIP_CSR6[23:16][10] for Port 1** ▪ Bit[7:0]: XPIP_CSR6[7:0] ▪ Bit[12]: port disable **Device Specific PM Capability for Port 1** ▪ Bit[13]: device specific PM capability **XPIP_CSR[11] Port 1** ▪ Bit[14]: reset sel
F4h	**8Ch (Port 2)** 8Ch: Bit[23:16] 8Ch: Bit[10] **9Ch (Port 2)** 9Ch: Bit[0] **8Ch (Port 2)** 8Ch: Bit[11]	**XPIP_CSR6[23:16][10] for Port 2** ▪ Bit[7:0]: XPIP_CSR6[7:0] ▪ Bit[12]: port disable **Device Specific PM Capability for Port 2** ▪ Bit[13]: device specific PM capability **XPIP_CSR[11] for Port 2** ▪ Bit[14]: reset sel
F6h	**8Ch (Port 3)** 8Ch: Bit[23:16] 8Ch: Bit[10] **9Ch (Port 3)** 9Ch: Bit[0] **8Ch (Port 3)** 8Ch: Bit[11]	**XPIP_CSR6[23:16][10] for Port 3** ▪ Bit[7:0]: XPIP_CSR6[7:0] ▪ Bit[12]: port disable **Device Specific PM Capability for Port 3** ▪ Bit[13]: device specific PM capability **XPIP_CSR[11] for Port 3** ▪ Bit[14]: reset sel
F8h	**8Ch (Port 4)** 8Ch: Bit[23:16] 8Ch: Bit[10] **9Ch (Port 4)** 9Ch: Bit[0] **8Ch (Port 4)** 8Ch: Bit[11]	**XPIP_CSR6[23:16][10] for Port 4** ▪ Bit[7:0]: XPIP_CSR6[7:0] ▪ Bit[12]: port disable **Device Specific PM Capability for Port 4** ▪ Bit[13]: device specific PM capability **XPIP_CSR[11] for Port 4** ▪ Bit[14]: reset sel
FAh	**8Ch (Port 5)** 8Ch: Bit[23:16] 8Ch: Bit[10] **9Ch (Port 5)** 9Ch: Bit[0] **8Ch (Port 5)** 8Ch: Bit[11]	**XPIP_CSR6[23:16][10] for Port 5** ▪ Bit[7:0]: XPIP_CSR6[7:0] ▪ Bit[12]: port disable **Device Specific PM Capability for Port 5** ▪ Bit[13]: device specific PM capability **XPIP_CSR[11] for Port 5** ▪ Bit[14]: reset sel
100h	**15Ch (Port 0)** 15Ch: Bit [22:16] **160h (Port 0)** 160h: Bit [7:0]	**VC1 MAX Time Slot for Port 0** ▪ Bit [6:0]: the maximum time slot supported by VC1 **TC/VC Map for Port 0** ▪ Bit [15:8]: when set, it indicates the corresponding TC is mapped into VC1
102h	**15Ch (Port 1)** 15Ch: Bit [22:16] **160h (Port 1)** 160h: Bit [7:0]	**VC1 MAX Time Slot for Port 1** ▪ Bit [6:0]: the maximum time slot supported by VC1 **TC/VC Map for Port 1** ▪ Bit [15:8]: when set, it indicates the corresponding TC is mapped into VC1
104h	**15Ch (Port 2)** 15Ch: Bit [22:16] **160h (Port 2)** 160h: Bit [7:0]	**VC1 MAX Time Slot for Port 2** ▪ Bit [6:0]: the maximum time slot supported by VC1 **TC/VC Map for Port 2** ▪ Bit [15:8]: when set, it indicates the corresponding TC is mapped into VC1

ADDRESS	PCI CFG OFFSET	DESCRIPTION
106h	**15Ch (Port 3)** 15Ch: Bit [22:16] **160h (Port 3)** 160h: Bit [7:0]	**VC1 MAX Time Slot for Port 3** ▪ Bit [6:0]: the maximum time slot supported by VC1 **TC/VC Map for Port 3** ▪ Bit [15:8]: when set, it indicates the corresponding TC is mapped into VC1
108h	**15Ch (Port 4)** 15Ch: Bit [22:16] **160h (Port 4)** 160h: Bit [7:0]	**VC1 MAX Time Slot for Port 4** ▪ Bit [6:0]: the maximum time slot supported by VC1 **TC/VC Map for Port 4** ▪ Bit [15:8]: when set, it indicates the corresponding TC is mapped into VC1
10Ah	**15Ch (Port 5)** 15Ch: Bit [22:16] **160h (Port 5)** 160h: Bit [7:0]	**VC1 MAX Time Slot for Port 5** ▪ Bit [6:0]: the maximum time slot supported by VC1 **TC/VC Map for Port 5** ▪ Bit [15:8]: when set, it indicates the corresponding TC is mapped into VC1
110h	**98h (Port 0)** 98h: Bit[27:24] **244h (Port 0)** 244h: Bit[1] 244h: Bit[3] 244h: Bit[4] **33Ch (Port 0)** 33Ch: Bit[7:0]	**L1 PM CSR for Port 0** ▪ Bit[3:0]: L1 PM option[3:0] **L1 PM Substates Capability for Port 0** ▪ Bit[4]: pci_pm_L1.1 sup ▪ Bit[5]: aspm_pm_L1.1 sup ▪ Bit[6]: L1pm_substate_sup **LTSSM _CSR for Port 0** ▪ Bit[15:8]: ltssm_csr
112h	**98h (Port 1)** 98h: Bit[27:24] **244h (Port 1)** 244h: Bit[1] 244h: Bit[3] 244h: Bit[4] **33Ch (Port 1)** 33Ch: Bit[7:0]	**L1 PM CSR for Port 1** ▪ Bit[3:0]: L1 PM option[3:0] **L1 PM Substates Capability for Port 1** ▪ Bit[4]: pci_pm_L1.1 sup ▪ Bit[5]: aspm_pm_L1.1 sup ▪ Bit[6]: L1pm_substate_sup **LTSSM _CSR for Port 1** ▪ Bit[15:8]: ltssm_csr
114h	**98h (Port 2)** 98h: Bit[27:24] **244h (Port 2)** 244h: Bit[1] 244h: Bit[3] 244h: Bit[4] **33Ch (Port 2)** 33Ch: Bit[7:0]	**L1 PM CSR for Port 2** ▪ Bit[3:0]: L1 PM option[3:0] **L1 PM Substates Capability for Port 2** ▪ Bit[4]: pci_pm_L1.1 sup ▪ Bit[5]: aspm_pm_L1.1 sup ▪ Bit[6]: L1pm_substate_sup **LTSSM _CSR for Port 2** ▪ Bit[15:8]: ltssm_csr
116h	**98h (Port 3)** 98h: Bit[27:24] **244h (Port 3)** 244h: Bit[1] 244h: Bit[3] 244h: Bit[4] **33Ch (Port 3)** 33Ch: Bit[7:0]	**L1 PM CSR for Port 3** ▪ Bit[3:0]: L1 PM option[3:0] **L1 PM Substates Capability for Port 3** ▪ Bit[4]: pci_pm_L1.1 sup ▪ Bit[5]: aspm_pm_L1.1 sup ▪ Bit[6]: L1pm_substate_sup **LTSSM _CSR for Port 3** ▪ Bit[10:8]: ltssm_csr

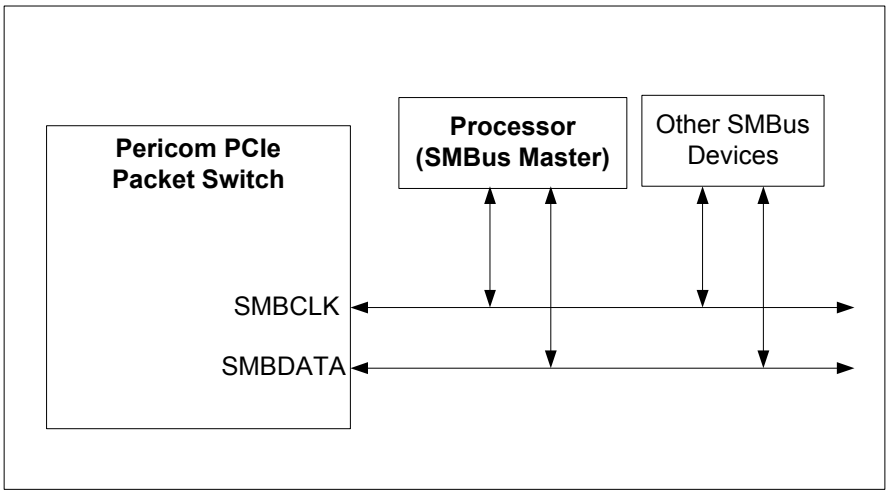
ADDRESS	PCI CFG OFFSET	DESCRIPTION
118h	**98h (Port 4)** 98h: Bit[27:24] **244h (Port 4)** 244h: Bit[1] 244h: Bit[3] 244h: Bit[4] **33Ch (Port 4)** 33Ch: Bit[7:0]	**L1 PM CSR for Port 4** ▪ Bit[3:0]: L1 PM option[3:0] **L1 PM Substates Capability for Port 4** ▪ Bit[4]: pci_pm_L1.1 sup ▪ Bit[5]: aspm_pm_L1.1 sup ▪ Bit[6]: L1pm_substate_sup **LTSSM _CSR for Port 4** ▪ Bit[15:8]: ltssm_csr
11Ah	**98h (Port 5)** 98h: Bit[27:24] **244h (Port 5)** 244h: Bit[1] 244h: Bit[3] 244h: Bit[4] **33Ch (Port 5)** 33Ch: Bit[7:0]	**L1 PM CSR for Port 5** ▪ Bit[3:0]: L1 PM option[3:0] **L1 PM Substates Capability for Port 5** ▪ Bit[4]: pci_pm_L1.1 sup ▪ Bit[5]: aspm_pm_L1.1 sup ▪ Bit[6]: L1pm_substate_sup **LTSSM _CSR for Port 5** ▪ Bit[10:8]: ltssm_csr
120h	**340h (Port 0)** 340h: Bit [15:0]	**Hotplug_CSR for Port 0** ▪ Bit [15:0]: hotplug csr
122h	**340h (Port 1)** 340h: Bit [15:0]	**Hotplug_CSR for Port 1** ▪ Bit [15:0]: hotplug csr
124h	**340h (Port 2)** 340h: Bit [15:0]	**Hotplug_CSR for Port 2** ▪ Bit [15:0]: hotplug csr
126h	**340h (Port 3)** 340h: Bit [15:0]	**Hotplug_CSR for Port 3** ▪ Bit [15:0]: hotplug csr
128h	**340h (Port 4)** 340h: Bit [15:0]	**Hotplug_CSR for Port 4** ▪ Bit [15:0]: hotplug csr
12Ah	**340h (Port 5)** 340h: Bit [15:0]	**Hotplug_CSR for Port 5** ▪ Bit [15:0]: hotplug csr
130h	**340h (Port 0)** 340h: Bit [31:16]	**MAC_CSR1 for Port 0** ▪ Bit [15:0]: mac csr1
132h	**340h (Port 1)** 340h: Bit [31:16]	**MAC_CSR1 for Port 1** ▪ Bit [15:0]: mac csr1
134h	**340h (Port 2)** 340h: Bit [31:16]	**MAC_CSR1 for Port 2** ▪ Bit [15:0]: mac csr1
136h	**340h (Port 3)** 340h: Bit [31:16]	**MAC_CSR1 for Port 3** ▪ Bit [15:0]: mac csr1
138h	**340h (Port 4)** 340h: Bit [31:16]	**MAC_CSR1 for Port 4** ▪ Bit [15:0]: mac csr1
13Ah	**340h (Port 5)** 340h: Bit [31:16]	**MAC_CSR1 for Port 5** ▪ Bit [15:0]: mac csr1
140h	**350h (Port 1~5)** 350h: Bit [5:1]	**CPLD Flow Control Enable for Port 1~5** ▪ Bit [1]: Port 1 CPLD flow control enable ▪ Bit [2]: Port 4 CPLD flow control enable ▪ Bit [3]: Port 5 CPLD flow control enable ▪ Bit [4]: Port 7 CPLD flow control enable ▪ Bit [5]: Port 9 CPLD flow control enable
142h	**354h (Port 1~5)** 354h: Bit [15:0]	**X1 CPLD Flow Control Threshold for Port 1~5** ▪ Bit [15:0]: x1 CPLD flow control threshold
144h	**354h (Port 1~5)** 354h: Bit [31:16]	**X2 CPLD Flow Control Threshold for Port 1~5** ▪ Bit [15:0]: x2 CPLD flow control threshold
146h	**358h (Port 1~5)** 358h: Bit [15:0]	**X4 CPLD Flow Control Threshold for Port 1~5** ▪ Bit [15:0]: x4 CPLD flow control threshold
150h	**360h (Port 0)** 360h: Bit [0]	**PWR_SAVING Disable for Port 0** ▪ Bit [0]: pwr_saving disable for Port 0
152h	**360h (Port 1)** 360h: Bit [0]	**PWR_SAVING Disable for Port 1** ▪ Bit [0]: pwr_saving disable for Port 1
154h	**360h (Port 2)** 360h: Bit [0]	**PWR_SAVING Disable for Port 2** ▪ Bit [0]: pwr_saving disable for Port 2
156h	**360h (Port 3)** 360h: Bit [0]	**PWR_SAVING Disable for Port 3** ▪ Bit [0]: pwr_saving disable for Port 3
158h	**360h (Port 4)** 360h: Bit [0]	**PWR_SAVING Disable for Port 4** ▪ Bit [0]: pwr_saving disable for Port 4

ADDRESS	PCI CFG OFFSET	DESCRIPTION
15Ah	**360h (Port 5)** 360h: Bit [0]	**PWR_SAVING Disable for Port 5** ▪ Bit [0]: pwr_saving disable for Port 5

7.2 SMBUS INTERFACE

The Packet Switch provides the System Management Bus (SMBus), a two-wire interface through which a simple device can communicate with the rest of the system. The SMBus interface on the Packet Switch is a bi-directional slave interface. It can receive data from the SMBus master or send data to the master. The interface allows full access to the configuration registers. A SMBus master, such as the processor or other SMBus devices, can read or write to every RW configuration register (read/write register). In addition, the RO and HwInt registers (read-only and hardware initialized registers) that can be auto-loaded by the EEPROM interface can also be read and written by the SMBus interface. This feature allows increases in the system expandability and flexibility in system implementation.

Figure 7-1 SMBus Architecture Implementation



The SMBus interface on the Packet Switch consists of one SMBus clock pin (SCL_I2C), a SMBus data pin (SDA_I2C), and 3 SMBus address pins (I2C_ADDR[2:0]). The SMBus clock pin provides or receives the clock signal. The SMBus data pin facilitates the data transmission and reception. Both of the clock and data pins are bi-directional. The SMBus address pins determine the address to which the Packet Switch responds to. The SMBus address pins generate addresses according to the following table:

Table 7-1 SMBus Address Pin Configuration

BIT	SMBus Address
0	I2C_ADDR[0]
1	I2C_ADDR[1]
2	I2C_ADDR[2]
3	1
4	0
5	1
6	1

Software can change the SMBus Slave address, by programming the SMBus/I2C Control Register SMBus/I2C Device Address field (Upstream Port, offset 344h [7:1]).

The PI7C9X2G606PR SMBus Slave interface supports three command protocols for register access:

- Block Write
- Block Read
- Block Read - Block Write Process Call

The PI7C9X2G606PR also supports Packet Error Checking and Packet Error Code (PEC) generation, as explained in the SMBus v2.0.

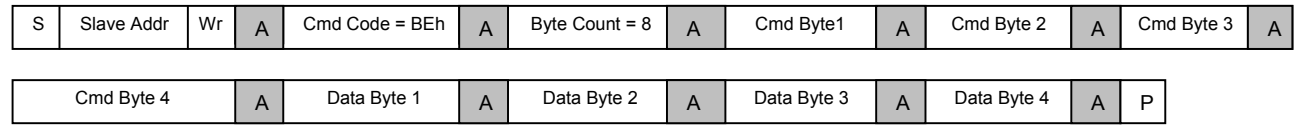
PI7C9X2G606PR supports three commands:

- Block Write (command BEh) is used to write CFG registers
- Block Write (command BAh), followed by Block Read (command BDh), are used to read CFG registers
- Block Read - Block Write Process Call (commands BAh, CDh) can also be used to read CFG registers

7.2.1 SMBUS BLOCK WRITE

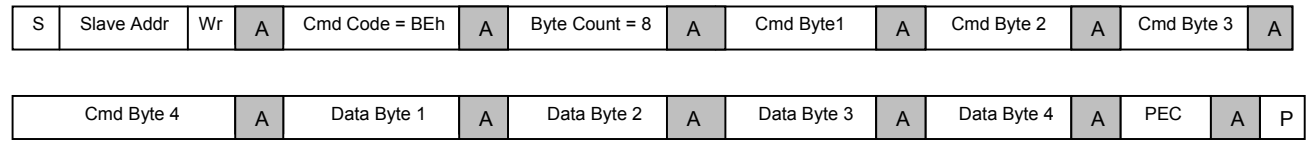
The Block Write command is used to write to the PI7C9X2G606PR registers. General SMBus Block Writes are illustrated in Figure 7-2 and Figure 7-3. Table 7-2 explains the elements used in Figure 7-2 and Figure 7-3.

Figure 7-2 SMBus Block Write Command Format, to Write to a PI7C9X2G606PR Register without PEC



: Master to Slave
: Slave to Master

Figure 7-3 SMBus Block Write Command Format, to Write to a PI7C9X2G606PR Register with PEC



: Master to Slave
: Slave to Master

Block Write transactions that are received with incorrect Cmd Code are NACKed, starting from the wrong byte setting, and including subsequent bytes in the packet. For example, if the Byte Count value is not 8, the PI7C9X2G606PR NACKs the byte corresponding to the Byte Count value, as well as any Data bytes following within the same packet.

The byte after Data Byte 4, if present, is taken as the PEC byte, and if present, the PEC is checked. If a packet fails Packet Error Checking, the PI7C9X2G606PR drops the packet (ignores the Write), and returns NACK for the PEC byte, to the SMBus Master. Packet Error Checking can be disabled, by Setting the SMBus/I^2C Control Register PEC Check Disable bit (Upstream Port, offset 344h[9]). The Byte Count value, by definition, does not include the PEC byte.

Table 7-2 Bytes for SMBus Block Write

Field (Byte) On Bus	Bit(s)	Value/ Description
S	1	**START** condition
P	1	**STOP** condition
A	1	**Acknowledge** (this bit position may be 0 for an ACK or 1 for a NACK)
Command Code	7:0	**BEh** for Block Write
Byte Count	7:0	**08h** = 8 bytes to follow (4 Command and 4 Data bytes). The PEC byte is not counted.
Command Byte 1	7:3	**Reserved**
	2:0	**Command** 011b = Write register 100b = Read register
Command Byte 2	7:4	**Reserved**
	3:0	**Port Select[4:1]** 2nd Command byte, bits [3:0], and 3rd Command byte, bit 7, combine to form a 5-bit Port Select.
Command Byte 3	7	**Port Select[0]** 2nd Command byte, bits [3:0], and 3rd Command byte, bit 7, combine to form a 5-bit Port Select. Port Select[4:0] is used to select Port to access. 0… Port 0 1… Port 1 2… Port 2 3… Port 3 4… Port 4 5… Port 5
	6	**Reserved**
	5:2	**Byte Enable** **Bit** **Description** 2 Byte Enable for Data Byte 4 (PI7C9X2G606PR register bits [7:0]) 3 Byte Enable for Data Byte 3 (PI7C9X2G606PR register bits [15:8]) 4 Byte Enable for Data Byte 2 (PI7C9X2G606PR register bits [23:16]) 5 Byte Enable for Data Byte 1 (PI7C9X2G606PR register bits [31:24]) 0 = Corresponding PI7C9X2G606PR register byte will not be modified 1 = Corresponding PI7C9X2G606PR register byte will be modified
	1:0	**PI7C9X2G606PR Register Address [11:10]**
Command Byte 4	7:0	**PI7C9X2G606PR Register Address [9:2]** Note: Address bits[1:0] are fixed to 0.
Data Byte 1	7:0	**Data write to register bits [31:24]**
Data Byte 2	7:0	**Data write to register bits [23:16]**
Data Byte 3	7:0	**Data write to register bits [15:8]**
Data Byte 4	7:0	**Data write to register bits [7:0]**
PEC	7:0	**Packet Error Code**

Table 7-3 is a sample to write SSID/SSVID register (offset F8h) in Port 1. The register value is 1234_5678h, with all bytes enabled, and without PEC. The default SMBus Address is 1101000b.

Table 7-3 Sample SMBus Block Write Byte Sequence

Byte Number	Byte Type	Value	Description
1	Address	D0h	Bits [7:1] for the PI7C9X2G606PR default Slave address of 68h, with bit 0 Cleared to indicate a Write.
2	Command Code	BEh	Command Code for register Write, using a Block Write
3	Byte Count	08h	Byte Count. Four Command Bytes and Four Data Bytes
4	Command Byte 1	03h	For Write command
5	Command Byte 2	00h	Bits [3:0] - Port Select [4:1] (for Port 1)
6	Command Byte 3	BCh	Bit 7 is Port Select[0] Bit 6 is reserved Bits [5:2] are the for Byte Enables; all are active Bits [1:0] are register Address bits [11:10]
7	Command Byte 4	3Eh	PI7C9X2G606PR Register Address bits [9:2] (for offset F8h)
8	Data Byte 1	12h	Data Byte for register bits [31:24]
9	Data Byte 2	34h	Data Byte for register bits [23:16]
10	Data Byte 3	56h	Data Byte for register bits [15:8]

Byte Number	Byte Type	Value	Description
11	Data Byte 4	78h	Data Byte for register bits[7:0]

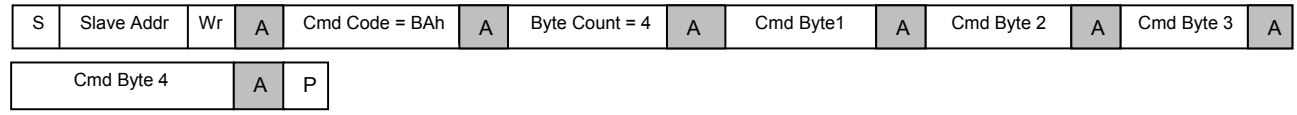
7.2.2 SMBUS BLOCK READ

A Block Read command is used to read PI7C9X2G606PR CFG registers. Similar to CFG register Reads using I^2C, a SMBus Write sequence must first be performed to select the register to read, followed by a SMBus Read of the corresponding register. There are two ways a PI7C9X2G606PR register can be read:

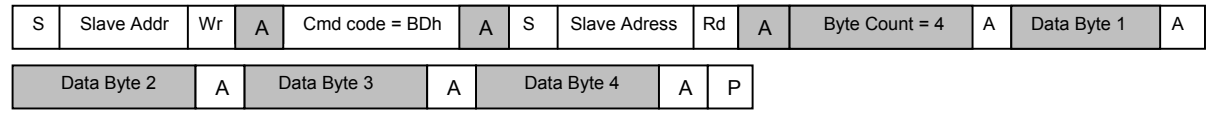
- Use a Block Write, followed by a Block Read. The Block Write sets up the parameters including Port Number, register address and Byte Enables, and the Block Read performs the actual Read operation.
- Use a Block Read - Block Write Process Call. This command is defined by the SMBus v2.0, and performs a Block Write and Block Read, using a single command. The Block Write portion of the message sets up the register to be read, and then a repeated START followed by the Block Read portion of the message returns the register data specified by the Block Write

The PI7C9X2G606PR always NACKs any incorrect command sequences, starting with the wrong Byte. Upon receiving the Block Read command, the PI7C9X2G606PR returns a PEC to the Master, if after the 4th byte of register data, the Master still requests one more Byte. As a Slave, the PI7C9X2G606PR recognizes the end of the Master's Read cycle, by observing the Master's NACK response for the last Data Byte transmitted by the PI7C9X2G606PR.
Incorrect command sequences are always NACK, starting with the byte that is incorrect. (Refer to Table 7-4.) On the Block Read command, a PEC is returned to the Master, if after the 4th byte of CSR data, the return Master still requests for one additional byte. As a Slave, the PI7C9X2G606PR will know the end of the Master Read cycle, by observing the NACK for the last byte read from the Master.

Figure 7-4 SMBus Block Write to Set up Read, and Resulting Read that Returns CFG Register Value



A Block Write to set up Read



A Block Read which returns CFG Register Value

: Master to Slave
: Slave to Master

Table 7-4 Bytes for SMBus Block Read

Field (Byte) On Bus	Bit(s)	Value / Description
S	1	**START** condition
P	1	**STOP** condition
A	1	**Acknowledge** (this bit position may be 0 for an ACK or 1 for a NACK)
Command Code	7:0	**BAh**, to set up Read, using Block Writes
Byte Count	7:0	**04h**, 4 Command bytes
Command Byte 1	7:3	**Reserved**
	2:0	**Command** 011b = Write register 100b = Read register
Command Byte 2	7:4	**Reserved**

Field (Byte) On Bus	Bit(s)	Value / Description
	3:0	**Port Select[4:1]** 2nd Command byte, bits [3:0], and 3rd Command byte, bit 7, combine to form a 5-bit Port Select.
Command Byte 3	7	**Port Select[0]** 2nd Command byte, bits [3:0], and 3rd Command byte, bit 7, combine to form a 5-bit Port Select. Port Select[4:0] is used to select Port to access. 0… Port 0 1… Port 1 2… Port 2 3… Port 3 4… Port 4 5… Port 5
	6	**Reserved**
	5:2	**Byte Enable** **Bit** **Description** 2 Byte Enable for Data Byte 4 (PI7C9X2G606PR register bits [7:0]) 3 Byte Enable for Data Byte 3 (PI7C9X2G606PR register bits [15:8]) 4 Byte Enable for Data Byte 2 (PI7C9X2G606PR register bits [23:16]) 5 Byte Enable for Data Byte 1 (PI7C9X2G606PR register bits [31:24]) 0 = Corresponding PI7C9X2G606PR register byte will not be modified 1 = Corresponding PI7C9X2G606PR register byte will be modified
	1:0	**PI7C9X2G606PR Register Address [11:10]**
Command Byte 4	7:0	**PI7C9X2G606PR Register Address [9:2]** Note: Address bits[1:0] are fixed to 0.
Command Code	7:0	**BDh for Block Read**
Data Byte 1	7:0	**Return value for CFG register bits [31:24]**
Data Byte 2	7:0	**Return value for CFG register bits [23:16]**
Data Byte 3	7:0	**Return value for CFG register bits [15:8]**
Data Byte 4	7:0	**Return value for CFG register bits [7:0]**

Table 7-5, Table 7-6, Table 7-7 and Table 7-8 are a sample to Read SSID/SSVID register (offset F8h) in Port 1. The register value is 0000_0000h, with all bytes enabled, and without PEC. The default SMBus Address is 1101000b.

Table 7-5 SMBus Block Write Portion

Byte Number	Byte Type	Value	Description
1	Address	D0h	Bits [7:1] for the PI7C9X2G606PR default Slave address of 68h, with bit 0 Cleared to indicate a Write.
2	Command Code	BAh	Command Code for register Write, using a Block Write
3	Byte Count	04h	Byte Count. Four Command Bytes
4	Command Byte 1	04h	For Read command
5	Command Byte 2	00h	Bits [3:0] - Port Select [4:1] (for Port 1)
6	Command Byte 3	BCh	Bit 7 is Port Select[0] Bit 6 is reserved Bits [5:2] are the for Byte Enables; all are active Bits [1:0] are register Address bits [11:10]
7	Command Byte 4	3Eh	PI7C9X2G606PR Register Address bits [9:2] (for offset F8h)

Table 7-6 SMBus Block Read Portion

Byte Number	Byte Type	Value	Description
1	Address	D0h	Bits [7:1] value for the PI7C9X2G606PR Slave address of 68h, with bit 0 Cleared to indicate to indicate a Write.
2	Block Read Command Code	BDh	Command code for Block Read of PI7C9X2G606PR registers.

Table 7-7 SMBus Read Command following Repeat START from Master

Byte Number	Byte Type	Value	Description
1	Address	D1h	Bits [7:1] value for the PI7C9X2G606PR Slave address of 68h, with bit 0 Set

			to indicate a Read.

Table 7-8 SMBus Return Bytes

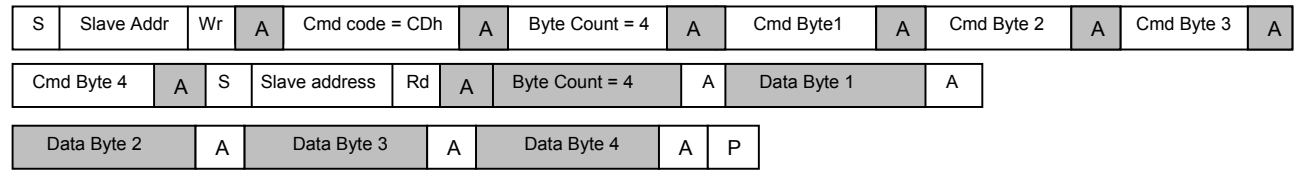
Byte Number	Byte Type	Value	Description
1	Byte Count	04h	Four Bytes in register
2	Data Byte 1	00h	Register data [31:24]
3	Data Byte 2	00h	Register data [23:16]
4	Data Byte 3	00h	Register data [15:8]
5	Data Byte 4	00h	Register data [7:0]

7.2.3 CSR READ, USING SMBUS BLOCK READ – BLOCK WRITE PROCESS CALL

A general SMBus Block Read - Block Write Process Call sequence is illustrated in Figure 7-5. Alternatively, a general SMBus Block Read - Block Write Process Call with PEC sequence is illustrated in Figure 7-6.

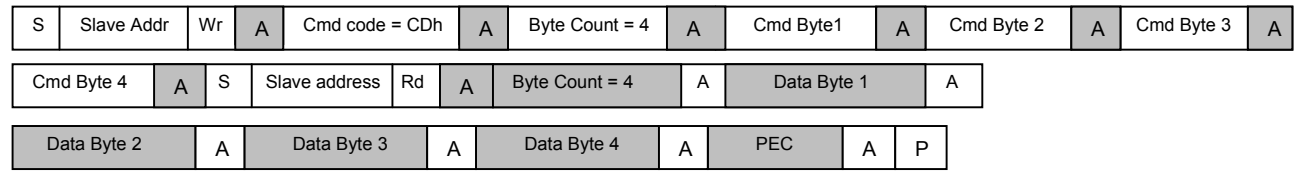
Using this command, the register to be read can be set up and read back with one SMBus cycle (a transaction with a START and ending in STOP). There is no STOP condition before the repeated START condition. The command format for the Block Write part of this command has the same sequence as in Table 7-5, except that the Command Code changes to CDh, as illustrated below. Other Bytes remain the same as used in the sequence for SMBus Block Write followed by Block Read. Table 7-9 lists the Command format for Block Read.

Figure 7-5 CSR Read Operation Using SMBus Block Read – Block Write Process Call



: Master to Slave
: Slave to Master

Figure 7-6 CSR Read Operation Using SMBus Block Read – Block Write Process Call with PEC



: Master to Slave
: Slave to Master

Table 7-9 Command Format for SMBus Block Read

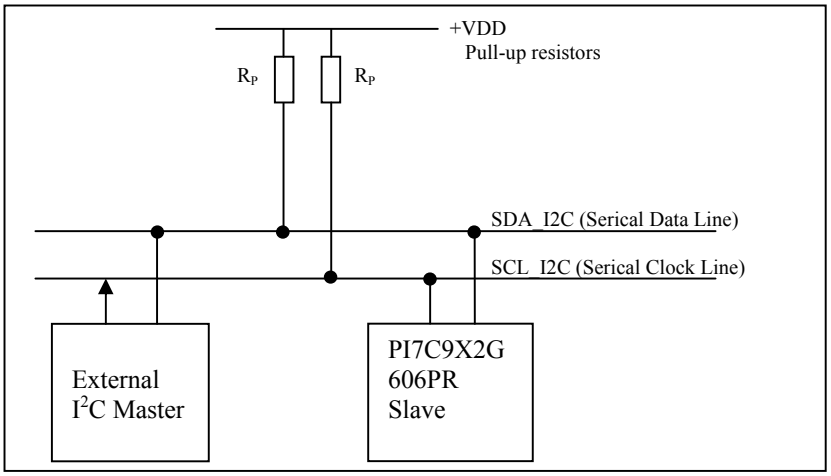
Field (Byte) On Bus	Bit(s)	Value/Description
Command Code	7:0	CDh for Block Read (Process Call Read)

7.3 I²C SLAVE INTERFACE

Inter-Integrated Circuit (I²C) is a bus used to connect Integrated Circuits (ICs). Multiple ICs can be connected to an I²C Bus, and I²C devices that have I²C mastering capability can initiate a Data transfer. I²C is used for Data transfers between ICs at relatively low rates (100 Kbps), and is used in a variety of applications. For further details regarding I²C Buses, refer to the *I²C Bus v2.1*.

The PI7C9X2G606PR is an I²C Slave. Slave operations allow the PI7C9X2G606PR Configuration registers to be read from or written to by an I²C Master, external from the device. I²C is a sideband mechanism that allows the device Configuration registers to be programmed, read from, or written to, independent of the PCI Express upstream Link.

Figure 7-7 Standard Devices to I²C Bus Connection Block Diagram



The I²C interface on the Packet Switch consists of a I²C clock pin (SCL_I2C), a I²C data pin (SDA_I2C), and 3 I²C address pins (I2C_ADDR[2:0]). The I²C clock pin provides or receives the clock signal. The I²C data pin facilitates the data transmission and reception. Both of the clock and data pins are bi-directional. The I²C address pins determine the address to which the Packet Switch responds to. The I²C address pins generate addresses according to the following table:

Table 7-10 I²C Address Pin Configuration

BIT	I2C Address
0	I2C_ADDR[0]
1	I2C_ADDR[1]
2	I2C_ADDR[2]
3	1
4	0
5	1
6	1

Software can change the I²C Slave address, by programming the SMBus/I²C Control Register SMBus/I²C Device Address field (Upstream Port, offset 344h [7:1]).

7.3.1 I²C REGISTER WRITE ACCESS

The PI7C9X2G606PR Configuration registers can be read from and written to, based upon I²C register Read and Write operations, respectively. An I²C Write packet consists of Address Phase bytes and Command Phase bytes, followed by one to four additional I²C Data bytes. Table 7-11 defines mapping of the I²C Data bytes to the Configuration register Data bytes.

The I²C packet starts with the S (START condition) bit. Data bytes are separated by the A (Acknowledge Control Packet (ACK)) or N (Negative Acknowledge (NAK)) bit. The packet ends with the P (STOP condition) bit.
If the Master generates an invalid command， the targeted PI7C9X2G606PR register is not modified.
The PI7C9X2G606PR considers the 1st Data byte of the 4-byte Data phase, following the four Command bytes in the Command phase, as register Byte 3 (bits [31:24]). The next three Data bytes access register Bytes 2 through 0, respectively. Four Data bytes are required, regardless of the Byte Enable Settings in the Command phase. The Master can then generate either a STOP condition (to finish the transfer) or a repeated START condition (to start a new transfer). If the I²C Master sends more than the four Data bytes (violating PI7C9X2G606PR protocol), further details regarding J2C protocol, the PI7C9X2G606PR returns a NAK for the extra Data byte(s).

Table 7-12 describes each I²C Command byte for Write access. In the packet described in Figure 7-8, Command Bytes 0 through 3 for Writes follow the format specified in Table 7-12.

Table 7-11 I²C Register Write Access

I2C Data Byte Order	PCI Express Configuration Register Byte
0	Written to register Byte 3
1	Written to register Byte 2
2	Written to register Byte 1
3	Written to register Byte 0

Table 7-12 I²C Command Format for Write Access

Byte	Bit(s)	Description
1st (0)	7:3	**Reserved**
	2:0	**Command** 011b = Write register
2nd (1)	7:4	**Reserved**
	3:0	**Port Select[4:1]** 2nd Command byte, bits [3:0], and 3rd Command byte, bit 7, combine to form a 5-bit Port Select.
3rd (2)	7	**Port Select[0]** 2nd Command byte, bits [3:0], and 3rd Command byte, bit 7, combine to form a 5-bit Port Select. Port Select[4:0] is used to select Port to access. 0… Port 0 1… Port 1 2… Port 2 3… Port 3 4… Port 4 5… Port 5
	6	**Reserved**
	5:2	**Byte Enable** **Bit** **Description** 2 Byte Enable for Data Byte 4 (PI7C9X2G606PR register bits [7:0]) 3 Byte Enable for Data Byte 3 (PI7C9X2G606PR register bits [15:8]) 4 Byte Enable for Data Byte 2 (PI7C9X2G606PR register bits [23:16]) 5 Byte Enable for Data Byte 1 (PI7C9X2G606PR register bits [31:24]) 0 = Corresponding PI7C9X2G606PR register byte will not be modified 1 = Corresponding PI7C9X2G606PR register byte will be modified
	1:0	**PI7C9X2G606PR Register Address [11:10]**
4th (3)	7:0	**PI7C9X2G606PR Register Address [9:2]** Note: Address bits[1:0] are fixed to 0.

Figure 7-8 I²C Write Packet

I²C Write Packet Address Phase Byte

Address Cycle			
START	**7654321**	**0**	**ACK/NAK**
S	Slave Address [7:1]	Read/Write Bit 0 = Write	A

I2C Write Packet Command Phase Byte

Command Cycle							
76543210	**ACK/NAK**	**76543210**	**ACK/NAK**	**76543210**	**ACK/NAK**	**76543210**	**ACK/NAK**
Command Byte 0	A	Command Byte 1	A	Command Byte 2	A	Command Byte 3	A

I²C Write Packet Data Phase Byte

Write Cycle								
76543210	**ACK/NAK**	**76543210**	**ACK/NAK**	**76543210**	**ACK/NAK**	**76543210**	**ACK/NAK**	**STOP**
Register Byte 3	A	Register Byte 2	A	Register Byte 1	A	Register Byte 0	A	P

The following tables illustrate a sample I2C packet for writing the PI7C9X2G606PR SSID/SSVID register (offset F8h) for Port 0, with data 1234_5678h.

Note: *The PI7C9X2G606PR has a default I²C Slave address [6:0] value of 68h, with the I2C_ADDR [2:0] input having a value of 000. The byte sequence on the I²C Bus, as listed in the following tables, occurs after the START and before the STOP bits, by which the I²C Master frames the transfer.*

Figure 7-9 I²C Register Write Access Example

I²C Register Write Access Example – Address Cycle

Phase	Value	Description
Address	D0h	Bits [7:1] for PI7C9X2G606PR I²C Slave Address (68h) with last bit (bit 0) for Write = 0

I²C Register Write Access Example – Command Cycle

Byte	Value	Description
0	03h	[7:3] Reserved [2:0] Command, 011b = Write register
1	00h for Port 0	[7:4] Reserved [3:0] Port Select[4:1]
2	3Ch for Port 0	[7] Port Select[0] [6] Reserved [5:2] Byte Enable, all active. [1:0] PI7C9X2G606PR Register Address, Bits [11:10]
3	3Eh	[7:0] PI7C9X2G606PR Register Address, Bits [9:2]

I²C Register Write Access Example – Data Cycle

Byte	Value	Description
0	12h	Data to Write for Byte 3
1	34h	Data to Write for Byte 2
2	56h	Data to Write for Byte 1
3	78h	Data to Write for Byte 0

Figure 7-10 I²C Write Command Packet Example

I²C Write Packet Address Phase Bytes

1st Cycle			
START	**7654321**	**0**	**ACK/NAK**
S	Slave Address 1101_000b	Read/Write Bit 0 = Write	A

I²C Write Packet Command Phase Bytes

Command Cycle							
76543210	**ACK/NAK**	**76543210**	**ACK/NAK**	**76543210**	**ACK/NAK**	**76543210**	**ACK/NAK**
Command Byte 0 0000_0011b	A	Command Byte 1 0000_0000b	A	Command Byte 2 0011_1100b	A	Command Byte 3 0011_1110b	A

I²C Write Packet Data Phase Bytes

Write Cycle								
76543210	**ACK/NAK**	**76543210**	**ACK/NAK**	**76543210**	**ACK/NAK**	**76543210**	**ACK/NAK**	**STOP**
Register Byte 3	A	Register Byte 2	A	Register Byte 1	A	Register Byte 0	A	P

7.3.2 I²C REGISTER READ ACCESS

When the I²C Master attempts to read a PI7C9X2G606PR register, two packets are transmitted. The 1st packet consists of Address and Command Phase bytes to the Slave. The 2nd packet consists of Address and Data Phase bytes.

According to the I²C Bus, v2.1, a Read cycle is triggered when the Read/Write bit (bit 0) of the 1st cycle is Set. The Command phase reads the requested register content into the internal buffer. When the I²C Read access occurs, the internal buffer value is transferred on to the I²C Bus, starting from Byte 3 (bits [31: 24]), followed by the subsequent bytes, with Byte 0 (bits [7:0]) being transferred last. If the I²C Master requests more than four bytes, the PI7C9X2G606PR re-transmits the same byte sequence, starting from Byte 3 of the internal buffer.

The 1st and 2nd I²C Read packets perform the following functions:

- 1st packet - Selects the register to read
- 2nd packet - Reads the register (sample 2nd packet provided is for a 7-bit PI7C9X2G606PR I²C Slave address)

Although two packets are shown for the I²C Read, the I²C Master can merge the two packets together into a single packet, by not generating the STOP at the end of the first packet (Master does not relinquish the bus) and generating REPEAT START.

Table 7-13 describes each I²C Command byte for Read access. In the packet described in Figure 7-11, Command Bytes 0 through 3 for Reads follow the format specified in Table 7-13.

Table 7-13 I²C Command Format for Read Access

Byte	Bit(s)	Description
1st (0)	7:3	**Reserved**
	2:0	**Command** 100b = Read register
2nd (1)	7:4	**Reserved**
	3:0	**Port Select, Bits [4:1]** 2nd Command byte, bit [3:0], and 3rd Command byte, bit 7, combine to form a 5-bit Port Select.
3rd (2)	7	**Port Select[0]** 2nd Command byte, bits [3:0], and 3rd Command byte, bit 7, combine to form a 5-bit Port Select. Port Select[4:0] is used to select Port to access.

Byte	Bit(s)	Description
		0… Port 0 1… Port 1 2… Port 2 3… Port 3 4… Port 4 5… Port 5
	6	**Reserved**
	5:2	**Byte Enable** **Bit** **Description** 2 Byte Enable for Data Byte 4 (PI7C9X2G606PR register bits [7:0]) 3 Byte Enable for Data Byte 3 (PI7C9X2G606PR register bits [15:8]) 4 Byte Enable for Data Byte 2 (PI7C9X2G606PR register bits [23:16]) 5 Byte Enable for Data Byte 1 (PI7C9X2G606PR register bits [31:24]) 0 = Corresponding PI7C9X2G606PR register byte will not be modified 1 = Corresponding PI7C9X2G606PR register byte will be modified
	1:0	**PI7C9X2G606PR Register Address [11:10]**
4th (3)	7:0	**PI7C9X2G606PR Register Address [9:2]** Note: Address bits[1:0] are fixed to 0.

Figure 7-11 I²C Read Command Packet

I²C Read Command Packet Address Phase Byte (1st Packet)

1st Cycle			
START	**7654321**	**0**	**ACK/NAK**
S	Slave Address[7:1]	Read/Write Bit 0 = Write	A

I²C Read Command Packet Command Phase Byte (1st Packet)

Write Cycle							
76543210	**ACK/NAK**	**76543210**	**ACK/NAK**	**76543210**	**ACK/NAK**	**76543210**	**ACK/NAK**
Command Byte 0	A	Command Byte 1	A	Command Byte 2	A	Command Byte 3	A

I²C Read Data Packet Address Phase Byte (2nd Packet)

1st Cycle			
START	**7654321**	**0**	**ACK/NAK**
S	Slave Address[7:1]	Read/Write Bit 1 = Read	A

I²C Read Data Packet Data Phase Byte (2nd Packet)

Write Cycle								
76543210	**ACK/NAK**	**76543210**	**ACK/NAK**	**76543210**	**ACK/NAK**	**76543210**	**ACK/NAK**	**STOP**
Register Byte 3	A	Register Byte 2	A	Register Byte 1	A	Register Byte 0	A	P

The following tables illustrate a sample I2C packet for reading the PI7C9X2G606PR SSID/SSVID register (offset F8h) for Port 0. The default value for SSID/SSVID register is 0000_0000h.

Note: *The PI7C9X2G606PR has a default I²C Slave address [6:0] value of 68h, with the I2C_ADDR [2:0] inputs having a value of 000. The byte sequence on the I²C Bus, as listed in the following tables, occurs after the START and before the STOP bits, by which the I²C Master frames the transfer.*

Figure 7-12 I²C Register Read Access Example

I²C Register Read Access Example – Address Cycle (1st Packet)

Phase	Value	Description
Address	D0h	Bits [7:1] for PI7C9X2G606PR I²C Slave Address (68h) with last bit (bit 0) for Write = 0

I²C Register Read Access Example – Command Cycle (1st Packet)

Byte	Value	Description
0	04h	[7:3] Reserved [2:0] Command , 100b = Read register
1	00h for Port 0	[7:4] Reserved [3:0] Port Select[4:1]
2	3Ch for Port 0	[7] Port Select[0] [6] Reserved [5:2] Byte Enable, All active. [1:0] PI7C9X2G606PR Register Address, Bits [11:10]
3	3Eh	[7:0] PI7C9X2G606PR Register Address, Bits [9:2]

I²C Register Read Access Example – 2nd Packet

Phase	Value	Description
Address	D1h	Bits [7:1] for PI7C9X2G606PR I2C Slave Address (68h) with last bit (bit 0) for Read = 1
Read	00h	Byte 3 of Register Read
	00h	Byte 2 of Register Read
	00h	Byte 1 of Register Read
	00h	Byte 0 of Register Read

Figure 7-13 I²C Read Command Packet

I²C Read Command Packet Address Phase Bytes (1st Packet)

1st Cycle			
START	**7654321**	**0**	**ACK/NAK**
S	Slave Address 1101_000b	Read/Write Bit 0 = Write	A

I²C Read Command Packet Command Phase Bytes (1st Packet)

Command Cycle						
76543210	**ACK/NAK**	**76543210**	**ACK/NAK**	**76543210**	**ACK/NAK**	**76543210**
Command Byte 0 0000_0100b	A	Command Byte 1 0000_0000b	A	Command Byte 2 0011_1100b	A	Command Byte 3 0011_1110b

I²C Read Data Packet Address Phase Bytes (2nd Packet)

1st Cycle			
START	**7654321**	**0**	**ACK/NAK**
S	Slave Address [7:1] 1101_000b	Read/Write Bit 1 = Read	A

I²C Read Data Packet Data Phase Bytes (2nd Packet)

Command Cycle							
76543210	**ACK/NAK**	**76543210**	**ACK/NAK**	**76543210**	**ACK/NAK**	**76543210**	**Stop**
Register Byte3 0000_0000b	A	Register Byte2 0000_0000b	A	Register Byte1 0000_0000b	A	Register Byte0 0000_00000b	P

8 REGISTER DESCRIPTION

8.1 REGISTER TYPES

REGISTER TYPE	DEFINITION
HwInt	Hardware Initialization
RO	Read Only
RW	Read / Write
RWC	Read / Write 1 to Clear
RWCS	Sticky – Read Only / Write 1 to Clear
RWS	Sticky – Read / Write
ROS	Sticky – Read Only

8.2 TRANSPARENT MODE CONFIGURATION REGISTERS

When the port of the Switch is set to operate at the transparent mode, it is represented by a logical PCI-to-PCI Bridge that implements type 1 configuration space header. The following table details the allocation of the register fields of the PCI 2.3 compatible type 1 configuration space header.

31 –24	23 – 16	15 – 8	7 –0	BYTE OFFSET
Device ID		Vendor ID		00h
Primary Status		Command		04h
Class Code			Revision ID	08h
Reserved	Header Type	Primary Latency Timer	Cache Line Size	0Ch
Reserved				10h – 14h
Secondary Latency Timer	Subordinate Bus Number	Secondary Bus Number	Primary Bus Number	18h
Secondary Status		I/O Limit Address	I/O Base Address	1Ch
Memory Limit Address		Memory Base Address		20h
Prefetchable Memory Limit Address		Prefetchable Memory Base Address		24h
Prefetchable Memory Base Address Upper 32-bit				28h
Prefetchable Memory Limit Address Upper 32-bit				2Ch
I/O Limit Address Upper 16-bit		I/O Base Address Upper 16-bit		30h
Reserved			Capability Pointer to 80h(40h)	34h
Reserved				38h
Bridge Control		Interrupt Pin	Interrupt Line	3Ch
Power Management Capabilities		Next Item Pointer	Capability ID=01	40h
PM Data	PPB Support Extensions	Power Management Data		44h
Message Control		Next Item Pointer	Capability ID=05	4Ch
Message Address				50h
Message Upper Address				54h
Reserved		Message Data		58h
VPD Register		Next Item Pointer	Capability ID=03	5Ch
VPD Data Register				60h
Length in Bytes (34h)		Next Item Pointer	Capability ID=09	64h
XPIP_CSR0				68h
XPIP_CSR1				6Ch
ACK Latency Timer		Replay Time-out Counter		70h
PHY Parameter 0		Switch Modes		74h
PHY Parameter 1		XPIP_CSR2		78h
PHY Parameter 2				7Ch
XPIP_CSR3				80h
XPIP_CSR4				84h
XPIP_CSR5				88h
XPIP_CSR7	XPIP_CSR6	Port Misc	TL_CSR	8Ch
PHY Parameter 3				90h
Reserved		PHY TX Margin Parameter		94h

31 –24	23 – 16	15 – 8	7 –0	BYTE OFFSET
L1PM	Buffer Ctrl	OP Mode		98h
Device specific PME				9Ch
Reserved		EEPROM status	EPPROM Control	A0h
EEPROM Data		EEPROM Address		A4h
LED Debug	Reserved		DebugOut Control	A8h
DebugOut Data				ACh
Reserved		Next Item Pointer	SSID/SSVID Capability ID=0D	B0h
SSID		SSVID		B4h
GPIO Data and Control				B8h
Reserved				BCh
PCI Express Capabilities Register		Next Item Pointer	Capability ID=10	C0h
Device Capabilities				C4h
Device Status		Device Control		C8h
Link Capabilities				CCh
Link Status		Link Control		D0h
Slot Capabilities				D4h
Slot Status		Slot Control		D8h
Reserved				DCh
Reserved				E0h
Device Capabilities 2				E4h
Device Status 2		Device Control 2		E8h
Link Capabilities 2				ECh
Link Status 2		Link Control 2		F0h
Slot Capabilities 2				F4h
Slot Status 2		Slot Control 2		F8h
Reserved				FCh

Other than the PCI 2.3 compatible configuration space header, the Switch also implements PCI express extended configuration space header, which includes advanced error reporting, virtual channel, and power budgeting capability registers. The following table details the allocation of the register fields of PCI express extended capability space header. The first extended capability always begins at offset 100h with a PCI Express Enhanced Capability header and the rest of capabilities are located at an offset greater than 0FFh relative to the beginning of PCI compatible configuration space.

31 –24	23 – 16	15 - 8	7 –0	BYTE OFFSET
Next Capability Offset	Cap. Version	PCI Express Extended Capability ID=0001h		100h
Uncorrectable Error Status Register				104h
Uncorrectable Error Mask Register				108h
Uncorrectable Error Severity Register				10Ch
Correctable Error Status Register				110h
Correctable Error Mask Register				114h
Advanced Error Capabilities and Control Register				118h
Header Log Register				11Ch – 128h
Reserved				12Ch – 13Ch
Next Capability Offset	Cap. Version	PCI Express Extended Capability ID=0002h		140h
Port VC Capability Register 1				144h
VC Arbitration Table Offset=3	Port VC Capability Register 2			148h
Port VC Status Register		Port VC Control Register		14Ch
Port Arbitration Table Offset=4	VC Resource Capability Register (0)			150h
VC Resource Control Register (0)				154h
VC Resource Status Register (0)		Reserved		158h
Port Arbitration Table Offset=6	VC Resource Capability Register (1)			15Ch
VC Resource Control Register (1)				160h
VC Resource Status Register (1)		Reserved		164h
Reserved				168h – 16Ch
VC Arbitration Table with 32 Phases				170h – 17Ch
Port Arbitration Table with 128 Phases for VC0				180h – 1BCh

31 –24	23 – 16	15 - 8	7 –0	BYTE OFFSET
Port Arbitration Table with 128 Phases for VC1				1C0h – 1FCh
Reserved				200h – 208h
Next Capability Offset	Cap. Version	PCI Express Extended Capability ID=0004h		20Ch
Reserved			Data Select Register	210h
Data Register				214h
Reserved			Power Budget Capability Register	218h
Reserved				21Ch
Next Capability Offset	Cap version	PCI Express Extended Capability ID=000Dh		220h
ACS Control		ACS Capability		224h
Reserved			Egress Control Vector	228h
Reserved				22Ch
Next Capability Offset	Cap version	PCI Express Extended Capability ID=0018h		230h
Reserved / Max No-Snoop Latency Scale	Max No-Snoop Latency Value	Reserved / Max Snoop Latency Scale	Max Snoop Latency Value	234h
Reserved				238h - 23Ch
Next Capability Offset	Cap version	PCI Express Extended Capability ID=001Eh		240h
L1 PM Substates Capability				244h
L1 PM Substates Control 1				248h
L1 PM Substates Control 2				24Ch
Reserved				250h - 338h
LTSSM CSR				33Ch
MAC_CSR1		Hotplug_CSR		340h
SMBUS Control				344h
Reserved				348h – 34Ch
Reserved			CPLD Flow Control Enable	350h
X2 CPLD Flow Control Threshold		X1 CPLD Flow Control Threshold		354h
Reserved		X4 CPLD Flow Control Threshold		358h
Reserved				35Ch
Power Saving Disable				360h
LED Display CSR				364h

8.2.1 VENDOR ID REGISTER – OFFSET 00h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Vendor ID	RO	Identifies Pericom as the vendor of this device. The default value may be changed by auto-loading from EEPROM. Reset to 12D8h.

8.2.2 DEVICE ID REGISTER – OFFSET 00h

BIT	FUNCTION	TYPE	DESCRIPTION
31:16	Device ID	RO	Identifies this device as the PI7C9X2G606PR. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Resets to 2608h.

8.2.3 COMMAND REGISTER – OFFSET 04h

BIT	FUNCTION	TYPE	DESCRIPTION
0	I/O Space Enable	RW	0b: Ignores I/O transactions on the primary interface 1b: Enables responses to I/O transactions on the primary interface Resets to 0b.
1	Memory Space Enable	RW	0b: Ignores memory transactions on the primary interface 1b: Enables responses to memory transactions on the primary interface Reset to 0b.
2	Bus Master Enable	RW	0b: Does not initiate memory or I/O transactions on the upstream port and handles as an Unsupported Request (UR) to memory and I/O transactions on the downstream port. For Non-Posted Requests, a completion with UR completion status must be returned 1b: Enables the Switch Port to forward memory and I/O Read/Write transactions in the upstream direction Reset to 0b.
3	Special Cycle Enable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
4	Memory Write And Invalidate Enable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
5	VGA Palette Snoop Enable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
6	Parity Error Response Enable	RW	0b: Switch may ignore any parity errors that it detects and continue normal operation 1b: Switch must take its normal action when a parity error is detected Reset to 0b.
7	Wait Cycle Control	RO	Does not apply to PCI Express. Must be hardwired to 0b.
8	SERR# enable	RW	0b: Disables the reporting of Non-fatal and Fatal errors detected by the Switch to the Root Complex 1b: Enables the Non-fatal and Fatal error reporting to Root Complex Reset to 0b.
9	Fast Back-to-Back Enable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
10	Interrupt Disable	RW	Controls the ability of a PCI Express device to generate INTx Interrupt Messages. In the Switch, this bit does not affect the forwarding of INTx messages from the downstream ports. Reset to 0b.
15:11	Reserved	RsvdP	Not Support.

8.2.4 PRIMARY STATUS REGISTER – OFFSET 04h

BIT	FUNCTION	TYPE	DESCRIPTION
18:16	Reserved	RsvdP	Not Support.
19	Interrupt Status	RO	Indicates that an INTx Interrupt Message is pending internally to the device. In the Switch, the forwarding of INTx messages from the downstream device of the Switch port is not reflected in this bit. Must be hardwired to 0b.
20	Capabilities List	RO	Set to 1b to enable support for the capability list (offset 34h is the pointer to the data structure). Reset to 1b.
21	66MHz Capable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
22	Reserved	RsvdP	Not Support.
23	Fast Back-to-Back Capable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
24	Master Data Parity Error	RWC	Set to 1b (by a requester) whenever a Parity error is detected or forwarded on the primary side of the port in a Switch. If the Parity Error Response Enable bit is cleared, this bit is never set.

BIT	FUNCTION	TYPE	DESCRIPTION
			Reset to 0b.
26:25	DEVSEL# timing	RO	Does not apply to PCI Express. Must be hardwired to 0b.
27	Signaled Target Abort	RO	Set to 1b (by a completer) whenever completing a request on the primary side using the Completer Abort Completion Status. Reset to 0b.
28	Received Target Abort	RO	Set to 1b (by a requestor) whenever receiving a Completion with Completer Abort Completion Status on the primary side. Reset to 0b.
29	Received Master Abort	RO	Set to 1b (by a requestor) whenever receiving a Completion with Unsupported Request Completion Status on primary side. Reset to 0b.
30	Signaled System Error	RWC	Set to 1b when the Switch sends an ERR_FATAL or ERR_NONFATAL Message, and the SERR Enable bit in the Command register is 1b. Reset to 0b.
31	Detected Parity Error	RWC	Set to 1b whenever the primary side of the port in a Switch receives a Poisoned TLP. Reset to 0b.

8.2.5 REVISION ID REGISTER – OFFSET 08h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Revision	RO	Indicates revision number of device. Hardwired to 00h.

8.2.6 CLASS CODE REGISTER – OFFSET 08h

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Programming Interface	RO	Read as 00h to indicate no programming interfaces have been defined for PCI-to-PCI Bridges.
23:16	Sub-Class Code	RO	Read as 04h to indicate device is a PCI-to-PCI Bridge.
31:24	Base Class Code	RO	Read as 06h to indicate device is a Bridge device.

8.2.7 CACHE LINE REGISTER – OFFSET 0Ch

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Cache Line Size	RW	The cache line size register is set by the system firmware and the operating system cache line size. This field is implemented by PCI Express devices as a RW field for legacy compatibility, but it has no impact on any PCI Express device functionality. Reset to 00h.

8.2.8 PRIMARY LATENCY TIMER REGISTER – OFFSET 0Ch

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Primary Latency timer	RO	Does not apply to PCI Express. Must be hardwired to 00h.

8.2.9 HEADER TYPE REGISTER – OFFSET 0Ch

BIT	FUNCTION	TYPE	DESCRIPTION
23:16	Header Type	RO	Read as 01h to indicate that the register layout conforms to the standard PCI-to-PCI Bridge layout.

8.2.10 PRIMARY BUS NUMBER REGISTER – OFFSET 18h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Primary Bus Number	RW	Indicates the number of the PCI bus to which the primary interface is connected. The value is set in software during configuration. Reset to 00h.

8.2.11 SECONDARY BUS NUMBER REGISTER – OFFSET 18h

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Secondary Bus Number	RW	Indicates the number of the PCI bus to which the secondary interface is connected. The value is set in software during configuration. Reset to 00h.

8.2.12 SUBORDINATE BUS NUMBER REGISTER – OFFSET 18h

BIT	FUNCTION	TYPE	DESCRIPTION
23:16	Subordinate Bus Number	RW	Indicates the number of the PCI bus with the highest number that is subordinate to the Bridge. The value is set in software during configuration. Reset to 00h.

8.2.13 SECONDARY LATENCY TIMER REGISTER – OFFSET 18h

BIT	FUNCTION	TYPE	DESCRIPTION
31:24	Secondary Latency Timer	RO	Does not apply to PCI Express. Must be hardwired to 00h.

8.2.14 I/O BASE ADDRESS REGISTER – OFFSET 1Ch

BIT	FUNCTION	TYPE	DESCRIPTION
3:0	32-bit Indicator	RO	Read as 1h to indicate 32-bit I/O addressing.
7:4	I/O Base Address [15:12]	RW	Defines the bottom address of the I/O address range for the Bridge to determine when to forward I/O transactions from one interface to the other. The upper 4 bits correspond to address bits [15:12] and are writable. The lower 12 bits corresponding to address bits [11:0] are assumed to be 0. The upper 16 bits corresponding to address bits [31:16] are defined in the I/O base address upper 16 bits address register. Reset to 0h.

8.2.15 I/O LIMIT ADDRESS REGISTER – OFFSET 1Ch

BIT	FUNCTION	TYPE	DESCRIPTION
11:8	32-bit Indicator	RO	Read as 1h to indicate 32-bit I/O addressing.
15:12	I/O Limit Address [15:12]	RW	Defines the top address of the I/O address range for the Bridge to determine when to forward I/O transactions from one interface to the other. The upper 4 bits correspond to address bits [15:12] and are writable. The lower 12 bits corresponding to address bits [11:0] are assumed to be FFFh. The upper 16 bits corresponding to address bits [31:16] are defined in the I/O limit address upper 16 bits address register. Reset to 0h.

8.2.16 SECONDARY STATUS REGISTER – OFFSET 1Ch

BIT	FUNCTION	TYPE	DESCRIPTION
20:16	Reserved	RsvdP	Not Support.
21	66MHz Capable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
22	Reserved	RsvdP	Not Support.
23	Fast Back-to-Back Capable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
24	Master Data Parity Error	RWC	Set to 1b (by a requester) whenever a Parity error is detected or forwarded on the secondary side of the port in a Switch. If the Parity Error Response Enable bit is cleared, this bit is never set. Reset to 0b.
26:25	DEVSEL_L timing	RO	Does not apply to PCI Express. Must be hardwired to 0b.
27	Signaled Target Abort	RO	Set to 1b (by a completer) whenever completing a request in the secondary side using Completer Abort Completion Status. Reset to 0b.
28	Received Target Abort	RO	Set to 1b (by a requestor) whenever receiving a Completion with Completer Abort Completion Status in the secondary side. Reset to 0b.
29	Received Master Abort	RO	Set to 1b (by a requestor) whenever receiving a Completion with Unsupported Request Completion Status in secondary side. Reset to 0b.
30	Received System Error	RWC	Set to 1b when the Switch sends an ERR_FATAL or ERR_NONFATAL Message, and the SERR Enable bit in the Bridge Control register is 1. Reset to 0b.
31	Detected Parity Error	RWC	Set to 1b whenever the secondary side of the port in a Switch receives a Poisoned TLP. Reset to 0b.

8.2.17 MEMORY BASE ADDRESS REGISTER – OFFSET 20h

BIT	FUNCTION	TYPE	DESCRIPTION
3:0	Reserved	RO	Reset to 0h.
15:4	Memory Base Address [31:20]	RW	Defines the bottom address of an address range for the Bridge to determine when to forward memory transactions from one interface to the other. The upper 12 bits correspond to address bits [31:20] and are able to be written to. The lower 20 bits corresponding to address bits [19:0] are assumed to be 0. Reset to 000h.

8.2.18 MEMORY LIMIT ADDRESS REGISTER – OFFSET 20h

BIT	FUNCTION	TYPE	DESCRIPTION
19:16	Reserved	RO	Reset to 0h.
31:20	Memory Limit Address [31:20]	RW	Defines the top address of an address range for the Bridge to determine when to forward memory transactions from one interface to the other. The upper 12 bits correspond to address bits [31:20] and are writable. The lower 20 bits corresponding to address bits [19:0] are assumed to be FFFFFh. Reset to 000h.

8.2.19 PREFETCHABLE MEMORY BASE ADDRESS REGISTER – OFFSET 24h

BIT	FUNCTION	TYPE	DESCRIPTION
3:0	64-bit addressing	RO	Read as 1h to indicate 64-bit addressing.
15:4	Prefetchable Memory Base Address [31:20]	RW	Defines the bottom address of an address range for the Bridge to determine when to forward memory read and write transactions from one interface to the other. The upper 12 bits correspond to address bits [31:20] and are writable. The lower 20 bits are assumed to be 0. The memory base register upper 32 bits contain the upper half of the base address. Reset to 000h.

8.2.20 PREFETCHABLE MEMORY LIMIT ADDRESS REGISTER – OFFSET 24h

BIT	FUNCTION	TYPE	DESCRIPTION
19:16	64-bit addressing	RO	Read as 1h to indicate 64-bit addressing.
31:20	Prefetchable Memory Limit Address [31:20]	RW	Defines the top address of an address range for the Bridge to determine when to forward memory read and write transactions from one interface to the other. The upper 12 bits correspond to address bits [31:20] and are writable. The lower 20 bits are assumed to be FFFFFh. The memory limit upper 32 bits register contains the upper half of the limit address. Reset to 000h.

8.2.21 PREFETCHABLE MEMORY BASE ADDRESS UPPER 32-BITS REGISTER – OFFSET 28h

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Prefetchable Memory Base Address, Upper 32-bits [63:32]	RW	Defines the upper 32-bits of a 64-bit bottom address of an address range for the Bridge to determine when to forward memory read and write transactions from one interface to the other. Reset to 0000_0000h.

8.2.22 PREFETCHABLE MEMORY LIMIT ADDRESS UPPER 32-BITS REGISTER – OFFSET 2Ch

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Prefetchable Memory Limit Address, Upper 32-bits [63:32]	RW	Defines the upper 32-bits of a 64-bit top address of an address range for the Bridge to determine when to forward memory read and write transactions from one interface to the other. Reset to 0000_0000h.

8.2.23 I/O BASE ADDRESS UPPER 16-BITS REGISTER – OFFSET 30h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	I/O Base Address, Upper 16-bits [31:16]	RW	Defines the upper 16-bits of a 32-bit bottom address of an address range for the Bridge to determine when to forward I/O transactions from one interface to the other. Reset to 0000h.

8.2.24 I/O LIMIT ADDRESS UPPER 16-BITS REGISTER – OFFSET 30h

BIT	FUNCTION	TYPE	DESCRIPTION
31:16	I/O Limit Address, Upper 16-bits [31:16]	RW	Defines the upper 16-bits of a 32-bit top address of an address range for the Bridge to determine when to forward I/O transactions from one interface to the other. Reset to 0000h.

8.2.25 CAPABILITY POINTER REGISTER – OFFSET 34h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Capability Pointer	RO	Pointer points to the PCI power management registers (40h). Reset to 40h.

8.2.26 INTERRUPT LINE REGISTER – OFFSET 3Ch

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Interrupt Line	RW	Reset to 00h.

8.2.27 INTERRUPT PIN REGISTER – OFFSET 3Ch

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Interrupt Pin	RO	The Switch implements INTA virtual wire interrupt signals to represent hot-plug events at downstream ports. The default value on the downstream ports may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 00h.

8.2.28 BRIDGE CONTROL REGISTER – OFFSET 3Ch

BIT	FUNCTION	TYPE	DESCRIPTION
16	Parity Error Response	RW	0b: Ignore Poisoned TLPs on the secondary interface 1b: Enable the Poisoned TLPs reporting and detection on the secondary interface Reset to 0b.
17	S_SERR# enable	RW	0b: Disables the forwarding of EER_COR, ERR_NONFATAL and ERR_FATAL from secondary to primary interface 1b: Enables the forwarding of EER_COR, ERR_NONFATAL and ERR_FATAL from secondary to primary interface Reset to 0b.
18	ISA Enable	RW	0b: Forwards downstream all I/O addresses in the address range defined by the

BIT	FUNCTION	TYPE	DESCRIPTION
			I/O Base, I/O Base, and Limit registers 1b: Forwards upstream all I/O addresses in the address range defined by the I/O Base and Limit registers that are in the first 64KB of PCI I/O address space (top 768 bytes of each 1KB block) Reset to 0b.
19	VGA Enable	RW	0b: Ignores access to the VGA memory or IO address range 1b: Forwards transactions targeted at the VGA memory or IO address range VGA memory range starts from 000A 0000h to 000B FFFFh VGA IO addresses are in the first 64KB of IO address space. AD [9:0] is in the ranges 3B0 to 3BBh and 3C0h to 3DFh. Reset to 0b.
20	VGA 16-bit decode	RW	0b: Executes 10-bit address decoding on VGA I/O accesses 1b: Executes 16-bit address decoding on VGA I/O accesses Reset to 0b.
21	Master Abort Mode	RO	Does not apply to PCI Express. Must be hardwired to 0b.
22	Secondary Bus Reset	RW	0b: Does not trigger a hot reset on the corresponding PCI Express Port 1b: Triggers a hot reset on the corresponding PCI Express Port At the downstream port, it asserts PORT_RST# to the attached downstream device. At the upstream port, it asserts the PORT_RST# at all the downstream ports. Reset to 0b.
23	Fast Back-to-Back Enable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
24	Primary Master Timeout	RO	Does not apply to PCI Express. Must be hardwired to 0b.
25	Secondary Master Timeout	RO	Does not apply to PCI Express. Must be hardwired to 0b.
26	Master Timeout Status	RO	Does not apply to PCI Express. Must be hardwired to 0b.
27	Discard Timer SERR# enable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
31:28	Reserved	RsvdP	Not Support.

8.2.29 POWER MANAGEMENT CAPABILITY REGISTER – OFFSET 40h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Enhanced Capabilities ID	RO	Read as 01h to indicate that these are power management enhanced capability registers.
15:8	Next Item Pointer	RO	The pointer points to the Vital Protocol Data (VPD) capability register / Message capability register. Reset to 5Ch (Upstream Port). Reset to 4Ch (Downstream Ports).
18:16	Power Management Revision	RO	Read as 011b to indicate the device is compliant to Revision 1.2 of *PCI Power Management Interface Specifications.*
19	PME# Clock	RO	Does not apply to PCI Express. Must be hardwired to 0b.
20	Reserved	RsvdP	Not Support.
21	Device Specific Initialization	RO	Read as 0b to indicate Switch does not have device specific initialization requirements. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM.
24:22	AUX Current	RO	Reset as 111b to indicate the Switch needs 375 mA in D3 state. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM.
25	D1 Power State Support	RO	Read as 1b to indicate Switch supports the D1 power management state. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM.
26	D2 Power State Support	RO	Read as 1b to indicate Switch supports the D2 power management state. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM.
31:27	PME# Support	RO	Read as 1_1111b to indicate Switch supports the forwarding of PME# message in all power states. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM.

8.2.30 POWER MANAGEMENT DATA REGISTER – OFFSET 44h

BIT	FUNCTION	TYPE	DESCRIPTION
1:0	Power State	RW	Indicates the current power state of the Switch. Writing a value of D0 when the previous state was D3 cause a hot reset without asserting DWNRST_L. 00b: D0 state 01b: D1 state 10b: D2 state 11b: D3 hot state Reset to 00b.
2	Reserved	RsvdP	Not Support.
3	No_Soft_Reset	RO	When set, this bit indicates that device transitioning from D3hot to D0 does not perform an internal reset. When clear, an internal reset is performed when power state transits from D3hot to D0. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 1b.
7:4	Reserved	RsvdP	Not Support.
8	PME# Enable	RW	When asserted, the Switch will generate the PME# message. Reset to 1'b0.
12:9	Data Select	RW	Select data registers. Reset to 0h.
14:13	Data Scale	RO	Reset to 00b.
15	PME Status	RO	Read as 0b as the PME# message is not implemented.

8.2.31 PPB SUPPORT EXTENSIONS – OFFSET 44h

BIT	FUNCTION	TYPE	DESCRIPTION
21:16	Reserved	RO	Reset to 00_0000b.
22	B2_B3 Support for $D3_{HOT}$	RO	Does not apply to PCI Express. Must be hardwired to 0b.
23	Bus Power / Clock Control Enable	RO	Does not apply to PCI Express. Must be hardwired to 0b.

8.2.32 DATA REGISTER – OFFSET 44h

BIT	FUNCTION	TYPE	DESCRIPTION
31:24	Data Register	RO	Data Register. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 00h.

8.2.33 MSI CAPABILITY REGISTER – OFFSET 4Ch (Downstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Enhanced Capabilities ID	RO	Read as 05h to indicate that this is message signal interrupt capability register.
15:8	Next Item Pointer	RO	Pointer points to the Vendor specific capability register. Reset to 64h.

8.2.34 MESSAGE CONTROL REGISTER – OFFSET 4Ch (Downstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
16	MSI Enable	RW	0b: The function is prohibited from using MSI to request service 1b: The function is permitted to use MSI to request service and is prohibited from using its INTx # pin Reset to 0b.
19:17	Multiple Message Capable	RO	Read as 000b.
22:20	Multiple Message Enable	RW	Reset to 000b.
23	64-bit address capable	RO	0b: The function is not capable of generating a 64-bit message address 1b: The function is capable of generating a 64-bit message address Reset to 1b.
31:24	Reserved	RsvdP	Not Support.

8.2.35 MESSAGE ADDRESS REGISTER – OFFSET 50h (Downstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
1:0	Reserved	RsvdP	Not Support.
31:2	Message Address	RW	If the message enable bit is set, the contents of this register specify the DWORD aligned address for MSI memory write transaction. Reset to 0000_0000h.

8.2.36 MESSAGE UPPER ADDRESS REGISTER – OFFSET 54h (Downstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Message Upper Address	RW	This register is only effective if the device supports a 64-bit message address is set. Reset to 0000_0000h.

8.2.37 MESSAGE DATA REGISTER – OFFSET 58h (Downstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Message Data	RW	Reset to 0000h.
31:16	Reserved	RsvdP	Not Support.

8.2.38 VPD CAPABILITY ID REGISTER – OFFSET 5Ch (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Enhanced Capabilities ID	RO	Read as 03h to indicate that these are VPD enhanced capability registers.
15:8	Next Item Pointer	RO	Pointer points to the Vendor specific capability register. Reset to 64h.

8.2.39 VPD REGISTER – OFFSET 5Ch (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
17:16	Reserved	RsvdP	Not Support.
23:18	VPD Address	RW	Contains DWORD address that is used to generate read or write cycle to the VPD table stored in EEPROM. Reset to 00_0000b.
29:24	Reserved	RsvdP	Not Support.
30	VPD Write Enable	RW	Enable the write operation. Reset to 0b.
31	VPD operation	RW	0b: Performs VPD read command to VPD table at the location as specified in VPD address. This bit is kept '0' and then set to '1' automatically after EEPROM cycle is finished 1b: Performs VPD write command to VPD table at the location as specified in VPD address. This bit is kept '1' and then set to '0' automatically after EEPROM cycle is finished. Reset to 0b.

8.2.40 VPD DATA REGISTER – OFFSET 60h (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	VPD Data	RW	When read, it returns the last data read from VPD table at the location as specified in VPD Address. When written, it places the current data into VPD table at the location as specified in VPD Address. Reset to 0000_0000h.

8.2.41 VENDOR SPECIFIC CAPABILITY REGISTER – OFFSET 64h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Enhanced Capabilities ID	RO	Read as 09h to indicate that these are vendor specific capability registers.
15:8	Next Item Pointer	RO	Pointer points to the SSID/SSVID capability register. Reset to B0h.
31:16	Length Information	RO	The length field provides the information for number of bytes in the capability structure (including the ID and Next pointer bytes). Reset to 34h.

8.2.42 XPIP_CSR0 – OFFSET 68h (Test Purpose Only)

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	XPIP_CSR0	RW	The default value for bit [14:13] may be changed by auto-loading from EEPROM. Bit[1]: Enable to change LTSSM Role 1b: enable to change LTSSM role 0b: disable to change LTSSM role Bit[2]: Disable hot reset (Upstream Port Only) 1b: do not fire hot reset to downstream ports if upstream port link is down 0b: do fire hot reset to downstream ports if upstream port link is down Bit[3]: LTSSM CFG_DN_Port Select 1b: set LTSSM role to packet switch downstream port 0b: set LTSSM role to packet switch upstream port Reset to 0400_1060h.

8.2.43 XPIP_CSR1 – OFFSET 6Ch (Test Purpose Only)

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	XPIP_CSR1	RW	Reset to 0400_0800h.

8.2.44 REPLAY TIME-OUT COUNTER – OFFSET 70h

BIT	FUNCTION	TYPE	DESCRIPTION
11:0	User Replay Timer	RW	A 12-bit register contains a user-defined value. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 000h.
12	Enable User Replay Timer	RW	When asserted, the user-defined replay time-out value is be employed. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 0b.
13	Power Management Capability Disable	RO	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 0b.
14	MSI Capability Disable	RO	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 0b.
15	Reserved	RsvdP	Not Support.

8.2.45 ACKNOWLEDGE LATENCY TIMER – OFFSET 70h

BIT	FUNCTION	TYPE	DESCRIPTION
29:16	User ACK Latency Timer	RW	A 14-bit register contains a user-defined value. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 0000h.
30	Enable User ACK Latency	RW	When asserted, the user-defined ACK latency value is be employed. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 0b.

BIT	FUNCTION	TYPE	DESCRIPTION
31	VGA Decode Enable	RO	Enable the VGA range decodes. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 1b.

8.2.46 SWITCH OPERATION MODE – OFFSET 74h (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
0	Store-Forward	RW	When set, a store-forward mode is used. Otherwise, the chip is working under cut-through mode. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 0b.
2:1	Cut-through Threshold	RW	Cut-through Threshold. When forwarding a packet from low-speed port to high-speed mode, the chip provides the capability to adjust the forwarding threshold. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. 00b: the threshold is set at the middle of forwarding packet 01b: the threshold is set ahead 1-cycle of middle point 10b: the threshold is set ahead 2-cycle of middle point. 11b: the threshold is set ahead 3-cycle of middle point. Reset to 01b.
3	Port Arbitration Mode	RW	When set, the round-robin arbitration will stay in the arbitrated port even if the credit is not enough but request is pending. When clear, the round-robin arbitration will always go to the requesting port, which the outgoing credit is enough for the packet queued in the port. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 0b.
4	Credit Update Mode	RW	When set, the frequency of releasing new credit to the link partner will be all types per update. When clear, the frequency of releasing new credit to the link partner will be type oriented per update. The default value may be changed by SMBus, I2C or auto-loading from EEPROM. Reset to 0b.
5	Ordering on Different Egress Port Mode	RW	When set, there has ordering rule on packets for different egress port. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 0b.
6	Ordering on Different Tag of Completion Mode	RW	When set, there has ordering rule between completion packet with different tag. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 0b.
7	NonPost TLP Store-Forward	RO	When set, for Non-port TLP store-forward mode is used . Otherwise, Non-post TLP is working under cut-through mode. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 0b.
13:8	Power Management Control Parameter	RW	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 00_0001b.
14	RX Polarity Inversion Disable	RO	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 0b.

BIT	FUNCTION	TYPE	DESCRIPTION
15	Compliance Pattern Parity Control Disable	RO	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 0b.
20:16	C_DRV_LVL_3P5_NOM	RO	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 1_0011b.
25:21	C_DRV_LVL_6P0_NOM	RO	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 1_0011b.
30:26	C_DRV_LVL_HALF_NOM	RO	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 0_0010b.
31	Reserved	RsvdP	Not Support.

8.2.47 SWITCH OPERATION MODE – OFFSET 74h (Downstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Reserved	RsvdP	Not Support.
13:8	Power Management Control Parameter	RW	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 00_0001b.
14	RX Polarity Inversion Disable	RO	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 0b.
15:31	Reserved	RsvdP	Not Support.

8.2.48 XPIP_CSR2 – OFFSET 78h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	FTS Number	RO	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 80h.
9:8	Scrambler Control	RO	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 00b.
10	L0s	RO	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 0b.
11	Compliance to Detect	RO	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 0b.
13:12	Change_Speed_Sel	RO	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 00b.
14	Change_Speed_En	RO	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 0b.
15	Reserved	RsvdP	Not Support.

8.2.49 PHY PARAMETER 1 – OFFSET 78h (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
20:16	C_EMP_POST_ GEN1_3P5_NOM	RO	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 1_0101b.
25:21	C_EMP_POST_ GEN2_3P5_NOM	RO	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 1_0101b.
30:26	C_EMP_POST_ GEN2_6P0_NOM	RO	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 1_1101b.
31	Reserved	RsvdP	Not Support.

8.2.50 PHY PARAMETER 2 – OFFSET 7Ch

BIT	FUNCTION	TYPE	DESCRIPTION
3:0	C_TX_PHY_ LATENACY	RO	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. It is set by Upstream Port Only. Reset to 0111b.
6:4	C_REC_DETEC_ USEC	RO	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. It is set by Upstream Port Only. Reset to 010b.
7	Reserved	RsvdP	Not Support.
8	P_CDR_FREQLOOP _EN	RO	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 1b.
10:9	P_CDR_ THRESHOLD	RO	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 10b.
12:11	P_CDR_FREQLOOP _GAIN	RO	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 11b.
15:13	Reserved	RsvdP	Not Support.
16	P_DRV_LVL_MGN _DELATA_EN	RO	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 0b.
17	P_DRV_LVL_NOM _DELATA_EN	RO	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 0b.
18	P_EMP_POST_MGN _DELATA_EN	RO	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 0b.
19	P_EMP_POST_NOM _DELATA_EN	RO	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 0b.
21:20	P_RX_SIGDET_ LVL	RO	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 01b.

BIT	FUNCTION	TYPE	DESCRIPTION
25:22	P_RX_EQ_1	RO	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 0110b.
29:26	P_RX_EQ_2	RO	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 1000b.
30	P_TXSWING	RO	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 0b.
31	Reserved	RsvdP	Not Support.

8.2.51 XPIP_CSR3 – OFFSET 80h

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	XPIP_CSR3	RW	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 000F_0000h.

8.2.52 XPIP_CSR4 – OFFSET 84h (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	XPIP_CSR4	RO	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 0000_0000h.

8.2.53 XPIP_CSR5 – OFFSET 88h

BIT	FUNCTION	TYPE	DESCRIPTION
29:0	XPIP_CSR5[29:0]	RO	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. It is set by Upstream Port Only. Bit[11]: UP_CFG_Reset Select 0b: cfg data will be reset upon the link down of upstream port 1b: cfg data is not affected when link down of upstream port Reset to 3308_3333h.
30	DO_CHG_DATA_ RATE_CTRL	RW	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 1b (Upstream Port). Reset to 0b (Downstream Ports).
31	Gen1_Cap_Only	RW	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 0b.

8.2.54 TL_CSR – OFFSET 8Ch

BIT	FUNCTION	TYPE	DESCRIPTION
0	TX_SOF_FORM	RO	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. It is set by Upstream Port Only. Reset to 0b.
1	PM Data Select Register R/W Capability	RO	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. It is set by Upstream Port Only. Reset to 0b.
2	ARBITER_ABORT_SEL	RO	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. It is set by Upstream Port Only. Reset to 1b.
3	4K Boundary Check Enable	RO	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. It is set by Upstream Port Only. Reset to 0b.
4	FIFOERR_FIX_SEL	RO	Reset to 1b.
5	MW Overpass Disable	RW	The default value may be changed by SMBus, I2C or auto-loading from EEPROM. It is set by Upstream Port Only. Reset to 0b.
6	Ordering Frozen Disable	RW	Disable the RO ordering rule. The default value may be changed by auto-loading from EEPROM. It is set by Upstream Port Only. Reset to 0b.
7	GNT_FAIL2IDLE	RO	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. It is set by Upstream Port Only. Reset to 1b.
8:9	DO_CHG_DATA_CNT_SEL	RO	The trying number for doing change data rate. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 00b.
10	Port Disable	RO	Disable this port. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 0b.
11	Reset Select	RO	Reset select (upstream port only). The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 1b.
12	ARB_VCFLG_SEL	RO	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. It is set by Upstream Port Only. Reset to 1b.
15:13	Reserved	RsvdP	Not Support.
23:16	XPIP_CSR6[7:0]	RO	XPIP_CSR6 Value. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Bit[0]: Disable phy error retrain 1b: disable phy error retrain function 0b: enable phy error retrain function Reset to 79h.
25:24	REV_TS_CTR	RO	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 00b.
29:26	MAC Control Parameter	RO	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. It is set by Upstream Port Only. Reset to 0h.
30	Reserved	RsvdP	Not Support.

BIT	FUNCTION	TYPE	DESCRIPTION
31	P35_GEN2_MODE	RO	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 0b.

8.2.55 PHY PARAMETER 3 – OFFSET 90h

BIT	FUNCTION	TYPE	DESCRIPTION
6:0	PHY Parameter 3 (Per Lane)	RO	PHY's Lane mode. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 00h.
14:7	Reserved	RsvdP	Not Support.
31:15	PHY Parameter 3 (Global)	RO	PHY's delta value setting. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. It is set by Upstream Port Only. Reset to 0_0001h.

8.2.56 PHY PARAMETER 4 - OFFSET 94h (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	PHY TX Margin Parameter	RO	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 116Bh.
31:16	Reserved	RsvdP	Not Support.

8.2.57 OPERATION MODE – OFFSET 98h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Operation Mode	RO	Bit[0]: SROM_BYPASS Bit[1]: IDDQB Bit[2]: FAST_MODE Bit[3]: DEBUG_MODE Bit[4]: PHY_MODE Bit[7:5]: PKG_SEL[2:0] Bit[8]: SCAN_MODE Bit[15:9]: Reserved Reset to 0002h in 505 mode. Reset to 0022h in 606 mode.
23:16	Clock Buffer Control	RO	For reference clock buffer control. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. It is set by Upstream Port Only. Reset to 7Fh in 606 mode. Reset to 5Fh in 505 mode.
27:24	L1PM Option	RO	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 0h.
31:28	Reserved	RsvdP	Not Support.

8.2.58 DEVICE SPECIFIC POWER MANAGEMENT EVENT– OFFSET 9Ch (Downstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
0	Device Specific PME Capability	RO	1b indicate enable device specific PME. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 1b.
1	PME Turnoff Message Request	R/W	Request to send PME turnoff message. Reset to 0b.
2	Port Power	R/W	Control GPIO[4:0] pins when Device Specific PME Capability is enabled. Downstream port 1 controls GPIO[0], Downstream port 2 controls GPIO[1], … and so on. Reset to 1b.
3	Port Reset	R/W	This bit when reset asserts an active low reset signal to the attached device. When set, the reset signal is de-asserted. Reset to 1b.
15:4	Reserved	RsvdP	Not Support.
17:16	Link Status	RO	These two bits represent the link status of device connected to the downstream port. 00b: L0 01b: L0s 10b: L1 11b: L2/L3 Reset to 00b.
31:18	Reserved	RsvdP	Not Support.

8.2.59 EEPROM CONTROL REGISTER – OFFSET A0h (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
0	EEPROM Start	RW	Starts the EEPROM read or write cycle. Reset to 0b.
3:1	EEPROM Command	RW	Sends the command to the EEPROM. 001b: write STATUS register 010b: EEPROM write 011b: EEPROM read 100b: disable write operation 101b: read STATUS register 110b: enable the write operation Reset to 000b.
4	EEPROM Autoload Status	RO	0b: EEPROM autoload was unsuccessful or is disabled 1b: EEPROM autoload occurred successfully after PREST. Configuration registers were loaded with values stored in the EEPROM Reset to 0b.
5	EEPROM Autoload Disable	RW	0b: EEPROM autoload enabled 1b: EEPROM autoload disabled Reset to 1b.

BIT	FUNCTION	TYPE	DESCRIPTION
7:6	EEPROM Clock Rate	RW	Determines the frequency of the EEPROM clock, which is derived from the primary clock. 00b: Reserved 01b: PEXCLK / 64 (PEXCLK is 250MHz) 10b: Reserved 11b: Test Mode Reset to 01b.
8	EEPROM Status[0]: Write In Process	RO	Indicate whether the eeprom is busy with write a operation. Reset to 0b.
9	EEPROM Status[1]: Write Enable Latch	RO	Indicate the status of the write enable latch. Reset to 0b.
10	EEPROM Status[2]: Block Protection 0	R/W	Indicate the block is currently write protected. Reset to 0b.
11	EEPROM Status[3]: Block Protection 1	R/W	Indicate the block is currently write protected. Reset to 0b.
14:12	EEPROM Status[6:4]]:	RO	Reset to 000b.
15	EEPROM Status[7] Write Protect Enable	R/W	Write enable Protect bit. Reset to 0b.

8.2.60 EEPROM ADDRESS REGISTER – OFFSET A4h (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	EEPROM Address	RW	Contains the EEPROM address. Reset to 0000h.

8.2.61 EEPROM DATA REGISTER – OFFSET A4h (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
31:16	EEPROM Data	RW	Contains the EEPROM data. Reset to 0000h.

8.2.62 DEBUGOUT CONTROL REGISTER – OFFSET A8h (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
4:0	Debug Mode Select	RW	Debug mode select. Reset to 0_0000b.
7:5	Debug Port Select	RW	Debug port select. Reset to 000b.
8	Debug Output Start	RW	Start to select debug output data. Reset to 0b.
23:9	Reserved	RsvdP	Support.
31:24	LED Debug	WO	Reset to 00h.

8.2.63 DEBUGOUT DATA REGISTER – OFFSET ACh (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Debug Output Data	RO	Contains the debug output data. When Debug Mode Select is set to 0Ch (A8h.bit[4:0]), this register will show LTSSM state machine. bit[0]=1… the port is in Detect state bit[1]=1… the port is in Polling state bit[2]=1… the port is in Config state bit[3]=1… the port is in L0 state (link up) bit[4]=1… the port is in L0s state bit[5]=1… the port is in L1 state bit[6]=1…the port is in L2 state bit[7]=1… the port is in Disabled state bit[8]=1… the port is in Hot_Reset state bit[9]=1… the port is in Loopback state bit[10]=1… the port is in Recovery state Reset to 0000_0000h.

8.2.64 SSID/SSVID CAPABILITY REGISTER – OFFSET B0h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	SSID/SSVID Capabilities ID	RO	Read as 0Dh to indicate that these are SSID/SSVID capability registers.
15:8	Next Item Pointer	RO	Pointer points to the PCI Express capability register. Reset to C0h.

8.2.65 SUBSYSTEM VENDOR ID REGISTER – OFFSET B4h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	SSVID	RO	It indicates the sub-system vendor id. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 0000h.

8.2.66 SUBSYSTEM ID REGISTER – OFFSET B4h

BIT	FUNCTION	TYPE	DESCRIPTION
31:16	SSID	RO	It indicates the sub-system device id. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 0000h.

8.2.67 GPIO CONTROL REGISTER – OFFSET B8h (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
0	GPIO [0] Input	HwInt RO	State of GPIO [0] pin. Reset to 1b.

BIT	FUNCTION	TYPE	DESCRIPTION
1	GPIO [0] Output Enable	RW	0b: GPIO [0] is an input pin 1b: GPIO [0] is an output pin Reset to 0b.
2	GPIO [0] Output Register	RW	Value of this bit will be output to GPIO [0] pin if GPIO [0] is configured as an output pin. This register is valid when Device Specific PME Capability of downstream port 1 is disabled. Reset to 0b
3	Reserved	RsvdP	Not Support.
4	GPIO [1] Input	HwInt RO	State of GPIO [1] pin. Reset to 1b.
5	GPIO [1] Output Enable	RW	0b: GPIO [1] is an input pin 1b: GPIO [1] is an output pin Reset to 0b.
6	GPIO [1] Output Register	RW	Value of this bit will be output to GPIO [1] pin if GPIO [1] is configured as an output pin. This register is valid when Device Specific PME Capability of downstream port 2 is disabled. Reset to 0b.
7	Reserved	RsvdP	Not Support.
8	GPIO [2] Input	HwInt RO	State of GPIO [2] pin. Reset to 1b.
9	GPIO [2] Output Enable	RW	0b: GPIO [2] is an input pin 1b: GPIO [2] is an output pin Reset to 0b.
10	GPIO [2] Output Register	RW	Value of this bit will be output to GPIO [2] pin if GPIO [2] is configured as an output pin. Reset to 0b.
11	Reserved	RsvdP	Not Support.
12	GPIO [3] Input	HWInit RO	State of GPIO [3] pin. Reset to 1b.
13	GPIO [3] Output Enable	RW	0b: GPIO [3] is an input pin 1b: GPIO [3] is an output pin Reset to 0b.
14	GPIO [3] Output Register	RW	Value of this bit will be output to GPIO [3] pin if GPIO [3] is configured as an output pin. Reset to 0b.
15	Reserved	RsvdP	Not Support.
16	GPIO [4] Input	HwInt RO	State of GPIO [4] pin. Reset to 1b.
17	GPIO [4] Output Enable	RW	0b: GPIO [4] is an input pin 1b: GPIO [4] is an output pin Reset to 0b
18	GPIO [4] Output Register	RW	Value of this bit will be output to GPIO [4] pin if GPIO [4] is configured as an output pin. Reset to 0b.
19	Reserved	RsvdP	Not Support.
20	GPIO [5] Input	HwInt RO	State of GPIO [5] pin. Reset to 1b.

BIT	FUNCTION	TYPE	DESCRIPTION
21	GPIO [5] Output Enable	RW	0b: GPIO [5] is an input pin 1b: GPIO [5] is an output pin Reset to 0b.
22	GPIO [5] Output Register	RW	Value of this bit will be output to GPIO [5] pin if GPIO [5] is configured as an output pin. Reset to 0b.
23	Reserved	RsvdP	Not Support.
24	GPIO [6] Input	HwInt RO	State of GPIO [6] pin. Reset to 1b.
25	GPIO [6] Output Enable	RW	0b: GPIO [6] is an input pin 1b: GPIO [6] is an output pin Reset to 0b.
26	GPIO [6] Output Register	RW	Value of this bit will be output to GPIO [6] pin if GPIO [6] is configured as an output pin. Reset to 0b.
27	Reserved	RsvdP	Not Support.
28	GPIO [7] Input	HwInt RO	State of GPIO [7] pin. Reset to 1b.
29	GPIO [7] Output Enable	RW	0b: GPIO [7] is an input pin 1b: GPIO [7] is an output pin Reset to 0b.
30	GPIO [7] Output Register	RW	Value of this bit will be output to GPIO [7] pin if GPIO [7] is configured as an output pin. Reset to 0b.
31	Reserved	RsvdP	Not Support.

8.2.68 PCI EXPRESS CAPABILITY ID REGISTER – OFFSET C0h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Enhanced Capabilities ID	RO	Read as 10h to indicate that these are PCI express enhanced capability registers.
15:8	Next Item Pointer	RO	Read as 00h. No other ECP registers.
19:16	Capability Version	RO	Read as 2h to indicate the device is compliant to Revision .2.0 of *PCI Express Base Specifications.*
23:20	Device/Port Type	RO	Indicates the type of PCI Express logical device. Reset to 0101b (Upstream port). Reset to 0110b (Downstream ports).
24	Slot Implemented	RO	When set, indicates that the PCIe Link associated with this Port is connected to a slot. This field is valid for downstream ports of the Switch. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 0b (Upstream port). Reset to 1b (Downstream ports).
29:25	Interrupt Message Number	RO	Read as 0b. No MSI messages are generated in the transparent mode.
31:30	Reserved	RsvdP	Not Support.

8.2.69 DEVICE CAPABILITIES REGISTER – OFFSET C4h

BIT	FUNCTION	TYPE	DESCRIPTION
2:0	Max_Payload_Size Supported	RO	Indicates the maximum payload size that the device can support for TLPs. Each port of the Switch supports 512 bytes max payload size. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. 000b: 128 bytes 001b: 256 bytes 010b: 512 bytes Others: Reserved Reset to 001b.
4:3	Phantom Functions Supported	RO	Indicates the support for use of unclaimed function numbers as Phantom functions. Read as 00b, since the Switch does not act as a requester. Reset to 00b.
5	Extended Tag Field Supported	RO	Indicates the maximum supported size of Tag field as a Requester. Read as 0, since the Switch does not act as a requester. Reset to 0b.
8:6	Endpoint L0s Acceptable Latency	RO	Acceptable total latency that an Endpoint can withstand due to the transition from L0s state to the L0 state. For Switch, the ASPM software would not check this value. Reset to 000b.
11:9	Endpoint L1 Acceptable Latency	RO	Acceptable total latency that an Endpoint can withstand due to the transition from L1 state to the L0 state. For Switch, the ASPM software would not check this value. Reset to 000b.
14:12	Reserved	RsvdP	Not Support.
15	Role_Based Error Reporting	RO	When set, indicates that the device implements the functionality originally defined in the Error Reporting ECN. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 1b.
17:16	Reserved	RsvdP	Not Support.
25:18	Captured Slot Power Limit Value	RO	It applies to Upstream Port only. In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by slot. This value is set by the Set_Slot_Power_Limit message or hardwired to 00h. Reset to 00h.
27:26	Captured Slot Power Limit Scale	RO	It applies to Upstream Port only. Specifies the scale used for the Slot Power Limit Value. This value is set by the Set_Slot_Power_Limit message or hardwired to 00b. Reset to 00b.
31:28	Reserved	RsvdP	Not Support.

8.2.70 DEVICE CONTROL REGISTER – OFFSET C8h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Correctable Error Reporting Enable	RW	0b: Disable Correctable Error Reporting 1b: Enable Correctable Error Reporting Reset to 0b.
1	Non-Fatal Error Reporting Enable	RW	0b: Disable Non-Fatal Error Reporting 1b: Enable Non-Fatal Error Reporting Reset to 0b.

BIT	FUNCTION	TYPE	DESCRIPTION
2	Fatal Error Reporting Enable	RW	0b: Disable Fatal Error Reporting 1b: Enable Fatal Error Reporting Reset to 0b.
3	Unsupported Request Reporting Enable	RW	0b: Disable Unsupported Request Reporting 1b: Enable Unsupported Request Reporting Reset to 0b.
4	Enable Relaxed Ordering	RO	When set, it permits the device to set the Relaxed Ordering bit in the attribute field of transaction. Since the Switch can not either act as a requester or alter the content of packet it forwards, this bit always returns '0' when read. Reset to 0b.
7:5	Max_Payload_Size	RW	This field sets maximum TLP payload size for the device. Permissible values that can be programmed are indicated by the Max_Payload_Size Supported in the Device Capabilities register. Any value exceeding the Max_Payload_Size Supported written to this register results into clamping to the Max_Payload_Size Supported value. Reset to 000b.
8	Extended Tag Field Enable	RW	Does not apply to PCI Express Switch. Returns '0' when read. Reset to 0b.
9	Phantom Function Enable	RW	Does not apply to PCI Express Switch. Returns '0' when read. Reset to 0b.
10	Auxiliary (AUX) Power PM Enable	RW	When set, indicates that a device is enabled to draw AUX power independent of PME AUX power. Reset to 0b.
11	Enable No Snoop	RO	When set, it permits to set the No Snoop bit in the attribute field of transaction. Since the Switch can not either act as a requester or alter the content of packet it forwards, this bit always returns '0' when read. Reset to 0b.
14:12	Max_Read_ Request_Size	RO	This field sets the maximum Read Request size for the device as a Requester. Since the Switch does not generate read request by itself, these bits are hardwired to 000b. Reset to 000b.
15	Reserved	RsvdP	Not Support.

8.2.71 DEVICE STATUS REGISTER – OFFSET C8h

BIT	FUNCTION	TYPE	DESCRIPTION
16	Correctable Error Detected	RW1C	Asserted when correctable error is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. Reset to 0b.
17	Non-Fatal Error Detected	RW1C	Asserted when non-fatal error is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. Reset to 0b.
18	Fatal Error Detected	RW1C	Asserted when fatal error is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. Reset to 0b.
19	Unsupported Request Detected	RW1C	Asserted when unsupported request is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. Reset to 0b.

BIT	FUNCTION	TYPE	DESCRIPTION
20	AUX Power Detected	RO	Asserted when the AUX power is detected by the Switch Reset to 1b.
21	Transactions Pending	RO	Each port of Switch does not issue Non-posted Requests on its own behalf, so this bit is hardwired to 0b. Reset to 0b.
31:22	Reserved	RsvdP	Not Support.

8.2.72 LINK CAPABILITIES REGISTER – OFFSET CCh

BIT	FUNCTION	TYPE	DESCRIPTION
3:0	Maximum Link Speed	RO	Indicates the maximum speed of the Express link. 0001b: 2.5 Gb/s 0010b: 5.0 Gb/s Reset to 0010b.
9:4	Maximum Link Width	RO	Indicates the maximum width of the given PCIe Link. Reset to 00_0010b (x2) (Upstream port in 506 mode). Reset to 00_0001b (x1) (Upstream port in 505/606 mode and Downstream Ports).
11:10	Active State Power Management (ASPM) Support	RO	Indicates the level of ASPM supported on the given PCIe Link. Each port of Switch supports L0s and L1 entry. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 00b.
14:12	L0s Exit Latency	RO	Indicates the L0s exit latency for the given PCIe Link. The length of time this port requires to complete transition from L0s to L0 is in the range of 256ns to less than 512ns. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 011b.
17:15	L1 Exit Latency	RO	Indicates the L1 exit latency for the given PCIe Link. The length of time this port requires to complete transition from L1 to L0 is in the range of 16us to less than 32us. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 000b.
18	Clock Power Management	RO	For upstream port, a value of 1b indicates that component tolerates the removal of any reference clock via CLKREQ#. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. For downstream ports, this bit must be hardwired to 0b. Reset to 1b.
19	Surprise Down Capability Enable	RO	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 0b.
20	Data Link Layer Active Reporting Capable	RO	For downstream ports, this bit must be set to 1b if the component supports the optional capability of reporting the DL_Active state of the Data Link Control and Management State Machine. For a hot-plug capable downstream port, this bit must be set to 1b. For upstream port, this bit must be hardwired to 0b. Reset to 0b (Upstream Port). Reset to 1b (Downstream Ports).

BIT	FUNCTION	TYPE	DESCRIPTION
21	Link BW Notify Cap.	RO	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 0b (Upstream Port). Reset to 0b (Downstream Ports).
23:21	Reserved	RsvdP	Not Support.
31:24	Port Number	RO	Indicates the PCIe Port Number for the given PCIe Link. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 00h for Port 0. Reset to 01h for Port 1. Reset to 02h for Port 2. Reset to 03h for Port 3. Reset to 04h for Port 4. Reset to 05h for Port 5.

8.2.73 LINK CONTROL REGISTER – OFFSET D0h

BIT	FUNCTION	TYPE	DESCRIPTION
1:0	Active State Power Management (ASPM) Control	RW	00b: ASPM is Disabled 01b: L0s Entry Enabled 10b: L1 Entry Enabled 11b: L0s and L1 Entry Enabled Note that the receiver must be capable of entering L0s even when the field is disabled. Reset to 00b.
2	Reserved	RsvdP	Not Support.
3	Read Completion Boundary (RCB)	RO	Does not apply to PCI Express Switch. Returns '0' when read. Reset to 0b.
4	Link Disable	RW	At upstream port, it is not allowed to disable the link, so this bit is hardwired to '0'. For downstream ports, it disables the link when this bit is set. Reset to 0b.
5	Retrain Link	RW	At upstream port, it is not allowed to retrain the link, so this bit is hardwired to 1'b0. For downstream ports, it initiates Link Retraining when this bit is set. This bit always returns 0b when read.
6	Common Clock Configuration	RW	0b: The components at both ends of a link are operating with asynchronous reference clock 1b: The components at both ends of a link are operating with a distributed common reference clock Reset to 0b.
7	Extended Synch	RW	When set, it transmits 4096 FTS ordered sets in the L0s state for entering L0 state and transmits 1024 TS1 ordered sets in the L1 state for entering L0 state. Reset to 0b.
8	Enable Clock Power Management	RW	0b: clock power management is disable and must hold CLKREQ# low. 1b: device is permitted to use CLKREQ# to power manage Link clock. Reset to 0b. For downstream ports must hardwire this bit to 0b.
9	HW Autonomous Width Disable	RW	Reset to 0b.
10	Link Bandwidth Management Interrupt Enable	RO/RW	For upstream port is RO. For downstream port is RW. Reset to 0b.

BIT	FUNCTION	TYPE	DESCRIPTION
11	Link Autonomous Bandwidth Interrupt Enable	RO/RW	For upstream port is RO. For downstream port is RW. Reset to 0b.
15:12	Reserved	RsvdP	Not Support.

8.2.74 LINK STATUS REGISTER – OFFSET D0h

BIT	FUNCTION	TYPE	DESCRIPTION
19:16	Link Speed	RO	Indicate the negotiated speed of the Express link. 0001b: 2.5 Gb/s 0010b: 5.0 Gb/s Reset to 0010b.
25:20	Negotiated Link Width	RO	Indicates the negotiated width of the given PCIe link. Reset to 00_0001b (x1).
26	Training Error	RO	When set, indicates a Link training error occurred. This bit is cleared by hardware upon successful training of the link to the L0 link state. Reset to 0b.
27	Link Training	RO	When set, indicates the link training is in progress. Hardware clears this bit once link training is complete. Reset to 1b.
28	Slot Clock Configuration	RO	0b: the Switch uses an independent clock irrespective of the presence of a reference on the connector 1b: the Switch uses the same reference clock that the platform provides on the connector The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 1b.
29	Data Link Layer Link Active	RO	Indicates the status of the Data Link Control and Management State Machine. 1b: indicate the DL_Active state 0b: otherwise Reset to 0b.
30	Link Bandwidth Management Status	RW1C	Reset to 0b.
31	Link Autonomous Bandwidth Status	RW1C	Reset 0b.

8.2.75 SLOT CAPABILITIES REGISTER – OFFSET D4h (Downstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
0	Attention Button Present	RO	When set, it indicates that an Attention Button is implemented on the chassis for this slot. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 1b.
1	Power Controller Present	RO	When set, it indicates that a Power Controller is implemented for this slot. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 1b.

BIT	FUNCTION	TYPE	DESCRIPTION
2	MRL Sensor Present	RO	When set, this bit indicates that an MRL Sensor is implemented on the chassis for this slot. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 1b.
3	Attention Indicator Present	RO	When set, it indicates that an Attention Indicator is implemented on the chassis for this slot. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 1b.
4	Power Indicator Present	RO	When set, it indicates that a Power Indicator is implemented on the chassis for this slot. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 1b.
5	Hot-Plug Surprise	RO	When set, it indicates that a device present in this slot might be removed from the system without any prior notification. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 0b.
6	Hot-Plug Capable	RO	When set, it indicates that this slot is capable of supporting Hot-Plug operation. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 1b.
14:7	Slot Power Limit Value	RW	It applies to downstream ports only. In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by slot. Writes to this register also cause the Port to send the Set_Slot_Power_Limit message. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 19h.
16:15	Slot Power Limit Scale	RW	It applies to downstream ports only. Specifies the scale used for the Slot Power Limit Value. Writes to this register also cause the Port to send the Set_Slot_Power_Limit message. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 00b.
18:17	Reserved	RsvdP	Not Support.
31:19	Physical Slot Number	RO	It indicates the physical slot number attached to this Port. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 0000h.

8.2.76 SLOT CONTROL REGISTER – OFFSET D8h (Downstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
0	Attention Button Pressed Enable	RW	When set, it enables the generation of Hot-Plug interrupt or wakeup event on an attention button pressed event. Reset to 0b.
1	Power Fault Detected Enable	RW	When set, it enables the generation of Hot-Plug interrupt or wakeup event on a power fault event. Reset to 0b.
2	MRL Sensor Enable	RW	When set, it enables the generation of Hot-Plug interrupt or wakeup even Reset to 0b.
3	Presence Detect Changed Enable	RW	When set, it enables the generation of Hot-Plug interrupt or wakeup event on a presence detect changed event. Reset to 0b.

BIT	FUNCTION	TYPE	DESCRIPTION
4	Command Completed Interrupt Enable	RW	When set, it enables the generation of Hot-Plug interrupt when the Hot-Plug Controller completes a command. Reset to 0b.
5	Hot-Plug Interrupt Enable	RW	When set, it enables generation of Hot-Plug interrupt on enabled Hot-Plug events. Reset to 0b.
7:6	Attention Indicator Control	RW	Controls the display of Attention Indicator. 00b: Reserved 01b: On 10b: Blink 11b: Off Writes to this register also cause the Port to send the ATTENTION_INDICATOR_* Messages. Reset to 11b.
9:8	Power Indicator Control	RW	Controls the display of Power Indicator. 00b: Reserved 01b: On 10b: Blink 11b: Off Writes to this register also cause the Port to send the POWER_INDICATOR_* Messages. Reset to 01b.
10	Power Controller Control	RW	0b: reset the power state of the slot (Power On) 1b: set the power state of the slot (Power Off) Reset to 0b.
11	EM_INTRELOCK Control	RW	Reset to 0b.
12	Data Link Layer State Changed Enable	RW	If the Data Link Layer Link Active capability is implemented, when set to 1b, this field enables software notification when Data Link Layer Link Active field is changed. Reset to 0b.
15:13	Reserved	RsvdP	Not Support.

8.2.77 SLOT STATUS REGISTER – OFFSET D8h (Downstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
16	Attention Button Pressed	RW1C	When set, it indicates the Attention Button is pressed. Reset to 0b.
17	Power Fault Detected	RW1C	When set, it indicates a Power Fault is detected. Reset to 0b.
18	MRL Sensor Changed	RO	When set, it indicates a MRL Sensor Changed is detected. Reset to 0b.
19	Presence Detect Changed	RW1C	When set, it indicates a Presence Detect Changed is detected. Reset to 0b.
20	Command Completed	RW1C	When set, it indicates the Hot-Plug Controller completes an issued command. Reset to 0b.

BIT	FUNCTION	TYPE	DESCRIPTION
21	MRL Sensor State	RO	Reflects the status of MRL Sensor. 0b: MRL Closed 1b: MRL Opened Reset to 0b.
22	Presence Detect State	RO	Indicates the presence of a card in the slot. 0b: Slot Empty 1b: Card Present in slot This register is implemented on all downstream ports that implement slots. For downstream ports not connected to slots (where the Slot Implemented bit of the PCI Express Capabilities register is 0b), this bit returns 1b. Reset to 0b.
23	Reserved	RsvdP	Not Support.
24	Data Link Layer State Changed	RW1C	This bit is set when the value reported in the Data Link Layer Link Active field of the Link Status register is changed.
31:25	Reserved	RsvdP	Not Support.

8.2.78 DEVICE CAPABILITIES REGISTER 2 – OFFSET E4h

BIT	FUNCTION	TYPE	DESCRIPTION
10:0	Device Capabilities 2	RO	Reset to 000h.
11	LTR Mechanism Supported	RO	A value of 1b indicates support for the optional Latency Tolerance Reporting (LTR) mechanism. Reset to 1b.
12	Flow Control Update Type LTR Capability Enable	RO	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 0b.
17:13	Device Capabilities 2	RO	Reset to 00h.
19:18	OBFF Supported	RO	This field indicates if OBFF is supported. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 00b.
31:20	Device Capabilities 2	RO	Reset to 000h.

8.2.79 DEVICE CONTROL REGISTER 2 – OFFSET E8h

BIT	FUNCTION	TYPE	DESCRIPTION
9:0	Device Control 2	RO	Reset to 000h.
10	LTR Mechanism Enable	RW	Enable LTR Mechanism. Reset to 0b.
12:11	Device Control 2	RO	Reset to 00b.
14:13	OBFF Enable	RW	Enable OBFF Mechanism and select the signaling method. Reset to 00b.
15	Device Control 2	RO	Reset to 0b.

8.2.80 DEVIDE STATUS REGISTER 2 – OFFSET E8h

BIT	FUNCTION	TYPE	DESCRIPTION
31:16	Device Status 2	RO	Reset to 0000h.

8.2.81 LINK CAPABILITIES REGISTER 2 – OFFSET ECh

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Link Capabilities 2	RO	Reset to 0000_0000h.

8.2.82 LINK CONTROL REGISTER 2 – OFFSET F0h

BIT	FUNCTION	TYPE	DESCRIPTION
3:0	Target Link Speed	RW	Reset to 0010b.
4	Enter Compliance	RW	Reset to 0b.
5	HW_AutoSpeed_Dis	RW	Reset to 0b.
6	Select_Deemp	RO	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. It is valid for downstream port only. Reset to 0b (Upstream Port). Reset to 1b (Downstream Ports).
9:7	Tran_Margin	RW	Reset to 000b.
10	Enter Modify Compliance	RW	Reset to 0b.
11	Compliance SOS	RW	Reset to 0b.
12	Compliance_Deemp	RW	Reset to 0b.
15:13	Reserved	RsvdP	Not Support.

8.2.83 LINK STATUS REGISTER 2 – OFFSET F0h

BIT	FUNCTION	TYPE	DESCRIPTION
16	Current De-emphasis Level	RO	Reset to 0b (Upstream Port). Reset to 1b (Downstream Ports).
31:17	Link Status 2	RO	Reset to 0000h.

8.2.84 SLOT CAPABILITIES REGISTER 2 – OFFSET F4h

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Slot Capabilities 2	RO	Reset to 0000_0000h.

8.2.85 SLOT CONTORL REGISTER 2 – OFFSET F8h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Slot Control 2	RO	Reset to 0000h.

8.2.86 SLOT STATUS REGISTER 2 – OFFSET F8h

BIT	FUNCTION	TYPE	DESCRIPTION
31:16	Slot Status 2	RO	Reset to 0000h.

8.2.87 PCI EXPRESS ADVANCED ERROR REPORTING CAPABILITY REGISTER – OFFSET 100h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Extended Capabilities ID	RO	Read as 0001h to indicate that these are PCI express extended capability registers for advance error reporting.
19:16	Capability Version	RO	Read as 1h. Indicates PCI-SIG defined PCI Express capability structure version number.
31:20	Next Capability Offset	RO	Pointer points to the PCI Express Extended VC capability register. Reset to 140h.

8.2.88 UNCORRECTABLE ERROR STATUS REGISTER – OFFSET 104h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Training Error Status	RW1C	When set, indicates that the Training Error event has occurred. Reset to 0b.
3:1	Reserved	RsvdP	Not Support.
4	Data Link Protocol Error Status	RW1C	When set, indicates that the Data Link Protocol Error event has occurred. Reset to 0b.
11:5	Reserved	RsvdP	Not Support.
12	Poisoned TLP Status	RW1C	When set, indicates that a Poisoned TLP has been received or generated. Reset to 0b.
13	Flow Control Protocol Error Status	RW1C	When set, indicates that the Flow Control Protocol Error event has occurred. Reset to 0b.
14	Completion Timeout Status	RW1C	When set, indicates that the Completion Timeout event has occurred. Reset to 0b.
15	Completer Abort Status	RW1C	When set, indicates that the Completer Abort event has occurred. Reset to 0b.
16	Unexpected Completion Status	RW1C	When set, indicates that the Unexpected Completion event has occurred. Reset to 0b.
17	Receiver Overflow Status	RW1C	When set, indicates that the Receiver Overflow event has occurred. Reset to 0b.
18	Malformed TLP Status	RW1C	When set, indicates that a Malformed TLP has been received. Reset to 0b.
19	ECRC Error Status	RW1C	When set, indicates that an ECRC Error has been detected. Reset to 0b.
20	Unsupported Request Error Status	RW1C	When set, indicates that an Unsupported Request event has occurred. Reset to 0b.
21	ACS Violation Status	RW1C	When set, indicates that an ACS Violation event has occurred. Reset to 0b.
31:21	Reserved	RsvdP	Not Support.

8.2.89 UNCORRECTABLE ERROR MASK REGISTER – OFFSET 108h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Training Error Mask	RW	When set, the Training Error event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
3:1	Reserved	RsvdP	Not Support.
4	Data Link Protocol Error Mask	RW	When set, the Data Link Protocol Error event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
11:5	Reserved	RsvdP	Not Support.
12	Poisoned TLP Mask	RW	When set, an event of Poisoned TLP has been received or generated is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
13	Flow Control Protocol Error Mask	RW	When set, the Flow Control Protocol Error event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
14	Completion Timeout Mask	RW	When set, the Completion Timeout event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
15	Completer Abort Mask	RW	When set, the Completer Abort event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
16	Unexpected Completion Mask	RW	When set, the Unexpected Completion event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
17	Receiver Overflow Mask	RW	When set, the Receiver Overflow event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
18	Malformed TLP Mask	RW	When set, an event of Malformed TLP has been received is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
19	ECRC Error Mask	RW	When set, an event of ECRC Error has been detected is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
20	Unsupported Request Error Mask	RW	When set, the Unsupported Request event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
21	ACS Violation Mask	RW	Reset to 0b.
31:22	Reserved	RsvdP	Not Support.

8.2.90 UNCORRECTABLE ERROR SEVERITY REGISTER – OFFSET 10Ch

BIT	FUNCTION	TYPE	DESCRIPTION
0	Training Error Severity	RW	0b: Non-Fatal 1b: Fatal Reset to 1b.
3:1	Reserved	RsvdP	Not Support.

BIT	FUNCTION	TYPE	DESCRIPTION
4	Data Link Protocol Error Severity	RW	0b: Non-Fatal 1b: Fatal Reset to 1b.
11:5	Reserved	RsvdP	Not Support.
12	Poisoned TLP Severity	RW	0b: Non-Fatal 1b: Fatal Reset to 0b.
13	Flow Control Protocol Error Severity	RW	0b: Non-Fatal 1b: Fatal Reset to 1b.
14	Completion Timeout Error Severity	RW	0b: Non-Fatal 1b: Fatal Reset to 0b.
15	Completer Abort Severity	RW	0b: Non-Fatal 1b: Fatal Reset to 0b.
16	Unexpected Completion Severity	RW	0b: Non-Fatal 1b: Fatal Reset to 0b.
17	Receiver Overflow Severity	RW	0b: Non-Fatal 1b: Fatal Reset to 1b.
18	Malformed TLP Severity	RW	0b: Non-Fatal 1b: Fatal Reset to 1b.
19	ECRC Error Severity	RW	0b: Non-Fatal 1b: Fatal Reset to 0b.
20	Unsupported Request Error Severity	RW	0b: Non-Fatal 1b: Fatal Reset to 0b.
21	ACS Violation Severity	RW	0b: Non-Fatal 1b: Fatal Reset to 0b.
31:21	Reserved	RsvdP	Not Support.

8.2.91 CORRECTABLE ERROR STATUS REGISTER – OFFSET 110 h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Receiver Error Status	RW1C	When set, the Receiver Error event is detected. Reset to 0b.
5:1	Reserved	RsvdP	Not Support.
6	Bad TLP Status	RW1C	When set, the event of Bad TLP has been received is detected. Reset to 0b.
7	Bad DLLP Status	RW1C	When set, the event of Bad DLLP has been received is detected. Reset to 0b.
8	REPLAY_NUM Rollover Status	RW1C	When set, the REPLAY_NUM Rollover event is detected. Reset to 0b.
11:9	Reserved	RsvdP	Not Support.

BIT	FUNCTION	TYPE	DESCRIPTION
12	Replay Timer Timeout Status	RW1C	When set, the Replay Timer Timeout event is detected. Reset to 0b.
13	Advisory Non-Fatal Error Status	RW1C	When set, the Advisory Non-Fatal Error event is detected. Reset to 0b.
31:14	Reserved	RsvdP	Not Support.

8.2.92 CORRECTABLE ERROR MASK REGISTER – OFFSET 114 h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Receiver Error Mask	RW	When set, the Receiver Error event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
5:1	Reserved	RsvdP	Not Support.
6	Bad TLP Mask	RW	When set, the event of Bad TLP has been received is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
7	Bad DLLP Mask	RW	When set, the event of Bad DLLP has been received is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
8	REPLAY_NUM Rollover Mask	RW	When set, the REPLAY_NUM Rollover event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
11:9	Reserved	RsvdP	Not Support.
12	Replay Timer Timeout Mask	RW	When set, the Replay Timer Timeout event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
13	Advisory Non-Fatal Error Mask	RW	When set, the Advisory Non-Fatal Error event is not logged in the Header Long register and not issued as an Error Message to RC either. Reset to 1b.
31:14	Reserved	RsvdP	Not Support.

8.2.93 ADVANCE ERROR CAPABILITIES AND CONTROL REGISTER – OFFSET 118h

BIT	FUNCTION	TYPE	DESCRIPTION
4:0	First Error Pointer	RO	It indicates the bit position of the first error reported in the Uncorrectable Error Status register. Reset to 0_0000b.
5	ECRC Generation Capable	RO	When set, it indicates the Switch has the capability to generate ECRC. Reset to 1b.
6	ECRC Generation Enable	RW	When set, it enables the generation of ECRC when needed. Reset to 0b.
7	ECRC Check Capable	RO	When set, it indicates the Switch has the capability to check ECRC. Reset to 1b.
8	ECRC Check Enable	RW	When set, the function of checking ECRC is enabled. Reset to 0b.
31:9	Reserved	RsvdP	Not Support.

8.2.94 HEADER LOG REGISTER – OFFSET From 11Ch to 128h

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	1st DWORD	RO	Hold the 1st DWORD of TLP Header. The Head byte is in big endian.
63:32	2nd DWORD	RO	Hold the 2nd DWORD of TLP Header. The Head byte is in big endian.
95:64	3rd DWORD	RO	Hold the 3rd DWORD of TLP Header. The Head byte is in big endian.
127:96	4th DWORD	RO	Hold the 4th DWORD of TLP Header. The Head byte is in big endian.

8.2.95 PCI EXPRESS VIRTUAL CHANNEL CAPABILITY REGISTER – OFFSET 140h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Extended Capabilities ID	RO	Read as 0002h to indicate that these are PCI express extended capability registers for virtual channel.
19:16	Capability Version	RO	Read as 1h. Indicates PCI-SIG defined PCI Express capability structure version number.
31:20	Next Capability Offset	RO	Pointer points to the PCI Express Power Budgeting Capability register. Reset to 20Ch.

8.2.96 PORT VC CAPABILITY REGISTER 1 – OFFSET 144h

BIT	FUNCTION	TYPE	DESCRIPTION
2:0	Extended VC Count	RO	It indicates the number of extended Virtual Channels in addition to the default VC supported by the Switch. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 000b.
3	Reserved	RsvdP	Not Support.
6:4	Low Priority Extended VC Count	RO	It indicates the number of extended Virtual Channels in addition to the default VC belonging to the low-priority VC (LPVC) group. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 000b.
7	Reserved	RsvdP	Not Support.
9:8	Reference Clock	RO	It indicates the reference clock for Virtual Channels that support time-based WRR Port Arbitration. Defined encoding is 00b for 100 ns reference clock. Reset to 00b.
11:10	Port Arbitration Table Entry Size	RO	Read as 2'b10 to indicate the size of Port Arbitration table entry in the device is 4 bits. Reset to 10b.
31:12	Reserved	RsvdP	Not Support.

8.2.97 PORT VC CAPABILITY REGISTER 2 – OFFSET 148h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	VC Arbitration Capability	RO	It indicates the types of VC Arbitration supported by the device for the LPVC group. This field is valid when LPVC is greater than 0. The Switch supports Hardware fixed arbitration scheme, e.g., Round Robin and Weight Round Robin arbitration with 32 phases in LPVC. Reset to 00h if offset 144h.bit[2:0]=0. Reset to 03h if offset 144h.bit[2:0]=1.
23:8	Reserved	RsvdP	Not Support.

BIT	FUNCTION	TYPE	DESCRIPTION
31:24	VC Arbitration Table Offset	RO	It indicates the location of the VC Arbitration Table as an offset from the base address of the Virtual Channel Capability register in the unit of DQWD (16 bytes). Reset to 00h if offset 144h.bit[2:0]=0. Reset to 03h if offset 144h.bit[2:0]=1.

8.2.98 PORT VC CONTROL REGISTER – OFFSET 14Ch

BIT	FUNCTION	TYPE	DESCRIPTION
0	Load VC Arbitration Table	RW	When set, the programmed VC Arbitration Table is applied to the hardware. This bit always returns 0b when read. Reset to 0b.
3:1	VC Arbitration Select	RW	This field is used to configure the VC Arbitration by selecting one of the supported VC Arbitration schemes. The valid values for the schemes supported by Switch are 0b and 1b. Other value than these written into this register will be treated as default. Reset to 000b.
15:4	Reserved	RsvdP	Not Support.

8.2.99 PORT VC STATUS REGISTER – OFFSET 14Ch

BIT	FUNCTION	TYPE	DESCRIPTION
16	VC Arbitration Table Status	RO	When set, it indicates that any entry of the VC Arbitration Table is written by software. This bit is cleared when hardware finishes loading values stored in the VC Arbitration Table after the bit of “Load VC Arbitration Table” is set. Reset to 0b.
31:17	Reserved	RsvdP	Not Support.

8.2.100 VC RESOURCE CAPABILITY REGISTER (0) – OFFSET 150h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Port Arbitration Capability	RO	It indicates the types of Port Arbitration supported by the VC resource. The Switch supports Hardware fixed arbitration scheme, e.g., Round Robin, Weight Round Robin (WRR) arbitration with 128 phases (3~4 enabled ports) and Time-based WRR with 128 phases (3~4 enabled ports). Note that the Time-based WRR is only valid in VC1. Reset to 09h.
13:8	Reserved	RsvdP	Not Support.
14	Advanced Packet Switching	RO	When set, it indicates the VC resource only supports transaction optimized for Advanced Packet Switching (AS). Reset to 0b.
15	Reject Snoop Transactions	RO	This bit is not applied to PCIe Switch. Reset to 0b.
22:16	Maximum Time Slots	RO	It indicates the maximum numbers of time slots (minus one) are allocated for Isochronous traffic. Reset to 7Fh.
23	Reserved	RsvdP	Not Support.

BIT	FUNCTION	TYPE	DESCRIPTION
31:24	Port Arbitration Table Offset	RO	It indicates the location of the Port Arbitration Table (n) as an offset from the base address of the Virtual Channel Capability register in the unit of DQWD (16 bytes). Reset to 04h for Port Arbitration Table (0).

8.2.101 VC RESOURCE CONTROL REGISTER (0) – OFFSET 154h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	TC/VC Map	RW	This field indicates the TCs that are mapped to the VC resource. Bit locations within this field correspond to TC values. When the bits in this field are set, it means that the corresponding TCs are mapped to the VC resource. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to FFh.
15:8	Reserved	RsvdP	Not Support.
16	Load Port Arbitration Table	RW	When set, the programmed Port Arbitration Table is applied to the hardware. This bit always returns 0b when read. Reset to 0b
19:17	Port Arbitration Select	RW	This field is used to configure the Port Arbitration by selecting one of the supported Port Arbitration schemes. The permissible values for the schemes supported by Switch are 000b and 011b at VC0, other value than these written into this register will be treated as default. Reset to 000b.
23:20	Reserved	RsvdP	Not Support.
26:24	VC ID	RO	This field assigns a VC ID to the VC resource. Reset to 000b.
30:27	Reserved	RsvdP	Not Support.
31	VC Enable	RW	0b: disables this Virtual Channel 1b: enables this Virtual Channel Reset to 1b.

8.2.102 VC RESOURCE STATUS REGISTER (0) – OFFSET 158h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Reserved	RsvdP	Not Support.
16	Port Arbitration Table Status	RO	When set, it indicates that any entry of the Port Arbitration Table is written by software. This bit is cleared when hardware finishes loading values stored in the Port Arbitration Table after the bit of "Load Port Arbitration Table" is set. Reset to 0b.
17	VC Negotiation Pending	RO	When set, it indicates that the VC resource is still in the process of negotiation. This bit is cleared after the VC negotiation is complete. Reset to 0b.
31:18	Reserved	RsvdP	Not Support.

8.2.103 VC RESOURCE CAPABILITY REGISTER (1) – OFFSET 15Ch

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Port Arbitration Capability	RO	It indicates the types of Port Arbitration supported by the VC resource. The Switch supports Hardware fixed arbitration scheme, e.g., Round Robin, Weight Round Robin (WRR) arbitration with 128 phases (3~4 enabled ports) and Time-based WRR with 128 phases (3~4 enabled ports). Note that the Time-based WRR is only valid in VC1. Reset to 00h if offset 144h.bit[2:0]=0. Reset to 19h if offset 144h.bit[2:0]=1.
13:8	Reserved	RsvdP	Not Support.
14	Advanced Packet Switching	RO	When set, it indicates the VC resource only supports transaction optimized for Advanced Packet Switching (AS). Reset to 0b.
15	Reject Snoop Transactions	RO	This bit is not applied to PCIe Switch. Reset to 0b.
22:16	Maximum Time Slots	RO	It indicates the maximum numbers of time slots (minus one) are allocated for Isochronous traffic. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 00h if offset 144h.bit[2:0]=0. Reset to 7Fh if offset 144h.bit[2:0]=1.
23	Reserved	RsvdP	Not Support.
31:24	Port Arbitration Table Offset	RO	It indicates the location of the Port Arbitration Table (n) as an offset from the base address of the Virtual Channel Capability register in the unit of DQWD (16 bytes). Reset to 00h for Port Arbitration Table (1) if offset 144h.bit[2:0]=0. Reset to 08h for Port Arbitration Table (1) if offset 144h.bit[2:0]=1.

8.2.104 VC RESOURCE CONTROL REGISTER (1) – OFFSET 160h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	TC/VC Map	RW (Exception for bit0)	This field indicates the TCs that are mapped to the VC resource. Bit locations within this field correspond to TC values. When the bits in this field are set, it means that the corresponding TCs are mapped to the VC resource. Bit 0 of this filed is read-only and must be set to "0" for the VC1. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 00h.
15:8	Reserved	RsvdP	Not Support.
16	Load Port Arbitration Table	RW	When set, the programmed Port Arbitration Table is applied to the hardware. This bit always returns 0b when read. Reset to 0b.
19:17	Port Arbitration Select	RW	This field is used to configure the Port Arbitration by selecting one of the supported Port Arbitration schemes. The permissible values for the schemes supported by Switch are 000b, 011b and 100b at VC1, other value than these written into this register will be treated as default. Reset to 000b.
23:20	Reserved	RO	Reset to 4'h0.
26:24	VC ID	RW	This field assigns a VC ID to the VC resource. Reset to 000h if offset 144h.bit[2:0]=0. Reset to 001h if offset 144h.bit[2:0]=1.
30:27	Reserved	RsvdP	Not Support.
31	VC Enable	RW	0b: disables this Virtual Channel 1b: enables this Virtual Channel Reset to 0b.

8.2.105 VC RESOURCE STATUS REGISTER (1) – OFFSET 164h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Reserved	RsvdP	Not Support.
16	Port Arbitration Table Status	RO	When set, it indicates that any entry of the Port Arbitration Table is written by software. This bit is cleared when hardware finishes loading values stored in the Port Arbitration Table after the bit of "Load Port Arbitration Table" is set. Reset to 0b.
17	VC Negotiation Pending	RO	When set, it indicates that the VC resource is still in the process of negotiation. This bit is cleared after the VC negotiation is complete. Reset to 0b.
31:18	Reserved	RsvdP	Not Support.

8.2.106 VC ARBITRATION TABLE REGISTER – OFFSET 170h

The VC arbitration table is a read-write register array that contains a table for VC arbitration. Each table entry allocates four bits, of which three bits are used to represent VC ID and one bit is reserved. A total of 32 entries are used to construct the VC arbitration table. The layout for this register array is shown below.

Table 8-1 Register Array Layout for VC Arbitration

31 - 28	27 - 24	23 - 20	19 - 16	15 - 12	11 - 8	7 - 4	3 - 0	Byte Location
Phase [7]	Phase [6]	Phase [5]	Phase [4]	Phase [3]	Phase [2]	Phase [1]	Phase [0]	00h
Phase [15]	Phase [14]	Phase [13]	Phase [12]	Phase [11]	Phase [10]	Phase [9]	Phase [8]	04h
Phase [23]	Phase [22]	Phase [21]	Phase [20]	Phase [19]	Phase [18]	Phase [17]	Phase [16]	08h
Phase [31]	Phase [30]	Phase [29]	Phase [28]	Phase [27]	Phase [26]	Phase [25]	Phase [24]	0Ch

8.2.107 PORT ARBITRATION TABLE REGISTER (0) and (1) – OFFSET 180h and 1C0h

The Port arbitration table is a read-write register array that contains a table for Port arbitration. Each table entry allocates two bits to represent Port Number. The table entry size is dependent on the number of enabled ports (refer to bit 10 and 11 of Port VC capability register 1). The arbitration table contains 128 entries if three or four ports are to be enabled. The following table shows the register array layout for the size of entry equal to two.

Table 8-2 Table Entry Size in 4 Bits

63 - 56	55 - 48	47 - 40	39 - 32	31 - 24	23 - 16	15 - 8	7 - 0	Byte Location
Phase [15:14]	Phase [13:12]	Phase [11:10]	Phase [9:8]	Phase [7:6]	Phase [5:4]	Phase [3:2]	Phase [1:0]	00h
Phase [31:30]	Phase [29:28]	Phase [27:26]	Phase [25:24]	Phase [23:22]	Phase [21:20]	Phase [19:18]	Phase [17:16]	08h
Phase [47:46]	Phase [45:44]	Phase [43:42]	Phase [41:40]	Phase [39:38]	Phase [37:36]	Phase [35:34]	Phase [33:32]	10h
Phase [63:62]	Phase [61:60]	Phase [59:58]	Phase [57:56]	Phase [55:54]	Phase [53:52]	Phase [51:50]	Phase [49:48]	18h
Phase [79:78]	Phase [77:76]	Phase [75:74]	Phase [73:72]	Phase [71:70]	Phase [69:68]	Phase [67:66]	Phase [65:64]	20h
Phase	Phase	Phase	Phase	Phase	Phase	Phase	Phase	28h

63 - 56	55 - 48	47 - 40	39 - 32	31 - 24	23 - 16	15 - 8	7 - 0	Byte Location
[95:94]	[93:92]	[91:90]	[89:88]	[87:86]	[85:84]	[83:82]	[81:80]	
Phase [111:110]	Phase [109:108]	Phase [107:106]	Phase [105:104]	Phase [103:102]	Phase [101:100]	Phase [99:98]	Phase [97:96]	30h
Phase [127:126]	Phase [125:124]	Phase [123:122]	Phase [121:120]	Phase [119:118]	Phase [117:116]	Phase [115:114]	Phase [113:112]	38h

8.2.108 PCI EXPRESS POWER BUDGETING CAPABILITY REGISTER – OFFSET 20Ch

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Extended Capabilities ID	RO	Read as 0004h to indicate that these are PCI express extended capability registers for power budgeting.
19:16	Capability Version	RO	Read as 1h. Indicates PCI-SIG defined PCI Express capability structure version number.
31:20	Next Capability Offset	RO	Pointer points to the PCI Express Extended ACS capability register /LTR capability register. Reset to 230h (Upstream Port). Reset to 220h (Downstream Ports).

8.2.109 DATA SELECT REGISTER – OFFSET 210h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Data Selection	RW	It indexes the power budgeting data reported through the data register. When 00h, it selects D0 Max power budget When 01h, it selects D0 Sustained power budget Other values would return zero power budgets, which means not supported Reset to 00h.
31:8	Reserved	RsvdP	Not Support.

8.2.110 POWER BUDGETING DATA REGISTER – OFFSET 214h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Base Power	RO	It specifies the base power value in watts. This value represents the required power budget in the given operation condition. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 04h.
9:8	Data Scale	RO	It specifies the scale to apply to the base power value. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 00b.
12:10	PM Sub State	RO	It specifies the power management sub state of the given operation condition. It is initialized to the default sub state. Reset to 000b.
14:13	PM State	RO	It specifies the power management state of the given operation condition. It defaults to the D0 power state. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 00b.
17:15	Type	RO	It specifies the type of the given operation condition. It defaults to the Maximum power state. Reset to 111b.

BIT	FUNCTION	TYPE	DESCRIPTION
20:18	Power Rail	RO	It specifies the power rail of the given operation condition. Reset to 010b.
31:21	Reserved	RsvdP	Not Support.

8.2.111 POWER BUDGET CAPABILITY REGISTER – OFFSET 218h

BIT	FUNCTION	TYPE	DESCRIPTION
0	System Allocated	RO	When set, it indicates that the power budget for the device is included within the system power budget. The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 0b.
31:1	Reserved	RsvdP	Not Support.

8.2.112 ACS EXTENDED CAPABILITY HEADER – OFFSET 220h (Downstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	PCI Express Extended Capability ID	RO	Read as 000Dh to indicate PCI Express Extended Capability ID for ACS Extended Capability.
19:16	Capability Version	RO	Must be 1h for this version.
31:20	Next Capability ID	RO	Pointer points to the PCI Express Extended L1PM Substates Extended Capability Header register. Reset to 240h.

8.2.113 ACS CAPABILITY REGISTER – OFFSET 224h (Downstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
0	ACS Source Validation	RO	Indicated the implements of ACS Source Validation. Reset to 1b.
1	ACS Translation Blocking	RO	Indicated the implements of ACS Translation Blocking. Reset to 1b.
2	ACS P2P Request Redirect	RO	Indicated the implements of ACS P2P Request Redirect. Reset to 1b.
3	ACS P2P Completion Redirect	RO	Indicated the implements of ACS P2P Completion Redirect. Reset to 1b.
4	ACS Upstream Forwarding	RO	Indicated the implements of ACS Upstream Forwarding. Reset to 1b.
5	ACS P2P Egress control	RO	Indicated the implements of ACS P2P Egress control. Reset to 1b.
6	ACS Direct Translated P2P	RO	Indicated the implements of ACS Direct Translated P2P. Reset to 1b.
7	Reserved	RsvdP	Not Support.
15:8	Egress Control Vector Size	RO	Encodings 01h – FFh directly indicate the number of applicable bits in the Egress Control Vector. Reset to 08h.

BIT	FUNCTION	TYPE	DESCRIPTION
16	ACS Source Validation Enable	RW	Enable the source validation. Reset to 0b.
17	ACS Translation Blocking Enable	RW	Enable ACS Translation Blocking. Reset to 0b.
18	ACS P2P Request Redirect	RW	Enable ACS P2P Request Redirect. Reset to 0b.
19	ACS P2P Completion Redirect Enable	RW	Enable ACS P2P Completion Redirect. Reset to 0b.
20	ACS Upstream Forwarding Enable	RW	Enable ACS Upstream Forwarding. Reset to 0b.
21	ACS P2P Egress control Enable	RW	Enable ACS P2P Egress control. Reset to 0b.
22	ACS Direct Translated P2P Enable	RW	Enable ACS Direct Translated P2P. Reset to 0b.
31:23	Reserved	RsvdP	Not Support.

8.2.114 EGRESS CONTROL VECTOR – OFFSET 228h (Downstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Egress Control Vector	RW	When a given bit is set, peer-to-peer requests targeting the associated Port are blocked or redirected. Reset to 00h.
31:8	Reserved	RsvdP	Not Support.

8.2.115 LTR EXTENDED CAPABILITY HEADER – OFFSET 230h (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	PCI Express Extended Capability ID	RO	Read as 0018h to indicate PCI Express Extended Capability ID for LTR Extended Capability.
19:16	Capability Version	RO	Must be 1h for this version.
31:20	Next Capability ID	RO	Pointer points to the PCI Express Extended L1PM Substates Extended Capability Header register. Reset to 240h.

8.2.116 MAX SNOOP LATENCY REGISTER – OFFSET 234h (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
9:0	Max Snoop Latency Value	RW	.Specifies the maximum snoop latency that a device is permitted to request Reset to 000h.
12:10	Max Snoop Latency Scale	RW	This register provides a scale for the value contained within the Maximum Snoop Latency Value field Reset to 000b.
15:13	Reserved	RsvdP	Not Support.

8.2.117 MAX NO-SNOOP LATENCY REGISTER – OFFSET 234h (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
25:16	Max No-Snoop Latency Value	RW	.Specifies the maximum no-snoop latency that a device is permitted to request Reset to 000h.
28:26	Max No-Snoop Latency Scale	RW	This register provides a scale for the value contained within the Maximum No-Snoop Latency Value field Reset to 000b.
31:29	Reserved	RsvdP	Not Support.

8.2.118 LI PM SUBSTATES EXTENDED CAPABILITY HEADER – OFFSET 240h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	PCI Express Extended Capability ID	RO	Read as 001Eh to indicate PCI Express Extended Capability ID for L1 PM Substates Extended Capability.
19:16	Capability Version	RO	Must be 1h for this version.
31:20	Next Capability ID	RO	Read as 000h. No other ECP registers.

8.2.119 L1 PM SUBSTATES CAPABILITY REGISTER – OFFSET 244h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Reserved	RsvdP	Not Support.
1	PCI-PM L1.1 Supported	RO	When set this bit indicates that PCI-PM L1.1 is supported and must be set by all ports implementing L1 OM Substates. The default value may be changed by SMBus, I2C or auto-loading from EEPROM. Reset to 1b.
2	Reserved	RsvdP	Not Support.
3	ASPM L1.1 Supported	RO	When set this bit indicates that ASPM L1.1 is supported. The default value may be changed by SMBus, I2C or auto-loading from EEPROM. Reset to 0b.
4	L1 PM Substates Supported	RO	When set this bit indicates that this port supports L1 PM Substates. The default value may be changed by SMBus, I2C or auto-loading from EEPROM. Reset to 1b.
31:5	Reserved	RsvdP	Not Support.

8.2.120 L1 PM SUBSTATES CONTROL 1 REGISTER – OFFSET 248h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Reserved	RsvdP	Not Support.
1	PCI-PM L1.1 Enable	RW	When set this bit enables PCI-PM L1.1. Required for both upstream and downstream ports. Reset to 0b.
2	Reserved	RsvdP	Not Support.
3	ASPM L1.1 Enable	RW	When set this bit enables ASPM L1.1. Required for both upstream and downstream ports. Reset to 0b.
31:4	Reserved	RsvdP	Not Support.

8.2.121 L1 PM SUBSTATES CONTROL 2 REGISTER – OFFSET 24Ch

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Reserved	RO	Reset to 0000_0000h.

8.2.122 LTSSM_CSR REGISTER – OFFSET 33Ch

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	LTSSM_CSR	RO	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 00h.
31:8	Reserved	RsvdP	Not Support.

8.2.123 HOTPLUG_CSR REGISTER – OFFSET 340h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Hotplug_CSR	RO	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 0000h.

8.2.124 MAC_CSR1 REGISTER – OFFSET 340h

BIT	FUNCTION	TYPE	DESCRIPTION
31:16	MAC_CSR1	RO	The default value may be changed by SMBUS, I2C or auto-loading from EEPROM. Reset to 0004h.

8.2.125 SMBUS CONTROL REGISTER – OFFSET 344h (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
0	SMBus Enable	HwInt RW	0b: disable SMBUS, enable I2C 1b: enable SMBUS Reset to 1b.
7:1	SMBUS Address	HwInt RW	Set SMBUS Address. Bit [7:4] reset to 1101b. Bit [3:1] are decided by the status of strapped pins (GPIO[7:5]).
8	Reserved	RsvdP	Not Support.
9	PEC Check Disable	RW	0b: enable PEC check 1b: disable PEC check Reset to 1b.
28:10	Reserved	RsvdP	Not Support.
29	PEC Check Fail	RW1C	0b: PEC check successfully 1b: PEC check failed Reset to 0b.
30	Unsupported SMBUS Command	RW1C	0b: supported command. 1b: unsupported command. Reset to 0b.
31	Reserved	RsvdP	Not Support.

8.2.126 CPLD FLOW CONTRL ENABLE REGISTER– OFFSET 350h (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
0	Reserved	RsvdP	Not Support.
1	Port 1 CPLD Flow Control Enable	RW	Enable port 1 CPLD flow control Reset to 0b.
2	Port 2 CPLD Flow Control Enable	RW	Enable port 2 CPLD flow control Reset to 0b.
3	Port 3 CPLD Flow Control Enable	RW	Enable port 3 CPLD flow control Reset to 0b.
4	Port 4 CPLD Flow Control Enable	RW	Enable port 4 CPLD flow control Reset to 0b.
5	Port 5 CPLD Flow Control Enable	RW	Enable port 5 CPLD flow control Reset to 0b.
31:6	Reserved	RsvdP	Not Support.

8.2.127 CPLD FLOW CONTROL THRESHOLD RGISTER – OFFSET 354h (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	X1 CPLD Flow Control Threshold	RW	Threshold for x1 link Reset to 0080h.
31:16	X2 CPLD Flow Control Threshold	RW	Threshold for x2 link Reset to 0200h.

8.2.128 CPLD FLOW CONTROL THRESHOLD RGISTER – OFFSET 358h (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	X4 CPLD Flow Control Threshold	RW	Threshold for x4 link Reset to 0800h.
31:16	Reserved	RsvdP	Not Support.

8.2.129 POWER DAVING DISABLE RGISTER – OFFSET 360h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Power Saving Disable	RW	Disable power saving. The default value may be changed by SMBus, I2C or audo-loading from EEPROM. Reset to 0b.
31:1	Reserved	RsvdP	Not Support.

8.2.130 LED DISPLAY CSR 364h (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
4:0	LED Display Mode Select	RW	Reset to 0_0000b.
5	LED Enable	RW	Reset to 0b.
6	LED Mode	RW	Reset to 0b.
31:7	Reserved	RsvdP	Not Support.

9 CLOCK SCHEME

The PI7C9X2G606PR requires 100MHz differential clock inputs through REFCLKP and REFCLKN Pins as shown in the following table.

Table 9-1 DC Electrical Characteristics

Symbol	Parameters	Min.	Typ.	Max.	Unit
F_{IN}	Reference Clock Frequency		100		MHz
T_{rise}/ T_{fall} [1]	Rise and Fall Time in 20-80%	175		700	ps
DT_{rise}/ DT_{fall} [1]	Rise and Fall Time Variation			125	ps
T_{pd}	Propagation Delay	2.5		6.5	ns
V_{swing} [1]	Voltage including overshoot	550		1150	mV
T_{DC} [2]	Duty Cycle	45		55	%

Note:
1 Measurement taken from Single Ended waveform.
2 Measurement taken from Differential waveform.

10 POWER MANAGEMENT

The PI7C9X2G606PR supports D0, D1, D2, D3-hot, and D3-cold Power States. The PCI Express Physical Link Layer of the PI7C9X606PR device supports the PCI Express Link Power Management with L0, L0s, L1, L2/L3 ready and L3 Power States.

Not only focusing on device or link level of power management, the PI7C9X2G606PR is implemented to facilitate platform-wise power saving by enabling the capability of Latency Tolerance Reporting (LTR) and Optimized Buffer Flush/Fill (OBFF) mechanisms to synchronize both Root Complex and Device entering or leaving power down state almost in the same time window. This can prevent from unconditionally waking up the Root Complex or device to make power saving much efficient.

PI7C9X2G606PR also supports ASPM (Active State Power Management) to facilitate the link power saving.

11 POWER SEQUENCE

As long as PERST# is active, all PCI Express functions are held in reset. The main supplies ramp up to their specified levels (2.5V). Sometime during this stabilization time, the REFCLK starts and stabilizes. After there has been time (100 ms) for the power and clock to become stable, PERST# is deasserted high and the PCI Express functions can start up.

It is recommended to power up the I/O voltage (2.5V) first and then the core voltage (1.0V) or power up I/O voltage and core voltage simultaneously.

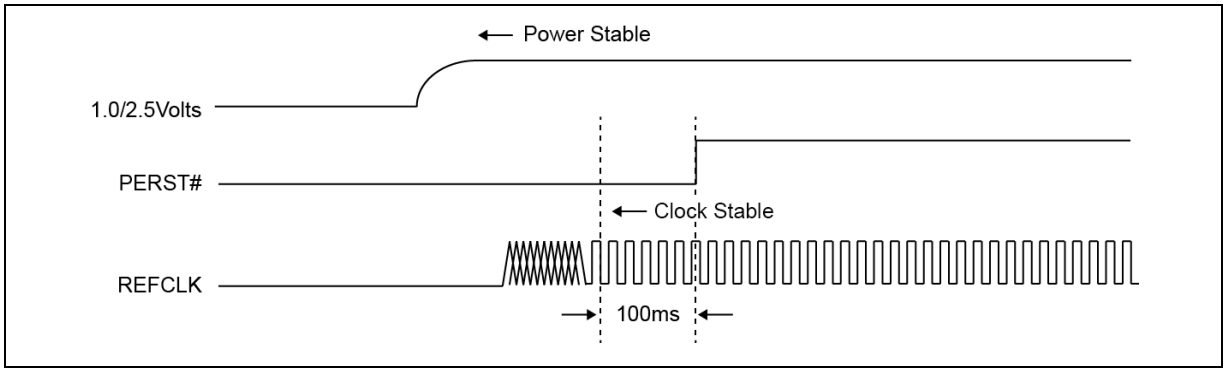


Figure 11-1 Initial Power-Up Sequence

Power-down sequence is the reverse of power-up sequence.

12 ELECTRICAL AND TIMING SPECIFICATIONS

12.1 ABSOLUTE MAXIMUM RATINGS

Table 12-1 Absolute Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Item	Absolute Max. Rating
Storage Temperature	-65°C to 150°C
Junction Temperature, Tj	125 °C
Digital core and analog supply voltage to ground potential (VDDC and AVDD)	-0.3v to 1.2v
Digital I/O and analog high supply voltage to ground potential (VDDR and AVDDH)	-0.3v to 3.8v
DC input voltage for Digital I/O signals	-0.3v to 3.8v
ESD Rating Human Body Model (JEDEC Class 2) Charge Device Model (JEDEC Class 3)	 2kv 500v

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

12.2 DC SPECIFICATIONS

Table 12-2 DC Electrical Characteristics

Symbol	Description	Min.	Typ.	Max.	Unit
VDDC	Digital Core Power	0.95	1.0	1.1	V
VDDR	Digital I/O Power	2.45	2.5	2.65	
AVDD	PCI Express Analog Power	0.95	1.0	1.1	
AVDDH	PCI Express Analog High Voltage Power	2.45	2.5	2.65	
V_{IH}	Input High Voltage	2.0		3.6	
V_{IL}	Input Low Voltage	-0.3		0.8	
V_{OH}	Output High Voltage	2.4	-	-	
V_{OL}	Output Low Voltage	-	-	0.4	
R_{PU}	Pull-up Resistor	63K	92K	142K	Ω
R_{PD}	Pull-down Resistor	57K	91K	159K	
$RST\#_{Slew}$ [1]	PERST_L Slew Rate	50			mV/ns

Note:
1. The min. value for PERST_L Slew Rate is 50 mV/ns, which translates to the requirement that the time for PERST_L from 0V to 2.5V should be less than 50 ns.

12.3 AC SPECIFICATIONS

Table 12-3 PCI Express Interface - Differential Transmitter (TX) Output (5.0 Gbps) Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Unit Interval	UI	199.94	200.0	200.06	ps
Differential p-p TX voltage swing	$V_{TX-DIFF-P-P}$	800	-	-	mV ppd
Low power differential p-p TX voltage swing	$V_{TX-DIFF-P-P-LOW}$	400	-	-	mV ppd
TX de-emphasis level ratio	$V_{TX-DE-RATIO-3.5dB}$	-3.0	-	-4.0	dB
TX de-emphasis level ratio	$V_{TX-DE-RATIO-6dB}$	-5.5		-6.5	dB
Transmitter Eye including all jitter sources	T_{TX-EYE}	0.75	-	-	UI

Parameter	Symbol	Min	Typ	Max	Unit
TX deterministic jitter > 1.5 MHz	$T_{TX-HF-DJ-DD}$	-	-	0.15	UI
TX RMS jitter < 1.5 MHz	$T_{TX-LF-RMS}$	-	-	3.0	Ps RMS
Transmitter rise and fall time	$T_{TX-RISE-FALL}$	0.15	-	-	UI
TX rise/fall mismatch	$T_{RF-MISMATCH}$	-	-	0.1	UI
Maximum TX PLL Bandwidth	BW_{TX-PLL}	-	-	16	MHz
Minimum TX PLL BW for 3dB peaking	$BW_{TX-PLL-LO-3DB}$	8	-	-	MHz
TX PLL peaking with 8 MHz min BW	$PKG_{TX-PLL1}$	-	-	3.0	dB
DC Differential TX Impedance	$Z_{TX-DIFF-DC}$	80	-	120	Ω
Transmitter Short-Circuit Current Limit	$I_{TX-SHORT}$	-	-	90	mA
TX DC Common Mode Voltage	$V_{TX-DC-CM}$	0	-	3.6	V
Absolute Delta of DC Common Mode Voltage During L0 and Electrical Idle	$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	0	-	100	mV
Absolute Delta of DC Common Mode Voltage between D+ and D–	$V_{TX-CM-DC-LINE-DELTA}$	0	-	25	mV
Electrical Idle Differential Peak Output Voltage	$V_{TX-IDLE-DIFF-AC-p}$	0	-	20	mV
DC Electrical Idle Differential Output Voltage	$V_{TX-IDLE-DIFF-DC}$	0	-	5	mV
The Amount of Voltage Change Allowed During Receiver Detection	$V_{TX-RCV-DETECT}$	-	-	600	mV
Lane-to-Lane Output Skew	$L_{TX-SKEW}$	-	-	500 ps + 4 UI	ps

Table 12-4 PCI Express Interface - Differential Transmitter (TX) Output (2.5 Gbps) Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Unit Interval	UI	399.88	400.0	400.12	ps
Differential p-p TX voltage swing	$V_{TX-DIFF-P-P}$	800	-	-	mV ppd
Low power differential p-p TX voltage swing	$V_{TX-DIFF-P-P-LOW}$	400	-	-	mV ppd
TX de-emphasis level ratio	$V_{TX-DE-RATIO}$	-3.0	-	-4.0	dB
Minimum TX eye width	T_{TX-EYE}	0.75	-	-	UI
Maximum time between the jitter median and max deviation from the median	$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	-	-	0.125	UI
Transmitter rise and fall time	$T_{TX-RISE-FALL}$	0.125	-	-	UI
Maximum TX PLL Bandwidth	BW_{TX-PLL}	-	-	22	MHz
Maximum TX PLL BW for 3dB peaking	$BW_{TX-PLL-LO-3DB}$	1.5	-	-	MHz
Absolute Delta of DC Common Mode Voltage During L0 and Electrical Idle	$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	0	-	100	mV
Absolute Delta of DC Common Mode Voltage between D+ and D–	$V_{TX-CM-DC-LINE-DELTA}$	0	-	25	mV
Electrical Idle Differential Peak Output Voltage	$V_{TX-IDLE-DIFF-AC-p}$	0	-	20	mV
The Amount of Voltage Change Allowed During Receiver Detection	$V_{TX-RCV-DETECT}$	-	-	600	mV
Transmitter DC Common Mode Voltage	$V_{TX-DC-CM}$	0	-	3.6	V
Transmitter Short-Circuit Current Limit	$I_{TX-SHORT}$	-	-	90	mA
DC Differential TX Impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω
Lane-to-Lane Output Skew	$L_{TX-SKEW}$	-	-	500 ps + 2 UI	ps

Table 12-5 PCI Express Interface - Differential Receiver (RX) Input (5.0 Gbps) Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Unit Interval	UI	199.94	200.0	200.06	ps
Differential RX Peak-to-Peak Voltage	$V_{RX-DIFF-PP-CC}$	120	-	1200	mV
Total jitter tolerance	TJ_{RX}	0.68	-	-	UI
Receiver DC common mode impedance	Z_{RX-DC}	40	-	60	Ω
RX AC Common Mode Voltage	$V_{RX-CM-AC-P}$	-	-	150	mV
Electrical Idle Detect Threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	-	175	mV

Table 12-6 PCI Express Interface - Differential Receiver (RX) Input (2.5 Gbps) Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Unit Interval	UI	399.88	400.0	400.12	ps
Differential RX Peak-to-Peak Voltage	$V_{RX-DIFF-PP-CC}$	175	-	1200	mV
Receiver eye time opening	T_{RX-EYE}	0.4	-	-	UI
Maximum time delta between median and deviation from median	$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	-	-	0.3	UI
Receiver DC common mode impedance	Z_{RX-DC}	40	-	60	Ω
DC differential impedance	$Z_{RX-DIFF-DC}$	80	-	120	Ω
RX AC Common Mode Voltage	$V_{RX-CM-AC-P}$	-	-	150	mV
DC input CM input impedance during reset or power down	$Z_{RX-HIGH-IMP-DC}$	200	-	-	kΩ
Electrical Idle Detect Threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	-	175	mV
Lane to Lane skew	$L_{RX-SKEW}$	-	-	20	ns

12.4 OPERATING AMBIENT TEMPERATURE

Table 12-7 Operating Ambient Temperature

(The Operating Ambient Temperature be associated with Chapter 13.)

Item	Low	High	Unit
Ambient Temperature with power applied	-40	85	°C

Note:
Exposure to high temperature conditions for extended periods of time may affect reliability.

12.5 POWER CONSUMPTION

Table 12-8 Power Consumption

Active Lane per Port	1.0VDDC		1.0VAVDD		2.5AVDDH		2.5VDDR		Total		Unit
	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max	
1/1/1/1/1/1	222	612	241	595	108	119	5	6	576	1,331	mW

Test Conditions:
- Typical power measured under the conditions of 1.0V/ 2.5V power rail without device usage on all downstream ports.
- Maximum power measured under the conditions of 1.1V/ 2.75V with PCIe2 devices usage on all downstream ports
- Ambient Temperature at 25°C
- Power consumption in the table is a reference, be affected by various environment, bus traffic and power supply etc.

13 THERMAL DATA

The information described in this section is provided for reference only.

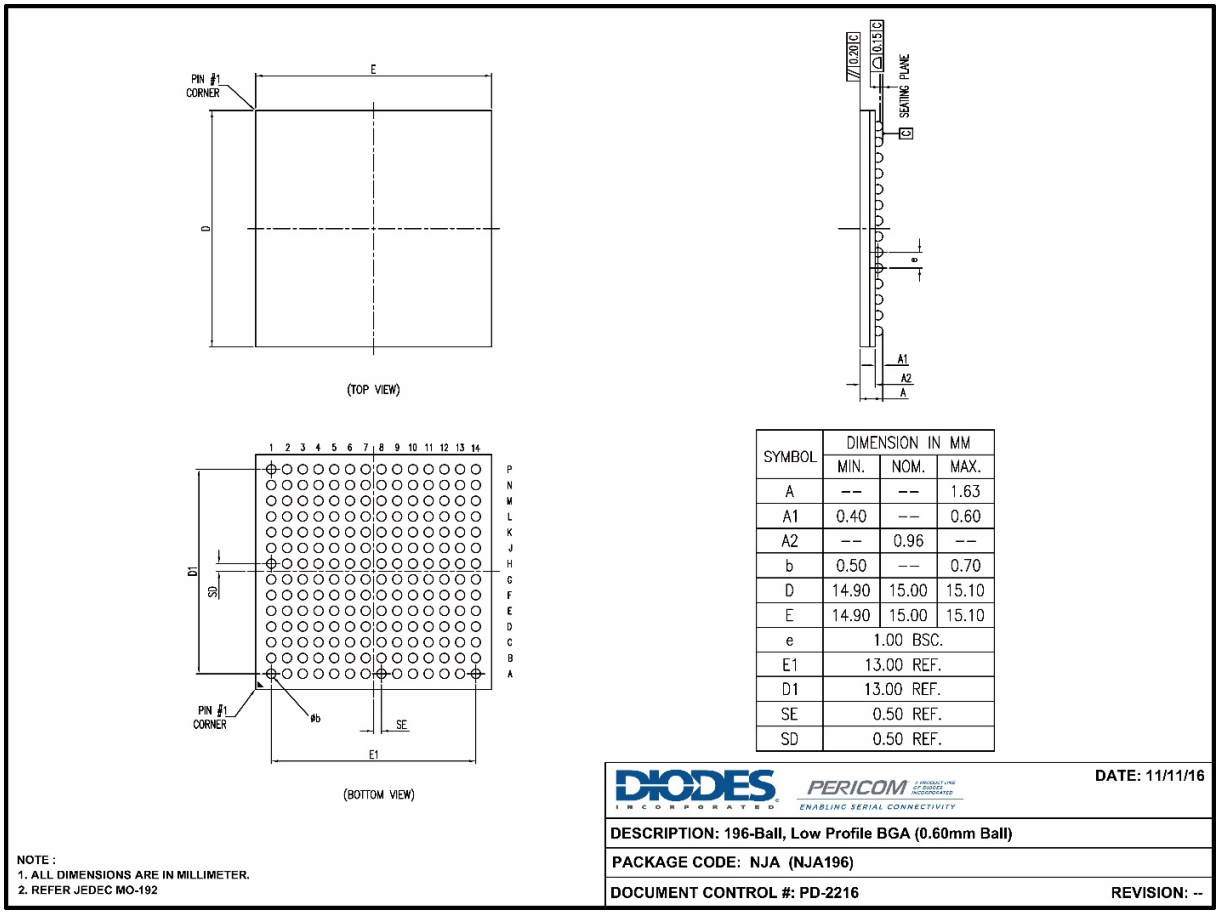
Table 13-1 Thermal Data

Power (Watt)	T_a (℃)	JEDEC Board	Airflow (m/s)	Θ_{JA} (℃/W)	T_j (℃)	Θ_{JC} (℃/W)
1.2	85	4-Layer	0	26.65	116.98	8.96
			1	23.71	113.45	
			2	22.57	112.08	
		8-Layer	0	17.75	106.3	8.44
			1	16.65	104.98	
			2	16.33	104.60	

Note:
1. T_a: Ambient Temperature
2. T_J: Junction Temperature
3. Maximum allowable junction temperature = 125℃
4. Θ_{JA}: Thermal Resistance, Junction-to-Ambient
5. Θ_{JC}: Thermal Resistance, Junction-to-Case
6. Power measured under the conditions of 1.0V/ 2.5V with PCIe2 devices usage on all downstream ports
7. The shaded fields provide a recommendation that allows PI7C9X2G606PR to support Industrial Temperature Range.

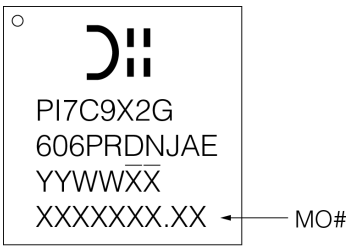
14 PACKAGE INFORMATION

The package of PI7C9X2G606PR is 15mm x 15mm LBGA (196 Pin) package with ball pitch of 1.0mm.
The detailed package information, mechanical dimension and package of drawing are shown below.



SYMBOL	DIMENSION IN MM		
	MIN.	NOM.	MAX.
A	--	--	1.63
A1	0.40	--	0.60
A2	--	0.96	--
b	0.50	--	0.70
D	14.90	15.00	15.10
E	14.90	15.00	15.10
e	1.00 BSC.		
E1	13.00 REF.		
D1	13.00 REF.		
SE	0.50 REF.		
SD	0.50 REF.		

Figure 14-1 Package Outline Drawing



YY: Year
WW: Workweek
1st X: Assembly Code
2nd X: Fab Code
Bar above fab code means Cu wire
Bar above assy code means ULA BOM

Figure 14-2 Part Marking