PICO-IMX6

VER. 1.03

February 24, 2017

REVISION HISTORY

Revision	Date	Originator	Notes
1.00	September 30, 2015	TechNexion	Initial Public release
1.01	January 28, 2016	TechNexion	Minor changes and updated regarding NXP instead Freescale
1.02	July 11, 2016	TechNexion	Added TTL display options in chapter 5
1.03	February 24, 2017	TechNexion	Minor edits on partnumbers and accessories

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1. Introduction

1.1. General Introduction

The PICO-IMX6 is a high performance highly integrated PICO Compute Module designed around the NXP i.MX6 Multicore ARM Cortex-A9. The PICO-IMX6 provides an ideal building block that easily integrates with a wide range of target markets requiring rich multimedia functionality, powerful graphics and video capabilities, as well as high-processing power, compact, cost effective and with low power consumption.

The modular approach offered by the PICO Compute Module gives your project scalability, fast time to market and upgradability while reducing engineering risk and maintain a competitive total cost of ownership.

1.2. General Care and Maintenance

Your device is a product of superior design and craftsmanship and should be treated with care.

The following suggestions will help you.

- Keep the device dry. Precipitation, humidity, and all types of liquids or moisture can contain minerals that will corrode electronic circuits. If your device does get wet, allow it to dry completely.
- Do not use or store the device in dusty, dirty areas. Its moving parts and electronic components can be damaged.
- Do not store the device in hot areas. High temperatures can shorten the life of electronic devices, damage batteries, and warp or melt certain plastics.
- Do not store the device in cold areas. When the device returns to its normal temperature, moisture can form inside the device and damage electronic circuit boards.
- Do not attempt to open the device.
- Do not drop, knock, or shake the device. Rough handling can break internal circuit boards and fine mechanics.
- Do not use harsh chemicals, cleaning solvents, or strong detergents to clean the device.
- Do not paint the device. Paint can clog the moving parts and prevent proper operation.
- Unauthorized modifications or attachments could damage the device and may violate regulations governing radio devices.

These suggestions apply equally to your device, battery, charger, or any enhancement. If any device is not working properly, take it to the nearest authorized service facility for service.
Regulatory information

Disposal of Waste Equipment by Users in Private Household in the European Union
This symbol on the product or on its packaging indicates that this product must not be disposed of with your other household waste. Instead, it is your responsibility to dispose of your waste equipment by handing it over to a designated collection point for the recycling of waste electrical and electronic equipment. The separate collection and recycling of your waste equipment at the time of disposal will help to conserve natural resources and ensure that it is recycled in a manner that protects human health and the environment. For more information about where you can drop off your waste equipment for recycling, please contact your local city office, your household waste disposal service or the shop where you purchased the product.

We hereby declare that the product is in compliance with the essential requirements and other relevant provisions of European Directive 1999/5/EC (radio equipment and telecommunications terminal equipment Directive).

Federal Communications Commission (FCC) Unintentional emitter per FCC Part 15
This device has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio or television reception. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause interference to radio and television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna
- Increase the separation between the equipment and receiver
- Connect the equipment to an outlet on a different circuit from that to which the receiver is connected
- Consult the dealer or an experienced radio/TV technician for help.

WARNING! To reduce the possibility of heat-related injuries or of overheating the computer, do not place the computer directly on your lap or obstruct the computer air vents. Use the computer only on a hard, flat surface. Do not allow another hard surface, such as an adjoining optional printer, or a soft surface, such as pillows or rugs or clothing, to block airflow. Also, do not allow the AC adapter to contact the skin or a soft surface, such as pillows or rugs or clothing, during operation. The computer and the AC adapter comply with the user-accessible surface temperature limits defined by the International Standard for Safety of Information Technology Equipment (IEC 60950).

1.3. Block Diagram

Figure 1 - PICO-IMX6-SD Block Diagram

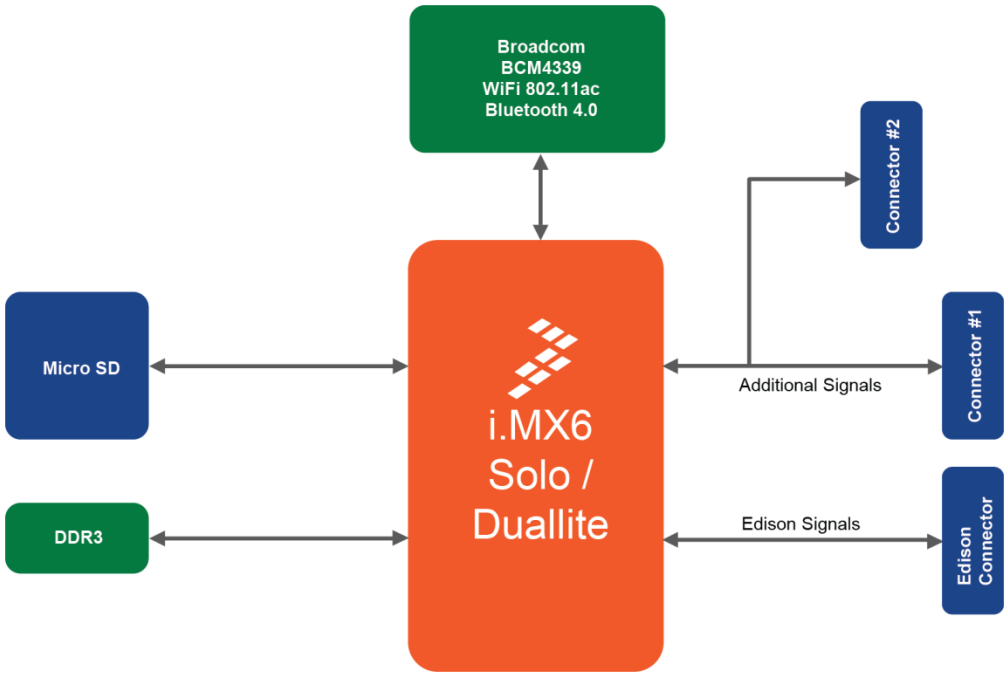
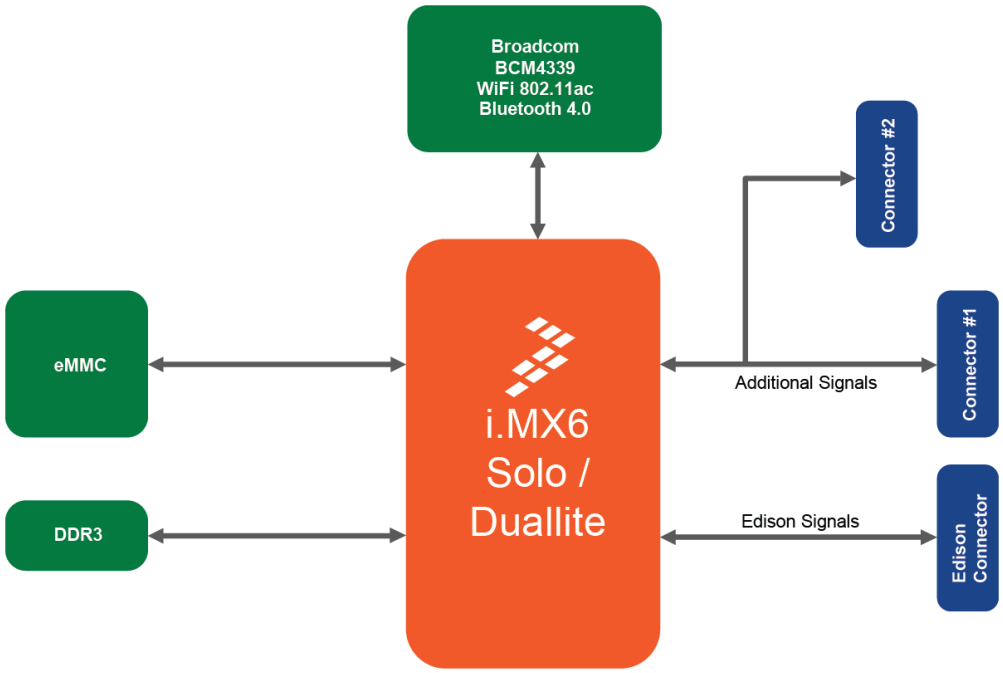


Figure 2 - PICO-IMX6-EMMC Block Diagram



1.4. PICO Compute Module Compatibility

The PICO-IMX6 is function compatible with Intel® Edison and adds additional multimedia I/O Interfaces on two additional expansion interfaces.

Figure 3 - PICO-IMX6 Compatibility Chart

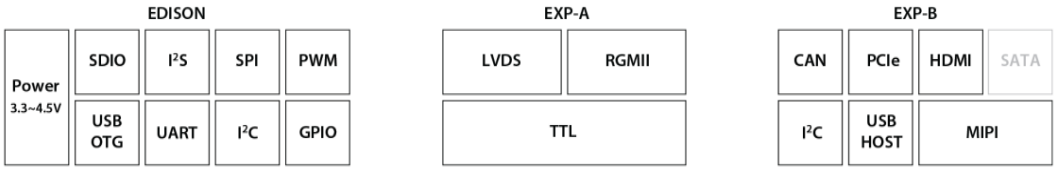


Table 1 - PICO Compatibility Overview

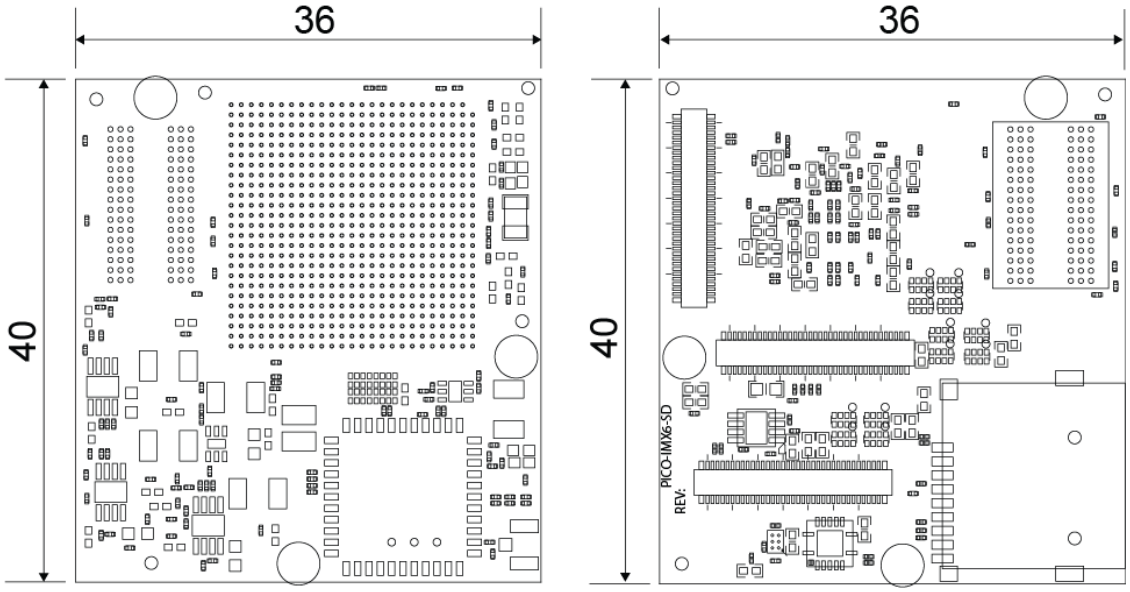
Interface	Description
LAN	1 Gigabit Ethernet Signaling
LVDS	1 single channel 18/24 bit
HDMI	1 HDMI ver.1.4 compatible
TTL Display	1 TTL 18/24 bit Display
MIPI Display	2 Lane MIPI DSI Interface
MIPI Camera	Upto 4 Lane MIPI CSI Interface
PCIe	1 Lane PCIe 2.0
SATA	Not available (Check PICO-IMX6POP for availability)
USB Host	1 USB 2.0 Host port
USB OTG	1 USB 2.0 OTG port (possible to use in Host mode)
I^2S	1 I^2S interface
CAN Bus	2 FlexCAN CAN 2.0B protocol compliant interfaces
UART	1 UART (2 wire) 1 UART (4 wire)
SDIO	1 SDIO interface 4 bit
SPI	1 SPI interfaces with 2 chip selects
I^2C	3 independent I^2C channels
GPIO	13 dedicated GPIO's available
PWM	4 PWM available

1.5. Dimensional Drawing

The PICO-IMX6 Compute Module is partly size compatible with Intel® Edison and adds several additional I/O expansion interfaces on an enlarged footprint.

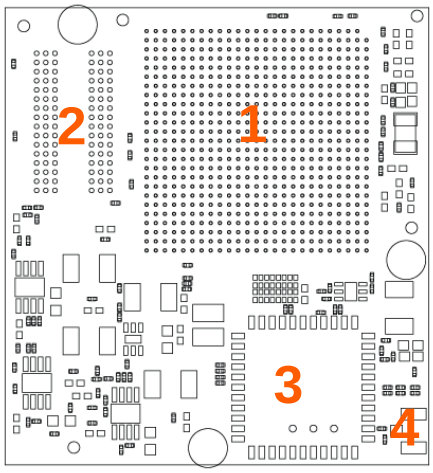
2D and 3D files can be obtained from the **www.technexion.com** homepage.

Figure 4 - PICO-IMX6 Dimensional Drawing



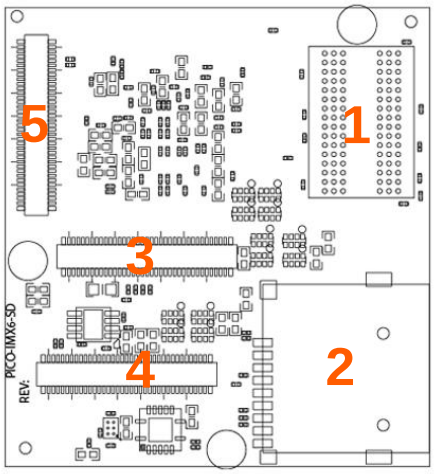
1.6. Component Location

Figure 5 - PICO-IMX6 Top view



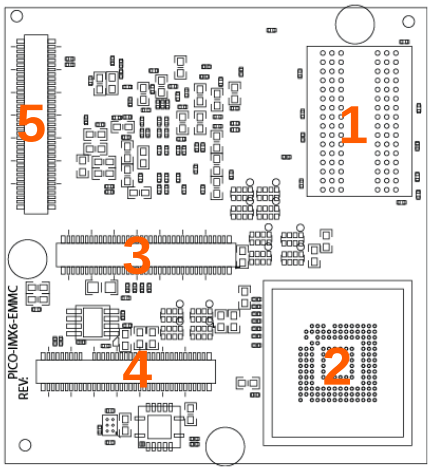
Item	Description	Item	Description
1	NXP i.MX6 Processor	2	Memory IC
3	BCM4339 WiFi/Bluetooth IC	4	Antenna connector

Figure 6 - PICO-IMX6-SD Bottom view



Item	Description	Item	Description
1	Memory IC	2	Micro-SD Slot
3	Intel® Edison Compatible Connector	4	Expansion Connector 1
5	Expansion Connector 2		

Figure 7 - PICO-IMX6-EMMC Bottom view



Item	Description	Item	Description
1	Memory IC	2	eMMC Storage IC
3	Intel® Edison Compatible Connector	4	Expansion Connector 1
5	Expansion Connector 2		

2. Core Components

2.1. NXP i.MX6 Cortex-A9 Multi-core Processor

The NXP i.MX6 processor is an implementation of the Single/Dual/Quad ARM Cortex™-A9 core, which operates at frequencies up to 1.2 GHz. The i.MX6 provides a variety of interfaces and supports the following main features:

- Single / Dual / Quad Core ARM Cortex™-A9. Core configuration is symmetric, where each core includes:
  - 32 KByte L1 Instruction Cache
  - 32 KByte L1 Data Cache
  - Private Timer and Watchdog
  - Cortex-A9 NEON MPE (Media Processing Engine) Co-processor
- Level 2 Cache—Unified instruction and data (up to 1 MByte)
- General Interrupt Controller (GIC) with 128 interrupt support
- Global Timer
- Snoop Control Unit (SCU)
- NEON MPE coprocessor:
  - SIMD Media Processing Architecture
  - NEON register file with 32x64-bit general-purpose registers
  - NEON Integer execute pipeline (ALU, Shift, MAC)
  - NEON dual, single-precision floating point execute pipeline (FADD, FMUL)
  - NEON load/store and permute pipeline
- Integrated Power Management unit:
  - Temperature Sensor for monitoring the die temperature
  - DVFS techniques for low power modes
  - Flexible clock gating control scheme
- Multimedia Hardware Accelerators

Figure 8 - NXP i.MX6 Processor Blocks

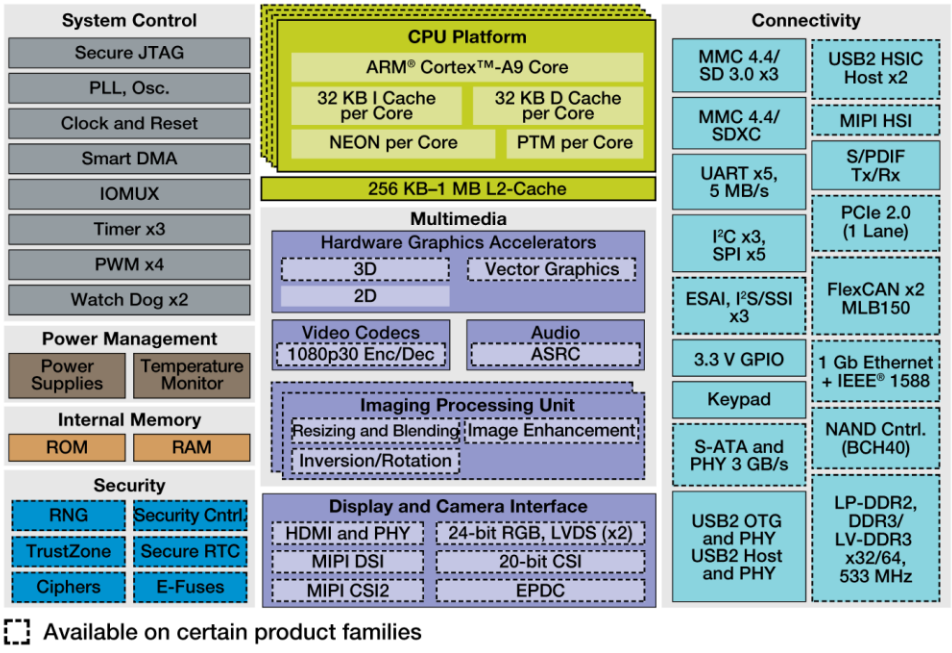
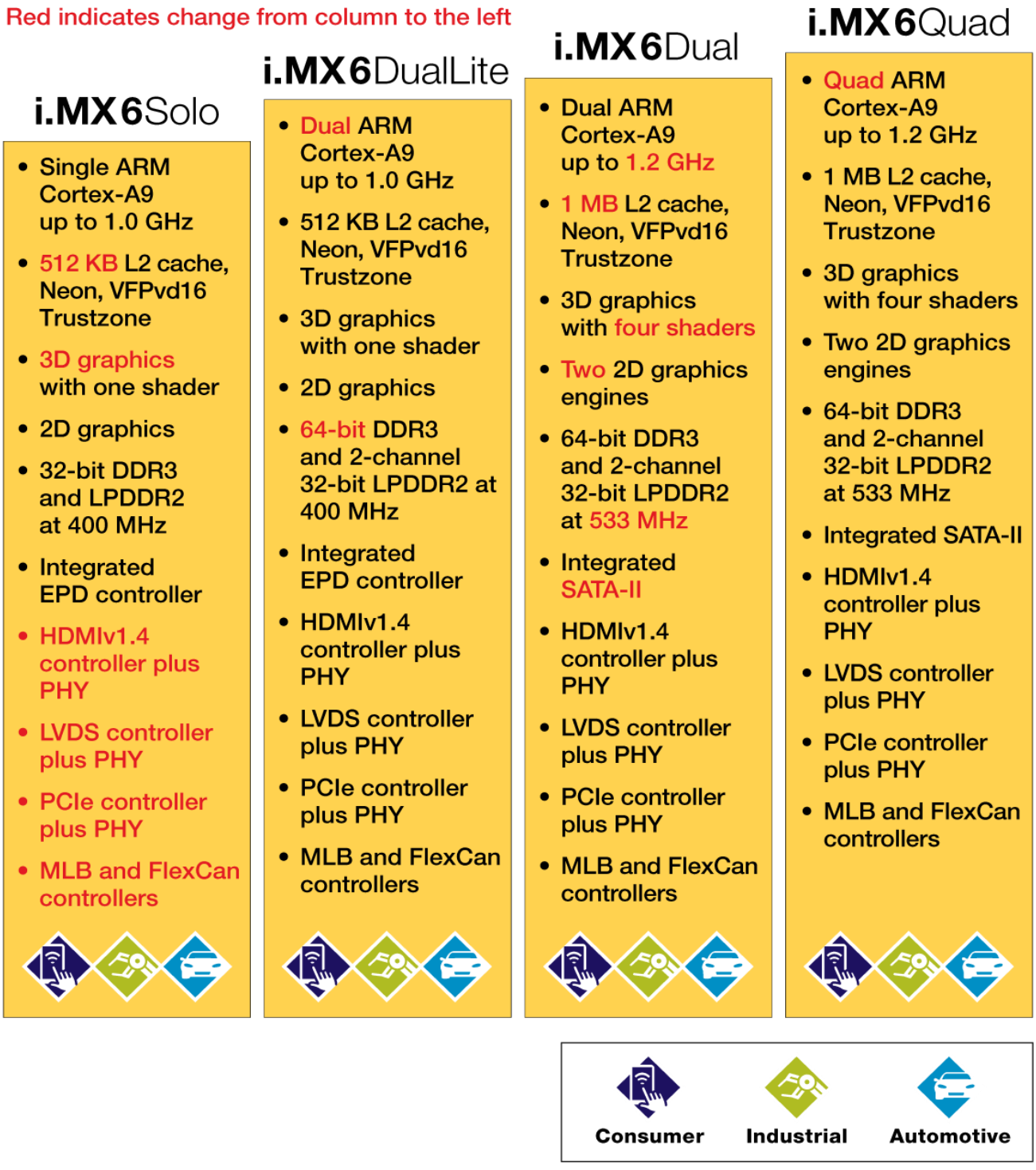


Figure 9 - NXP i.MX6 Processor Scalability Overview (Solo/Duallite/Dual/Quad)



2.1.1. i.MX6 Memory Interfaces

- The memory system consists of the following components:
  - Level 1 Cache—32 KB Instruction, 32 KB Data cache per core
  - Level 2 Cache—Unified instruction and data (1 MByte)
- On-Chip Memory:
  - Boot ROM, including HAB (96 KB)
  - Internal multimedia / shared, fast access RAM (OCRAM, 256 KB)
  - Secure/non-secure RAM (16 KB)
- External memory interfaces:
  - 16-bit, 32-bit, and 64-bit DDR3-1066 and LV-DDR3-1066
  - 8-bit NAND-Flash, including support for Raw MLC/SLC, 2 KB, 4 KB, and 8 KB page size,
  - BA-NAND, PBA-NAND, LBA-NAND, OneNAND™ and others. BCH ECC up to 32 bit.

2.1.2. i.MX6 DMA Engine

The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by off-loading the various cores in dynamic data routing. It has the following features:

- Powered by a 16-bit Instruction-Set micro-RISC engine
- Multi-channel DMA supporting up to 32 time-division multiplexed DMA channels
- 48 events with total flexibility to trigger any combination of channels
- Memory accesses including linear, FIFO, and 2D addressing
- Shared peripherals between ARM and SDMA
- Very fast Context-Switching with 2-level priority based preemptive multi-tasking
- DMA units with auto-flush and prefetch capability
- Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address)
- DMA ports can handle unit-directional and bi-directional flows (copy mode)
- Up to 8-word buffer for configurable burst transfers
- Support of byte-swapping and CRC calculations
- Library of Scripts and API is available

2.1.3. i.MX6 Video and Graphics Subsystems

The PICO-IMX6 video graphics subsystem consists of the following i.MX6 sub-blocks.

- VPU: A multi-standard high performance video codec engine supporting encode/decode operations of the following:
    - Decoding: H.264 BP/CBP/MP/HP, VC-1 SP/MP/AP, MPEG-4 SP/ASP, H.263 P0/P3, MPEG-1/2 MP, Divx (Xvid) HP/PP/HTP/HDP, VP8 (1280x720), AVS, H.264-MVC (1280x720), MJPEG BP (max. 8192x8192) up to full-HD 1920x1088 @30fps plus D1 @30fps.
    - Encoding: H.264 BP/CBP, MPEG-4 SP, H.263 P0/P3, MJPEG BP (max. 192x8192) up to full-HD 1920x1088@30fps.
- GPU2Dv2: Hardware acceleration of 2D graphics (Bit BLT and Stretch BLT). Based on the Vivante GC320 IP core.
- GPUVG: An OpenVG 1.1 Graphics Processing Unit providing hardware acceleration of vector graphics. Based on the Vivante GC355 IP core

Additionally the PICO-IMX6 incorporates the following 3D GPU engine

The PICO-IMX6 featuring an i.MX6 Dual or Quad processor (Availability restrictions apply):

- GPU3Dv4: A 3D GPU (Vivante GC2000), compliant with OpenGL ES2.0, OpenGL ES1.1 and OpenVG 1.1.

The PICO-IMX6 featuring an i.MX6 Duallite or Solo processor:

- GPU3Dv5: A 3D GPU (Vivante GC880), compliant with OpenGL ES2.0, OpenGL ES1.1 and OpenVG 1.1.

2.2. Memory

The PICO-IMX6 integrates Double Data Rate III (DDR3) Synchronous DRAM in a single (32 bit) channel configuration.

The following memory chips have been validated and tested on the PICO-IMX6 Compute Module:

- SKHynix
- Samsung
- ISSI
- Micron

For more information, please contact your TechNexion sales representative.

2.3. eMMC Storage (PICO-IMX6-EMMC Only)

The PICO-IMX6 can be ordered with onboard eMMC storage in different configurations and capacity.

The onboard eMMC device is connected on the SD3 pins of the i.MX6 processor in an 8 bit width configuration.

The following eMMC chips have been validated and tested on the PICO-IMX6 System-on-Module:

- Sandisk iNAND
- Kingston eMMC
- Micron eMMC

For more information, please contact your TechNexion sales representative.

Table 2 - eMMC Signal Description

CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
E14	SD3_DAT0	eMMC_DATA0	3V3	I/O	MMC/SDIO Data bit 0
F14	SD3_DAT1	eMMC_DATA1	3V3	I/O	MMC/SDIO Data bit 1
A15	SD3_DAT2	eMMC_DATA2	3V3	I/O	MMC/SDIO Data bit 2
B15	SD3_DAT3	eMMC_DATA3	3V3	I/O	MMC/SDIO Data bit 3
D13	SD3_DAT4	eMMC_DATA4	3V3	I/O	MMC/SDIO Data bit 4
C13	SD3_DAT5	eMMC_DATA5	3V3	I/O	MMC/SDIO Data bit 5
E13	SD3_DAT6	eMMC_DATA6	3V3	I/O	MMC/SDIO Data bit 6
F13	SD3_DAT7	eMMC_DATA7	3V3	I/O	MMC/SDIO Data bit 7
B13	SD3_CMD	eMMC_CMD	3V3	I/O	MMC/SDIO Command
D14	SD3_CLK	eMMC_CLK	3V3	O	MMC/SDIO Clock
D15	SD3_RST	eMMC_RST	3V3	O	MMC/SDIO Reset Signal

2.3.3. Micro-SD Cardslot (PICO-IMX6-SD only)

Kingston e•MMC™ products follow the JEDEC e•MMC™ 4.5 standard. It is an ideal universal storage solutions for many electronic devices, including smartphones, tablet PCs, PDAs, eBook readers, digital cameras, recorders, MP3, MP4 players, electronic learning products, digital TVs and set-top boxes. E•MMC™ encloses the MLC NAND and e•MMC™ controller inside as one JEDEC standard package, providing a standard interface to the host. The e•MMC™ controller directly manages NAND flash, including ECC, wear-leveling, IOPS optimization and read sensing.

Table 3 - SD Cardslot Signal Description

CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
E14	SD3_DAT0	SD3_DATA0	3V3	I/O	MMC/SDIO Data bit 0
F14	SD3_DAT1	SD3_DATA1	3V3	I/O	MMC/SDIO Data bit 1
A15	SD3_DAT2	SD3_DATA2	3V3	I/O	MMC/SDIO Data bit 2
B15	SD3_DAT3	SD3_DATA3	3V3	I/O	MMC/SDIO Data bit 3
B13	SD3_CMD	SD3_CMD	3V3	I/O	MMC/SDIO Command
D14	SD3_CLK	SD3_CLK	3V3	O	MMC/SDIO Clock
T1	GPIO_2	SD3_CD	3V3	I/O	MMC/SDIO Card Detect

2.5. WiFi / Bluetooth SiP Module

The PICO-IMX6 can be ordered with an optional onboard WiFI/Bluetooth SIP module. The WiFi / Bluetooth SiP module is a small sized BGA mounted module.

The small size & low profile physical design make it easier for system design to enable high performance wireless connectivity without space constrain. The low power consumption and excellent radio performance make it the best solution for OEM customers who require embedded Wi-Fi + Bluetooth features.

The SIP module radio architecture & high integration MAC/BB chip provide excellent sensitivity with rich system performance.

In addition to WEP 64/128, WPA and TKIP, AES, CCX is supported to provide the latest security requirement on your network.

The SiP module is designed to operate with a single antenna for WiFi and Bluetooth to be connected to the u.FL connector available on the PICO-IMX6.

For more information, please contact your TechNexion sales representative.

Figure 10 - PICO-IMX6 Antenna u.FL Connector Location

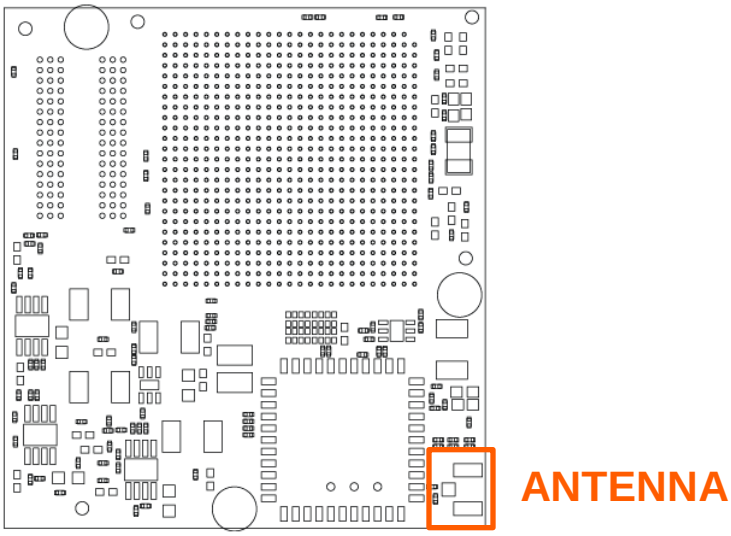


Table 4 - WiFi Signal Description

i.MX6 BALL	PAD NAME	Signal	I/O	Description
A22	SD2_DAT0	SDIO_D0	I/O	MMC/SDIO Data bit 0
E20	SD2_DAT1	SDIO_D1	I/O	MMC/SDIO Data bit 1
A23	SD2_DAT2	SDIO_D2	I/O	MMC/SDIO Data bit 2
B22	SD2_DAT3	SDIO_D3	I/O	MMC/SDIO Data bit 3
F19	SD2_CMD	SDIO_CMD	I/O	MMC/SDIO Command
C21	SD2_CLK	SDIO_CLK	I/O	MMC/SDIO Clock
R2	GPIO_16	WL_HOST_WAKE	O	General purpose interface pin. This pin is high-impedance on power up and reset. Subsequently, it becomes an input or output through software control. This pin has a programmable weak pull-up/down.
R3	GPIO_7	WL_REG_ON	I	Used by PMU (OR-gated with BT_REG_ON) to power up or power down internal BCM4339 regulators used by the WLAN section. This pin is also a low-asserting reset for WLAN only (Bluetooth is not affected by this pin).

Table 5 - Bluetooth Signal Description

i.MX6 BALL	PAD NAME	Signal	I/O	Description
D19	SD4_DAT7 “UART2_TXD”	BT_UART_RXD	I	Bluetooth UART Serial Input. Serial data input for the HCI UART Interface
E18	SD4_DAT4 “UART2_RXD”	BT_UART_TXD	O	Bluetooth UART Serial Output. Serial data output for the HCI UART Interface.
B20	SD4_DAT6 “UART2_CTS”	BT_UART_CTS	I/O	Bluetooth UART Clear to Send. Active-low clear-to-send signal for the HCI UART interface.
C19	SD4_DAT5 “UART2_RTS”	BT_UART_RTS	I/O	Bluetooth UART Request to Send. Active-low request-to-send signal for the HCI UART interface.
V6	KEY_ROW0 “AUD5_TXD”	BT_PCM_IN	I	PCM data input
U6	KEY_ROW1 “AUD5_RXD”	BT_PCM_OUT	O	PCM data output
W5	KEY_COL0 “AUD5_TXC”	BT_PCM_CLK	I/O	PCM clock
U7	KEY_COL1 “AUD5_TXFS”	BT_PCB_SYNC	I/O	PCM sync signal
R6	GPIO_4	BT_WAKE	I	Bluetooth device wake-up: Signal from the host to the module indicating that the host requires attention. • Asserted: Bluetooth device must wake-up or remain awake. • Deserted: Bluetooth device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low.
R1	GPIO_17	BT_RST_N	I	Low asserting reset for BT core
R4	GPIO_5	BT_HOST_WAKE	O	Host UART wake up. Signal from the module to the host indicating that the module requires Attention. • Asserted: Host device must wake-up or remain awake. • Deserted: Host device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low.

3. PICO Compute Module Connector Interfaces

3.1 Ethernet

The PICO-IMX6 implements a triple speed 10/100/1000 Mbit/s Ethernet MAC compliant with the IEEE802.3-2002 standard. The MAC layer provides compatibility with half- or full-duplex 10/100 Mbit/s Ethernet LANs and full-duplex gigabit Ethernet LANs.

The Ethernet MAC supports the following features:

- Implements the full 802.3 specification with preamble/SFD generation, frame padding generation, CRC generation and checking
- Supports zero-length preamble
- Dynamically configurable to support 10/100 Mbit/s and gigabit operation
- Supports 10/100 Mbit/s full-duplex and configurable half-duplex operation
- Supports gigabit full-duplex operation
- Compliant with the AMD magic packet detection with interrupt for node remote power management
- Seamless interface to commercial ethernet PHY devices via one of the following:
    - 4-bit Media Independent Interface (MII) operating at 2.5/25 MHz.
    - 4-bit non-standard MII-Lite (MII without the CRS and COL signals) operating at 2.5/25 MHz.
    - 2-bit Reduced MII (RMII) operating at 50 MHz.
    - (Double data rate) 4-bit Reduced GMII (RGMII) operating at 125 MHz.

For additional details, please refer to the “10/100/1000-Mbps Ethernet MAC (ENET)” chapter of the “i.MX6 Reference Manual”.

Table 6 - Ethernet Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
X1_33	V20	ENET_MDC	RGMII_MDC	3V3		Management data clock reference
X1_35	V23	ENET_MDIO	RGMII_MDIO	3V3		Management data
X1_37	W22	ENET_RXD1	RGMII_nRST	3V3		Ethernet reset
X1_39	V21	ENET_TX_EN	RGMII_INT	3V3		Ethernet interrupt output
X1_41	V22	ENET_REF_CLK	RGMII_REF_CLK	3V3		Synchronous Ethernet recovered clock
X1_43	C23	RGMII_TX_CTL	RGMII_TXEN	1V5		RGMII transmit enable
X1_45	D22	RGMII_RX_CTL	RGMII_RXDV	1V5		RGMII receive data valid
X1_49	D21	RGMII_TXC	RGMII_TXCLK	1V5	O	RGMII transmit clock
X1_51	C22	RGMII_TD0	RGMII_TXD0	1V5	O	RGMII transmit data 0
X1_53	F20	RGMII_TD1	RGMII_TXD1	1V5	O	RGMII transmit data 1
X1_55	E21	RGMII_TD2	RGMII_TXD2	1V5	O	RGMII transmit data 2
X1_57	A24	RGMII_TD3	RGMII_TXD3	1V5	O	RGMII transmit data 3
X1_61	B25	RGMII_RXC	RGMII_RXCLK	1V5	I	RGMII receive clock
X1_63	C24	RGMII_RD0	RGMII_RXD0	1V5	I	RGMII receive data 0
X1_65	B23	RGMII_RD1	RGMII_RXD1	1V5	I	RGMII receive data 1
X1_67	B24	RGMII_RD2	RGMII_RXD2	1V5	I	RGMII receive data 2
X1_69	D23	RGMII_RD3	RGMII_RXD3	1V5	I	RGMII receive data 3

3.2. HDMI (High Definition Multi-Media Interface)

The HDMI interface available with PICO-IMX6 is based on the “HDMI transmitter” & “HDMI 3D Tx PHY” integrated into the i.MX6 processor. The “HDMI transmitter” combines video/display data from the IPU, Audio data from i.MX6 memory & control/status data from the ARM complex, into TMDS data & clock channels. The “HDMI 3D TX PHY” transmits the combined data by means of 3 TMDS data pairs and a TMDS clock pair together with the DDC/I^2C configuration signals.

The HDMI 3D TX PHY integrated into the i.MX6 processor supports the following standards & features:

- High-Definition Multimedia Interface Specification, Version 1.4a
- Digital Visual Interface, Revision 1.0
- HDMI Compliance Test Specification, Version 1.4a
- Support for up to 720p at 100Hz and 720i at 200Hz or 1080p at 60Hz and 1080i/720i at 120Hz HDTV display resolutions and up to QXGA graphic display resolutions.
- Support for 4k x 2k and 3D video formats
- Support for up to 16-bit Deep Color modes

For additional details, please refer to the “Multimedia” chapter of the “i.MX6 Reference Manual”.

Table 7 - HDMI Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
X2_16	K6	HDMI_D0P	HDMI1_D0P	3V3	O	HDMI differential pair 0 positive signal
X2_18	K5	HDMI_D0M	HDMI1_D0M	3V3	O	HDMI differential pair 0 negative signal
X2_22	J4	HDMI_D1P	HDMI1_D1P	3V3	O	HDMI differential pair 1 positive signal
X2_24	J3	HDMI_D1M	HDMI1_D1M	3V3	O	HDMI differential pair 1 negative signal
X2_28	K4	HDMI_D2P	HDMI1_D2P	3V3	O	HDMI differential pair 2 positive signal
X2_30	K3	HDMI_D2M	HDMI1_D2M	3V3	O	HDMI differential pair 2 negative signal
X2_34	J6	HDMI_CLKP	HDMI1_CLKP	3V3	O	HDMI differential pair clock positive signal
X2_36	J5	HDMI_CLKM	HDMI1_CLKM	3V3	O	HDMI differential pair clock negative signal
X2_40	H19	EIM_A25	HDMI1_CEC	1V8	I/O	HDMI Consumer Electronics Control
X2_42	K1	HDMI_HPD	HDMI1_HPD	3V3	I	HDMI/DP Hot plug detection signal that serves as an interrupt request
X2_13	U5	KEY_COL3	I2C2_SCL	3V3	I/O	I^2C bus clock line
X2_15	T7	KEY_ROW3	I2C2_SDA	3V3	I/O	I^2C bus data line

3.3. LVDS Interface

The PICO-IMX6 is equipped with single LVDS Display interfaces. The LVDS Display Bridge (LDB) connects the IPU (Image Processing Unit) to an External LVDS Display Interface. The purpose of the LDB is to support flow of synchronous RGB data from the IPU to external display devices through LVDS interface.

The LDB output complies with the EIA-644-A standard and supports the following features:

- Connectivity to relevant devices - Displays with LVDS receivers.
- Arranging the data as required by the external display receiver and by LVDS display standards.
- Synchronization and control capabilities.
- Data input interface (inside the i.MX6 processor)
    - RGB Data of 18 or 24 bits
    - Pixel clock
    - Control signals: HSYNC, VSYNC, DE, and 1 additional optional general purpose control (I^2C)
- Single channel output data output interface
    - Total of up to 28 bits per data interface are transferred per pixel clock cycle.
- Data Rates
    - Overall: LDB supports rates needed by WUXGA 16:10 aspect ratio (1920 x 1200 @ 60 frames per second, data rate supported up to 170 MHz)
    - For single input data interface case: Up to 170 MHz pixel clock (WUXGA 1920x1200)
    - For dual input data interface case: Up to 85 MHz per interface. (WXGA 1366x768 @ 60 frames per second, 35% blanking).

For additional details, please refer to the “LVDS Display Bridge (LDB)” chapter of the “i.MX6 Reference Manual”.

Table 8 - LVDS Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
X1_3	W2	LVDS0_TX3_N	LVDS0_DATA3_N	2V5	O	LVDS differential pair 3 negative signal
X1_4	D18	SD4_DAT0	GPIO2_IO08	3V3	O	LVDS panel backlight enable
X1_5	W1	LVDS0_TX3_P	LVDS0_DATA3_P	2V5	O	LVDS differential pair 3 positive signal
X1_6	B19	SD4_DAT1	LVDS0_BLT_CTRL	3V3	O	LVDS panel backlight control
X1_9	V4	LVDS0_CLK_N	LVDS0_CLK_N	2V5	O	LVDS clock negative signal
X1_11	V3	LVDS0_CLK_P	LVDS0_CLK_P	2V5	O	LVDS clock positive signal
X1_15	V2	LVDS0_TX2_N	LVDS0_DATA2_N	2V5	O	LVDS differential pair 2 negative signal
X1_17	V1	LVDS0_TX2_P	LVDS0_DATA2_P	2V5	O	LVDS differential pair 2 positive signal
X1_21	U4	LVDS0_TX1_N	LVDS0_DATA1_N	2V5	O	LVDS differential pair 1 negative signal
X1_23	U3	LVDS0_TX1_P	LVDS0_DATA1_P	2V5	O	LVDS differential pair 1 positive signal
X1_27	U2	LVDS0_TX0_N	LVDS0_DATA0_N	2V5	O	LVDS differential pair 0 negative signal
X1_29	U1	LVDS0_TX0_P	LVDS0_DATA0_P	2V5	O	LVDS differential pair 0 positive signal

NOTE: LVDS_BLT_CTRL is also used as PWM3_1V8 signal.

3.4. Digital Display Sub-System (DSS) or TTL Interface

The Parallel Display interface of PICO-IMX6 is derived directly from the DI0 port of the IPU, effectively bypassing all the i.MX6 integrated display bridges.

Each DI port supports the following:

- Compatible with MIPI-DPI standard.
- Supports BT.656 (8-bit) and BT.1120 (16-bit) protocols.
- Supports HDTV standards SMPTE274 (1080i/p) and SMPTE296 (720p)
- Scan Order: progressive or interlaced
- Synchronization:
- Programmable horizontal and vertical synchronization output signals
- Data enabling output signal
- The combined data rate for the two DI ports is up to 240 MP/sec
- Supported pixel data formats:
- RGB - color depth fully configurable; up to 8 bits/value (color component)
- YUV 4:2:2, 8 bits/value
- All mandatory formats in MIPI DBI, DPI and DSI

For examples of valid mappings, please refer to the “IPU Display Interface Signal Mapping” chapter of the i.MX6 datasheet.

Table 9 - TTL Display Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
X1_8	W24	DISP0_DAT23	DISP0_DAT23	3V3	O	LCD Pixel Data bit 23
X1_10	V24	DISP0_DAT22	DISP0_DAT22	3V3	O	LCD Pixel Data bit 22
X1_12	T20	DISP0_DAT21	DISP0_DAT21	3V3	O	LCD Pixel Data bit 21
X1_14	U22	DISP0_DAT20	DISP0_DAT20	3V3	O	LCD Pixel Data bit 20
X1_16	U23	DISP0_DAT19	DISP0_DAT19	3V3	O	LCD Pixel Data bit 19
X1_18	V25	DISP0_DAT18	DISP0_DAT18	3V3	O	LCD Pixel Data bit 18
X1_20	U24	DISP0_DAT17	DISP0_DAT17	3V3	O	LCD Pixel Data bit 17
X1_22	T21	DISP0_DAT16	DISP0_DAT16	3V3	O	LCD Pixel Data bit 16
X1_24	T22	DISP0_DAT15	DISP0_DAT15	3V3	O	LCD Pixel Data bit 15
X1_26	U25	DISP0_DAT14	DISP0_DAT14	3V3	O	LCD Pixel Data bit 14
X1_28	R20	DISP0_DAT13	DISP0_DAT13	3V3	O	LCD Pixel Data bit 13
X1_30	T24	DISP0_DAT12	DISP0_DAT12	3V3	O	LCD Pixel Data bit 12
X1_32	T23	DISP0_DAT11	DISP0_DAT11	3V3	O	LCD Pixel Data bit 11
X1_34	R21	DISP0_DAT10	DISP0_DAT10	3V3	O	LCD Pixel Data bit 10
X1_36	T25	DISP0_DAT9	DISP0_DAT9	3V3	O	LCD Pixel Data bit 9
X1_38	R22	DISP0_DAT8	DISP0_DAT8	3V3	O	LCD Pixel Data bit 8
X1_40	R24	DISP0_DAT7	DISP0_DAT7	3V3	O	LCD Pixel Data bit 7
X1_42	R23	DISP0_DAT6	DISP0_DAT6	3V3	O	LCD Pixel Data bit 6
X1_44	R25	DISP0_DAT5	DISP0_DAT5	3V3	O	LCD Pixel Data bit 5
X1_46	P20	DISP0_DAT4	DISP0_DAT4	3V3	O	LCD Pixel Data bit 4
X1_48	P21	DISP0_DAT3	DISP0_DAT3	3V3	O	LCD Pixel Data bit 3
X1_50	P23	DISP0_DAT2	DISP0_DAT2	3V3	O	LCD Pixel Data bit 2
X1_52	P22	DISP0_DAT1	DISP0_DAT1	3V3	O	LCD Pixel Data bit 1
X1_54	P24	DISP0_DAT0	DISP0_DAT0	3V3	O	LCD Pixel Data bit 0
X1_56	P25	DI0_PIN4	DISP0_BLT_EN	3V3	O	LCD backlight enable/disable
X1_58	N25	DI0_PIN2	DISP0_HSYNC	3V3	O	LCD Horizontal Synchronization
X1_60	N21	DI0_PIN15	DISP0_DE	3V3	O	LCD dot enable pin signal
X1_62	N20	DI0_PIN3	DISP0_VSYNC	3V3	O	LCD Vertical Synchronization
X1_64	N19	DI0_DISP_CLK	DISP0_CLK	3V3	O	LCD Pixel Clock
X1_66	F17	SD4_DAT2	DISP0_BLT_CTRL	3V3	O	LCD Backlight brightness Control
X1_68	A20	SD4_DAT3	DISP0_VDD_EN	3V3	O	LCD Voltage On

NOTE: DISP0_BLT_CTRL is also used as PWM4_1V8 signal.

3.5. MIPI Display

The PICO-IMX6 provides MIPI Serial Interface camera signals.

The MIPI DSI Host Controller supports the following features:

IPU SIDE (input):

- Compliant with MIPI Alliance Specification for Display Serial Interface (DSI), Version 1.01.00 - 21 February 2008
- Fully Compliant with MIPI Alliance Standard for Display Pixel Interface (DPI-2), Version 2.00 15 September 2005 with Pixel Data bus width up to 24bits
- Compliant with MIPI Alliance Standard for Display Bus Interface (DBI-2) Version 2.00 - 29 November 2005.

Supported DBI types are:

- Type B
- 16bit, 9bit and 8bit Data bus width
- DBI and DPI interface can coexist (only one is operational at a time)
- Support all commands defined in MIPI Alliance Specification for Display Command Set (DCS), Version 1.02.00 - 23 July 2009

D-PHY side (output):

- Interface with MIPI D-PHY following PHY Protocol Interface (PPI), as defined in MIPI Alliance Specification for D-PHY, Version 1.00.00 - 14 May 2009
- Supports up to 2 D-PHY Data Lanes:
- Bidirectional Communication and Escape Mode Support through Data Lane 0.
- Programmable display resolutions, from 160x120(QQVGA) to 1024x768(XVGA).
- Multiple Peripheral Support capability, configurable Virtual Channels.
- Video Mode Pixel Formats, 16bpp(RGB565), 18bpp(RGB666) packed, 18bpp(RGB666) loosely, 24bpp(RGB888).

For additional details, please refer to the “MIPI DSI Host Controller” chapter of the “i.MX6 Reference Manual”.

Table 10 - MIPI Display Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
X2_53	G1	DSI_D0P	DSI_D0P	2V5	O	MIPI Display Serial Interface data pair 0 positive signal
X2_55	G2	DSI_D0M	DSI_D0M	2V5	O	MIPI Display Serial Interface data pair 0 negative signal
X2_57	H1	DSI_D1P	DSI_D1P	2V5	O	MIPI Display Serial Interface data pair 1 positive signal
X2_59	H2	DSI_D1M	DSI_D1M	2V5	O	MIPI Display Serial Interface data pair 1 negative signal
X2_61	H3	DSI_CLK0M	DSI_CLK0M	2V5	O	MIPI Display Serial Interface clock pair negative signal
X2_63	H4	DSI_CLK0P	DSI_CLK0P	2V5	O	MIPI Display Serial Interface clock pair positive signal

3.6. MIPI Camera

The PICO-IMX6 provides MIPI Serial Interface camera signals.

The MIPI CSI-2 Host Controller supports the following features:

- Compliant with MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2), Version 1.00 – 29 November 2005
- Supports up to 4 Data Lanes
- Dynamically configurable multi-lane merging
- Long and Short packet decoding
- Timing accurate signaling of Frame and Line synchronization packets
- Supports all primary and secondary data formats:
- RGB, YUV and RAW color space definitions
- From 24-bit down to 6-bit per pixel
- Generic or user-defined byte-based data types

For additional details, please refer to the “MIPI - Camera Serial Interface Host Controller (MIPI_CSI)” chapter of the “i.MX6 Reference Manual”.

Table 11 - MIPI Camera Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
X2_31	F4	CSI_CLK0M	CSI_CLK0M	2V5	I	MIPI Camera Serial Interface clock pair negative signal
X2_33	F3	CSI_CLK0P	CSI_CLK0P	2V5	I	MIPI Camera Serial Interface clock pair positive signal
X2_35	E4	CSI_D0M	CSI_D0M	2V5	I	MIPI Camera Serial Interface data pair 0 negative signal
X2_37	E3	CSI_D0P	CSI_D0P	2V5	I	MIPI Camera Serial Interface data pair 0 positive signal
X2_39	D2	CSI_D1P	CSI_D1P	2V5	I	MIPI Camera Serial Interface data pair 1 positive signal
X2_41	D1	CSI_D1M	CSI_D1M	2V5	I	MIPI Camera Serial Interface data pair 1 negative signal
X2_43	E2	CSI_D2P	CSI_D2P	2V5	I	MIPI Camera Serial Interface data pair 2 positive signal
X2_45	E1	CSI_D2M	CSI_D2M	2V5	I	MIPI Camera Serial Interface data pair 2 negative signal
X2_47	F2	CSI_D3M	CSI_D3M	2V5	I	MIPI Camera Serial Interface data pair 3 negative signal
X2_49	F1	CSI_D3P	CSI_D3P	2V5	I	MIPI Camera Serial Interface data pair 3 positive signal

NOTE: MIPI Camera Serial Interface data pair 2 and data pair 3 are only available on the i.MX6 Dual and i.MX6 Quad processor.

3.7. Audio Interface

The PICO-IMX6 incorporates one I²S / AUDMUX instance and can as well provide surround audio over the HDMI data signals.

The AUDMUX provides flexible, programmable routing of the serial interfaces (SSI1 or SSI2) to and from off-chip devices. The AUDMUX routes audio data (and even splices together multiple time-multiplexed audio streams) but does not decode or process audio data itself. The AUDMUX is controlled by the ARM but can route data even when the ARM is in a low-power mode.

The ESAI (Enhanced Serial Audio Interface) provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, SPDIF transceivers, and other processors. The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. The ESAI is connected to the IOMUX and to the ESAI_BIFIFO module.

The ESAI_BIFIFO (ESAI Bus Interface and FIFO) is the interface between the ESAI module and the shared peripheral bus. It contains the FIFOs used to buffer data to and from the ESAI, as well as providing the data word alignment and padding necessary to match the 24-bit data bus of the ESAI to the 32-bit data bus of the shared peripheral bus.

The ASRC (Asynchronous Sample Rate Converter) converts the sampling rate of a signal associated to an input clock into a signal associated to a different output clock. The ASRC supports concurrent sample rate conversions of up to 10 channels of over 120dB THD+N. The sample rate conversion of each channel is associated to a pair of incoming and outgoing sampling rates. The ASRC supports up to three sampling rate pairs. The ASRC is connected to the shared peripheral bus.

Key features of the audio signal block include:

- Full 6-wire SSI interfaces for asynchronous receive and transmit
- Configurable 4-wire (synchronous) or 6-wire (asynchronous) peripheral interfaces
- Independent Tx/Rx frame sync and clock direction selection for host or peripheral
- Each host interface's capability to connect to any other host or peripheral interface in a point-to-point or point-to-multipoint (network mode)
- Transmit and receive data switching to support external network mode

Table 12 - I²S Audio Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
E1_50	N3	CSI0_DAT7	AUD3_RXD	1V8	I	Integrated Interchip Sound (I²S) channel receive data line
E1_52	N1	CSI0_DAT4	AUD3_TXC	1V8	O	Integrated Interchip Sound (I²S) channel word clock signal
E1_54	N4	CSI0_DAT6	AUD3_TXFS	1V8	O	Integrated Interchip Sound (I²S) channel frame synchronization signal
E1_56	P2	CSI0_DAT5	AUD3_TXD	1V8	O	Integrated Interchip Sound (I²S) channel transmit data line

3.8. PCI Express

The PICO-IMX6 is equipped with a single lane PCI Express interface, implemented in the i.MX6 processor.

The PCI Express interface complies with PCIe specification Gen 2.0 and supports the PCI Express 1.1/2.0 standards. The PCI Express module is a dual mode complex, supporting root complex operations and endpoint operations.

PCI Express PHY Features

- 5 Gbps data transmission rate
- Integrated PHY includes transmitter, receiver, PLL, digital core, and ESD.
- Programmable RX equalization
- Designed for excellent performance margin and receiver sensitivity
- Robust PHY architecture tolerates wide process, voltage and temperature variations
- Low-jitter PLL technology with excellent supply isolation
- IEEE 1149.6 (JTAG) boundary scan
- Built-in Self-Test (BIST) features for production, at-speed, testing on any digital tester
- 5Gb/s PCIe Gen 2 and 2.5Gb/s PCIe Gen 1.1 test modes supported
- Advanced built-in diagnostics including on-chip sampling scope for easy debug
- Visibility & controllability of hard macro functionality thru programmable registers in the design
- Over-rides on all ASIC side inputs for easy debug
- Access register space thru simple 16 bit parallel interface
- Access register space thru JTAG

For additional details, please refer to the “PCI Express (PCIe)” chapter of the “i.MX6 Reference Manual”.

Table 13 - PCI Express Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
X2_56	D7	CLK1_P	PCIEA_CLKP	2V5	O	PCI Express clock differential pair positive signal
X2_58	C7	CLK1_N	PCIEA_CLKN	2V5	O	PCI Express clock differential pair negative signal
X2_62	B3	PCIE_TXP	PCIEA_TXP	2V5	O	PCI Express Transmit output differential pair positive signal
X2_64	A3	PCIE_TXM	PCIEA_TXN	2V5	O	PCI Express Transmit output differential pair negative signal
X2_68	B2	PCIE_RXP	PCIEA_RXP	2V5	I	PCI Express Receive input differential pair positive signal
X2_70	B1	PCIE_RXM	PCIEA_RXN	2V5	I	PCI Express Receive input differential pair negative signal

NOTE: The PCIE_TX pair has decoupling capacitors on the PICO Compute Module valued 10nF

3.9. Serial ATA Interface

The PICO-IMX6 incorporates a single SATA-II port implemented with the NXP i.MX6 integrated SATA controller and PHY when the PICO-IMX6 is featured with a i.MX6 Dual or Quad Processor. (Availability restrictions apply)

The interface supports the following main features:

- The SATA block fully complies with AHCI specification version 1.10 and partially complies with AHCI specification version 1.3 (FIS-based switching is currently not supported).
- SATA 1.5 Gb/s and SATA 3.0 Gb/s speed.
- Power management features including automatic partial-to-slumber transition.
- eSATA (external analog logic also needs to support eSATA).
- Hardware-assisted Native Command Queuing (NCQ) for up to 32 entries.

For additional details, please refer to the “Serial Advanced Technology Attachment Controller (SATA)” chapter of the “i.MX6 Reference Manual”.

Table 14 - Serial ATA Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
X2_4	B14	SATA_RXP	SATA1_RXP	2V5	I	Serial ATA Receive differential pair positive signal
X2_6	A14	SATA_RXM	SATA1_RXN	2V5	I	Serial ATA Receive differential pair negative signal
X2_10	B12	SATA_TXM	SATA1_TXN	2V5	O	Serial ATA Transmit differential pair negative signal
X2_12	A12	SATA_TXP	SATA1_TXP	2V5	O	Serial ATA Transmit differential pair positive signal

NOTE: SATA is only available on PICO-IMX6 modules that feature the i.MX6 Dual or i.MX6 Quad processor and is not available on the i.MX6 Solo and i.MX6 Duallite processor.

3.10. Universal Serial Bus (USB) Interface

The PICO-IMX6 incorporates a single USB Host controller and an additional USB Host/OTG controller.

Each of the USB controllers provides the following main features:
USB 2.0 Host/OTG Controller

- High-Speed/Full-Speed/Low-Speed OTG core
- HS/FS/LS UTMI compliant interface
- High Speed, Full Speed and Low Speed operation in Host mode (with UTMI transceiver)
- High Speed, and Full Speed operation in Peripheral mode (with UTMI transceiver)
- Hardware support for OTG signaling, session request protocol, and host negotiation protocol
- Up to 8 bidirectional endpoints
- Support charger detection

USB 2.0 Host Controller

- High-Speed/Full-Speed/Low-Speed Host-Only core
- HS/FS/LS UTMI compliant interface

For additional details, please refer to the “Universal Serial Bus Controller (USB)” chapter of the “i.MX6 Reference Manual”.

Table 15 - USB Host Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
X2_46	F10	USB_H1_DN	USB_HOST_DN	3V3	I/O	Universal Serial Bus differential pair negative signal
X2_48	E10	USB_H1_DP	USB_HOST_DP	3V3	I/O	Universal Serial Bus differential pair positive signal
X2_50	D10	USB_H1_VBUS	USB_H1_VBUS	5V	I/O	Universal Serial Bus power
X2_52	P5	GPIO_19	USB_H1_OC	3V3	I	Active low input, to inform USB overcurrent condition (low = overcurrent detected)

Table 16 - USB OTG Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
E1_3	W23	ENET_RX_ER	USB_ID	3V3	I/O	USB OTG ID Pin
E1_16	A6	USB_OTG_DP	USB_OTG_DP	USB	I/O	Universal Serial Bus differential pair positive signal
E1_18	B6	USB_OTG_DN	USB_OTG_DN	USB	I/O	Universal Serial Bus differential pair negative signal
E1_19	J20	EIM_D30	FAULT	1V8	I	Over current detect input pin to monitor USB power over current
E1_20	E9	USB_OTG_VBUS	USB_OTG_VBUS	5V	I/O	Universal Serial Bus power
E1_21	E23	EIM_D22	USB_OTG_PWR_EN	USB	O	Universal Serial Bus power enable

NOTE: While using USB OTG in USB HOST mode. The USB_ID pin should have a pull-down resistor to GND.

3.11. SDIO/MMC Interface

The PICO-IMX6 features a MMC / SD / SDIO host interfaces connected to the NXP i.MX6 integrated "Ultra Secured Digital Host Controller" (uSDHC).

The following main features are supported by uSDHC:

- Compatible with the MMC System Specification version 4.2/4.3/4.4/4.5.
- Conforms to the SD Host Controller Standard Specification version 3.0.
- Compatible with the SD Memory Card Specification version 3.0 and supports the "Extended Capacity SD Memory Card".
- Compatible with the SDIO Card Specification version 3.0.
- Supports 1-bit / 4-bit SD and SDIO modes, 1-bit / 4-bit

The MMC/SD/SDIO host controller can support a single MMC / SD / SDIO card or device.

For additional details, please refer to the "Ultra Secured Digital Host Controller (uSDHC)" chapter of the "i.MX6 Reference Manual".

Table 17 - SDIO/MMC Interface Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
E1_58	D20	SD1_CLK	SD1_CLK	1V8	I/O	MMC/SDIO Clock
E1_60	M21	EIM_DA9	EIM_DA9	1V8	I	SD Card detect input (Active low)
E1_62	B21	SD1_CMD	SD1_CMD	1V8	I/O	MMC/SDIO Command
E1_64	E19	SD1_DAT2	SD1_DAT2	1V8	I/O	MMC/SDIO Data bit 2
E1_66	A21	SD1_DAT0	SD1_DAT0	1V8	I/O	MMC/SDIO Data bit 0
E1_68	F18	SD1_DAT3	SD1_DAT3	1V8	I/O	MMC/SDIO Data bit 3
E1_70	C20	SD1_DAT1	SD1_DAT1	1V8	I/O	MMC/SDIO Data bit 1

3.12. CAN BUS Interface signals

The PICO-IMX6 features two CAN bus interfaces. The CAN bus interfaces are implemented with the i.MX6 on chip “Flexible Controller Area Network” (FlexCAN) communication modules.

FlexCAN supports the following main features:

- Compliant with the CAN 2.0B protocol specification
- Programmable bit rate up to 1 Mb/sec

Integration of a CAN Bus transceiver and optional galvanic isolation should be incorporated on your carrier board.

For additional details, please refer to the “Flexible Controller Area Network (FLEXCAN)” chapter of the “i.MX6 Reference Manual”.

Table 18 - CAN Bus Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
X2_19	W6	KEY_COL2	CAN1_TX	3V3	I/O	CAN (controller Area Network) transmit signal
X2_21	W4	KEY_ROW2	CAN1_RX	3V3	I/O	CAN (controller Area Network) receive signal
X2_25	T6	KEY_COL4	CAN2_TX	3V3	I/O	CAN (controller Area Network) transmit signal
X2_27	V5	KEY_ROW4	CAN2_RX	3V3	I/O	CAN (controller Area Network) receive signal

3.13. Universal Asynchronous Receiver/Transmitter (UART) Interface

The PICO-IMX6 makes 2 UART ports available and utilizes an additional UART on the module to connect to the WiFi/Bluetooth module.

The i.MX6 processor integrated UARTs support the following features:

- High-speed TIA/EIA-232-F compatible, up to 5.0 Mbit/s.
- Serial IR interface low-speed, IrDA-compatible (up to 115.2 Kbit/s).
- 9-bit or Multidrop mode (RS-485) support (automatic slave address detection).
- 7 or 8 data bits for RS-232 characters or 9 bit RS-485 format, 1 or 2 stop bits.
- Programmable parity (even, odd, and no parity).
- Hardware flow control support for request to send (RTS) and clear to send (CTS) signals
- RXD input and TXD output can be inverted respectively in RS-232/RS-485 mode
- RS-485 driver direction control via CTS signal
- Auto baud rate detection (up to 115.2 Kbit/s)
- Two independent, 32-entry FIFOs for transmit and receive

For additional details, please refer to the “Universal Asynchronous Receiver/Transmitter (UART)” chapter of the “i.MX6 Reference Manual”.

Table 19 - UART Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
E1_22	M3	CSI0_DAT11	UART1_RX	1V8	I	Universal Asynchronous Receive Transmit receive data signal
E1_27	M1	CSI0_DAT10	UART1_TX	1V8	O	Universal Asynchronous Receive Transmit transmit data signal
E1_46	F22	EIM_D24	UART3_TXD	1V8	O	Universal Asynchronous Receive Transmit transmit data signal
E1_61	G22	EIM_D25	UART3_RXD	1V8	I	Universal Asynchronous Receive Transmit receive data signal
E1_63	H21	EIM_D31	UART3_RTS	1V8	O	Universal Asynchronous Receive Transmit request to send signal
E1_65	D25	EIM_D23	UART3_CTS	1V8	O	Universal Asynchronous Receive Transmit clear to send signal

NOTE: it is recommended to use the UART1 interface as system debug where possible and use the UART3 signals in applications where one serial port is required.

NOTE: UART2 is not listed in this section. This interface is connected from the i.MX6 processor towards the WiFi/Bluetooth interface present on PICO-IMX6 and can be found in the WiFi/Bluetooth section of this manual.

3.14. Serial Peripheral Interface (SPI)

The PICO -IMX6 features two Enhanced Configurable SPI ports, which are derived from the i.MX6 processor, integrated ECSPI IPs.

The following main features are supported:

- Full-duplex synchronous serial interface
- Master/Slave configurable
- Transfer continuation function allows unlimited length data transfers
- 32-bit wide by 64-entry FIFO for both transmit and receive data
- 32-bit wide by 16-entry FIFO for HT message data
- Polarity and phase of the Chip Select (SS) and SPI Clock (SCLK) are configurable Direct Memory Access (DMA) support

For additional details, please refer to the “Enhanced Configurable SPI (ECSPI)” chapter of the “i.MX6 Reference Manual”.

Table 20 - SPI Channel Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
E1_51	K22	EIM_LBA	SPI CS0	1V8		Serial Peripheral Interface Chip Select 0 signal
E1_53	K20	EIM_RW	SPI CS1	1V8		Serial Peripheral Interface Chip Select 1 signal
E1_55	H24	EIM_CS0	CSPI2_SCLK	1V8	O	Serial Peripheral Interface clock signal
E1_57	J23	EIM_CS1	CSPI2_MOSI	1V8	O	Serial Peripheral Interface master output slave input signal
E1_59	J24	EIM_OE	CSPI2_MISO	1V8	I	Serial Peripheral Interface master input slave output signal

3.15. I²C Bus

The PICO-IMX6 I²C interfaces are implemented with the i.MX6 integrated I²C controller. There are two general purpose I²C interfaces and one I²C interface dedicated towards display and system management functions.

The following features are supported:

- Compliance with Philips I²C specification version 2.1
- Multiple-master operation
- Support for standard mode (up to 100K bits/s) and fast mode (up to 400K bits/s)
- Arbitration-lost interrupt with automatic mode switching from master to slave

For additional details, please refer to the “I2C Controller (I2C)” chapter of the “i.MX6 Reference Manual”.

Table 21 - I²C Bus Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
X2_13	U5	KEY_COL3	I2C2_SCL	3V3	I/O	I²C bus clock line
X2_15	T7	KEY_ROW3	I2C2_SDA	3V3	I/O	I²C bus data line
E1_41	H20	EIM_D21	I2C1_SCL	1V8	I/O	I²C bus clock line
E1_43	G23	EIM_D28	I2C1_SDA	1V8	I/O	I²C bus data line
E1_45	F21	EIM_D17	I2C3_SCL	1V8	I/O	I²C bus clock line
E1_47	D24	EIM_D18	I2C3_SDA	1V8	I/O	I²C bus data line

NOTE: All I²C bus data and clock lines for all I²C interfaces have 2.2K Ω pull-up resistors present on the PICO-IMX6 module.

NOTE: It is recommended to use I2C2 signals for HDMI EDID functionality and set these pins in software DDC mode.

3.16. General Purpose Input/Output (GPIO)

The PICO-IMX6 has 10 dedicated GPIO pins at 1.8V and 3 dedicated GPIO pins at 3.3V. Many of the other pins used on the PICO Compute Module can be put in GPIO module however doing so might break scalability with other PICO Compute Modules.

The GPIO signals can be configured for the following applications:

- Data input / output
- Interrupt generation

For additional details, please refer to the “General Purpose Input/Output (GPIO)” chapter of the “i.MX6 Reference Manual”.

Table 22 - GPIO Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
E1_24	P4	CSI0_MCLK	GPIO_P24	1V8	I/O	General Purpose Input Output
E1_25	P1	CSI0_PIXCLK	GPIO_P25	1V8	I/O	General Purpose Input Output
E1_26	N2	CSI0_VSYNC	GPIO_P26	1V8	I/O	General Purpose Input Output
E1_28	P3	CSI0_DATA_EN	GPIO_P28	1V8	I/O	General Purpose Input Output
E1_30	N6	CSI0_DAT8	GPIO_P30	1V8	I/O	General Purpose Input Output
E1_32	N5	CSI0_DAT9	GPIO_P32	1V8	I/O	General Purpose Input Output
E1_34	M4	CSI0_DAT14	GPIO_P34	1V8	I/O	General Purpose Input Output
E1_42	M2	CSI0_DAT12	GPIO_P42	1V8	I/O	General Purpose Input Output
E1_44	L1	CSI0_DAT13	GPIO_P44	1V8	I/O	General Purpose Input Output
E1_48	M5	CSI0_DAT15	GPIO_P48	1V8	I/O	General Purpose Input Output
X2_65	R5	GPIO_8	GPIO_8	3V3	I/O	General Purpose Input Output
X2_67	T3	GPIO_6	GPIO_6	3V3	I/O	General Purpose Input Output
X2_69	R7	GPIO_3	GPIO3_CLKO	3V3	I/O	General Purpose Input Output

3.17. Pulse Width Modulation (PWM)

The PICO-IMX6 has 4 dedicated PWM pins at 1.8V.

The following features characterize the PWM:

- 16-bit up-counter with clock source selection
- 4 x 16 FIFO to minimize interrupt overhead
- 12-bit prescaler for division of clock
- Sound and melody generation
- Active high or active low configured output
- Can be programmed to be active in low-power mode
- Can be programmed to be active in debug mode
- Interrupts at compare and rollover

For additional details, please refer to the “Pulse Width Modulation (PWM)” chapter of the “i.MX6 Reference Manual”.

Table 23 - PWM Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
E1_33	T4	GPIO_1	PWM2_1V8	1V8	I/O	General Purpose Input Output with PWM control
E1_35	T2	GPIO_9	PWM1_1V8	1V8	I/O	General Purpose Input Output with PWM control
E1_37	B19	SD4_DAT1	PWM3_1V8	1V8	I/O	General Purpose Input Output with PWM control
E1_39	F17	SD4_DAT2	PWM4_1V8	1V8	I/O	General Purpose Input Output with PWM control

NOTE: PWM3_1V8 signal is also used for LVDS_BLT_CTRL: LVDS Display Brightness Control.

NOTE: PWM4_1V8 signal is also used for DISP0_BLT_CTRL: TTL Display Brightness Control.

3.18. Manufacturing and Boot Control

The PICO-IMX6 has a number of pins to override the default boot media present on the PICO-IMX6 Compute Module (eMMC or SD Cardslot).

Table 24 - Boot Selection Pins

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
X2_3	M24	EIM_DA12	EIM_DA12	1V8	I	Boot Select pin
X2_5	N23	EIM_DA14	EIM_DA14	1V8	I	Boot Select pin
X2_7	M23	EIM_DA13	EIM_DA13	1V8	I	Boot Select pin
X2_9	L23	EIM_DA5	EIM_DA5	1V8	I	Boot Select pin

To boot from an external carrierboard SD cardslot instead of the PICO-IMX6 Compute module boot media the following signals should be modified.

Table 25 - Boot Signal Configuration

PIN	CPU BALL	Carrier Board SD Cardslot Boot Configuration
X2_3	M24	HIGH
X2_5	N23	LOW
X2_7	M23	HIGH
X2_9	L23	LOW

3.19. Input Power Requirements

The PICO-IMX6 is designed to be driven with a single input power rail.

The power domain pins have to be connected as follow:

- All GND pins have to be connected to the carrier board ground pane.
- All VSYS pins should be connected to the main power source.

Table 26 - Input Power Signals

Power Rail	Nominal Input	Input Range	Maximum Input Ripple
VSYS (4 pin)	5V	+4.2V - +5.25V	±50 mV

3.19.1. Power Management Signals

The PICO-IMX6 has the following set of signals to control the system power states such as the power-on and reset conditions. This enables the system designer to implement a fully ACPI compliant system supporting system states.

Table 27 - Power Management Signals

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
E1_17	D12	ONOFF	ON_OFF	3V3	I	Power ON button input signal
E1_36	C11	POR_B	nRESETOUT	1V8	I/O	General Purpose Input Output

3.19.2. Power Sequence

PICO-IMX6 input power sequencing requirements are as follow:

If a backup Real Time Clock (RTC) is required in the host system. We recommend to design an RTC circuit on the PICO carrier board. For example the Maxim Integrated DS1337+ connected over the general purpose I²C can be used.

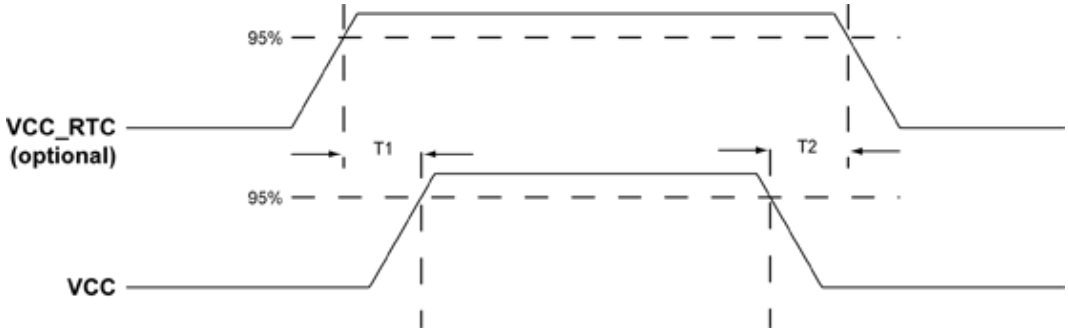
Start Sequence:
VCC_RTC must come up at the same time or before VCC comes up.

Stop Sequence:
VCC must go down at the same time or before VCC_RTC goes down

Table 28 - Input Power Sequencing

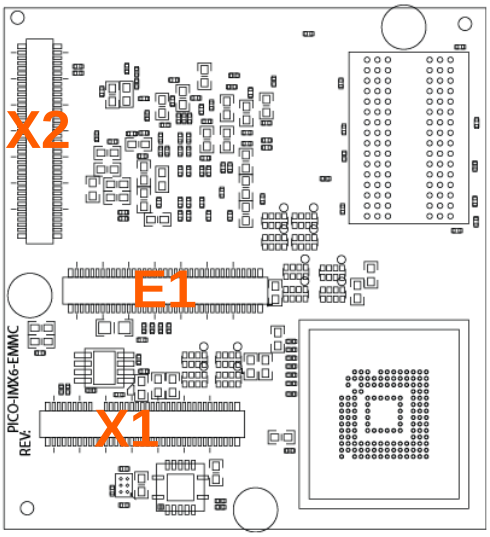
Item	Description	Value
T1	VCC_RTC rise to VCC rise	≥ 0 ms
T2	VCC fall to VCC_RTC fall	≥ 0 ms

Figure 11 - Input Power sequence



4. PICO Compute Module Pin Assignment

The PICO-IMX6 has three 70-pin Hirose board to board connectors.



PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
E1_1			GND		P	Ground
E1_2			VSYS		P	System input power (4.0 to 5.25V)
E1_3	W23	ENET_RX_ER	USB_ID	3V3	I/O	USB OTG ID Pin
E1_4			VSYS		P	System input power (4.0 to 5.25V)
E1_5			GND		P	Ground
E1_6			VSYS		P	System input power (4.0 to 5.25V)
E1_7			NC			Not Connected
E1_8			3V3		P	System 3.3V Output
E1_9			GND		P	Ground
E1_10			3V3		P	System 3.3V Output
E1_11			GND		P	Ground
E1_12			1V8		P	System 1.8V Output (same as E1 connector I/O voltage levels)
E1_13			GND		P	Ground
E1_14			VSYS		P	System input power (4.0 to 5.25V)
E1_15			GND		P	Ground
E1_16	A6	USB_OTG_DP	USB_OTG_DP	USB	I/O	Universal Serial Bus differential pair positive signal
E1_17	D12	ONOFF	ON_OFF	3V3	I	Power ON button input signal

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
E1_18	B6	USB_OTG_DN	USB_OTG_DN	USB	I/O	Universal Serial Bus differential pair negative signal
E1_19	J20	EIM_D30	FAULT	1V8	I	Over current detect input pin to monitor USB power over current
E1_20	E9	USB_OTG_VBUS	USB_OTG_VBUS	5V	I/O	Universal Serial Bus power
E1_21	E23	EIM_D22	USB_OTG_PWR_EN	USB	O	Universal Serial Bus power enable
E1_22	M3	CSI0_DAT11	UART1_RX	1V8	I	Universal Asynchronous Receive Transmit receive data signal
E1_23			NC			Not Connected
E1_24	P4	CSI0_MCLK	GPIO_P24	1V8	I/O	General Purpose Input Output
E1_25	P1	CSI0_PIXCLK	GPIO_P25	1V8	I/O	General Purpose Input Output
E1_26	N2	CSI0_VSYNC	GPIO_P26	1V8	I/O	General Purpose Input Output
E1_27	M1	CSI0_DAT10	UART1_TX	1V8	O	Universal Asynchronous Receive Transmit transmit data signal
E1_28	P3	CSI0_DATA_EN	GPIO_P28	1V8	I/O	General Purpose Input Output
E1_29			NC			Not Connected
E1_30	N6	CSI0_DAT8	GPIO_P30	1V8	I/O	General Purpose Input Output
E1_31			NC			Not Connected
E1_32	N5	CSI0_DAT9	GPIO_P32	1V8	I/O	General Purpose Input Output
E1_33	T4	GPIO_1	PWM2_1V8	1V8	I/O	General Purpose Input Output with PWM control
E1_34	M4	CSI0_DAT14	GPIO_P34	1V8	I/O	General Purpose Input Output
E1_35	T2	GPIO_9	PWM1_1V8	1V8	I/O	General Purpose Input Output with PWM control
E1_36	C11	POR_B	nRESETOUT	1V8	I/O	General Purpose Input Output
E1_37	B19	SD4_DAT1	PWM3_1V8	1V8	I/O	General Purpose Input Output with PWM control
E1_38			NC			Not Connected
E1_39	F17	SD4_DAT2	PWM4_1V8	1V8	I/O	General Purpose Input Output with PWM control
E1_40			NC			Not Connected
E1_41	H20	EIM_D21	I2C1_SCL	1V8	I/O	I^2C bus clock line
E1_42	M2	CSI0_DAT12	GPIO_P42	1V8	I/O	General Purpose Input Output
E1_43	G23	EIM_D28	I2C1_SDA	1V8	I/O	I^2C bus data line
E1_44	L1	CSI0_DAT13	GPIO_P44	1V8	I/O	General Purpose Input Output
E1_45	F21	EIM_D17	I2C3_SCL	1V8	I/O	I^2C bus clock line

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
E1_46	F22	EIM_D24	UART3_TXD	1V8	O	Universal Asynchronous Receive Transmit transmit data signal
E1_47	D24	EIM_D18	I2C3_SDA	1V8	I/O	I²C bus data line
E1_48	M5	CSI0_DAT15	GPIO_P48	1V8	I/O	General Purpose Input Output
E1_49			NC			Not Connected
E1_50	N3	CSI0_DAT7	AUD3_RXD	1V8	I	Integrated Interchip Sound (I²S) channel receive data line
E1_51	K22	EIM_LBA	SPI CS0	1V8		Serial Peripheral Interface Chip Select 0 signal
E1_52	N1	CSI0_DAT4	AUD3_TXC	1V8	O	Integrated Interchip Sound (I²S) channel word clock signal
E1_53	K20	EIM_RW	SPI CS1	1V8		Serial Peripheral Interface Chip Select 1 signal
E1_54	N4	CSI0_DAT6	AUD3_TXFS	1V8	O	Integrated Interchip Sound (I²S) channel frame synchronization signal
E1_55	H24	EIM_CS0	CSPI2_SCLK	1V8	O	Serial Peripheral Interface clock signal
E1_56	P2	CSI0_DAT5	AUD3_TXD	1V8	O	Integrated Interchip Sound (I²S) channel transmit data line
E1_57	J23	EIM_CS1	CSPI2_MOSI	1V8	O	Serial Peripheral Interface master output slave input signal
E1_58	D20	SD1_CLK	SD1_CLK	1V8	I/O	MMC/SDIO Clock
E1_59	J24	EIM_OE	CSPI2_MISO	1V8	I	Serial Peripheral Interface master input slave output signal
E1_60	M21	EIM_DA9	EIM_DA9	1V8	I	SD Card detect input (Active low)
E1_61	G22	EIM_D25	UART3_RXD	1V8	I	Universal Asynchronous Receive Transmit receive data signal
E1_62	B21	SD1_CMD	SD1_CMD	1V8	I/O	MMC/SDIO Command
E1_63	H21	EIM_D31	UART3_RTS	1V8	O	Universal Asynchronous Receive Transmit request to send signal
E1_64	E19	SD1_DAT2	SD1_DAT2	1V8	I/O	MMC/SDIO Data bit 2
E1_65	D25	EIM_D23	UART3_CTS	1V8	O	Universal Asynchronous Receive Transmit clear to send signal
E1_66	A21	SD1_DAT0	SD1_DAT0	1V8	I/O	MMC/SDIO Data bit 0
E1_67			NC			Not Connected
E1_68	F18	SD1_DAT3	SD1_DAT3	1V8	I/O	MMC/SDIO Data bit 3
E1_69			NC			Not Connected
E1_70	C20	SD1_DAT1	SD1_DAT1	1V8	I/O	MMC/SDIO Data bit 1

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
X1_1			GND		P	Ground
X1_2			GND		P	Ground
X1_3	W2	LVDS0_TX3_N	LVDS0_DATA3_N	2V5	O	LVDS differential pair 3 negative signal
X1_4	D18	SD4_DAT0	GPIO2_IO08	3V3	O	LVDS panel backlight enable
X1_5	W1	LVDS0_TX3_P	LVDS0_DATA3_P	2V5	O	LVDS differential pair 3 positive signal
X1_6	B19	SD4_DAT1	LVDS0_BLT_CTRL	3V3	O	LVDS panel backlight control
X1_7			GND		P	Ground
X1_8	W24	DISP0_DAT23	DISP0_DAT23	3V3	O	LCD Pixel Data bit 23
X1_9	V4	LVDS0_CLK_N	LVDS0_CLK_N	2V5	O	LVDS clock negative signal
X1_10	V24	DISP0_DAT22	DISP0_DAT22	3V3	O	LCD Pixel Data bit 22
X1_11	V3	LVDS0_CLK_P	LVDS0_CLK_P	2V5	O	LVDS clock positive signal
X1_12	T20	DISP0_DAT21	DISP0_DAT21	3V3	O	LCD Pixel Data bit 21
X1_13			GND		P	Ground
X1_14	U22	DISP0_DAT20	DISP0_DAT20	3V3	O	LCD Pixel Data bit 20
X1_15	V2	LVDS0_TX2_N	LVDS0_DATA2_N	2V5	O	LVDS differential pair 2 negative signal
X1_16	U23	DISP0_DAT19	DISP0_DAT19	3V3	O	LCD Pixel Data bit 19
X1_17	V1	LVDS0_TX2_P	LVDS0_DATA2_P	2V5	O	LVDS differential pair 2 positive signal
X1_18	V25	DISP0_DAT18	DISP0_DAT18	3V3	O	LCD Pixel Data bit 18
X1_19			GND		P	Ground
X1_20	U24	DISP0_DAT17	DISP0_DAT17	3V3	O	LCD Pixel Data bit 17
X1_21	U4	LVDS0_TX1_N	LVDS0_DATA1_N	2V5	O	LVDS differential pair 1 negative signal
X1_22	T21	DISP0_DAT16	DISP0_DAT16	3V3	O	LCD Pixel Data bit 16
X1_23	U3	LVDS0_TX1_P	LVDS0_DATA1_P	2V5	O	LVDS differential pair 1 positive signal
X1_24	T22	DISP0_DAT15	DISP0_DAT15	3V3	O	LCD Pixel Data bit 15
X1_25			GND		P	Ground
X1_26	U25	DISP0_DAT14	DISP0_DAT14	3V3	O	LCD Pixel Data bit 14
X1_27	U2	LVDS0_TX0_N	LVDS0_DATA0_N	2V5	O	LVDS differential pair 0 negative signal
X1_28	R20	DISP0_DAT13	DISP0_DAT13	3V3	O	LCD Pixel Data bit 13
X1_29	U1	LVDS0_TX0_P	LVDS0_DATA0_P	2V5	O	LVDS differential pair 0 positive signal
X1_30	T24	DISP0_DAT12	DISP0_DAT12	3V3	O	LCD Pixel Data bit 12
X1_31			GND		P	Ground
X1_32	T23	DISP0_DAT11	DISP0_DAT11	3V3	O	LCD Pixel Data bit 11
X1_33	V20	ENET_MDC	RGMII_MDC	3V3		Management data clock reference
X1_34	R21	DISP0_DAT10	DISP0_DAT10	3V3	O	LCD Pixel Data bit 10
X1_35	V23	ENET_MDIO	RGMII_MDIO	3V3		Management data
X1_36	T25	DISP0_DAT9	DISP0_DAT9	3V3	O	LCD Pixel Data bit 9
X1_37	W22	ENET_RXD1	RGMII_nRST	3V3		Ethernet reset
X1_38	R22	DISP0_DAT8	DISP0_DAT8	3V3	O	LCD Pixel Data bit 8
X1_39	V21	ENET_TX_EN	RGMII_INT	3V3		Ethernet interrupt output
X1_40	R24	DISP0_DAT7	DISP0_DAT7	3V3	O	LCD Pixel Data bit 7
X1_41	V22	ENET_REF_CLK	RGMII_REF_CLK	3V3		Synchronous Ethernet recovered clock

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
X1_42	R23	DISP0_DAT6	DISP0_DAT6	3V3	O	LCD Pixel Data bit 6
X1_43	C23	RGMII_TX_CTL	RGMII_TXEN	1V5		RGMII transmit enable
X1_44	R25	DISP0_DAT5	DISP0_DAT5	3V3	O	LCD Pixel Data bit 5
X1_45	D22	RGMII_RX_CTL	RGMII_RXDV	1V5		RGMII receive data valid
X1_46	P20	DISP0_DAT4	DISP0_DAT4	3V3	O	LCD Pixel Data bit 4
X1_47			GND		P	Ground
X1_48	P21	DISP0_DAT3	DISP0_DAT3	3V3	O	LCD Pixel Data bit 3
X1_49	D21	RGMII_TXC	RGMII_TXCLK	1V5	O	RGMII transmit clock
X1_50	P23	DISP0_DAT2	DISP0_DAT2	3V3	O	LCD Pixel Data bit 2
X1_51	C22	RGMII_TD0	RGMII_TXD0	1V5	O	RGMII transmit data 0
X1_52	P22	DISP0_DAT1	DISP0_DAT1	3V3	O	LCD Pixel Data bit 1
X1_53	F20	RGMII_TD1	RGMII_TXD1	1V5	O	RGMII transmit data 1
X1_54	P24	DISP0_DAT0	DISP0_DAT0	3V3	O	LCD Pixel Data bit 0
X1_55	E21	RGMII_TD2	RGMII_TXD2	1V5	O	RGMII transmit data 2
X1_56	P25	DI0_PIN4	DISP0_BLT_EN	3V3	O	LCD backlight enable/disable
X1_57	A24	RGMII_TD3	RGMII_TXD3	1V5	O	RGMII transmit data 3
X1_58	N25	DI0_PIN2	DISP0_HSYNC	3V3	O	LCD Horizontal Synchronization
X1_59			GND		P	Ground
X1_60	N21	DI0_PIN15	DISP0_DE	3V3	O	LCD dot enable pin signal
X1_61	B25	RGMII_RXC	RGMII_RXCLK	1V5	I	RGMII receive clock
X1_62	N20	DI0_PIN3	DISP0_VSYNC	3V3	O	LCD Vertical Synchronization
X1_63	C24	RGMII_RD0	RGMII_RXD0	1V5	I	RGMII receive data 0
X1_64	N19	DI0_DISP_CLK	DISP0_CLK	3V3	O	LCD Pixel Clock
X1_65	B23	RGMII_RD1	RGMII_RXD1	1V5	I	RGMII receive data 1
X1_66	F17	SD4_DAT2	DISP0_BLT_CTRL	3V3	O	LCD Backlight brightness Control
X1_67	B24	RGMII_RD2	RGMII_RXD2	1V5	I	RGMII receive data 2
X1_68	A20	SD4_DAT3	DISP0_VDD_EN	3V3	O	LCD Voltage On
X1_69	D23	RGMII_RD3	RGMII_RXD3	1V5	I	RGMII receive data 3
X1_70			GND		P	Ground

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
X2_1			GND		P	Ground
X2_2			GND		P	Ground
X2_3	M24	EIM_DA12	EIM_DA12	1V8	I	Boot Select pin
X2_4	B14	SATA_RXP	SATA1_RXP	2V5	I	Serial ATA Receive differential pair positive signal
X2_5	N23	EIM_DA14	EIM_DA14	1V8	I	Boot Select pin
X2_6	A14	SATA_RXM	SATA1_RXN	2V5	I	Serial ATA Receive differential pair negative signal
X2_7	M23	EIM_DA13	EIM_DA13	1V8	I	Boot Select pin
X2_8			GND		P	Ground
X2_9	L23	EIM_DA5	EIM_DA5	1V8	I	Boot Select pin
X2_10	B12	SATA_TXM	SATA1_TXN	2V5	O	Serial ATA Transmit differential pair negative signal
X2_11			GND		P	Ground
X2_12	A12	SATA_TXP	SATA1_TXP	2V5	O	Serial ATA Transmit differential pair positive signal
X2_13	U5	KEY_COL3	I2C2_SCL	3V3	I/O	I^2C bus clock line
X2_14			GND		P	Ground
X2_15	T7	KEY_ROW3	I2C2_SDA	3V3	I/O	I^2C bus data line
X2_16	K6	HDMI_D0P	HDMI1_D0P	3V3	O	HDMI differential pair 0 positive signal
X2_17			GND		P	Ground
X2_18	K5	HDMI_D0M	HDMI1_D0M	3V3	O	HDMI differential pair 0 negative signal
X2_19	W6	KEY_COL2	CAN1_TX	3V3	I/O	CAN (controller Area Network) transmit signal
X2_20			GND		P	Ground
X2_21	W4	KEY_ROW2	CAN1_RX	3V3	I/O	CAN (controller Area Network) receive signal
X2_22	J4	HDMI_D1P	HDMI1_D1P	3V3	O	HDMI differential pair 1 positive signal
X2_23			GND		P	Ground
X2_24	J3	HDMI_D1M	HDMI1_D1M	3V3	O	HDMI differential pair 1 negative signal
X2_25	T6	KEY_COL4	CAN2_TX	3V3	I/O	CAN (controller Area Network) transmit signal
X2_26			GND		P	Ground
X2_27	V5	KEY_ROW4	CAN2_RX	3V3	I/O	CAN (controller Area Network) receive signal
X2_28	K4	HDMI_D2P	HDMI1_D2P	3V3	O	HDMI differential pair 2 positive signal
X2_29			GND		P	Ground
X2_30	K3	HDMI_D2M	HDMI1_D2M	3V3	O	HDMI differential pair 2 negative signal
X2_31	F4	CSI_CLK0M	CSI_CLK0M	2V5	I	MIPI Camera Serial Interface clock pair negative signal
X2_32			GND		P	Ground

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
X2_33	F3	CSI_CLK0P	CSI_CLK0P	2V5	I	MIPI Camera Serial Interface clock pair positive signal
X2_34	J6	HDMI_CLKP	HDMI1_CLKP	3V3	O	HDMI differential pair clock positive signal
X2_35	E4	CSI_D0M	CSI_D0M	2V5	I	MIPI Camera Serial Interface data pair 0 negative signal
X2_36	J5	HDMI_CLKM	HDMI1_CLKM	3V3	O	HDMI differential pair clock negative signal
X2_37	E3	CSI_D0P	CSI_D0P	2V5	I	MIPI Camera Serial Interface data pair 0 positive signal
X2_38			GND		P	Ground
X2_39	D2	CSI_D1P	CSI_D1P	2V5	I	MIPI Camera Serial Interface data pair 1 positive signal
X2_40	H19	EIM_A25	HDMI1_CEC	1V8	I/O	HDMI Consumer Electronics Control
X2_41	D1	CSI_D1M	CSI_D1M	2V5	I	MIPI Camera Serial Interface data pair 1 negative signal
X2_42	K1	HDMI_HPD	HDMI1_HPD	3V3	I	HDMI/DP Hot plug detection signal that serves as an interrupt request
X2_43	E2	CSI_D2P	CSI_D2P	2V5	I	MIPI Camera Serial Interface data pair 2 positive signal
X2_44			GND		P	Ground
X2_45	E1	CSI_D2M	CSI_D2M	2V5	I	MIPI Camera Serial Interface data pair 2 negative signal
X2_46	F10	USB_H1_DN	USB_HOST_DN	3V3	I/O	Universal Serial Bus differential pair negative signal
X2_47	F2	CSI_D3M	CSI_D3M	2V5	I	MIPI Camera Serial Interface data pair 3 negative signal
X2_48	E10	USB_H1_DP	USB_HOST_DP	3V3	I/O	Universal Serial Bus differential pair positive signal
X2_49	F1	CSI_D3P	CSI_D3P	2V5	I	MIPI Camera Serial Interface data pair 3 positive signal
X2_50	D10	USB_H1_VBUS	USB_H1_VBUS	5V	I/O	Universal Serial Bus power
X2_51			GND		P	Ground
X2_52	P5	GPIO_19	USB_H1_OC	3V3	I	Active low input, to inform USB overcurrent condition (low = overcurrent detected)
X2_53	G1	DSI_D0P	DSI_D0P	2V5	O	MIPI Display Serial Interface data pair 0 positive signal
X2_54			GND		P	Ground
X2_55	G2	DSI_D0M	DSI_D0M	2V5	O	MIPI Display Serial Interface data pair 0 negative signal
X2_56	D7	CLK1_P	PCIEA_CLKP	2V5	O	PCI Express clock differential pair positive signal
X2_57	H1	DSI_D1P	DSI_D1P	2V5	O	MIPI Display Serial Interface data pair 1 positive signal
X2_58	C7	CLK1_N	PCIEA_CLKN	2V5	O	PCI Express clock differential pair negative signal
X2_59	H2	DSI_D1M	DSI_D1M	2V5	O	MIPI Display Serial Interface data pair 1 negative signal

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
X2_60			GND		P	Ground
X2_61	H3	DSI_CLK0M	DSI_CLK0M	2V5	O	MIPI Display Serial Interface clock pair negative signal
X2_62	B3	PCIE_TXP	PCIEA_TXP	2V5	O	PCI Express Transmit output differential pair positive signal
X2_63	H4	DSI_CLK0P	DSI_CLK0P	2V5	O	MIPI Display Serial Interface clock pair positive signal
X2_64	A3	PCIE_TXM	PCIEA_TXN	2V5	O	PCI Express Transmit output differential pair negative signal
X2_65	R5	GPIO_8	GPIO_8	3V3	I/O	General Purpose Input Output
X2_66			GND		P	Ground
X2_67	T3	GPIO_6	GPIO_6	3V3	I/O	General Purpose Input Output
X2_68	B2	PCIE_RXP	PCIEA_RXP	2V5	I	PCI Express Receive input differential pair positive signal
X2_69	R7	GPIO_3	GPIO3_CLKO	3V3	I/O	General Purpose Input Output
X2_70	B1	PCIE_RXM	PCIEA_RXN	2V5	I	PCI Express Receive input differential pair negative signal

5. Ordering Information

TechNexion provides a complete product portfolio for the PICO-IMX6 to assist our customers to evaluate, proto-type, integrate and mass produce solutions with our PICO Compute Modules.

5.1. PICO Compute Module Product Ordering Part Numbers

The PICO-IMX6 is available in a number of standard configurations. Custom tailored versions with other memory configuration, de-population of interfaces or extended and industrial temperature options are available upon request.

5.1.1 Standard Part Numbers

Standard part numbers can be easily found on the PICO-IMX6UL-EMMC product page on the TechNexion corporate homepage.

5.4.2. Custom Part Number Creation Rules

The PICO-IMX6 can be ordered in custom tailored to meet special application requirements and conditions according to the following custom part number creation rules.

Custom part numbers carry minimum order quantities. Please connect with your TechNexion representative for conditions and availability.

Part number format:

PICO-IMX6S10-R512-SD-BW-xx-xxxx

PICO-IMX6S10-R512-NI4G-BW-xx-xxxx

Interface	Code	Description
Processor	S	i.MX6 Solo
	U	i.MX6 Duallite
	D	i.MX6 Dual
	Q	i.MX6 Quad
Proccesor speed	08	800 Mhz
	10	1 Ghz (Default)
Memory	R512	512 MB DDR3
	R1GB	1GB DDR3
	R2GB	2GB DDR3
Storage	SD	MicroSD Cardslot
	NIxG	Other capacities of eMMC are possible (8GB, 16GB, 32GB, 64GB)
Wireless Networking	-	No
	BW	802.11ac + Bluetooth 4.0 (BCM4339)
Temperature Range	-	Commercial Temperature range (0~60°C) (Default)
	TE	Extended Temperature range (-20~70°C)
	TI	Industrial Temperature range (-35~85°C)
Custom ID	XXXX	Custom Partnumber ID for customized software loader and special component (BOM)

NOTE: Wireless Networking option is not available in “TI” Industrial Temperature Range.

6. Important Notice

TechNexion reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TechNexion terms and conditions of sale supplied at the time of order acknowledgment.

TechNexion warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TechNexion's standard warranty. Testing and other quality control techniques are used to the extent TechNexion deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TechNexion assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TechNexion components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

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TechNexion products are neither designed nor intended for use in automotive applications or environments unless the specific TechNexion products are designated by TechNexion as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TechNexion will not be responsible for any failure to meet such requirements.