



PICO-IMX7

PICO Compute Module with NXP i.MX7 SoC

VER. 1.01

February 24, 2017

REVISION HISTORY

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| 1.01 | February 24, 2017 | TechNexion | Update ordering section |
| | | | |
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1. Introduction

1.1. General Introduction

The PICO-IMX7 is a high performance highly integrated PICO Compute Module designed around the NXP i.MX7 Solo/Dual core ARM Cortex-A7 + Cortex-M4. The PICO-IMX7 provides an ideal building block that easily integrates with a wide range of target markets requiring compact, cost effective with low power consumption.

The modular approach offered by the PICO Compute Module gives your project scalability, fast time to market and upgradability while reducing engineering risk and maintain a competitive total cost of ownership.

1.2. General Care and Maintenance

Your device is a product of superior design and craftsmanship and should be treated with care.

The following suggestions will help you.

- Keep the device dry. Precipitation, humidity, and all types of liquids or moisture can contain minerals that will corrode electronic circuits. If your device does get wet, allow it to dry completely.
- Do not use or store the device in dusty, dirty areas. Its moving parts and electronic components can be damaged.
- Do not store the device in hot areas. High temperatures can shorten the life of electronic devices, damage batteries, and warp or melt certain plastics.
- Do not store the device in cold areas. When the device returns to its normal temperature, moisture can form inside the device and damage electronic circuit boards.
- Do not attempt to open the device.
- Do not drop, knock, or shake the device. Rough handling can break internal circuit boards and fine mechanics.
- Do not use harsh chemicals, cleaning solvents, or strong detergents to clean the device.
- Do not paint the device. Paint can clog the moving parts and prevent proper operation.
- Unauthorized modifications or attachments could damage the device and may violate regulations governing radio devices.

These suggestions apply equally to your device, battery, charger, or any enhancement. If any device is not working properly, take it to the nearest authorized service facility for service.

Regulatory information



Disposal of Waste Equipment by Users in Private Household in the European Union
This symbol on the product or on its packaging indicates that this product must not be disposed of with your other household waste. Instead, it is your responsibility to dispose of your waste equipment by handing it over to a designated collection point for the recycling of waste electrical and electronic equipment. The separate collection and recycling of your waste equipment at the time of disposal will help to conserve natural resources and ensure that it is recycled in a manner that protects human

health and the environment. For more information about where you can drop off your waste equipment for recycling, please contact your local city office, your household waste disposal service or the shop where you purchased the product.



We hereby declare that the product is in compliance with the essential requirements and other relevant provisions of European Directive 1999/5/EC (radio equipment and telecommunications terminal equipment Directive).



Federal Communications Commission (FCC) Unintentional emitter per FCC Part 15

This device has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio or television reception. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause interference to radio and television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna
- Increase the separation between the equipment and receiver
- Connect the equipment to an outlet on a different circuit from that to which the receiver is connected
- Consult the dealer or an experienced radio/TV technician for help.



WARNING! To reduce the possibility of heat-related injuries or of overheating the computer, do not place the computer directly on your lap or obstruct the computer air vents. Use the computer only on a hard, flat surface. Do not allow another hard surface, such as an adjoining optional printer, or a soft surface, such as pillows or rugs or clothing, to block airflow. Also, do not allow the AC adapter to contact the skin or a soft surface, such as pillows or rugs or clothing, during operation. The computer and the AC adapter comply with the user-accessible surface temperature limits defined by the International Standard for Safety of Information Technology Equipment (IEC 60950).

1.3. Block Diagram

Figure 1 - PICO-IMX7-EMMC Block Diagram

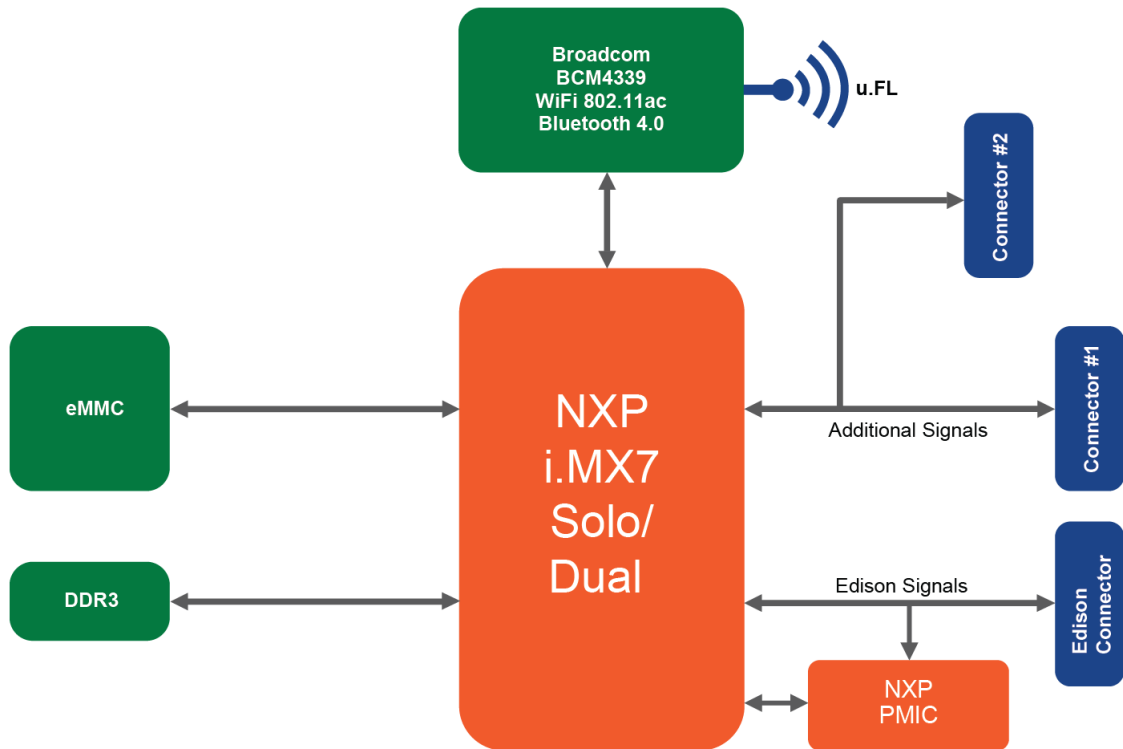
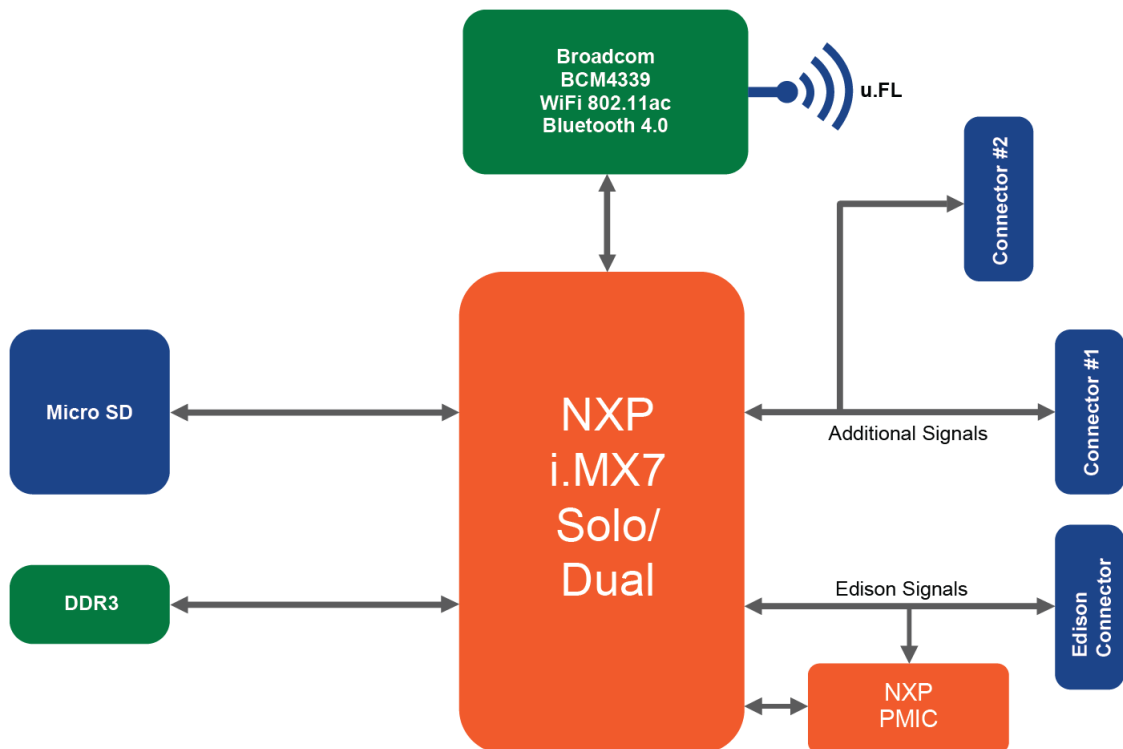


Figure 2 - PICO-IMX7-SD Block Diagram



1.4. PICO Compute Module Compatibility

The PICO-IMX7 is function compatible with Intel® Edison and adds additional multimedia I/O Interfaces on two additional expansion interfaces.

Many of the pins on PICO-IMX7 can be used for other functions.

Figure 3 - PICO-IMX7 Compatibility Chart

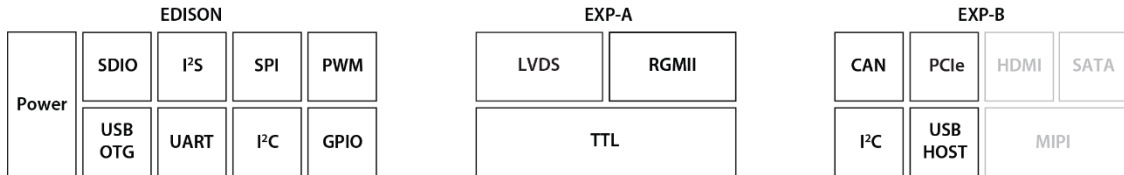


Table 1 - PICO Compatibility Overview

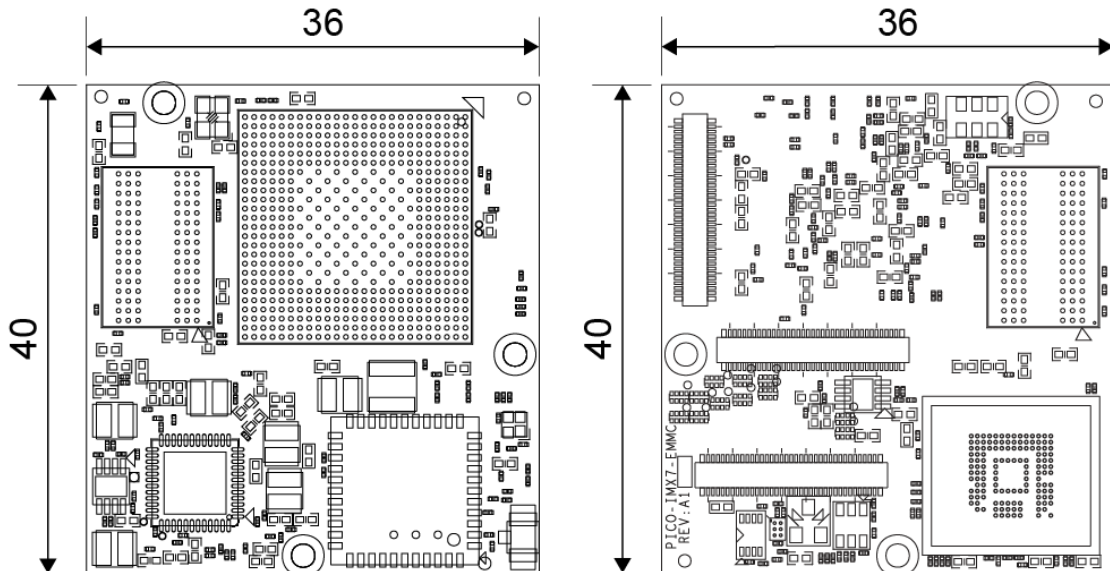
| Interface | Description |
|--------------|---|
| LAN | 1 Gigabit Ethernet |
| LVDS | Not available |
| HDMI | Not available |
| TTL Display | 1 TTL 18/24 bit Display |
| MIPI Display | 2 Lane MIPI DSI Interface |
| MIPI Camera | 2 Lane MIPI CSI Interface |
| PCIe | 1 Lane PCIe (i.MX7 Dual only) |
| SATA | Not available |
| USB Host | 1 USB 2.0 Host port |
| USB OTG | 1 USB 2.0 OTG port (possible to use in Host mode) |
| I²S | 1 I²S interface |
| CAN Bus | 2 FlexCAN CAN 2.0B protocol compliant interfaces |
| UART | 1 UART (2 wire) 1 UART (4 wire) |
| SDIO | 1 SDIO (8 bits) |
| SPI | 1 SPI interface |
| I²C | 3 independent I²C channels |
| GPIO | 13 dedicated GPIO's available |
| PWM | 4 PWM available |

1.5. Dimensional Drawing

The PICO-IMX7 Compute Module is partly size compatible with Intel® Edison and adds several additional I/O expansion interfaces on an enlarged footprint.

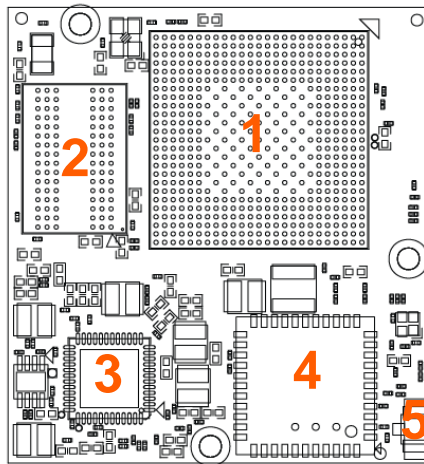
2D and 3D files can be obtained from the www.technexion.com homepage.

Figure 4 - PICO-IMX7 Dimensional Drawing



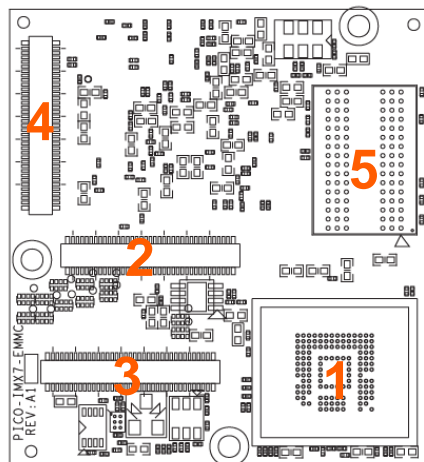
1.6. Component Location

Figure 5 - PICO-IMX7 Top view



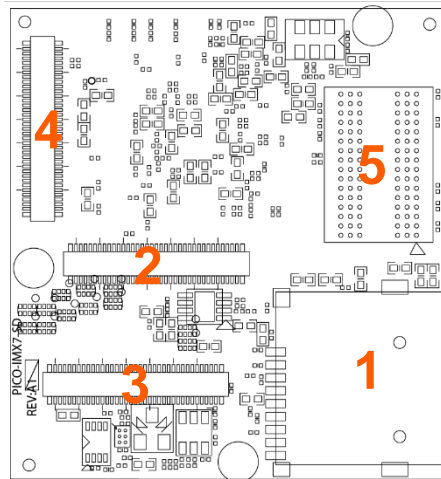
| Item | Description | Item | Description |
|------|-------------------------------|------|-------------------|
| 1 | NXP i.MX7 Processor | 2 | Memory IC |
| 3 | NXP PF300 Power Management IC | 4 | WiFi/Bluetooth IC |
| 5 | Antenna connector | | |

Figure 6 - PICO-IMX7-EMMC Bottom view



| Item | Description | Item | Description |
|------|-----------------------|------|------------------------------------|
| 1 | eMMC Storage IC | 2 | Intel® Edison Compatible Connector |
| 3 | Expansion Connector 1 | 4 | Expansion Connector 2 |
| 5 | Memory IC | | |

Figure 7 - PICO-IMX7-SD Bottom view



| Item | Description | Item | Description |
|------|-----------------------|------|------------------------------------|
| 1 | MicroSD cardslot | 2 | Intel® Edison Compatible Connector |
| 3 | Expansion Connector 1 | 4 | Expansion Connector 2 |
| 5 | Memory IC | | |

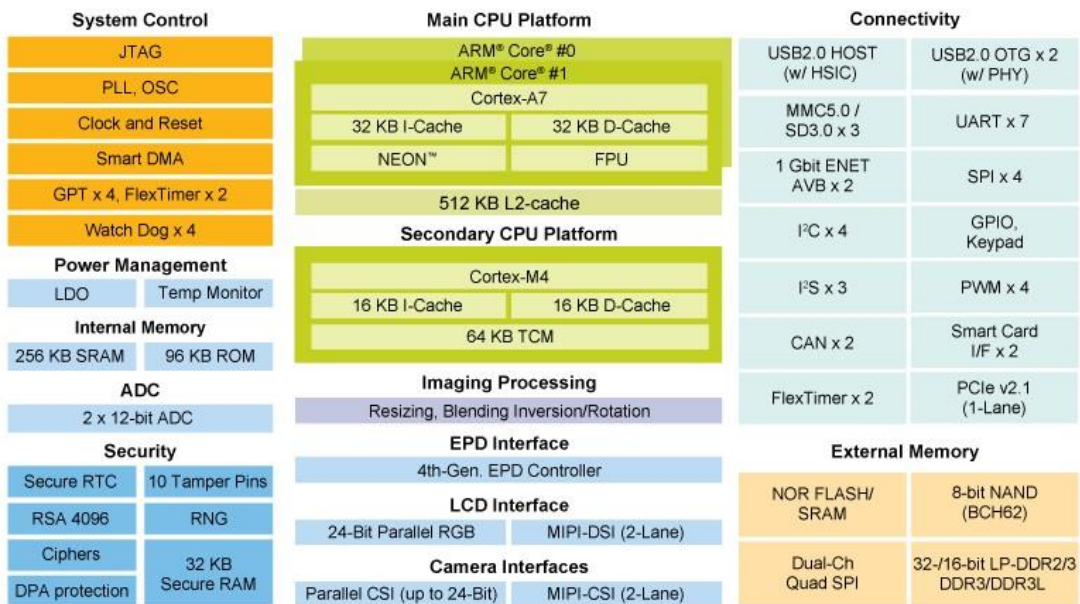
2. Core Components

2.1. NXP i.MX7 ARM Cortex-A7 + Cortex-M4 Processor

The i.MX7 is an ultra-efficient processor family with featuring NXP’s advanced implementation of the ARM Cortex®-A7+M4 core, which operates at speeds of up to 1 Ghz.

- The device is composed of the following major subsystems:
 - Upto Two ARM Cortex-A7 Cores (with TrustZone® technology)
 - Up to 1GHz operation frequency
 - 32 KByte L1 Instruction Cache, 32 KByte L1 Data Cache
 - Private Timer and Watchdog
 - NEON MPE coprocessor
- One ARM Cortex-M4 Core dedicated for real-time tasks, with the following features:
 - 200MHz operation frequency
 - MPU, FPU
 - 16 KByte instruction cache, 16 KByte data cache
 - 64 KByte TCM (tightly-coupled memory)
- Cryptographic acceleration and assurance module, containing cryptographic and hash engines supporting DPA (differential power analysis) protection, 32 KB secure RAM, and true and pseudo random number generator (NIST certified)
- PXP—PiXel processing pipeline for imagine resize, rotation, overlay and CSC. Offloading key pixel processing operations are required to support the display applications

Figure 8 - NXP i.MX7 Processor Blocks



2.2. Power Management IC (NXP PF3000)

The PICO-IMX7 has on onboard NXP PF3000 power management integrated circuit (PMIC) that features a configurable architecture supporting the numerous outputs with various current ratings as well as programmable voltage and sequencing required by the components on the PICO-IMX7 module.

Table 2 - PMIC Signal Description

| CPU BALL | CPU PAD NAME | Pinmux (mode) | Signal | V | I/O | Description |
|----------|---------------|---------------|-----------|-----|-----|--|
| D12 | SAI1_RXC | I2C4_SDA | SDA | 3V3 | I/O | I ² C bus data line |
| C12 | SAI1_RXFS | I2C4_SCL | SCL | 3V3 | I/O | I ² C bus clock line |
| AB8 | PMIC_ON_REQ | PMIC_ON_REQ | PWRON | 3V3 | I | PMIC Power ON/OFF Input from processor |
| E10 | SAI1_MCLK | GPIO6_IO18 | INT | 3V3 | I | PMIC Interrupt Signal |
| R6 | POR_B | POR_B | RESETBMCU | 3V3 | I | PMIC Reset Signal |
| AC7 | PMIC_STBY_REQ | PMIC_STBY_REQ | STANDBY | 3V3 | I | PMIC Standby Input Signal |

2.2.1. NXP PF3000 Reset Signal

To perform a hard-reset of the PICO-IMX7 a software reset signal can be implemented.

Table 3 - PMIC Reset Signal Description

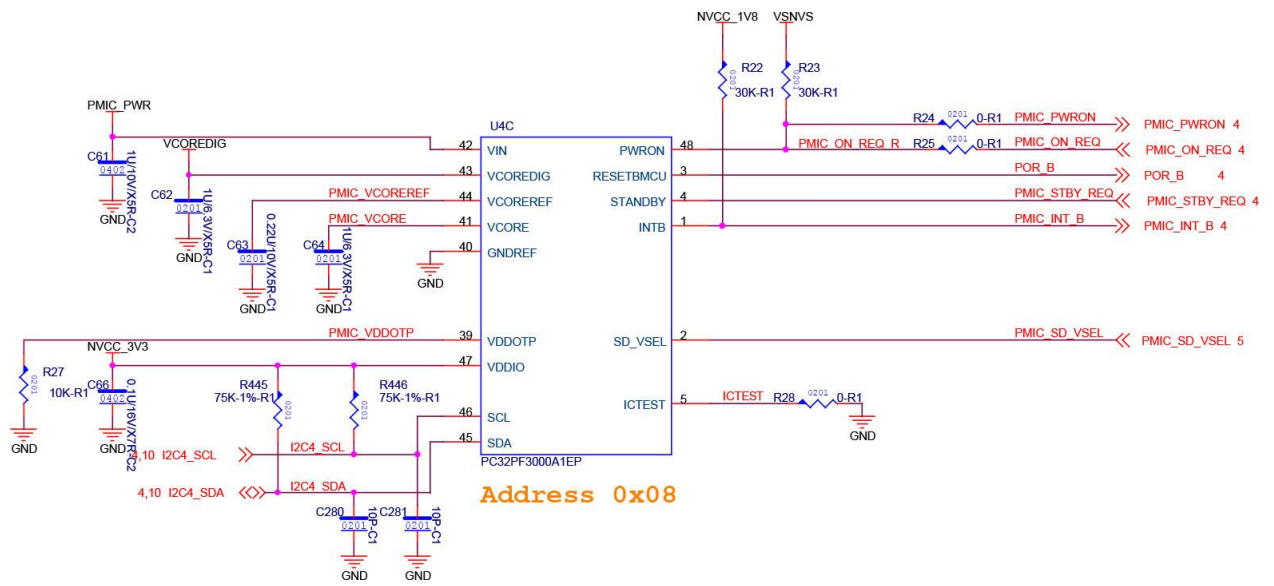
| CPU BALL | CPU PAD NAME | Pinmux (mode) | Signal | V | I/O | Description |
|----------|--------------|---------------|--------|-----|-----|---------------------------------------|
| N1 | GPIO1_IO00 | WDOG1_WDOG | RESET | 3V3 | I | Connected to the PWRON signal of PMIC |

To perform a hard-reset of the PICO-IMX7 an external circuit (for example a button or external watchdog IC) can be integrated on the carrier board.

Table 4 - PMIC Reset Signal Description

| Connector | Signal | V | I/O | Description |
|-----------|--------|-----|-----|-------------------------------|
| E1_36 | RESET | 1V8 | I | Connected to the PWRON signal |

Figure 9 - PMIC Schematics



2.3. Memory

The PICO-IMX7 integrates Double Data Rate III (DDR3) Synchronous DRAM in a single (16 bit) channel configuration.

The following memory chips have been validated and tested on the PICO-IMX7 Compute Module:

- SKHynix
- Samsung
- ISSI
- Micron

For more information, please contact your TechNexion sales representative.

2.4. eMMC Storage (PICO-IMX7-EMMC only)

The PICO-IMX7 can be ordered with onboard eMMC storage in different configurations and capacity.

The onboard eMMC device is connected on the SD3 pins of the i.MX7 processor in an 8 bit width configuration.

The following eMMC chips have been validated and tested on the PICO-IMX7 System-on-Module:

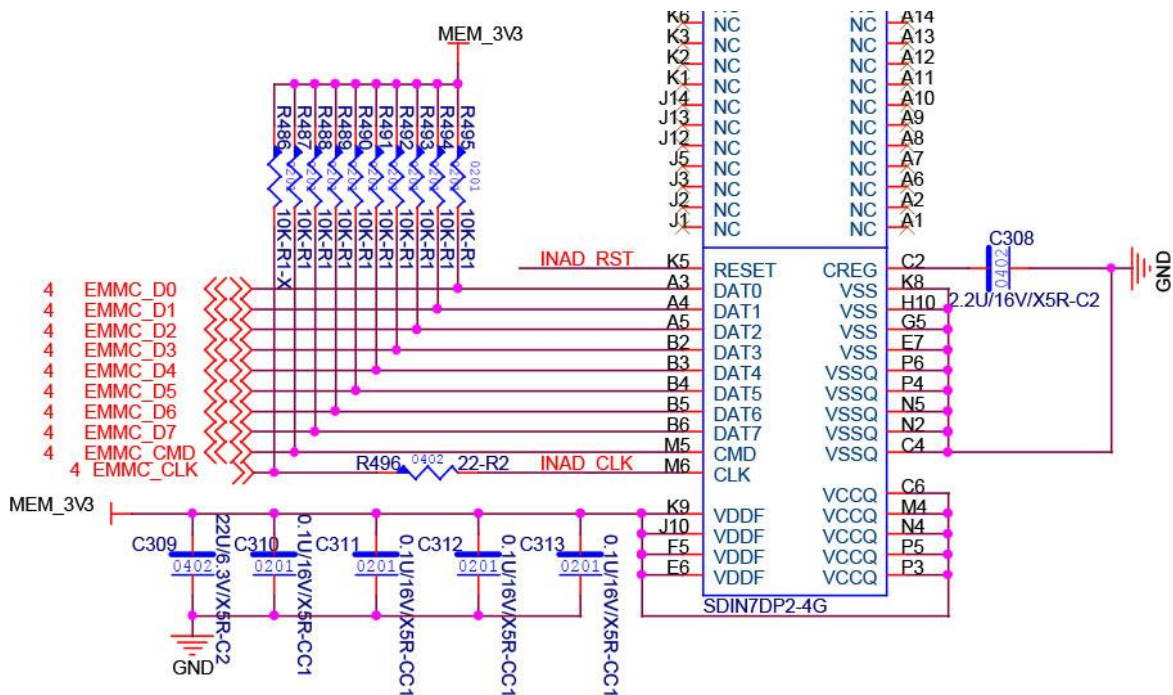
- Sandisk iNAND
- Kingston eMMC
- Micron eMMC

For more information, please contact your TechNexion sales representative.

Table 5 - eMMC Signal Description

| CPU BALL | CPU PAD NAME | Signal | V | I/O | Description |
|----------|--------------|------------|-----|-----|---------------------|
| B2 | SD3_DATA0 | eMMC_DATA0 | 3V3 | I/O | MMC/SDIO Data bit 0 |
| A2 | SD3_DATA1 | eMMC_DATA1 | 3V3 | I/O | MMC/SDIO Data bit 1 |
| G2 | SD3_DATA2 | eMMC_DATA2 | 3V3 | I/O | MMC/SDIO Data bit 2 |
| F1 | SD3_DATA3 | eMMC_DATA3 | 3V3 | I/O | MMC/SDIO Data bit 3 |
| F2 | SD3_DATA4 | eMMC_DATA4 | 3V3 | I/O | MMC/SDIO Data bit 4 |
| E2 | SD3_DATA5 | eMMC_DATA5 | 3V3 | I/O | MMC/SDIO Data bit 5 |
| C2 | SD3_DATA6 | eMMC_DATA6 | 3V3 | I/O | MMC/SDIO Data bit 6 |
| B1 | SD3_DATA7 | eMMC_DATA7 | 3V3 | I/O | MMC/SDIO Data bit 7 |
| E1 | SD3_CMD | eMMC_CMD | 3V3 | I/O | MMC/SDIO Command |
| C1 | SD3_CLK | eMMC_CLK | 3V3 | O | MMC/SDIO Clock |

Figure 10 - eMMC Schematics



2.5. Micro SD Cardslot (PICO-IMX7-SD only)

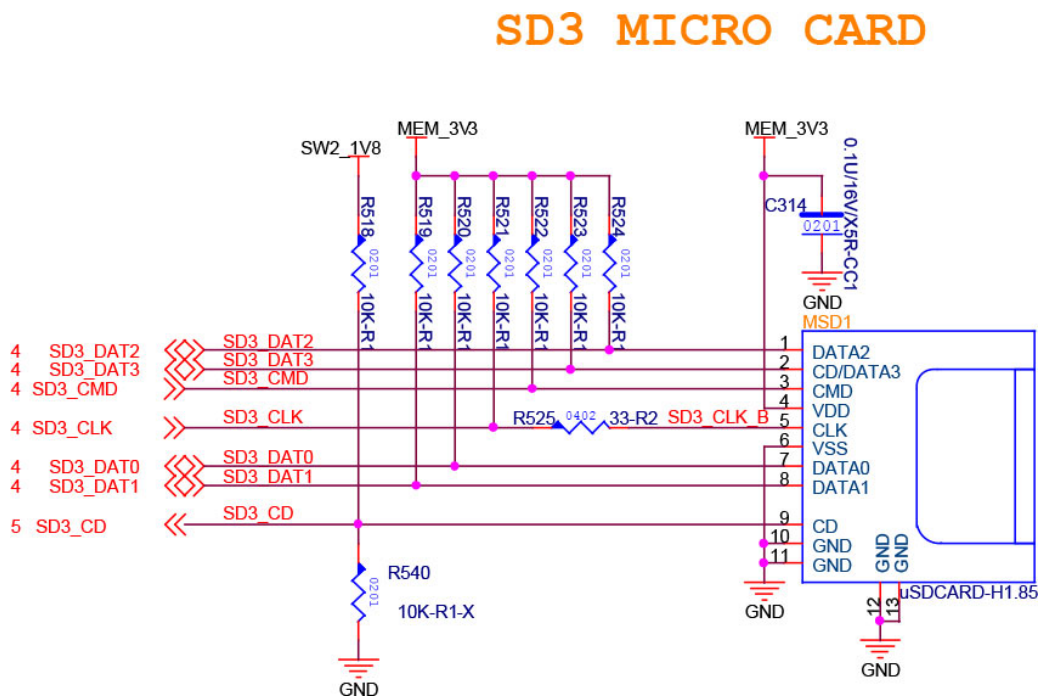
The PICO-IMX7 can be ordered with onboard SD Cardslot.

The onboard SD Cardslot is connected on the SD3 pins of the i.MX7 processor in an 4 bit width configuration.

Table 6 – SD Cardslot Signal Description

| CPU BALL | CPU PAD NAME | V | I/O | Description |
|----------|--------------|-----|-----|----------------------|
| B2 | SD3_DATA0 | 3V3 | I/O | MMC/SDIO Data bit 0 |
| A2 | SD3_DATA1 | 3V3 | I/O | MMC/SDIO Data bit 1 |
| G2 | SD3_DATA2 | 3V3 | I/O | MMC/SDIO Data bit 2 |
| F1 | SD3_DATA3 | 3V3 | I/O | MMC/SDIO Data bit 3 |
| E1 | SD3_CMD | 3V3 | I/O | MMC/SDIO Command |
| C1 | SD3_CLK | 3V3 | O | MMC/SDIO Clock |
| T5 | GPIO1_IO14 | 3V3 | I | MMC/SDIO Card Detect |

Figure 11 - SD Schematics



2.6. WiFi/Bluetooth SiP Module

The PICO-IMX7 can be ordered with an optional onboard WiFi/Bluetooth SiP module. The WiFi / Bluetooth SiP module is a small sized BGA mounted module.

The small size & low profile physical design make it easier for system design to enable high performance wireless connectivity without space constrain. The low power consumption and excellent radio performance make it the best solution for OEM customers who require embedded Wi-Fi + Bluetooth features.

The SiP module radio architecture & high integration MAC/BB chip provide excellent sensitivity with rich system performance.

In addition to WEP 64/128, WPA and TKIP, AES, CCX is supported to provide the latest security requirement on your network.

The SiP module is designed to operate with a single antenna for WiFi and Bluetooth to be connected to the u.FL connector available on the PICO-IMX7.

For more information, please contact your TechNexion sales representative.

Figure 12 - PICO-IMX7 Antenna u.FL Connector Location

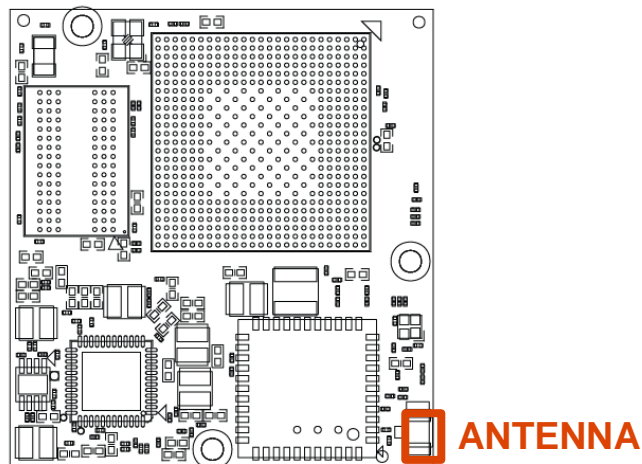


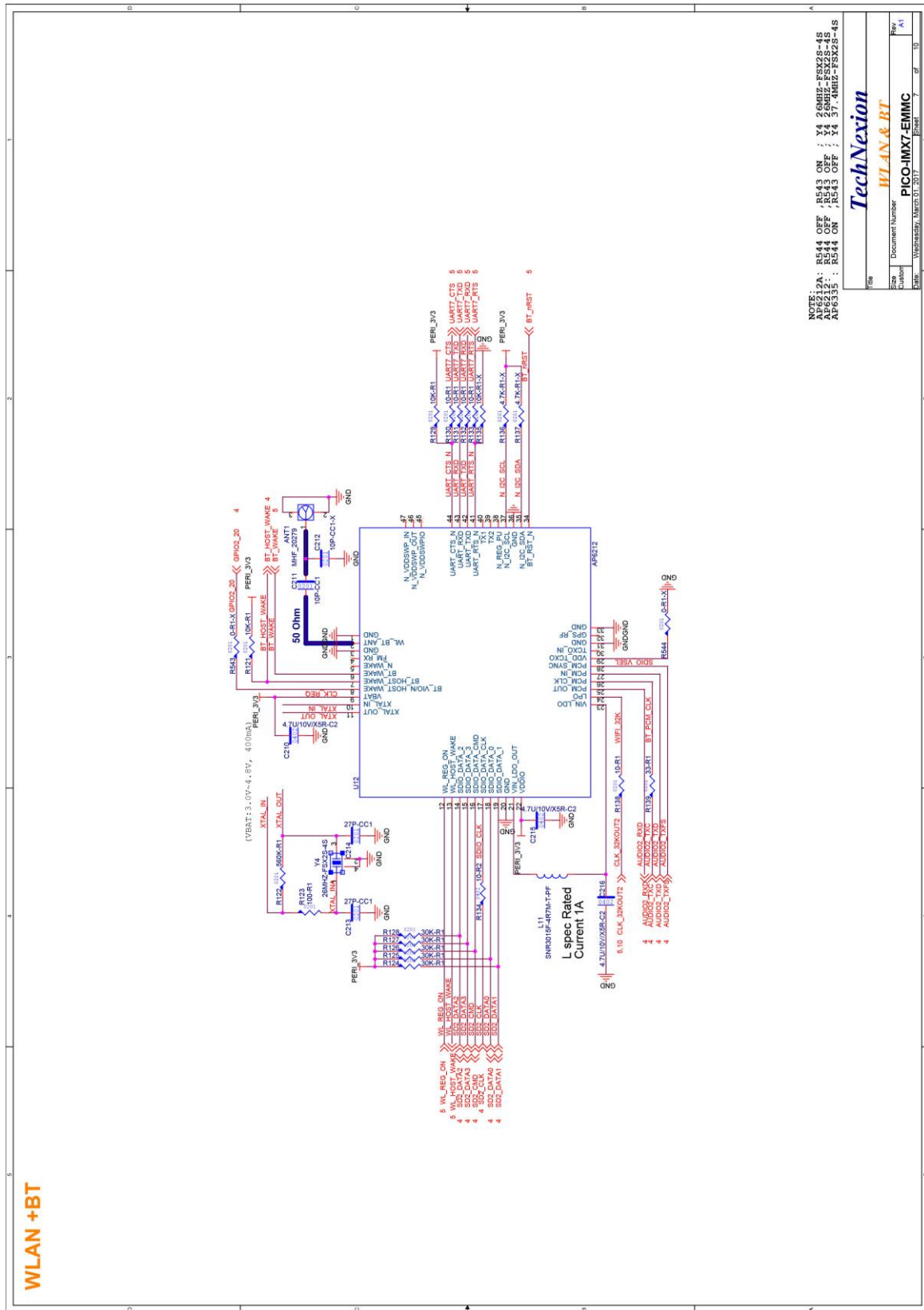
Table 7 - WiFi Signal Description

| i.MX7 BALL | PAD NAME | Signal | I/O | Description |
|------------|-------------|------------|-----|--|
| E4 | SD2_DATA0 | SD2_DATA_0 | I/O | MMC/SDIO Data bit 0 |
| E5 | SD2_DATA1 | SD2_DATA_1 | I/O | MMC/SDIO Data bit 1 |
| F5 | SD2_DATA2 | SD2_DATA_2 | I/O | MMC/SDIO Data bit 2 |
| E6 | SD2_DATA3 | SD2_DATA_3 | I/O | MMC/SDIO Data bit 3 |
| F6 | SD2_CMD | SD2_CMD | I/O | MMC/SDIO Command |
| E3 | SD2_CLK | SD2_CLK | I/O | MMC/SDIO Clock |
| H5 | ECSPI1_SS0 | GPIO4_IO19 | O | Host wake up. Signal from the module to the host indicating that the module requires Attention. <ul style="list-style-type: none"> • Asserted: Host device must wake-up or remain awake. • Deserterd: Host device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low. |
| H3 | ECSPI1_SCLK | GPIO4_IO16 | O | WiFi device wake-up: Signal from the host to the module indicating that the host requires attention. <ul style="list-style-type: none"> • Asserted: WiFi device must wake-up or remain awake. • Deserterd: WiFi device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low. |

Table 8 - Bluetooth Signal Description

| i.MX7 BALL | PAD NAME | Signal | I/O | Description |
|------------|----------------|------------|-----|--|
| G6 | ECSPI2_MOSI | UART7_TXD | O | Bluetooth UART Serial Input. Serial data input for the HCI UART Interface |
| J5 | ECSPI2_SCLK | UART7_RXD | I | Bluetooth UART Serial Output. Serial data output for the HCI UART Interface. |
| J6 | EIM_ECSPi2_SS0 | UART7_CTS | I/O | Bluetooth UART Clear to Send. Active-low clear-to-send signal for the HCI UART interface. |
| H6 | ECSPi2_MISO | UART7_RTS | I/O | Bluetooth UART Request to Send. Active-low request-to-send signal for the HCI UART interface. |
| E9 | SAI2_RXD | AUD2_RXD | I | Integrated Interchip Sound (I ² S) channel receive data line |
| E8 | SAI2_TXD | AUD2_TXD | O | Integrated Interchip Sound (I ² S) channel transmit data line |
| D8 | SAI2_TXC | AUD2_TXC | O | Integrated Interchip Sound (I ² S) channel word clock signal |
| D9 | SAI2_TXFS | AUD2_TXFS | O | Integrated Interchip Sound (I ² S) channel frame synchronization signal |
| H4 | ECSPi1_MISO | GPIO4_IO18 | O | Low asserting reset for BT core |
| G3 | SD2_RESET_B | GPIO5_IO11 | I | Host UART wake up. Signal from the module to the host indicating that the module requires Attention. <ul style="list-style-type: none"> • Asserted: Host device must wake-up or remain awake. • Deserted: Host device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low. |
| G5 | ECSPi1_MOSI | GPIO4_IO17 | O | Bluetooth device wake-up: Signal from the host to the module indicating that the host requires attention. <ul style="list-style-type: none"> • Asserted: Bluetooth device must wake-up or remain awake. • Deserted: Bluetooth device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low. |

Figure 13 - WiFi / BT Schematics



3. PICO Compute Module Connector Interfaces

3.1 Ethernet

The PICO-IMX7 implements a triple speed 10/100/1000 Mbit/s Ethernet MAC compliant with the IEEE802.3-2002 standard. The MAC layer provides compatibility with half- or full-duplex 10/100 Mbit/s Ethernet LANs and full-duplex gigabit Ethernet LANs.

The Ethernet MAC supports the following features:

- Implements the full 802.3 specification with preamble/SFD generation, frame padding generation, CRC generation and checking
- Supports zero-length preamble
- Dynamically configurable to support 10/100 Mbit/s and gigabit operation
- Supports 10/100 Mbit/s full-duplex and configurable half-duplex operation
- Supports gigabit full-duplex operation
- Compliant with the AMD magic packet detection with interrupt for node remote power management
- Seamless interface to commercial ethernet PHY devices via one of the following:
 - 4-bit Media Independent Interface (MII) operating at 2.5/25 MHz.
 - 4-bit non-standard MII-Lite (MII without the CRS and COL signals) operating at 2.5/25 MHz.
 - 2-bit Reduced MII (RMII) operating at 50 MHz.
 - (Double data rate) 4-bit Reduced GMII (RGMII) operating at 125 MHz.

For additional details, please refer to the “Ethernet MAC (ENET)” chapter of the “i.MX7 Reference Manual”.

Table 9 - Ethernet Signal Description

| PIN | CPU BALL | CPU PAD NAME | Signal | V | I/O | Description |
|-------|----------|--------------|-------------------|-----|-----|--------------------------------------|
| X1_33 | C3 | SD2_WP | ENET1_MDC | 3V3 | | Management data clock reference |
| X1_35 | D3 | SD2_CD_B | ENET1_MDIO | 3V3 | | Management data |
| X1_37 | G1 | SD3_RESET_B | GPIO6_IO11 | 3V3 | | Ethernet reset |
| X1_39 | J1 | SD3_STROBE | GPIO6_IO10 | 3V3 | | Ethernet interrupt output |
| X1_41 | N2 | GPIO1_IO01 | CCM_ENET_REF_CLK3 | 3V3 | | Synchronous Ethernet recovered clock |
| X1_43 | E16 | ENET1_TX_CTL | RGMII1_TX_CTL | 1V8 | O | RGMII transmit enable |
| X1_45 | E15 | ENET1_RX_CTL | RGMII1_RX_CTL | 1V8 | I | RGMII receive data valid |
| X1_49 | F16 | ENET1_TXC | RGMII1_TXC | 1V8 | O | RGMII transmit clock |
| X1_51 | F17 | ENET1_TDATA0 | RGMII1_TD0 | 1V8 | O | RGMII transmit data 0 |
| X1_53 | E17 | ENET1_TDATA1 | RGMII1_TD1 | 1V8 | O | RGMII transmit data 1 |
| X1_55 | E18 | ENET1_TDATA2 | RGMII1_TD2 | 1V8 | O | RGMII transmit data 2 |
| X1_57 | D18 | ENET1_TDATA3 | RGMII1_TD3 | 1V8 | O | RGMII transmit data 3 |
| X1_61 | F15 | ENET1_RXC | RGMII1_RXC | 1V8 | I | RGMII receive clock |
| X1_63 | E14 | ENET1_RDATA0 | RGMII1_RD0 | 1V8 | I | RGMII receive data 0 |
| X1_65 | F14 | ENET1_RDATA1 | RGMII1_RD1 | 1V8 | I | RGMII receive data 1 |
| X1_67 | D13 | ENET1_RDATA2 | RGMII1_RD2 | 1V8 | I | RGMII receive data 2 |
| X1_69 | E13 | ENET1_RDATA3 | RGMII1_RD3 | 1V8 | I | RGMII receive data 3 |

3.2. Digital Display Sub-System (DSS) or TTL Interface

The Parallel Display interface of PICO-IMX7 is derived from the eLCDIF subsystem. The eLCDIF is a general purpose display controller used to drive a wide range of display devices varying in size and capability. The eLCDIF is designed to support dumb (synchronous 24-bit Parallel RGB interface) and smart (asynchronous parallel MPU interface) LCD devices.

The block has several major features:

- Bus master interface to source frame buffer data for display refresh. This interface can also be used to drive data for "Smart" displays.
- PIO interface to manage data transfers between "Smart" displays and SoC.
- 8/16/18/24/32 bit LCD data bus support available depending on I/O mux options.
- Programmable timing and parameters for MPU, VSYNC and DOTCLK LCD interfaces to support a wide variety of displays.
- ITU-R BT.656 mode (called Digital Video Interface or DVI mode here) including progressive-to-interlace feature and RGB to YCbCr 4:2:2 color space conversion to support 525/60 and 625/50 operation.

For additional details, please refer to the "Enhanced LCD Interface" chapter and the "Pixel Pipeline (PXP)" chapter of the "i.MX7 Application Processor Reference Manual".

Table 10 - TTL Display Signal Description

| PIN | CPU BALL | CPU PAD NAME | Signal | V | I/O | Description |
|-------|----------|--------------|------------|-----|-----|----------------------------------|
| X1_8 | G23 | LCD1_DATA23 | LCD_DATA23 | 3V3 | O | LCD Pixel Data bit 23 |
| X1_10 | D25 | LCD1_DATA22 | LCD_DATA22 | 3V3 | O | LCD Pixel Data bit 22 |
| X1_12 | E24 | LCD1_DATA21 | LCD_DATA21 | 3V3 | O | LCD Pixel Data bit 21 |
| X1_14 | C25 | LCD1_DATA20 | LCD_DATA20 | 3V3 | O | LCD Pixel Data bit 20 |
| X1_16 | D24 | LCD1_DATA19 | LCD_DATA19 | 3V3 | O | LCD Pixel Data bit 19 |
| X1_18 | E23 | LCD1_DATA18 | LCD_DATA18 | 3V3 | O | LCD Pixel Data bit 18 |
| X1_20 | G21 | LCD1_DATA17 | LCD_DATA17 | 3V3 | O | LCD Pixel Data bit 17 |
| X1_22 | B25 | LCD1_DATA16 | LCD_DATA16 | 3V3 | O | LCD Pixel Data bit 16 |
| X1_24 | C24 | LCD1_DATA15 | LCD_DATA15 | 3V3 | O | LCD Pixel Data bit 15 |
| X1_26 | D23 | LCD1_DATA14 | LCD_DATA14 | 3V3 | O | LCD Pixel Data bit 14 |
| X1_28 | E22 | LCD1_DATA13 | LCD_DATA13 | 3V3 | O | LCD Pixel Data bit 13 |
| X1_30 | F21 | LCD1_DATA12 | LCD_DATA12 | 3V3 | O | LCD Pixel Data bit 12 |
| X1_32 | G20 | LCD1_DATA11 | LCD_DATA11 | 3V3 | O | LCD Pixel Data bit 11 |
| X1_34 | B24 | LCD1_DATA10 | LCD_DATA10 | 3V3 | O | LCD Pixel Data bit 10 |
| X1_36 | C23 | LCD1_DATA09 | LCD_DATA09 | 3V3 | O | LCD Pixel Data bit 9 |
| X1_38 | E21 | LCD1_DATA08 | LCD_DATA08 | 3V3 | O | LCD Pixel Data bit 8 |
| X1_40 | F20 | LCD1_DATA07 | LCD_DATA07 | 3V3 | O | LCD Pixel Data bit 7 |
| X1_42 | A24 | LCD1_DATA06 | LCD_DATA06 | 3V3 | O | LCD Pixel Data bit 6 |
| X1_44 | B23 | LCD1_DATA05 | LCD_DATA05 | 3V3 | O | LCD Pixel Data bit 5 |
| X1_46 | C22 | LCD1_DATA04 | LCD_DATA04 | 3V3 | O | LCD Pixel Data bit 4 |
| X1_48 | A23 | LCD1_DATA03 | LCD_DATA03 | 3V3 | O | LCD Pixel Data bit 3 |
| X1_50 | B22 | LCD1_DATA02 | LCD_DATA02 | 3V3 | O | LCD Pixel Data bit 2 |
| X1_52 | A22 | LCD1_DATA01 | LCD_DATA01 | 3V3 | O | LCD Pixel Data bit 1 |
| X1_54 | D21 | LCD1_DATA00 | LCD_DATA00 | 3V3 | O | LCD Pixel Data bit 0 |
| X1_56 | C21 | LCD1_RESET | LCD_RS | 3V3 | O | LCD backlight enable/disable |
| X1_58 | E25 | LCD1_HSYNC | LCD_HSYNC | 3V3 | O | LCD Horizontal Synchronization |
| X1_60 | F25 | LCD1_ENABLE | LCD_ENABLE | 3V3 | O | LCD dot enable pin signal |
| X1_62 | F24 | LCD1_VSYNC | LCD_VSYNC | 3V3 | O | LCD Vertical Synchronization |
| X1_64 | E20 | LCD1_CLK | LCD_CLK | 3V3 | O | LCD Pixel Clock |
| X1_66 | T1 | GPIO1_IO11 | PWM4_OUT | 3V3 | O | LCD Backlight brightness Control |
| X1_68 | P2 | GPIO1_IO06 | GPIO1_IO06 | 3V3 | O | LCD Voltage On |

3.3. MIPI Display

The PICO-IMX7 provides MIPI Serial Interface camera signals.

The MIPI DSI Host Controller supports the following features:

Complies to MIPI DSI Standard Specification V1.01r11

- Maximum resolution ranges up to SXGA+(1400 x 11050 @ 60 Hz, 24 bpp)
 - It should be decided on bandwidth between input clock (video clock) and output clock (D-PHY HS clock).
- Supports 1, 2 data lanes
- Supports pixel format: 16 bpp, 18 bpp packed, 18 bpp loosely packed (3 byte format), and 24bpp

Interfaces

- Complies with Protocol-to-PHY Interface (PPI) in 1.0 Gbps / 1.5 Gbps MIPI DPHY
- Supports RGB Interface for Video Image Input from general display controller
- Supports S-i80 (Synchronous i80) Interface for Command Mode Image input from display controller
- Supports PMS control interface for PLL to configure byte clock frequency
- Supports Prescaler to generate escape clock from byte clock

For additional details, please refer to the “MIPI DSI Host Controller” chapter of the “i.MX7 Reference Manual”.

Table 11 - MIPI Display Signal Description

| PIN | CPU BALL | CPU PAD NAME | V | I/O | Description |
|-------|----------|----------------|-----|-----|---|
| X2_53 | B20 | MIPI_DSI_D0_P | 2V5 | O | MIPI Display Serial Interface data pair 0 positive signal |
| X2_55 | A20 | MIPI_DSI_D0_N | 2V5 | O | MIPI Display Serial Interface data pair 0 negative signal |
| X2_57 | B18 | MIPI_DSI_D1_P | 2V5 | O | MIPI Display Serial Interface data pair 1 positive signal |
| X2_59 | A18 | MIPI_DSI_D1_N | 2V5 | O | MIPI Display Serial Interface data pair 1 negative signal |
| X2_61 | A19 | MIPI_DSI_CLK_N | 2V5 | O | MIPI Display Serial Interface clock pair negative signal |
| X2_63 | B19 | MIPI_DSI_CLK_P | 2V5 | O | MIPI Display Serial Interface clock pair positive signal |

3.4. MIPI Camera

The PICO-IMX7 provides MIPI Serial Interface camera signals.

The MIPI CSI-2 Host Controller supports the following features:

- Compliant to MIPI D-phy standard specification V1.1
- Compliant to previous version of Samsung D-phy
- Compliant to MIPI CSI2 Standard Specification V1.01r06
- Support primary and secondary Image format
- YUV420, YUV420 (Legacy), YUV420 (CSPS), YUV422 of 8-bits and 10-bits
- RGB565, RGB666, RGB888
- RAW6, RAW7, RAW8, RAW10, RAW12, RAW14
- Compressed format: 10-6-10, 10-7-10, 10-8-10, 14-10-14
- All of user defined byte-based Data packet
- Support embedded byte-based non-Image data packet and generic short packets
- Support interleave mode using Virtual channel
- Support up to two D-PHY Rx Data Lanes

Interfaces

- Compatible to PPI (Protocol-to-PHY Interface) in MIPI D-PHY Specification
- Image output data bus width: 32 bits (optional)
- Support four channel virtual channels or data interleave

Memory

- Non-image memory
- 8 KB SRAM for asynchronous clock domain
- This memory can store maximum 4 KB of non-image data per frame.

Image Memory

- 1KB SRAM for image memory
- This memory works as buffering for the difference of input / output bandwidth
- Pixel clock can be gated when no ppi data is coming.

For additional details, please refer to the “MIPI - Camera Serial Interface Host Controller (MIPI_CSI)” chapter of the “i.MX7 Reference Manual”.

Table 12 - MIPI Camera Signal Description

| PIN | CPU BALL | CPU PAD NAME | V | I/O | Description |
|-------|----------|----------------|-----|-----|--|
| X2_31 | A15 | MIPI_CSI_CLK_N | 2V5 | I | MIPI Camera Serial Interface clock pair negative signal |
| X2_33 | B15 | MIPI_CSI_CLK_P | 2V5 | I | MIPI Camera Serial Interface clock pair positive signal |
| X2_35 | A16 | MIPI_CSI_D0_N | 2V5 | I | MIPI Camera Serial Interface data pair 0 negative signal |
| X2_37 | B16 | MIPI_CSI_D0_P | 2V5 | I | MIPI Camera Serial Interface data pair 0 positive signal |
| X2_39 | B14 | MIPI_CSI_D1_P | 2V5 | I | MIPI Camera Serial Interface data pair 1 positive signal |
| X2_41 | A14 | MIPI_CSI_D1_N | 2V5 | I | MIPI Camera Serial Interface data pair 1 negative signal |

3.5. Audio Interface

The PICO-IMX7 synchronous audio interface (SAI) supports full-duplex serial interfaces with frame synchronization such as I2S, AC97, TDM, and codec/DSP interfaces.

Key features of the audio signal block include:

- Transmitter with independent bit clock and frame sync supporting 1 data line
- Receiver with independent bit clock and frame sync supporting 1 data line
- Maximum Frame Size of 32 words
- Word size of between 8-bits and 32-bits
- Word size configured separately for first word and remaining words in frame
- Asynchronous 32 x 32-bit FIFO for each transmit and receive channel
- Supports graceful restart after FIFO error

For additional details, please refer to the “Synchronous Audio Interface (SAI)” chapter of the “i.MX7 Application Processor Reference Manual”.

Table 13 - I²S Audio Signal Description

| PIN | CPU BALL | CPU PAD NAME | Signal | V | I/O | Description |
|-------|----------|--------------|--------------|-----|-----|--|
| E1_50 | D16 | ENET1_TX_CLK | SAI1_RX_DATA | 1V8 | I | Integrated Interchip Sound (I ² S) channel receive data line |
| E1_52 | D15 | ENET1_RX_CLK | SAI1_TX_BCLK | 1V8 | O | Integrated Interchip Sound (I ² S) channel word clock signal |
| E1_54 | E19 | ENET1_CRS | SAI1_TX_SYNC | 1V8 | I/O | Integrated Interchip Sound (I ² S) channel frame synchronization signal |
| E1_56 | D19 | ENET1_COL | SAI1_TX_DATA | 1V8 | O | Integrated Interchip Sound (I ² S) channel transmit data line |

3.6. PCI Express

The PICO-IMX7 is equipped with a single lane PCI Express interface.

PCI Express PHY Features

- 1.5 / 2.5 / 3.0 / 5.0 / 6.0 Gbps Serializer / Deserializer
- Compliant with PCI Express Base Specification 2.1
- Compliant with PIPE Specification 2.0
- 8 / 16 / 20 / 40-bit CMOS Interface for Transmitter and Receiver
- 25 / 100 MHz Reference Clock
- K28.5 Detection for Word Alignment
- 8B/10B Encoding / Decoding
- Receiver Detection
- Supports Spread Spectrum Clocking in Transmitter and Receiver

For additional details, please refer to the “PCI Express (PCIe)” chapter of the “i.MX7 Reference Manual”.

Table 14 - USB Host Signal Description

| PIN | CPU BALL | CPU PAD NAME | V | I/O | Description |
|-------|----------|------------------|-----|-----|---|
| X2_56 | AB10 | PCIE_REFCLKOUT_P | 2V5 | O | PCI Express clock differential pair positive signal |
| X2_58 | AC10 | PCIE_REFCLKOUT_N | 2V5 | O | PCI Express clock differential pair negative signal |
| X2_62 | AB11 | PCIE_TX_P | 2V5 | O | PCI Express Transmit output differential pair positive signal |
| X2_64 | AC11 | PCIE_TX_N | 2V5 | O | PCI Express Transmit output differential pair negative signal |
| X2_68 | AD11 | PCIE_RX_P | 2V5 | I | PCI Express Receive input differential pair positive signal |
| X2_70 | AE11 | PCIE_RX_N | 2V5 | I | PCI Express Receive input differential pair negative signal |

NOTE: The PCIE_TX pair has decoupling capacitors on the PICO Compute Module valued 10nF

3.7. Universal Serial Bus (USB) Interface

The PICO-IMX7 incorporates a single USB Host controller and an additional USB Host/OTG controller.

Each of the USB controllers provides the following main features:

USB 2.0 Host/OTG Controller

- High-Speed/Full-Speed/Low-Speed OTG core
- HS/FS/LS UTMI compliant interface
- High Speed, Full Speed and Low Speed operation in Host mode (with UTMI transceiver)
- High Speed, and Full Speed operation in Peripheral mode (with UTMI transceiver)
- Hardware support for OTG signaling, session request protocol, and host negotiation protocol
- Support charger detection

USB 2.0 Host Controller

- High-Speed/Full-Speed/Low-Speed Host-Only core
- HS/FS/LS UTMI compliant interface

For additional details, please refer to the “Universal Serial Bus Controller (USB)” chapter of the “i.MX7 Application Processor Reference Manual”.

Table 15 - USB Host Signal Description

| PIN | CPU BALL | CPU PAD NAME | Signal | V | I/O | Description |
|-------|----------|---------------|-------------|-----|-----|--|
| X2_46 | A10 | USB_OTG2_DN | | 3V3 | I/O | Universal Serial Bus differential pair negative signal |
| X2_48 | B10 | USB_OTG2_DP | | 3V3 | I/O | Universal Serial Bus differential pair positive signal |
| X2_50 | C10 | USB_OTG2_VBUS | | 5V | I/O | Universal Serial Bus power |
| X2_52 | M5 | UART3_RTS | USB_OTG2_OC | 3V3 | I | Active low input, to inform USB overcurrent condition (low = overcurrent detected) |

Table 16 - USB OTG Signal Description

| PIN | CPU BALL | CPU PAD NAME | Signal | V | I/O | Description |
|-------|----------|---------------|---------------|-----|-----|---|
| E1_3 | B7 | USB_OTG1_ID | USB_OTG1_ID | 3V3 | I | USB OTG ID Pin |
| E1_16 | B8 | USB_OTG1_DP | USB_OTG1_DP | 3V3 | I/O | Universal Serial Bus differential pair positive signal |
| E1_18 | A8 | USB_OTG1_DN | USB_OTG1_DN | 3V3 | I/O | Universal Serial Bus differential pair negative signal |
| E1_19 | M1 | UART3_RXD | USB_OTG1_OC | 1V8 | I | Over current detect input pin to monitor USB power over current |
| E1_20 | C8 | USB_OTG1_VBUS | USB_OTG1_VBUS | 5V | I/O | Universal Serial Bus power |
| E1_21 | M2 | UART3_TXD | USB_OTG1_PWR | 1V8 | O | Universal Serial Bus power enable |

NOTE: While using USB OTG in USB HOST mode. The USB_ID pin should have a pull-down resistor to GND.

3.8. SDIO/MMC Interface

The PICO-IMX7 features a MMC / SD / SDIO host interfaces connected to the NXP i.MX7 integrated “Ultra Secured Digital Host Controller” (uSDHC).

The following main features are supported by uSDHC:

- Conforms to the SD Host Controller Standard Specification version 3.0
- Compatible with the MMC System Specification version 4.2/4.3/4.4/4.41/4.5/5.0
- Compatible with the SD Memory Card Specification version 3.0 and supports the Extended Capacity SD Memory Card
- Compatible with the SDIO Card Specification version 3.0
- Designed to work with SD Memory, miniSD Memory, SDIO, miniSDIO, SD Combo, MMC, MMC plus, and MMC RS cards
- Card bus clock frequency up to 208 MHz
- Supports 1-bit / 4-bit SD and SDIO modes, 1-bit / 4-bit / 8-bit MMC modes

The MMC/SD/SDIO host controller can support a single MMC / SD / SDIO card or device.

For additional details, please refer to the “Ultra Secured Digital Host Controller (uSDHC)” chapter of the “i.MX7 Reference Manual”.

Table 17 - SDIO/MMC Interface Signal Description

| PIN | CPU BALL | CPU PAD NAME | Signal | V | I/O | Description |
|-------|----------|--------------|----------|-----|-----|-----------------------------------|
| E1_58 | D20 | SD1_CLK | SD1_CLK | 1V8 | I/O | MMC/SDIO Clock |
| E1_60 | M21 | EIM_DA9 | EIM_DA9 | 1V8 | I | SD Card detect input (Active low) |
| E1_62 | B21 | SD1_CMD | SD1_CMD | 1V8 | I/O | MMC/SDIO Command |
| E1_64 | E19 | SD1_DAT2 | SD1_DAT2 | 1V8 | I/O | MMC/SDIO Data bit 2 |
| E1_66 | A21 | SD1_DAT0 | SD1_DAT0 | 1V8 | I/O | MMC/SDIO Data bit 0 |
| E1_68 | F18 | SD1_DAT3 | SD1_DAT3 | 1V8 | I/O | MMC/SDIO Data bit 3 |
| E1_70 | C20 | SD1_DAT1 | SD1_DAT1 | 1V8 | I/O | MMC/SDIO Data bit 1 |

3.9. CAN BUS Interface signals

The PICO-IMX7 features two CAN bus interfaces. The Flexible Controller Area Network (FLEXCAN) module is a communication controller implementing the CAN protocol according to the CAN 2.0B protocol specification.

The CAN protocol was primarily designed to be used as a vehicle serial data bus meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth. The FLEXCAN module is a full implementation of the CAN protocol specification, which supports both standard and extended message frames. 64 Message Buffers are supported.

FlexCAN supports the following main features:

- Compliant with the CAN 2.0B protocol specification
- Programmable bit rate up to 1 Mb/sec

Integration of a CAN Bus transceiver and optional galvanic isolation should be incorporated on your carrier board.

For additional details, please refer to the “Flexible Controller Area Network (FLEXCAN)” chapter of the “i.MX7 Application Processor Reference Manual”.

Table 18 - CAN Bus Signal Description

| PIN | CPU BALL | CPU PAD NAME | Signal | V | I/O | Description |
|-------|----------|--------------|-------------|-----|-----|---|
| X2_19 | C11 | SAI1_TXC | FLEXCAN1_TX | 3V3 | O | CAN (controller Area Network) transmit signal |
| X2_21 | E12 | SAI1_RXD | FLEXCAN1_RX | 3V3 | I | CAN (controller Area Network) receive signal |
| X2_25 | E11 | SAI1_TXD | FLEXCAN2_TX | 3V3 | O | CAN (controller Area Network) transmit signal |
| X2_27 | D11 | SAI1_TXFS | FLEXCAN2_RX | 3V3 | I | CAN (controller Area Network) receive signal |

3.10. Universal Asynchronous Receiver/Transmitter (UART) Interface

The PICO-IMX7 Universal Asynchronous Receiver/Transmitter (UART) provides serial communication capability with external devices through a level converter.

The i.MX7 processor integrated UARTs support the following features:

- High-speed TIA/EIA-232-F compatible, up to 5.0 Mbit/s.
- Serial IR interface low-speed, IrDA-compatible (up to 115.2 Kbit/s).
- 9-bit or Multidrop mode (RS-485) support (automatic slave address detection).
- 7 or 8 data bits for RS-232 characters or 9 bit RS-485 format, 1 or 2 stop bits.
- Programmable parity (even, odd, and no parity).
- Hardware flow control support for request to send (RTS) and clear to send (CTS) signals
- RXD input and TXD output can be inverted respectively in RS-232/RS-485 mode
- RS-485 driver direction control via CTS signal
- Auto baud rate detection (up to 115.2 Kbit/s)
- Two independent, 32-entry FIFOs for transmit and receive

For additional details, please refer to the “Universal Asynchronous Receiver/Transmitter (UART)” chapter of the “i.MX7 Application Processor Reference Manual”.

Table 19 - UART Signal Description

| PIN | CPU BALL | CPU PAD NAME | Signal | V | I/O | Description |
|-------|----------|--------------|---------------|-----|-----|--|
| E1_22 | L1 | I2C4_SCL | UART5_RXD | 1V8 | I | Universal Asynchronous Receive Transmit receive data signal |
| E1_27 | L2 | I2C4_SDA | UART5_TXD | 1V8 | O | Universal Asynchronous Receive Transmit transmit data signal |
| E1_46 | L25 | EPDC1_DATA09 | UART6_TX_DATA | 1V8 | O | Universal Asynchronous Receive Transmit transmit data signal |
| E1_61 | M23 | EPDC1_DATA08 | UART6_RX_DATA | 1V8 | I | Universal Asynchronous Receive Transmit receive data signal |
| E1_63 | L24 | EPDC1_DATA10 | UART6_RTS_B | 1V8 | I | Universal Asynchronous Receive Transmit request to send signal |
| E1_65 | L23 | EPDC1_DATA11 | UART6_CTS_B | 1V8 | O | Universal Asynchronous Receive Transmit clear to send signal |

NOTE: it is recommended to use the UART5 interface as system debug where possible and use the UART6 signals in applications where one serial port is required.

3.11. Serial Peripheral Interface (SPI)

The PICO-IMX7 features an Enhanced Configurable Serial Peripheral Interface (ECSPI) full-duplex, synchronous, four-wire serial communication block.

The following main features are supported:

- Full-duplex synchronous serial interface
- Master/Slave configurable
- Transfer continuation function allows unlimited length data transfers
- 32-bit wide by 64-entry FIFO for both transmit and receive data
- Polarity and phase of the Chip Select (SS) and SPI Clock (SCLK) are configurable
- Direct Memory Access (DMA) support
- Max operation frequency up to the reference clock frequency.

For additional details, please refer to the “Enhanced Configurable SPI (ECSPI)” chapter of the “i.MX7 Application Processor Reference Manual”.

Table 20 - SPI Channel Signal Description

| PIN | CPU BALL | CPU PAD NAME | Signal | V | I/O | Description |
|-------|----------|--------------|-------------|-----|-----|--|
| E1_53 | K3 | I2C2_SDA | ECSPI3_SS0 | 1V8 | O | Serial Peripheral Interface Chip Select signal |
| E1_55 | K2 | I2C2_SCL | ECSPI3_SCLK | 1V8 | I/O | Serial Peripheral Interface clock signal |
| E1_57 | K1 | I2C1_SDA | ECSPI3_MOSI | 1V8 | I/O | Serial Peripheral Interface master output slave input signal |
| E1_59 | J2 | I2C1_SCL | ECSPI3_MISO | 1V8 | I/O | Serial Peripheral Interface master input slave output signal |

3.12. I²C Bus

The PICO-IMX7 incorporates several I²C interfaces. I²C is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange, minimizing the interconnection between devices. This bus is suitable for applications requiring occasional communications over a short distance between many devices.

The following features are supported:

- Compliance with Philips I²C specification version 2.1
- Multiple-master operation
- Support for standard mode (up to 100K bits/s) and fast mode (up to 400K bits/s)
- Arbitration-lost interrupt with automatic mode switching from master to slave

For additional details, please refer to the “I2C Controller (I2C)” chapter of the “i.MX7 Application Processor Reference Manual”.

Table 21 - I²C Bus Signal Description

| PIN | CPU BALL | CPU PAD NAME | Signal | V | I/O | Description |
|-------|----------|--------------|----------|-----|-----|---------------------------------|
| E1_41 | L3 | UART1_RXD | I2C1_SCL | 1V8 | I/O | I ² C bus clock line |
| E1_43 | L4 | UART1_TXD | I2C1_SDA | 1V8 | I/O | I ² C bus data line |
| E1_45 | L5 | UART2_RXD | I2C2_SCL | 1V8 | I/O | I ² C bus clock line |
| E1_47 | L6 | UART2_TXD | I2C2_SDA | 1V8 | I/O | I ² C bus data line |
| X2_13 | C12 | SAI1_RXFS | I2C4_SCL | 3V3 | I/O | I ² C bus clock line |
| X2_15 | D12 | SAI1_RXC | I2C4_SDA | 3V3 | I/O | I ² C bus data line |

NOTE: All 1V8 I²C bus data and clock lines for all I²C interfaces have 2.2K Ω pull-up resistors present on the PICO-IMX7 module.

NOTE: All 3V3 I²C bus data and clock lines for all I²C interfaces have 1.5K Ω pull-up resistors present on the PICO-IMX7 module.

3.13. General Purpose Input/Output (GPIO)

The PICO-7 has 10 dedicated GPIO pins at 1.8V and 3 dedicated GPIO at 3.3V. Many of the other pins used on the PICO Compute Module can be put in GPIO module however doing so might break scalability with other PICO Compute Modules.

The GPIO signals can be configured for the following applications:

- Data input / output
- Interrupt generation

For additional details, please refer to the “General Purpose Input/Output (GPIO)” chapter of the “i.MX7 Application Processor Reference Manual”.

Table 22 - GPIO Signal Description

| PIN | CPU BALL | CPU PAD NAME | Signal | V | I/O | Description |
|-------|----------|--------------|------------|-----|-----|------------------------------|
| E1_24 | P20 | EPDC1_DATA00 | GPIO2_IO00 | 1V8 | I/O | General Purpose Input Output |
| E1_25 | M21 | EPDC_D06 | GPIO2_IO06 | 1V8 | I/O | General Purpose Input Output |
| E1_26 | P21 | EPDC1_D01 | GPIO2_IO01 | 1V8 | I/O | General Purpose Input Output |
| E1_28 | N20 | EPDC1_D02 | GPIO2_IO02 | 1V8 | I/O | General Purpose Input Output |
| E1_30 | N21 | EPDC1_D03 | GPIO2_IO03 | 1V8 | I/O | General Purpose Input Output |
| E1_32 | N22 | EPDC1_D04 | GPIO2_IO04 | 1V8 | I/O | General Purpose Input Output |
| E1_34 | M20 | EPDC1_D05 | GPIO2_IO05 | 1V8 | I/O | General Purpose Input Output |
| E1_42 | L22 | EPDC1_D12 | GPIO2_IO12 | 1V8 | I/O | General Purpose Input Output |
| E1_44 | L21 | EPDC1_D13 | GPIO2_IO13 | 1V8 | I/O | General Purpose Input Output |
| E1_48 | M22 | EPDC1_D07 | GPIO2_IO07 | 1V8 | I/O | General Purpose Input Output |
| X2_65 | P1 | GPIO1_IO05 | GPIO1_IO05 | 3V3 | I/O | General Purpose Input Output |
| X2_67 | N6 | GPIO1_IO04 | GPIO1_IO04 | 3V3 | I/O | General Purpose Input Output |
| X2_69 | N3 | GPIO1_IO02 | GPIO1_IO02 | 3V3 | I/O | General Purpose Input Output |

3.14. Pulse Width Modulation (PWM)

The PICO-IMX7 has 4 dedicated PWM pins at 1.8V and 1 PWM for LCD brightness control at 3.3V.

The following features characterize the PWM:

- 16-bit up-counter with clock source selection
- 4 x 16 FIFO to minimize interrupt overhead
- 12-bit prescaler for division of clock
- Sound and melody generation
- Active high or active low configured output
- Can be programmed to be active in low-power mode
- Can be programmed to be active in debug mode
- Interrupts at compare and rollover

For additional details, please refer to the “Pulse Width Modulation (PWM)” chapter of the “i.MX7 Application Processor Reference Manual”.

Table 23 - PWM Signal Description

| PIN | CPU BALL | CPU PAD NAME | Signal | V | I/O | Description |
|--------|----------|--------------|----------|-----|-----|---|
| E1_33 | R1 | GPIO1_IO08 | PWM1_OUT | 1V8 | O | General Purpose Input Output with PWM control |
| E1_35 | R2 | GPIO1_IO09 | PWM2_OUT | 1V8 | O | General Purpose Input Output with PWM control |
| E1_37 | R5 | GPIO1_IO10 | PWM3_OUT | 1V8 | O | General Purpose Input Output with PWM control |
| E1_39* | T1 | GPIO1_IO11 | PWM4_OUT | 1V8 | O | General Purpose Input Output with PWM control |
| X1_66* | T1 | GPIO1_IO11 | PWM4_OUT | 3V3 | O | LCD Backlight brightness Control |

3.15. Manufacturing and Boot Control

The PICO-IMX7 has a number of pins to override the default boot media present on the PICO-IMX7 Compute Module or enable debug serial loader functionality.

Table 24 - Boot Selection Pins

| PIN | CPU BALL | CPU PAD NAME | Signal | V | I/O | Description |
|------|----------|--------------|----------|-----|-----|-----------------|
| X2_3 | G20 | BT_CFG11 | BT_CFG11 | 1V8 | I | Boot Select pin |
| X2_5 | C22 | BT_CFG4 | BT_CFG4 | 1V8 | I | Boot Select pin |
| X2_7 | F21 | BT_CFG12 | BT_CFG12 | 1V8 | I | Boot Select pin |
| X2_9 | E22 | BT_CFG13 | BT_CFG13 | 1V8 | I | Boot Select pin |

3.15.1. Boot Modes

The PICO-IMX7 Compute Module automatically boot from the internal eMMC if the above signals keep floating. Only when Serial Downloader Mode is required the signals need to be connected as **Table 25 - Serial Downloader Boot Mode Configuration** below.

Table 25 - Serial Downloader Boot Mode Configuration

| PIN | CPU BALL | Serial Downloader Mode |
|------|----------|------------------------|
| X2_3 | G20 | HIGH |
| X2_5 | C22 | LOW |
| X2_7 | F21 | Not Connected |
| X2_9 | E22 | Not Connected |

Table 26 - Internal Downloader Boot Mode Configuration

| PIN | CPU BALL | Internal (eMMC) Boot Mode |
|------|----------|---------------------------|
| X2_3 | G20 | LOW |
| X2_5 | C22 | HIGH |
| X2_7 | F21 | Not Connected |
| X2_9 | E22 | Not Connected |

3.16. Input Power Requirements

The PICO-IMX7 is designed to be driven with a single input power rail.

The power domain pins have to be connected as follow:

- All GND pins have to be connected to the carrier board ground pane.
- All VSYS pins should be connected to the main power source.

Table 27 - Input Power Signals

| Power Rail | Nominal Input | Input Range | Maximum Input Ripple |
|--------------|---------------|----------------|----------------------|
| VSYS (4 pin) | 5V | +4.2V - +5.25V | ±50 mV |

3.16.1. Power Management Signals

The PICO-IMX7 has the following set of signals to control the system power states such as the power-on and reset conditions. This enables the system designer to implement a fully ACPI compliant system supporting system states.

Table 28 - Power Management Signals

| PIN | CPU BALL | CPU PAD NAME | Signal | V | I/O | Description |
|-------|----------|--------------|--------|-----|-----|------------------------------|
| E1_17 | AC8 | ONOFF | ONOFF | 3V3 | I | Power ON button input signal |
| E1_36 | PMIC | RESET | RESET | 1V8 | I | Reset power signal |

NOTE: Pin E1_36 is described in detail in **chapter 2.2. Power Management IC** of this manual

3.16.2. Power Sequence

PICO-IMX7 input power sequencing requirements are as follow:

If a backup Real Time Clock (RTC) is required in the host system. We recommend to design an RTC circuit on the PICO carrier board. For example the Maxim Integrated DS1337+ connected over the general purpose I²C can be used.

Start Sequence:

VCC_RTC must come up at the same time or before VCC comes up.

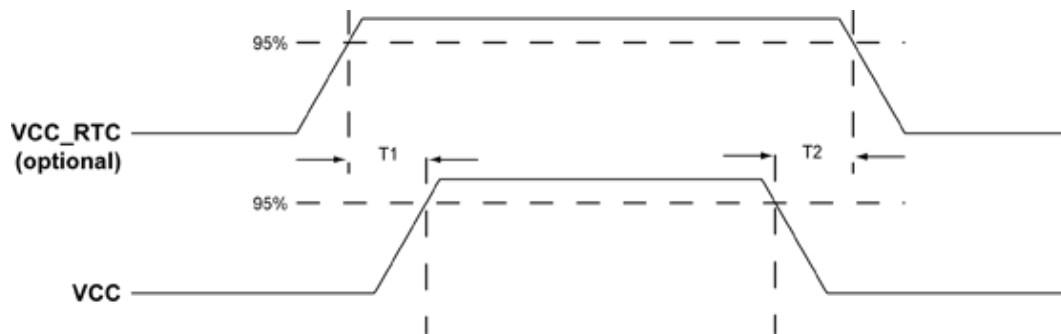
Stop Sequence:

VCC must go down at the same time or before VCC_RTC goes down

Table 29 - Input Power Sequencing

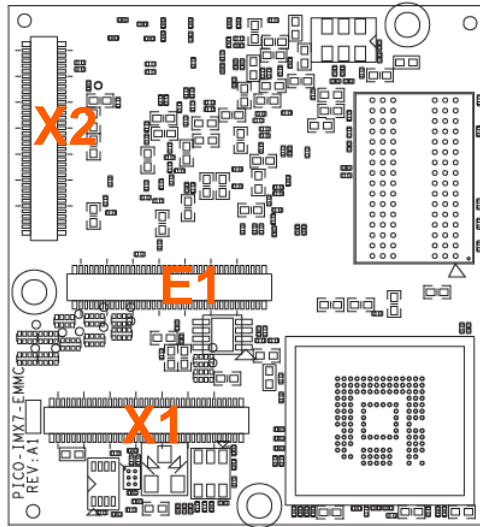
| Item | Description | Value |
|------|--------------------------|--------|
| T1 | VCC_RTC rise to VCC rise | ≥ 0 ms |
| T2 | VCC fall to VCC_RTC fall | ≥ 0 ms |

Figure 14 - Input Power sequence



4. PICO Compute Module Pin Assignment

The PICO-IMX7 has three 70-pin Hirose board to board connectors.



| PIN | CPU BALL | CPU PAD NAME | Signal | V | I/O | Description |
|-------|----------|--------------|-------------|-----|-----|--|
| E1_1 | | | GND | | P | Ground |
| E1_2 | | | VSYS | | P | System input power (4.0 to 5.25V) |
| E1_3 | B7 | USB_OTG1_ID | USB_OTG1_ID | 3V3 | I | USB OTG ID Pin |
| E1_4 | | | VSYS | | P | System input power (4.0 to 5.25V) |
| E1_5 | | | GND | | P | Ground |
| E1_6 | | | VSYS | | P | System input power (4.0 to 5.25V) |
| E1_7 | N5 | CLK_32K_OUT | CLK_32K_OUT | 3V3 | | |
| E1_8 | | | 3V3 | | P | System 3.3V Output |
| E1_9 | | | GND | | P | Ground |
| E1_10 | | | 3V3 | | P | System 3.3V Output |
| E1_11 | | | GND | | P | Ground |
| E1_12 | | | 1V8 | | P | System 1.8V Output (same as E1 connector I/O voltage levels) |
| E1_13 | | | GND | | P | Ground |
| E1_14 | | | VSYS | | P | System input power (4.0 to 5.25V) |
| E1_15 | | | GND | | P | Ground |
| E1_16 | B8 | USB_OTG1_DP | USB_OTG1_DP | 3V3 | I/O | Universal Serial Bus differential pair positive signal |

| PIN | CPU BALL | CPU PAD NAME | Signal | V | I/O | Description |
|-------|----------|---------------|---------------|-----|-----|---|
| E1_17 | AC8 | ONOFF | ONOFF | 3V3 | I | Power ON button input signal |
| E1_18 | A8 | USB_OTG1_DN | USB_OTG1_DN | 3V3 | I/O | Universal Serial Bus differential pair negative signal |
| E1_19 | M1 | UART3_RXD | USB_OTG1_OC | 1V8 | I | Over current detect input pin to monitor USB power over current |
| E1_20 | C8 | USB_OTG1_VBUS | USB_OTG1_VBUS | 5V | I/O | Universal Serial Bus power |
| E1_21 | M2 | UART3_TXD | USB_OTG1_PWR | 1V8 | O | Universal Serial Bus power enable |
| E1_22 | L1 | I2C4_SCL | UART5_RXD | 1V8 | I | Universal Asynchronous Receive Transmit receive data signal |
| E1_23 | | | VCC_RTC | 3V3 | P | RTC Power |
| E1_24 | P20 | EPDC1_DATA00 | GPIO2_IO00 | 1V8 | I/O | General Purpose Input Output |
| E1_25 | M21 | EPDC_D06 | GPIO2_IO06 | 1V8 | I/O | General Purpose Input Output |
| E1_26 | P21 | EPDC1_D01 | GPIO2_IO01 | 1V8 | I/O | General Purpose Input Output |
| E1_27 | L2 | I2C4_SDA | UART5_TXD | 1V8 | O | Universal Asynchronous Receive Transmit transmit data signal |
| E1_28 | N20 | EPDC1_D02 | GPIO2_IO02 | 1V8 | I/O | General Purpose Input Output |
| E1_29 | | | NC | | | Not Connected |
| E1_30 | N21 | EPDC1_D03 | GPIO2_IO03 | 1V8 | I/O | General Purpose Input Output |
| E1_31 | | | NC | | | Not Connected |
| E1_32 | N22 | EPDC1_D04 | GPIO2_IO04 | 1V8 | I/O | General Purpose Input Output |
| E1_33 | R1 | GPIO1_IO08 | PWM1_OUT | 1V8 | O | General Purpose Input Output with PWM control |
| E1_34 | M20 | EPDC1_D05 | GPIO2_IO05 | 1V8 | I/O | General Purpose Input Output |
| E1_35 | R2 | GPIO1_IO09 | PWM2_OUT | 1V8 | O | General Purpose Input Output with PWM control |
| E1_36 | PMIC | RESET | RESET | 1V8 | I | Reset power signal |
| E1_37 | R5 | GPIO1_IO10 | PWM3_OUT | 1V8 | O | General Purpose Input Output with PWM control |
| E1_38 | | | NC | | | Not Connected |
| E1_39 | T1 | GPIO1_IO11 | PWM4_OUT | 1V8 | O | General Purpose Input Output with PWM control |
| E1_40 | | | NC | | | Not Connected |
| E1_41 | L3 | UART1_RXD | I2C1_SCL | 1V8 | I/O | I ² C bus clock line |
| E1_42 | L22 | EPDC1_D12 | GPIO2_IO12 | 1V8 | I/O | General Purpose Input Output |
| E1_43 | L4 | UART1_TXD | I2C1_SDA | 1V8 | I/O | I ² C bus data line |
| E1_44 | L21 | EPDC1_D13 | GPIO2_IO13 | 1V8 | I/O | General Purpose Input Output |
| E1_45 | L5 | UART2_RXD | I2C2_SCL | 1V8 | I/O | I ² C bus clock line |

| PIN | CPU BALL | CPU PAD NAME | Signal | V | I/O | Description |
|-------|----------|--------------|---------------|-----|-----|--|
| E1_46 | L25 | EPDC1_DATA09 | UART6_TX_DATA | 1V8 | O | Universal Asynchronous Receive Transmit transmit data signal |
| E1_47 | L6 | UART2_TXD | I2C2_SDA | 1V8 | I/O | I ² C bus data line |
| E1_48 | M22 | EPDC1_D07 | GPIO2_IO07 | 1V8 | I/O | General Purpose Input Output |
| E1_49 | | | NC | | | Not Connected |
| E1_50 | D16 | ENET1_TX_CLK | SAI1_RX_DATA | 1V8 | I | Integrated Interchip Sound (I ² S) channel receive data line |
| E1_51 | M6 | UART3_CTS | ECSPI1_SS0 | 1V8 | O | Serial Peripheral Interface Chip Select Signal |
| E1_52 | D15 | ENET1_RX_CLK | SAI1_TX_BCLK | 1V8 | O | Integrated Interchip Sound (I ² S) channel word clock signal |
| E1_53 | K3 | I2C2_SDA | ECSPI3_SS0 | 1V8 | O | Serial Peripheral Interface Chip Select signal |
| E1_54 | E19 | ENET1_CRS | SAI1_TX_SYNC | 1V8 | I/O | Integrated Interchip Sound (I ² S) channel frame synchronization signal |
| E1_55 | K2 | I2C2_SCL | ECSPI3_SCLK | 1V8 | I/O | Serial Peripheral Interface clock signal |
| E1_56 | D19 | ENET1_COL | SAI1_TX_DATA | 1V8 | O | Integrated Interchip Sound (I ² S) channel transmit data line |
| E1_57 | K1 | I2C1_SDA | ECSPI3_MOSI | 1V8 | I/O | Serial Peripheral Interface master output slave input signal |
| E1_58 | B5 | SD1_CLK | SD1_CLK | 1V8 | I/O | MMC/SDIO Clock |
| E1_59 | J2 | I2C1_SCL | ECSPI3_MISO | 1V8 | I/O | Serial Peripheral Interface master input slave output signal |
| E1_60 | C6 | SD1_CD_B | SD1_CD_B | 1V8 | I | SD Card detect input (Active low) |
| E1_61 | M23 | EPDC1_DATA08 | UART6_RX_DATA | 1V8 | I | Universal Asynchronous Receive Transmit receive data signal |
| E1_62 | C5 | SD1_CMD | SD1_CMD | 1V8 | I/O | MMC/SDIO Command |
| E1_63 | L24 | EPDC1_DATA10 | UART6_RTS_B | 1V8 | I | Universal Asynchronous Receive Transmit request to send signal |
| E1_64 | A4 | SD1_DATA2 | SD1_DATA2 | 1V8 | I/O | MMC/SDIO Data bit 2 |
| E1_65 | L23 | EPDC1_DATA11 | UART6_CTS_B | 1V8 | O | Universal Asynchronous Receive Transmit clear to send signal |
| E1_66 | A5 | SD1_DATA0 | SD1_DATA0 | 1V8 | I/O | MMC/SDIO Data bit 0 |
| E1_67 | | | NC | | | Not Connected |
| E1_68 | D5 | SD1_DATA3 | SD1_DATA3 | 1V8 | I/O | MMC/SDIO Data bit 3 |
| E1_69 | | | NC | | | Not Connected |
| E1_70 | D6 | SD1_DATA1 | SD1_DATA1 | 1V8 | I/O | MMC/SDIO Data bit 1 |

| PIN | CPU BALL | CPU PAD NAME | Signal | V | I/O | Description |
|-------|----------|--------------|-------------------|-----|-----|--------------------------------------|
| X1_1 | | | GND | | P | Ground |
| X1_2 | | | GND | | P | Ground |
| X1_3 | | | NC | | | Not Connected |
| X1_4 | | | NC | | | Not Connected |
| X1_5 | | | NC | | | Not Connected |
| X1_6 | | | NC | | | Not Connected |
| X1_7 | | | GND | | P | Ground |
| X1_8 | G23 | LCD1_DATA23 | LCD_DATA23 | 3V3 | O | LCD Pixel Data bit 23 |
| X1_9 | | | NC | | | Not Connected |
| X1_10 | D25 | LCD1_DATA22 | LCD_DATA22 | 3V3 | O | LCD Pixel Data bit 22 |
| X1_11 | | | NC | | | Not Connected |
| X1_12 | E24 | LCD1_DATA21 | LCD_DATA21 | 3V3 | O | LCD Pixel Data bit 21 |
| X1_13 | | | GND | | P | Ground |
| X1_14 | C25 | LCD1_DATA20 | LCD_DATA20 | 3V3 | O | LCD Pixel Data bit 20 |
| X1_15 | | | NC | | | Not Connected |
| X1_16 | D24 | LCD1_DATA19 | LCD_DATA19 | 3V3 | O | LCD Pixel Data bit 19 |
| X1_17 | | | NC | | | Not Connected |
| X1_18 | E23 | LCD1_DATA18 | LCD_DATA18 | 3V3 | O | LCD Pixel Data bit 18 |
| X1_19 | | | GND | | P | Ground |
| X1_20 | G21 | LCD1_DATA17 | LCD_DATA17 | 3V3 | O | LCD Pixel Data bit 17 |
| X1_21 | | | NC | | | Not Connected |
| X1_22 | B25 | LCD1_DATA16 | LCD_DATA16 | 3V3 | O | LCD Pixel Data bit 16 |
| X1_23 | | | NC | | | Not Connected |
| X1_24 | C24 | LCD1_DATA15 | LCD_DATA15 | 3V3 | O | LCD Pixel Data bit 15 |
| X1_25 | | | GND | | P | Ground |
| X1_26 | D23 | LCD1_DATA14 | LCD_DATA14 | 3V3 | O | LCD Pixel Data bit 14 |
| X1_27 | | | NC | | | Not Connected |
| X1_28 | E22 | LCD1_DATA13 | LCD_DATA13 | 3V3 | O | LCD Pixel Data bit 13 |
| X1_29 | | | NC | | | Not Connected |
| X1_30 | F21 | LCD1_DATA12 | LCD_DATA12 | 3V3 | O | LCD Pixel Data bit 12 |
| X1_31 | | | GND | | P | Ground |
| X1_32 | G20 | LCD1_DATA11 | LCD_DATA11 | 3V3 | O | LCD Pixel Data bit 11 |
| X1_33 | C3 | SD2_WP | ENET1_MDC | 3V3 | | Management data clock reference |
| X1_34 | B24 | LCD1_DATA10 | LCD_DATA10 | 3V3 | O | LCD Pixel Data bit 10 |
| X1_35 | D3 | SD2_CD_B | ENET1_MDIO | 3V3 | | Management data |
| X1_36 | C23 | LCD1_DATA09 | LCD_DATA09 | 3V3 | O | LCD Pixel Data bit 9 |
| X1_37 | G1 | SD3_RESET_B | GPIO6_IO11 | 3V3 | | Ethernet reset |
| X1_38 | E21 | LCD1_DATA08 | LCD_DATA08 | 3V3 | O | LCD Pixel Data bit 8 |
| X1_39 | J1 | SD3_STROBE | GPIO6_IO10 | 3V3 | | Ethernet interrupt output |
| X1_40 | F20 | LCD1_DATA07 | LCD_DATA07 | 3V3 | O | LCD Pixel Data bit 7 |
| X1_41 | N2 | GPIO1_IO01 | CCM_ENET_REF_CLK3 | 3V3 | | Synchronous Ethernet recovered clock |
| X1_42 | A24 | LCD1_DATA06 | LCD_DATA06 | 3V3 | O | LCD Pixel Data bit 6 |
| X1_43 | E16 | ENET1_TX_CTL | RGMII1_TX_CTL | 1V8 | O | RGMII transmit enable |
| X1_44 | B23 | LCD1_DATA05 | LCD_DATA05 | 3V3 | O | LCD Pixel Data bit 5 |
| X1_45 | E15 | ENET1_RX_CTL | RGMII1_RX_CTL | 1V8 | I | RGMII receive data valid |
| X1_46 | C22 | LCD1_DATA04 | LCD_DATA04 | 3V3 | O | LCD Pixel Data bit 4 |

| PIN | CPU BALL | CPU PAD NAME | Signal | V | I/O | Description |
|-------|----------|--------------|------------|-----|-----|----------------------------------|
| X1_47 | | | GND | | P | Ground |
| X1_48 | A23 | LCD1_DATA03 | LCD_DATA03 | 3V3 | O | LCD Pixel Data bit 3 |
| X1_49 | F16 | ENET1_TXC | RGMII1_TXC | 1V8 | O | RGMII transmit clock |
| X1_50 | B22 | LCD1_DATA02 | LCD_DATA02 | 3V3 | O | LCD Pixel Data bit 2 |
| X1_51 | F17 | ENET1_TDATA0 | RGMII1_TD0 | 1V8 | O | RGMII transmit data 0 |
| X1_52 | A22 | LCD1_DATA01 | LCD_DATA01 | 3V3 | O | LCD Pixel Data bit 1 |
| X1_53 | E17 | ENET1_TDATA1 | RGMII1_TD1 | 1V8 | O | RGMII transmit data 1 |
| X1_54 | D21 | LCD1_DATA00 | LCD_DATA00 | 3V3 | O | LCD Pixel Data bit 0 |
| X1_55 | E18 | ENET1_TDATA2 | RGMII1_TD2 | 1V8 | O | RGMII transmit data 2 |
| X1_56 | C21 | LCD1_RESET | LCD_RS | 3V3 | O | LCD backlight enable/disable |
| X1_57 | D18 | ENET1_TDATA3 | RGMII1_TD3 | 1V8 | O | RGMII transmit data 3 |
| X1_58 | E25 | LCD1_HSYNC | LCD_HSYNC | 3V3 | O | LCD Horizontal Synchronization |
| X1_59 | | | GND | | P | Ground |
| X1_60 | F25 | LCD1_ENABLE | LCD_ENABLE | 3V3 | O | LCD dot enable pin signal |
| X1_61 | F15 | ENET1_RXC | RGMII1_RXC | 1V8 | I | RGMII receive clock |
| X1_62 | F24 | LCD1_VSYNC | LCD_VSYNC | 3V3 | O | LCD Vertical Synchronization |
| X1_63 | E14 | ENET1_RDATA0 | RGMII1_RD0 | 1V8 | I | RGMII transmit data 0 |
| X1_64 | E20 | LCD1_CLK | LCD_CLK | 3V3 | O | LCD Pixel Clock |
| X1_65 | F14 | ENET1_RDATA1 | RGMII1_RD1 | 1V8 | I | RGMII receive data 1 |
| X1_66 | T1 | GPIO1_IO11 | PWM4_OUT | 3V3 | O | LCD Backlight brightness Control |
| X1_67 | D13 | ENET1_RDATA2 | RGMII1_RD2 | 1V8 | I | RGMII receive data 2 |
| X1_68 | P2 | GPIO1_IO06 | GPIO1_IO06 | 3V3 | O | LCD Voltage On |
| X1_69 | E13 | ENET1_RDATA3 | RGMII1_RD3 | 1V8 | I | RGMII receive data 3 |
| X1_70 | | | GND | | P | Ground |

| PIN | CPU BALL | CPU PAD NAME | Signal | V | I/O | Description |
|-------|----------|----------------|-------------|-----|-----|--|
| X2_1 | | | GND | | P | Ground |
| X2_2 | | | GND | | P | Ground |
| X2_3 | G20 | BT_CFG11 | BT_CFG11 | 1V8 | I | Boot Select pin |
| X2_4 | | | NC | | | Not Connected |
| X2_5 | C22 | BT_CFG4 | BT_CFG4 | 1V8 | I | Boot Select pin |
| X2_6 | | | NC | | | Not Connected |
| X2_7 | F21 | BT_CFG12 | BT_CFG12 | 1V8 | I | Boot Select pin |
| X2_8 | | | GND | | P | Ground |
| X2_9 | E22 | BT_CFG13 | BT_CFG13 | 1V8 | I | Boot Select pin |
| X2_10 | | | NC | | | Not Connected |
| X2_11 | | | GND | | P | Ground |
| X2_12 | | | NC | | | Not Connected |
| X2_13 | C12 | SAI1_RXFS | I2C4_SCL | 3V3 | I/O | I ² C bus clock line |
| X2_14 | | | GND | | P | Ground |
| X2_15 | D12 | SAI1_RXC | I2C4_SDA | 3V3 | I/O | I ² C bus data line |
| X2_16 | | | NC | | | Not Connected |
| X2_17 | | | GND | | P | Ground |
| X2_18 | | | NC | | | Not Connected |
| X2_19 | C11 | SAI1_TXC | FLEXCAN1_TX | 3V3 | O | CAN (controller Area Network) transmit signal |
| X2_20 | | | GND | | P | Ground |
| X2_21 | E12 | SAI1_RXD | FLEXCAN1_RX | 3V3 | I | CAN (controller Area Network) receive signal |
| X2_22 | | | NC | | | Not Connected |
| X2_23 | | | GND | | P | Ground |
| X2_24 | | | NC | | | Not Connected |
| X2_25 | E11 | SAI1_TXD | FLEXCAN2_TX | 3V3 | O | CAN (controller Area Network) transmit signal |
| X2_26 | | | GND | | P | Ground |
| X2_27 | D11 | SAI1_TXFS | FLEXCAN2_RX | 3V3 | I | CAN (controller Area Network) receive signal |
| X2_28 | | | NC | | | Not Connected |
| X2_29 | | | GND | | P | Ground |
| X2_30 | | | NC | | | Not Connected |
| X2_31 | A15 | MIPI_CSI_CLK_N | | 2V5 | I | MIPI Camera Serial Interface clock pair negative signal |
| X2_32 | | | GND | | P | Ground |
| X2_33 | B15 | MIPI_CSI_CLK_P | | 2V5 | I | MIPI Camera Serial Interface clock pair positive signal |
| X2_34 | | | NC | | | Not Connected |
| X2_35 | A16 | MIPI_CSI_D0_N | | 2V5 | I | MIPI Camera Serial Interface data pair 0 negative signal |
| X2_36 | | | NC | | | Not Connected |
| X2_37 | B16 | MIPI_CSI_D0_P | | 2V5 | I | MIPI Camera Serial Interface data pair 0 positive signal |
| X2_38 | | | GND | | P | Ground |
| X2_39 | B14 | MIPI_CSI_D1_P | | 2V5 | I | MIPI Camera Serial Interface data pair 1 positive signal |
| X2_40 | | | NC | | | Not Connected |

| PIN | CPU BALL | CPU PAD NAME | Signal | V | I/O | Description |
|-------|----------|------------------|-------------|-----|-----|--|
| X2_41 | A14 | MIPI_CSI_D1_N | | 2V5 | I | MIPI Camera Serial Interface data pair 1 negative signal |
| X2_42 | | | NC | | | Not Connected |
| X2_43 | | | NC | | | Not Connected |
| X2_44 | | | GND | | P | Ground |
| X2_45 | | | NC | | | Not Connected |
| X2_46 | A10 | USB_OTG2_DN | | 3V3 | I/O | Universal Serial Bus differential pair negative signal |
| X2_47 | | | NC | | | Not Connected |
| X2_48 | B10 | USB_OTG2_DP | | 3V3 | I/O | Universal Serial Bus differential pair positive signal |
| X2_49 | | | NC | | | Not Connected |
| X2_50 | C10 | USB_OTG2_VBUS | | 5V | I/O | Universal Serial Bus power |
| X2_51 | | | GND | | P | Ground |
| X2_52 | M5 | UART3_RTS | USB_OTG2_OC | 3V3 | I | Active low input, to inform USB overcurrent condition (low = overcurrent detected) |
| X2_53 | B20 | MIPI_DSI_D0_P | | 2V5 | O | MIPI Display Serial Interface data pair 0 positive signal |
| X2_54 | | | GND | | P | Ground |
| X2_55 | A20 | MIPI_DSI_D0_N | | 2V5 | O | MIPI Display Serial Interface data pair 0 negative signal |
| X2_56 | AB10 | PCIE_REFCLKOUT_P | | 2V5 | O | PCI Express clock differential pair positive signal |
| X2_57 | B18 | MIPI_DSI_D1_P | | 2V5 | O | MIPI Display Serial Interface data pair 1 positive signal |
| X2_58 | AC10 | PCIE_REFCLKOUT_N | | 2V5 | O | PCI Express clock differential pair negative signal |
| X2_59 | A18 | MIPI_DSI_D1_N | | 2V5 | O | MIPI Display Serial Interface data pair 1 negative signal |
| X2_60 | | | GND | | P | Ground |
| X2_61 | A19 | MIPI_DSI_CLK_N | | 2V5 | O | MIPI Display Serial Interface clock pair negative signal |
| X2_62 | AB11 | PCIE_TX_P | | 2V5 | O | PCI Express Transmit output differential pair positive signal |
| X2_63 | B19 | MIPI_DSI_CLK_P | | 2V5 | O | MIPI Display Serial Interface clock pair positive signal |
| X2_64 | AC11 | PCIE_TX_N | | 2V5 | O | PCI Express Transmit output differential pair negative signal |
| X2_65 | P1 | GPIO1_IO05 | GPIO1_IO05 | 3V3 | I/O | General Purpose Input Output |

| PIN | CPU BALL | CPU PAD NAME | Signal | V | I/O | Description |
|-------|----------|--------------|------------|-----|-----|---|
| X2_66 | | | GND | | P | Ground |
| X2_67 | N6 | GPIO1_IO04 | GPIO1_IO04 | 3V3 | I/O | General Purpose Input Output |
| X2_68 | AD11 | PCIE_RX_P | | 2V5 | I | PCI Express Receive input differential pair positive signal |
| X2_69 | N3 | GPIO1_IO02 | GPIO1_IO02 | 3V3 | I/O | General Purpose Input Output |
| X2_70 | AE11 | PCIE_RX_N | | 2V5 | I | PCI Express Receive input differential pair negative signal |

5. Ordering Information

TechNexion provides a complete product portfolio for the PICO-IMX7 to assist our customers to evaluate, proto-type, integrate and mass produce solutions with our PICO Compute Modules.

5.1. PICO Compute Module Product Ordering Part Numbers

The PICO-IMX7 is available in a number of standard configurations. Custom tailored versions with other memory configuration, de-population of interfaces or extended and industrial temperature options are available upon request.

5.1.1 Standard Part Numbers

Standard part numbers can be easily found on the PICO-IMX7 product page on the TechNexion corporate homepage.

5.4.2. Custom Part Number Creation Rules

The PICO-IMX7 can be ordered in custom tailored to meet special application requirements and conditions according to the following custom part number creation rules.

Custom part numbers carry minimum order quantities. Please connect with your TechNexion representative for conditions and availability.

Part number format:

PICO-IMX7x-R20-E04-BW-xx-xxxx

| Interface | Code | Description |
|---------------------|------|---|
| Processor | S | i.MX7 Solo |
| | D | i.MX7 Dual |
| Memory | R05 | 512 MB DDR3 |
| | R10 | 1GB DDR3 |
| | R20 | 2GB DDR3 |
| Storage | MSD | MicroSD Cardslot |
| | E04 | eMMC 4GB (Default) |
| | Exx | Other capacities of eMMC are possible (8GB, 16GB, 32GB, 64GB) |
| Wireless Networking | - | No |
| | BB | 802.11bgn + Bluetooth 4.1 (BCM43438) |
| | BW | 802.11ac + Bluetooth 4.1 (BCM4339) |
| Temperature Range | - | Commercial Temperature range (0~60°C) (Default) |
| | TE | Extended Temperature range (-20~70°C) |
| | TI | Industrial Temperature range (-35~85°C) |
| Custom ID | XXXX | Custom Partnumber ID for customized software loader and special component (BOM) |

NOTE: Wireless Networking option is not available in “TI” Industrial Temperature Range.

6. Important Notice

TechNexion reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TechNexion terms and conditions of sale supplied at the time of order acknowledgment.

TechNexion warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TechNexion's standard warranty. Testing and other quality control techniques are used to the extent TechNexion deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TechNexion assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TechNexion components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

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