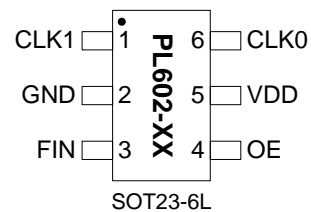
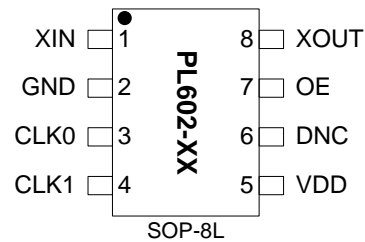


HCSL Compatible Clock Generator for PCI Express

FEATURES

- Input Frequency:
 - Fundamental Crystal or Reference Input: 25MHz
- Output Frequency:
 - PL602-21: 100MHz differential outputs.
 - PL602-22: 125MHz differential outputs.
 - PL602-23: 200MHz differential outputs.
 - PL602-26: 25MHz differential outputs.
 - PL602-27: 250MHz differential outputs.
 - PL602-15: 156.25 MHz differential outputs.
- Very low Jitter: 28ps Pk-Pk typ.
- Very low Phase Noise:
 - -130 dBc at 10kHz offset at 100MHz
- No external loop filter is required
- Power supply range: 2.25V to 3.63V
- Operating temperature range from -40°C to 85°C
- Available in 6-pin SOT or 8-pin SOP Green/RoHS compliant package.

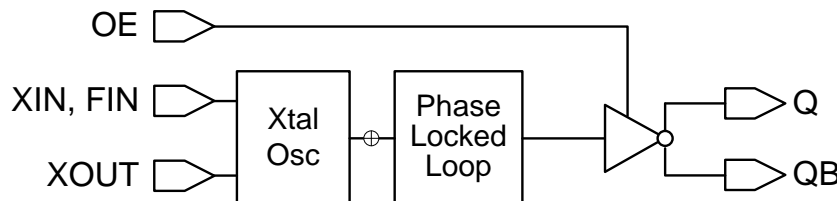
PIN CONFIGURATION



DESCRIPTION

The PL602-XX is the smallest, high performance, lowest power differential output clock IC available for HCSL timing applications. PL602-XX offers -130dBc at 10kHz offset at 100MHz, with a very low jitter (2 ps TIE RMS), making it ideal for HCSL applications requiring small size and low power.

BLOCK DIAGRAM



PIN DESCRIPTION

Name	Pin #		Type	Description
	SOP	SOT23		
XIN	1	-	I	Crystal input (SOP package only)
FIN	-	3	I	Reference clock input (SOT23 package only)
GND	2	2	P	GND connection
CLK[0:1]	3,4	1,6	O	Differential clock outputs [note:CLK0=~CLK1]
VDD	5	5	P	VDD connection
DNC	6	-	-	Do not connect
OE	7	4	I	Output enable (OE) input. Internal 60KΩ pull up resistor.
XOUT	8	-	O	Crystal output pin.

HCSL Compatible Clock Generator for PCI Express
ELECTRICAL SPECIFICATIONS
ABSOLUTE MAXIMUM RATINGS

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage Range	V_{DD}	-0.5	4.6	V
Input Voltage Range	V_I	-0.5	$V_{DD}+0.5$	V
Output Voltage Range	V_O	-0.5	$V_{DD}+0.5$	V
Soldering Temperature			260	°C
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*		-40	+85	°C

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied. *Operating temperature is guaranteed by design. Parts are tested to commercial grade only.

AC SPECIFICATIONS

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Input Frequency	Fundamental Crystal		25		MHz
Input (F_{IN}) Frequency			25		MHz
Input (F_{IN}) Signal Amplitude	Internally AC coupled	0.9		V_{DD}	Vpp
Output Frequency		25		200	MHz
Output Enable Time	OE Function; $T_a=25^\circ\text{C}$, Add one clock period to this measurement for a usable clock output.			10	ns
Output Disable Time	OE Function; $T_a=25^\circ\text{C}$			10	ns
Settling Time	At power-up ($V_{DD} \geq 2.25\text{V}$)			10	ms
VDD Sensitivity	Frequency vs. V_{DD} , $\pm 10\%$	-2		2	ppm
Output Rise Time	10/90% V_{OH}		0.3	0.5	ns
Output Fall Time	90/10% V_{OH}		0.3	0.5	ns
Skew Between Outputs	Measured at 50% V_{OH}			250	ps
Duty Cycle	At $V_{DD}/2$	45	50	55	%
Period Jitter, peak-to-peak	- With capacitive decoupling between V_{DD} and GND - At 100MHz - 20,000 samples measured		28		ps
Cycle-to-Cycle, RMS			9		ps
Cycle-to-Cycle, peak			25		ps
TIE, RMS			2		ps

HCSL Compatible Clock Generator for PCI Express
DC SPECIFICATIONS

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current, Dynamic	I_{DD}	At 100MHz, No Load		25		mA
Operating Voltage	V_{DD}		2.25		3.63	V
Output Low Voltage	V_{OL}	HCSL termination, (RS = 150Ω, RT = 49.9Ω) 3.3V (RS = 100Ω, RT = 49.9Ω) 2.5V			0.05	V
Output High Voltage	V_{OH}		0.65	0.75	0.85	V
Output Current	I_{OSD}		13	15	17	mA

CRYSTAL SPECIFICATIONS

PARAMETERS	SYMBOL	MIN.	TYP.	MAX.	UNITS
Fundamental Crystal Resonator Frequency	F_{XIN}		25		MHz
Crystal Loading Rating	$C_{L(xtal)}$		18		pF
Maximum Sustainable Drive Level				500	μW
Operating Drive Level			100		μW
Crystal Shunt Capacitance	C_0			6	pF
Effective Series Resistance, Fundamental	ESR			45	Ω

HCSL Compatible Clock Generator for PCI Express

PCI EXPRESS/HCSL COMPATIBLE LAYOUT GUIDELINES

Figure 1 below describes how to terminate the complementary LVCMOS outputs of PL602-XX for use with HCSL inputs.

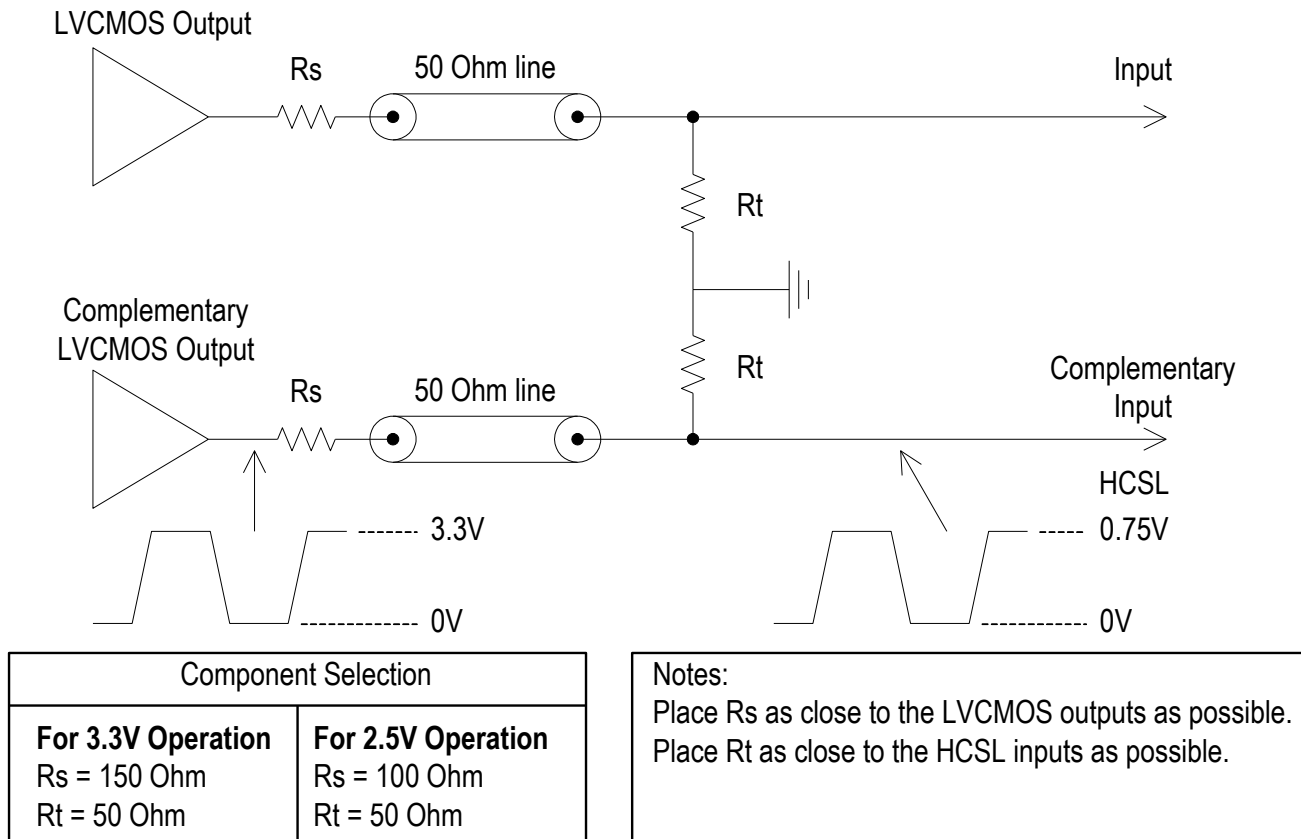


Figure 1

PCB LAYOUT CONSIDERATIONS FOR PERFORMANCE OPTIMIZATION

The following guidelines are to assist you with a performance optimized PCB design:

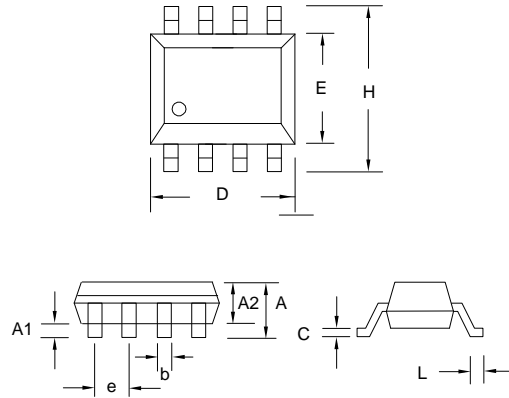
- Keep all the PCB traces to PL602-XX as short as possible, as well as keeping all other traces as far away from it as possible.
- Place the crystal as close as possible to both crystal pins of the device. This will reduce the cross-talk between the crystal and the other signals.
- Separate crystal pin traces from the other signals on the PCB, but allow ample distance between the two crystal pin traces.
- Place a 0.01μF~0.1μF decoupling capacitor between VDD and GND, on the component side of the PCB, close to the VDD pin. It is not recommended to place this component on the backside of the PCB.
- It is highly recommended to keep the VDD and GND traces as short as possible.
- When connecting long traces (> 1 inch) to a CMOS output, it is important to design the traces as a transmission line or 'stripline', to avoid reflections or ringing. In this case, the CMOS output needs to be matched to the trace impedance. Usually 'striplines' are designed for 50Ω impedance and CMOS outputs usually have lower than 50Ω impedance so matching can be achieved by adding a resistor in series with the CMOS output pin to the 'stripline' trace.

HCSL Compatible Clock Generator for PCI Express

PACKAGE DRAWINGS (GREEN PACKAGE COMPLIANT)

SOP-8L

Symbol	Dimension in MM	
	Min.	Max.
A	1.35	1.75
A1	0.10	0.25
A2	1.25	1.50
B	0.33	0.53
C	0.19	0.27
D	4.80	5.00
E	3.80	4.00
H	5.80	6.20
L	0.40	0.89
e	1.27 BSC	



SOT23-6L

Symbol	Dimension in MM	
	Min.	Max.
A	1.05	1.35
A1	0.05	0.15
A2	1.00	1.20
B	0.30	0.50
C	0.08	0.20
D	2.80	3.00
E	1.50	1.70
H	2.60	3.0
L	0.35	0.55
e	0.95 BSC	

