PM5426 HyPHY-10G

Optical Access Multi-Rate/Multi-Protocol OTN Processor

Summary

The PM5426 HyPHY-10G device is a feature-rich, system-on-a-chip solution optimized to enable a new generation of Compact Optical Access platforms for the network edge. HyPHY-10G addresses multi-service transponder and muxponder applications for Multi-Service Provisioning Platform (MSPPs), Wavelength Division Multiplexing (WDM) Platforms, Reconfigurable Optical Add-Drop Multiplexers (ROADMs), Optical Transport Platforms (OTPs), Packet-OTPs and Optical Access Platforms.

The HyPHY-10G delivers single-chip scalability and feature integration to enable optimal footprint, power and cost efficiency. The HyPHY-10G provides a rich set of framing, mapping and multi-plexing resources for a variety of protocols, including OTN, SONET/SDH, Ethernet, Fibre Channel, ESCON, FICON and multi-rate bit transparent services such as video.

The HyPHY-10G Supports an Array of Innovative Technologies

- Rate-Agile Programmable Transceiver IO (RAPTR IO): Gapless rate-agile SERDES from 16 Mbits to 5 Gbit/s for direct connect to SFPs and from 8.5 Gbit/s to 11.32 Gbit/s for direct connect to SFP+ (limiting) and XFP modules
- Tri-FEC: Interoperable ITU-T G.709 and G.975.1 (I.4 and I.7) FEC
- OTN Phase Signaling Algorithm (OPSA): Improve jitter performance when transporting clients over OTN
- OTN Payload Tributary Mapping (OPTM): Low-order mapping into OPU1
- Constant Bit Rate Interface (CBRI): Carry ODUks across system Fabrics

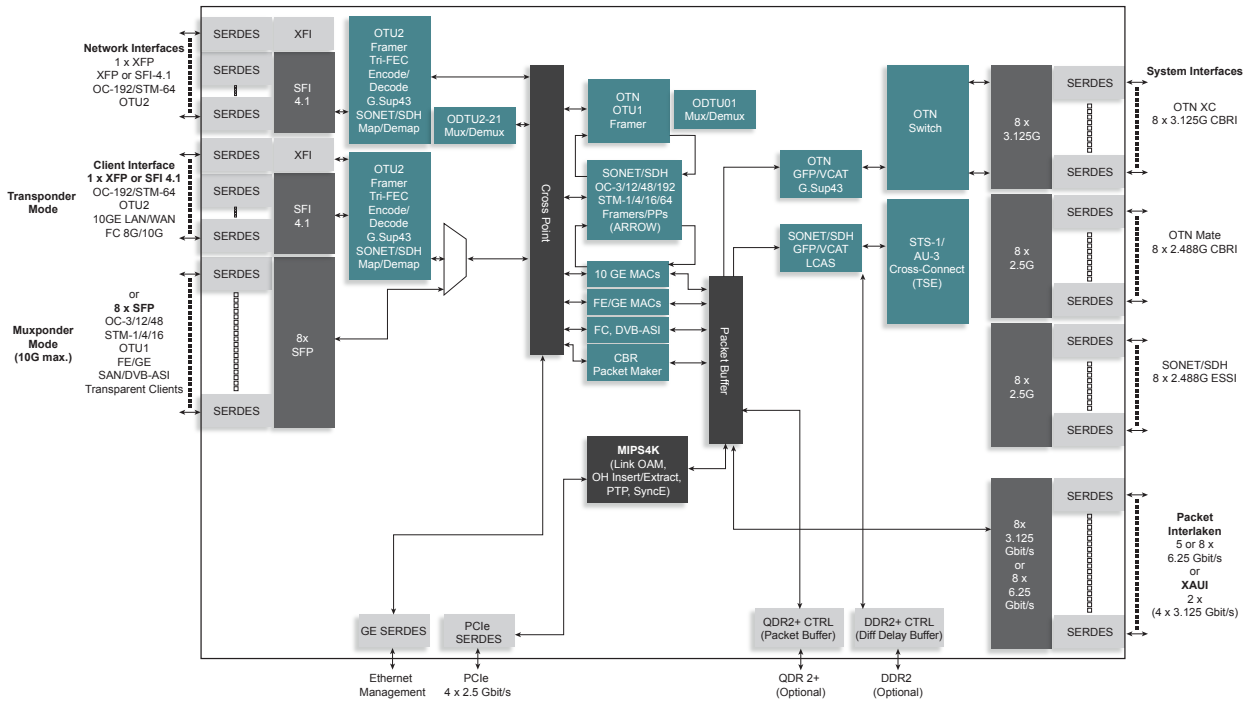
Benefits

- Carrier OPEX and CAPEX savings
  - Cost effectively delivers Ethernet, SAN and SONET/SDH services to customer premises
- Unprecedented service delivery flexibility
  - Supports per-port configurable OTN, SONET/SDH, Ethernet, SAN and bit transparent client services
  - Rich suite of client service mappings into OTN and SONET/SDH
  - OTN Tri-FEC for maximum network interoperability
- Processor-based Carrier Ethernet
  - Flexible implementations of Synchronous Ethernet, IEEE 1588 Precision Timing Protocol (PTP) and Ethernet Link OAM Optimized power and footprint for compact chassis designs
  - Direct connect to SFP, SFP+ (limiting), and XFP modules for all rates with no external SERDES or PLL components required
  - All frequencies derived from a single 155.52 MHz reference clock
  - Single-chip solution for muxponders, transponders and optical access platforms
  - Glueless interconnect to many off-the-shelf NPs and fabrics

The HyPHY-10G Supports Two Operational Modes:

- **Transponder Mode:** Maps a 10G client to OTU2, OC-192/STM-64 network or system interfaces
- **Muxponder Mode:** Maps SFP clients to OTU2 or OC-192/STM-64 network or system interfaces

Block Diagram



Product Highlights

10G Network Interface

- 1x multi-rate SERDES for direct connection to XFP/SFP+ modules, independently tunable from 8.5 Gbit/s to 11.32 Gbit/s or 1x SFI 4.1 interface for chip-to-chip interconnect or for direct connection to MSA modules
- Support for one of the following services
  - OTU2 (including overclocked rates up to 11.32 Gbit/s)
  - OC-192/STM-64

10G Client Interface (Transponder Mode)

- 1x multi-rate SERDES for direct connection to XFP/SFP+ modules, independently tunable from 8.5 Gbit/s to 11.32 Gbit/s or 1x SFI 4.1 interface for chip-to-chip interconnect or for direct connection to MSA modules
- Support for one of the following services
  - OTU2 (including overclocked rates up to 11.32 Gbit/s)
  - OC-192/STM-64
  - 10GE-LAN
  - 10GE-WAN
  - FC-800 / FC-1200
  - CPRI 9.8304 Gbit/s

SONET/SDH Subsystem (ARROW + TSE)

- Integration of field-proven CHESS SONET/SDH IP, reducing development cycles through reuse of CHESS software base
- SONET/SDH framing, high-order pointer processing and overhead processing
- Tandem connection monitoring
- Transport overhead transparency
- BLSR and MSSPRing protection switching with alarm processing, K-byte express, automatic payload configuration and other protection features
- Non-blocking 50 Gbit/s STS-1/AU-3 cross-connect
- 20 Gbit/s of delay management to adapt between frame alignment domains
- TOH byte insertion and extraction
- Active and standby configuration memory page support permits new switch settings to be updated in one page while the TSE operates from the control settings of the other page

Fibre Channel Subsystem

- FICON, ESCON, and Fibre Channel rates of FC-12, 25, 50, 100, 200, 400 and 800
- 8B/10B physical coding sub-layer (PCS) on a per-link basis with loss of signal and transmission error monitoring performance
- Per-link rate adaptation to bridge between local and transmit link timing domains
- FC-1200 as a transparent client support

Ethernet Subsystem

- Integrated IEEE 802.3 compliant Media Access Controllers (MAC)
- Integrated 10 GE WAN Interface Sublayer (WIS) framing and descrambling
- 4B/5B, 8B/10B and 64B/66B Physical Coding Sub-layer (PCS) on a per-link basis for FE, GE and 10 GE respectively
- Lossless IEEE 802.3 local flow-control with integrated packet buffers
- Comprehensive per-port Ethernet statistics
- Frame delineation and generation with configurable IPG, Preamble and CRC
- Transparent transmission of VLAN tagged Ethernet frames
- Frame sizes of 64 bytes to 9.6 Kbytes
- Dynamic programmable depth full-packet store-and-forward buffers for burst tolerance and rate adaptation
- Transmit and receive of IEEE 802.3ah Link OAM, LACP and Management VLAN messages
- Firmware-based (MIPS4K CPU), hardware assisted G.8261 Synchronous Ethernet and IEEE 1588v2 PTP Ethernet timing
- On-chip central packet buffer

OTN Subsystem

- Compatible with ITU-T G.709, ITU-T G.798 and ITU-T G.975
- Flexible OTU, ODU, and OPU overhead/data processing and frame alignment
- Transmit and receive facility and terminal loopback configurations
- ODTU12 multiplexing and de-multiplexing for an ODU2 stream
- Up to six levels of Tandem Connection Monitoring (TCM)
- Independent performance counters for the accumulation of BIP-8, BEI and other error conditions with optional interrupts
- O-E-O regeneration with adaptive clocking using Microchip's OTN Phase Signaling Algorithm (OPSA)

Forward Error Correction (FEC)

- Two instantiations of independently-configurable Tri-FEC for OTU2
  - Interoperable G.709 RS (255, 239) FEC with 6.2 dB coding gain at 10^{-15} BERout
  - Interoperable G.975.1 Annex I.4 Strong FEC (8.9 db gain at BERout = 10^{-15}@ 7% OH)
  - Interoperable G.975.1 Annex I.7 Strong FEC (8.4 db gain at BERout = 10^{-15} @ 7% OH)

Comprehensive statistics for use in EDC tuning, limited amplifier tuning and performance monitoring

Client Mapping into OTN and SONET/SDH

- Maps a wide variety of protocols over OTN and SONET/SDH
- Encapsulates packet streams into ITU-T G.7041 GFP-F and GFP-T, HDLC, LAPS and PPP
- Inserts and extracts GFP client management frames (CMF) as well as LCP, NCP and BCP control frames
- OTN client mapping
  - Synchronous and asynchronous CBR mapping per G.709
  - High-order (ODU-1) virtual and contiguous concatenation performed according to G.709 with LCAS support
  - OPTM for efficient mapping/multiplexing of wander-sensitive sub-ODU1 client data into OTN
  - GFP with extension headers for multiplexing of sub-ODU1 client data streams into ODU-ks or OPTM tributary slots
  - OPSA for rate encoding and adaptation of transparent client data streams over OTN
  - 10GE mapping into OTN compliant with ITU G.Sup43 6.1, 6.2, 7.1, 7.2 and 7.3 (FC-1200 also where applicable)
  - SONET/SDH client mapping:
  - High-order (STS-1-Xv/VC-3-xv & STS-3c-Xv/VC-4-Xv) virtual and contiguous concatenation performed according to ITU-T G.707 and ANSI T1.105
  - Up to 64 SONET/SDH virtual concatenation groups (VCGs) supported
  - Hitless Link Capacity Adjustment Scheme (LCAS) according to ITU-T G.7042
  - Up to 128 ms of differential delay between VCG members

System Expansion Interfaces

- SONET/SDH:
- 8 x 2.488 Gbit/s ESSI serial links with delay management supporting slicing and de-slicing for byte, nibble, dibit, and bit modes
- OTN
  - 8 x 2.488 Gbit/s CBRI serial links to mate device
  - 8 x 3.125 Gbit/s CBRI serial links to OTN cross-connect
  - Enables grooming of ODUk using an off-the-shelf packet fabric
- Packet traffic
  - 1 Interlaken v1.1 interface configurable to 5 or 8 lanes at 6.25 Gbit/s
  - 2 x XAUI interfaces (2 x 4 lanes at 3.125 GHz), extended XAUI mode can add format and flow-control channelization extensions to 802.3ae