PM5451 HyPHY-AXS

Multi-Service OTN Access Muxponder/Add-Drop Multiplexer

Summary

The PM5451 HyPHY-AXS is an OTN access platform on a chip that enables a new class of compact transport solutions for the Metro Access network. It is optimized for the backhaul of xPON OLTs, 3G/LTE mobile base stations and Enterprise Ethernet services over a unified Metro OTN infrastructure. By integrating multi-rate, multi-protocol client interfaces, Ethernet MACs with onboard support for PTP/SyncE and OTN framing, mapping and multiplexing, the HyPHY-AXS enables compact metro access platforms with the highest level of feature-integration at an optimal footprint, power and Bills-of-Material (BOM) cost.

The HyPHY-AXS supports a rich set of OTN framing, mapping and multiplexing resources for a variety of client protocols, including OTN, SONET/SDH, Ethernet, Fibre Channel, ESCON, FICON and multi-rate bit transparent services such as video. It provides a simple path towards extending designs to enable support for higher client port densities and fabric-connected applications using the PM5450 HyPHY 20Gflex OTN processor.

Optimal Features for Metro Access/ Aggregation Applications

- Support for ODU0/ODUflex
- Support for Tri-FEC
- G.709 compliant GMP multiplexing
- Add-drop ODUk capabilities from OTU2 ring
- PTP over OTN support
- SyncE and 1588v2 support

Product Highlights

SFP Client Interfaces

- 8x multi-rate SERDES for direct connection to SFP optical transceivers, independently tunable from 16 Mbit/s to 5 Gbit/s
- Any-Service Any-Port configurable:
  - OTU1
  - OC-3/12/48 or STM-1/4/16
  - 100/1000 Mbps full-duplex Ethernet
  - Bit transparent clients, including, but not limited to, DVB-ASI, SD-SDI, HD-SDI, DV6000, ISC, ISCIII and 2.5G/5G Infiniband
  - Fibre Channel FC-15, FC-25, FC-50, FC-100, FC-200, FC-400, FICON and ESCON
  - CPRI clients up to 4.9 Gbit/s

OTU2 Line Interfaces

- Dual integrated SERDES for direct connection to XFP modules

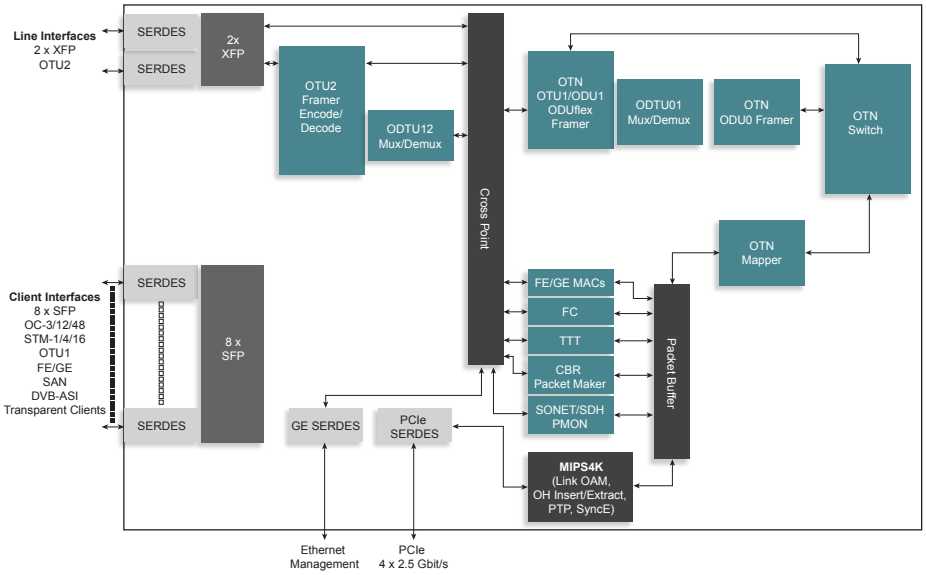
Fibre Channel Subsystem

- FICON, ESCON and Fibre Channel (FC-12, 25, 50, 100, 200, 400)
- Performs 8B/10B Physical Coding Sub-layer (PCS) on a per-link basis with loss of signal and transmission error monitoring
- Per-link rate adaptation to bridge between local and transmit link timing domains

Ethernet Subsystem

- Integrated IEEE 802.3 compliant Media Access Controllers (MAC)
- 4B/5B and 8B/10B physical coding sub-layer (PCS) on a per-link basis for FE and GE, respectively
- Lossless IEEE 802.3 local flow control; integrated packet buffers
- Comprehensive per-port Ethernet statistics
- Frame delineation and generation with configurable IPG, Preamble and CRC
- Transparent transmission of VLAN tagged Ethernet frames
- Frame sizes of 64 bytes to 9.6 Kbytes
- Dynamic programmable depth full-packet store-and-forward buffers for burst tolerance and rate adaptation

Block Diagram



Benefits

- Unprecedented flexibility of service delivery:
  - Supports per-port configurable OTN, SONET/SDH, Ethernet, SAN and bit transparent client services
  - Rich suite of client service mappings into OTN
  - Enables full SNCP-based protection switching for meshed network topologies
- Processor-based Carrier Ethernet:
  - Flexible implementation of Synchronous Ethernet, IEEE 1588 Precision Timing Protocol (PTP), and Ethernet Link OAM (IEEE 802.3ah)
- Optimized power and footprint for OEMs:
  - Direct connect to SFP and XFP modules for all rates with no external SERDES or PLL components required
  - All frequencies derived from a single 155.52 MHz reference clock
  - Single-chip solution for muxponders, ADMs, and optical access platforms
- OTN support in the Metro Access Network:
  - Enables greater reach through FEC and reduces the need for regeneration, resulting in Capex savings
  - Provides better management through a superior OAM framework
  - Leads to Opex savings in comparison to a L2-based solution
  - Transmit and receive of IEEE 802.3ah Link OAM, LACP and Management VLAN messages
  - Firmware-based (MIPS4K CPU), hardware assisted G.8261 Synchronous Ethernet and IEEE 1588v2 PTP Ethernet timing
  - On-chip central packet buffer

OTN Subsystem

- Compatible with ITU-T G.709, ITU-T G.798 and ITU-T G.975
- Supports ODU0 and ODUflex
- Flexible OTU, ODU and OPU overhead/data processing and frame alignment
- Transmit and receive facility and terminal loop back configurations
- One-stage or two-stage ODU multiplexing
- Support for GMP multiplexing
- Support for Tandem Connection Monitoring (TCM)
- O-E-O regeneration with adaptive clocking using Microchip's OTN Phase Signaling Algorithm (OPSA)

Forward Error Correction (FEC)

- Two instantiations of independently-configurable Tri-FEC for OTU2:
  - Interoperable G.709 RS (255, 239) FEC with 6.2 dB coding gain at 10- 15 BERout
  - Interoperable G.975.1 Annex I.4 Strong FEC (8.9 db gain at BERout = 10-15 @ 7% OH)
  - Interoperable G.975.1 Annex I.7 Strong FEC (8.4 db gain at BERout = 10-15 @ 7% OH)