Aries Smart Retimers for PCI-Express 4.0 and 5.0

1 Benefits and Features

- Compatible With PCIe 5.0 and 4.0 Technology
- Supports up to 32 Bi-Directional Lanes: 16 upstream Lanes and 16 Downstream Lanes
- Flexible Link Bifurcation Including 1x16, 2x8, 4x4, and More
- Advanced, Fully Adaptive on-chip Signal Conditioning extends PCIe Signal Reach, Enables Low-Cost PCB Materials
- BGA Package Footprint Optimized for Board Routing
- Supports SRIS, SRNS, and Common Clock Systems
- Low-Power Advanced CMOS Process
- Advanced In-Band and Out-of-Band Diagnostics for Fleet Management
- Device Configuration through SMBus or EEPROM
- IEEE 1149.6 AC-JTAG Boundary Scan
- Portfolio of Pin- and Register-Compatible Retimers Enables Easy Performance Scaling

2 Applications

- Server and High-Performance PC Motherboards
- PCIe Riser and Add-in Cards
- Server-to-Server Cabled Interfaces
- NVMe JBOFs, GPU/Deep-Learning Accelerators

Aries Smart Retimer Portfolio

Part Number	PCIe Gen	Package	Body Size (Nom)
PT516xx	Gen-5, x16	FC-CSP (354)	8.9 mm x 22.8 mm
PT416xx	Gen-4, x16	FC-CSP (354)	8.9 mm x 22.8 mm
PT508xx	Gen-5, x8	FC-CSP (332)	8.5 mm x 13.4 mm
PT408xx	Gen-4, x8	FC-CSP (332)	8.5 mm x 13.4 mm

3 Description

The Aries Smart Retimer is designed to easily eliminate signal integrity issues for PCI-Express (PCIe) 4.0 and 5.0 interconnects in data-centric applications. Aries is a protocol-aware low-latency Retimer platform designed to integrate seamlessly between a Root Complex and End Point(s) to extend PCIe signal reach. Compliant to all PCIe rates and Retimer functional requirements, the Aries Smart Retimer platform enables more system topologies and lower total solution cost while minimizing implementation overhead and Bill of Materials (BoM).

The innovative low-latency architecture of Aries significantly reduces latency through the Retimer while being transparent to system software and participating in Link Equalization with the Root Complex and End Point(s) to optimize Link performance. To enable a wide variety of End Points and port configurations, Aries supports a wide variety of bifurcation configurations: 1x16, 2x8, 4x4, and more. Each bifurcated Link operates independently, and diagnostics information such as Link status and Lane margin are accessible through in-band (Receiver margining) and out-of-band (SMBus) mechanisms on a per-Link basis.

The pinouts for the Aries portfolio are based on the industry standard Retimer Supplemental Specification. Each pinout allows for separate single-layer routing for all high-speed transmit and receive signals. The Gen-4 and Gen-5 versions of Aries are pin-compatible, allowing system designers to future-proof their systems, delivering a reach extension solution that can easily and quickly scale from PCIe 4.0 to PCIe 5.0.

Typical Application Block Diagram