PTN3816

DisplayPort 20Gbps 4-lane linear redriver

Rev. 1.0 — 7 June 2021 Product data sheet

1 General description

PTN3816 is a high performance 20 Gbps per lane, 4-lane DisplayPort linear redriver for DisplayPort upstream (DP source side) and downstream (DP Sink side) applications. It is used to improve high speed signal quality in DisplayPort interfaces in various platforms and applications.

The device provides pin programmable receive equalization, output linearity control to improve signal integrity and enable channel extension by reducing Inter-Symbol Interference (ISI). This IC also implements AUX snooping to monitor the AUX signals to optimally configure the link and achieve power saving and SI performance.

PTN3816 has control pins for application specific configurability. These pins can either be strapped appropriately on the PCB or connected to a microcontroller's GPIO pins. PTN3816 does not require any I2C software configuration.

PTN3816 is powered from 1.8 V supply. It is available in a small high performance HWFLGA36 package with 2.1 mm x 6.0 mm x 0.6 mm size and 0.4 mm pitch.

2 Features and benefits

- Implements DisplayPort linear redriver that can operate for various link rates - 1.62 Gbps (RBR), 2.7 Gbps (HBR), 5.4 Gbps (HBR2) 8.1 Gbps (HBR3), 10, 13.5 and 20 Gbps
  - Supports configurable number of lanes: 1, 2 and 4
  - DP AUX monitoring for link configuration and power management
  - Implements HPD for deep power saving
  - Configurable Rx Equalizer gain
  - Configurable output swing linearity control
- High Speed redriver path supports DP++ mode that targets DP to HDMI interface use
- Supports maximum voltage limit ($V_{voltage\_jump}$) to align to the latest system platform capabilities
- Integrated termination resistors provide impedance matching on transmit and receive sides
- Good linearity over the frequency band (50 MHz to 10.3 GHz) and voltage dynamic range
- Excellent Differential return loss performance: < -16 dB up to 10.3 GHz
- Flow-through pin-out to ease PCB layout and minimize crosstalk effects
- Low active current consumption for output linearity control setting of 950 mVppd
  - 1-lane DP : 62 mA (typ)
  - 2-lane DP : 125 mA (typ)
  - 4-lane DP : 250 mA (typ)

- Power–saving state:
  - DisplayPort sleep D3 mode: 3.2 mA (typ)
  - 10 µA (typ) when in deep power-saving state (when HPD is LOW)
- Configurable via GPIO control pins
- Power Supply 1.7 V to 1.9 V
- Small high performance HWFLGA36 package
  - 2.1 mm x 6.0 mm x 0.6 mm with 0.4 mm pitch
  - ESD HBM 1.5 kV CDM 1 kV
- Operating temperature range -20 °C to +85 °C

3 Applications

- DisplayPort source applications
  - Smartphones and tablets
  - Notebooks, AIO and desktop computers
  - Hub or dock devices
- DisplayPort sink applications
  - Docking stations
  - Display units

4 Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
PTN3816EW	16	HWFLGA36	plastic thermal enhanced very very thin fine-pitch land grid array package	SOT1948-1

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PTN3816EW	PTN3816EWY	HWFLGA36	reel dry pack, SMD, 13" Q1	7000	T_{amb} = -20 °C to 85 °C

5 Functional diagram

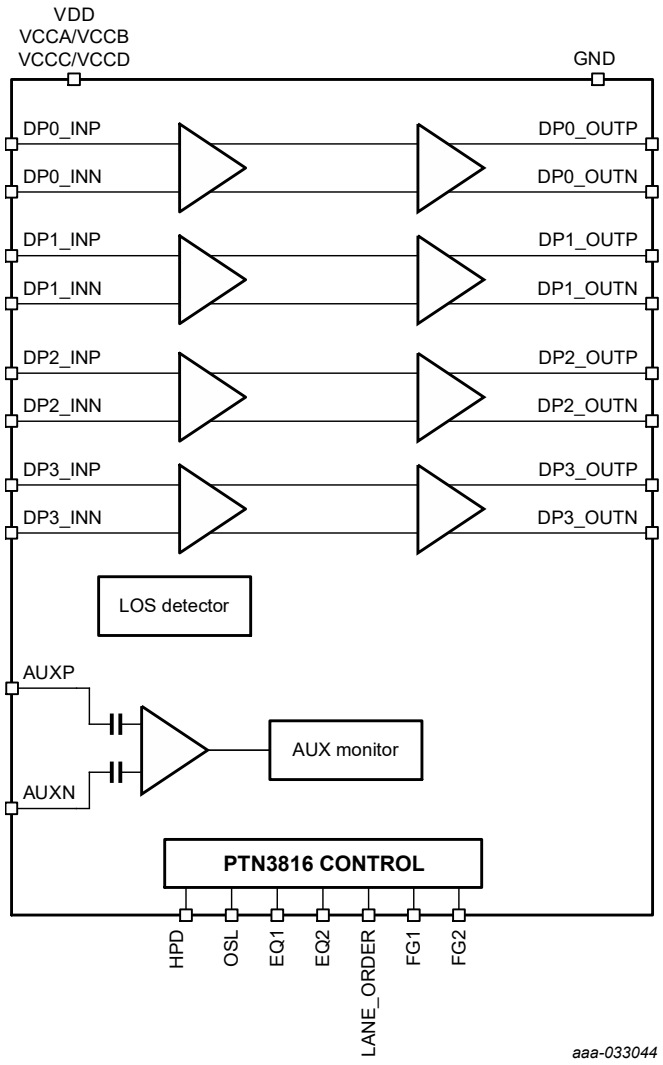


Figure 1. PTN3816 functional diagram

6 Pinning information

6.1 Pinning

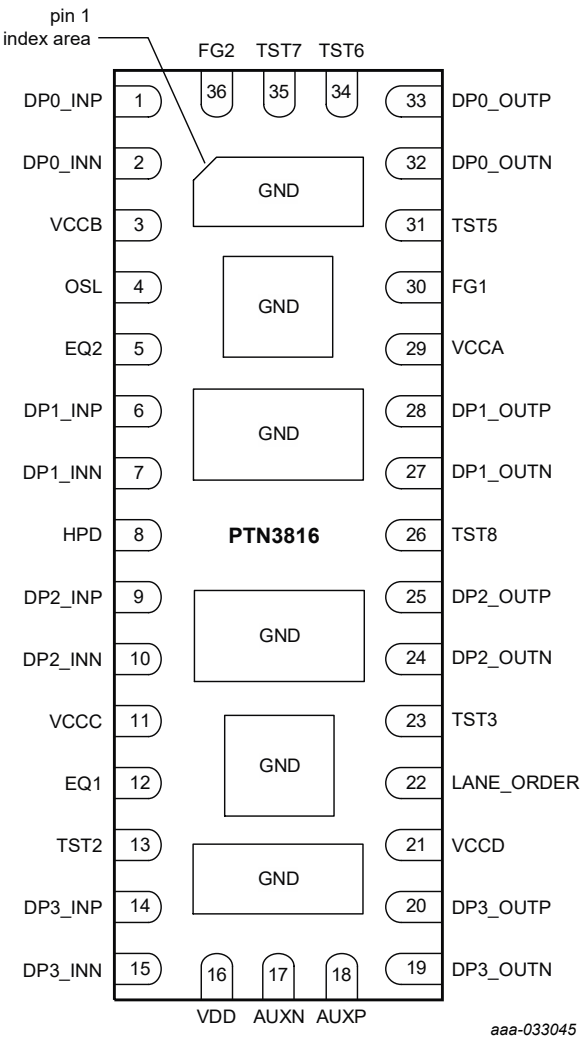


Figure 2. PTN3816 pinning (transparent top view)

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
1	DP0_INP	Self-biasing differential input/ output	Differential signal high-speed Rx input. DP0_ INP makes a differential pair with DP0_INN. The associated output pair is DP0_OUTP and DP0_ OUTN
2	DP0_INN		

Table 3. Pin description...*continued*

Symbol	Pin	Type	Description
29	VCCA	Power pins for high-speed paths	These dedicated power pins for high-speed differential pairs provide good signal integrity and noise isolation.
3	VCCB		
11	VCCC		
21	VCCD		
4	OSL	Ternary control input	Ternary input for controlling output swing linearity (-1 dB compression point) of the line driver. Please refer to Section 7.3 for details.
12	EQ1	Ternary control inputs	EQ1 and EQ2 are Receive equalization peaking gain setting pins of the chip. Please refer to Section 7.3 for details.
5	EQ2		
6	DP1_INP	Self-biasing differential input	Differential signal from high-speed RX path. DP1_INP makes a differential pair with DP1_INN. The associated TX output pair is DP1_OUTP and DP1_OUTN
7	DP1_INN		
8	HPD	CMOS control input	This pin is connected to Hot Plug Detect signal of DisplayPort interface and it controls whether the IC is in Deep power saving mode or otherwise
9	DP2_INP	Self-biasing differential input	Differential signal from high-speed RX path. DP2_INP makes a differential pair with DP2_INN. The associated output pair is DP2_OUTP and DP2_OUTN
10	DP2_INN		
13	TST2	Reserved Test pin	This pin is connected to GND in the application
14	DP3_INP	Self-biasing differential input/ output	Differential signal high-speed Rx input. DP3_INP makes a differential pair with DP3_INN. The associated output pair is DP3_OUTP and DP3_OUTN
15	DP3_INN		
16	VDD	Power	1.8 V Supply for AUX snooping and digital blocks
17	AUXN	Input	AUX channel snooping input
18	AUXP		
19	DP3_OUTN	Self-biasing differential input/ output	Differential signal high-speed Rx input. DP3_OUTP makes a differential pair with DP3_OUTN. The associated output pair is DP3_INP and DP3_INN
20	DP3_OUTP		
22	LANE_ORDER	CMOS control Input	This pin is used to control DP lane order control – DP0/1/2/3 or DP3/2/1/0. Refer to Table 7 for more details
23	TST3	Reserved Test pin	This pin is connected to GND in the application
24	DP2_OUTN	Self-biasing differential output	Differential signal high-speed output. DP2_OUTP makes a differential pair with DP2_OUTN. The associated input pair is DP2_INP and DP2_INN.
25	DP2_OUTP		
26	TST8	Reserved Test pin	Reserved for test purpose only. Must be connected to GND in the system application
27	DP1_OUTN	Self-biasing differential output	Differential signal high-speed output. DP1_OUTP makes a differential pair with DP1_OUTN. The associated input pair is DP1_INP and DP1_INN.
28	DP1_OUTP		

Table 3. Pin description...*continued*

Symbol	Pin	Type	Description
30	FG1	Ternary control input	Ternary input for controlling flat gain setting of the output driver. Please refer to Section 7.3 for details.
31	TST5	Reserved Test pin	Reserved for test purpose only. Must be connected to GND in the system application
32	DP0_OUTN	Self-biasing differential output	Differential signal high-speed output. DP0_OUTP makes a differential pair with DP0_OUTN. The associated input pair is DP0_INP and DP0_INN.
33	DP0_OUTP		
34	TST6	Reserved Test pins	This pin is connected to GND in the application
35	TST7		
36	FG2	Ternary control input	Ternary input for controlling flat gain setting of the output driver. Please refer to Section 7.3 for details.
Center pads	GND		These six center pads must be connected to GND plane for both electrical grounding and thermal relief

7 Functional description

7.1 DisplayPort operation

PTN3816 implements signal equalization to compensate for channel ISI loss and it supports DP operation at 1.62 Gbps, 2.7 Gbps, 5.4 Gbps, 8.1 Gbps, 10 Gbps, 13.5 Gbps and 20 Gbps. It provides configurability for receive equalization and output swing linearity control (EQ1, EQ2, OSL, FG1, FG2). It also performs AUX monitoring and decodes select AUX commands. It detects HPD level and determine whether to enter or exit Deep power saving state.

The DP lane count is configured during link training phase based on AUX communication exchanges between DP source and DP sink. PTN3816 uses lane count for configuring its high-speed lanes. It is possible that only a subset of lanes gets selected during DP Link training and the remaining lanes are not active. Depending on the number of lanes selected, PTN3816 is configured to operate with the selected lane count thereby saving power consumption on unused lanes.

The DP source can activate power down via AUX command. DP spec supports two modes – D0 or D3/Low power mode. In D0 mode, the linear redriver data path is active depending on the state of the DP link. In D3 mode, the AUX snooping logic is active while high-speed path is disabled resulting in lower current consumption.

7.2 AUX monitoring and configuration

PTN3816 monitors DP AUX communication exchanges that occur between DP source and DP sink. It detects AUX communication involving DPCD register controls – count, sleep, wake and configures its operation suitably.

The list of DPCD registers (with only the relevant bit fields) supported are as follows:

- LANE_COUNT_SET
- SET POWER
- Other DPCD registers and I^2C over AUX transactions are not decoded

When the Lane count is being initialized via AUX command, the acceptable values are 1, 2, and 4. If AUX command tries to set it to 0, PTN3816 ignores it, and continues with the last known legal value.

7.3 Redriver control and programmability

PTN3816 allows for programming of linear redriver functions – receive equalizer and output swing linearity as shown in Table 4, Table 5 and Table 6 below. In addition, LANE_ORDER is used to inform the PTN3816 to consider specific lane ordering on its high-speed input and output. It is necessary for the redriver to know the lane ordering given that AUX monitor configures the lanes based on lane-count selection. Table 7 and Table 8 capture HPD control and Lane ordering scheme implemented in PTN3816.

Table 4. EQ[2:1] configuration: Flat gain 0.7 dB

Peaking Gain is the equalization gain at specific frequency relative to gain at 100 MHz and for typical Flat Gain (FG) value of 0.7 dB

EQ2	EQ1	Unit	Gain at 100 MHz	0.81 GHz	1.35 GHz	2.7 GHz	4.05 GHz	6.75 GHz	8 GHz	10 GHz
LOW	OPEN	dB	0.5	-0.2	-0.4	-0.1	0.1	1.0	1.6	2.0
OPEN	LOW	dB	0.5	-0.1	-0.3	0.1	0.4	1.5	2.3	2.8
HIGH	HIGH	dB	0.5	0.1	0.0	0.7	1.3	3.0	4.1	5.4
HIGH	OPEN	dB	0.5	0.6	0.5	1.6	2.6	5.1	6.6	8.4
HIGH	LOW	dB	0.6	1.1	1.3	2.8	4.2	7.5	9.3	11.6
OPEN	HIGH	dB	0.6	1.7	2.0	4.0	5.7	9.7	11.7	14.2
LOW	HIGH	dB	0.6	2.4	2.8	5.3	7.4	11.9	14.2	16.8
OPEN	OPEN	dB	0.7	2.9	3.7	6.2	8.6	13.6	15.9	18.4
LOW	LOW	dB	0.7	2.9	3.7	6.2	8.6	13.6	16.0	18.4

Table 5. EQ[2:1] configuration: Flat gain -0.7 dB

Peaking Gain is the equalization gain at specific frequency relative to gain at 100 MHz and for typical Flat Gain (FG) value of -0.7 dB

EQ2	EQ1	Unit	Gain at 100 MHz	0.81 GHz	1.35 GHz	2.7 GHz	4.05 GHz	6.75 GHz	8 GHz	10 GHz
LOW	OPEN	dB	-1.1	-0.1	-0.2	0.6	1.3	2.6	3.4	3.8
OPEN	LOW	dB	-1.1	0.0	-0.1	0.8	1.6	3.1	4.0	4.6
HIGH	HIGH	dB	-1.1	0.3	0.2	1.6	2.6	4.7	5.9	7.2
HIGH	OPEN	dB	-1.1	0.9	1.0	2.7	4.0	6.9	8.4	10.2
HIGH	LOW	dB	-1.0	1.6	2.0	4.0	5.8	9.3	11.1	13.3
OPEN	HIGH	dB	-1.0	2.3	2.8	5.3	7.4	11.4	13.4	15.9
LOW	HIGH	dB	-1.0	3.1	3.8	6.7	9.1	13.6	15.8	18.4
OPEN	OPEN	dB	-0.9	3.7	4.7	7.7	10.2	15.2	17.5	20
LOW	LOW	dB	-0.9	3.7	4.7	7.7	10.2	15.2	17.6	20

Table 6. OSL configuration

OSL	Line driver output swing linearity (OSL) governing -1 dB compression level
OPEN	650 mVppd
LOW	800 mVppd
HIGH	950 mVppd

Table 7. Lane ordering configuration

LANE_ORDER	PTN3816 High speed Input pins	PTN3816 High speed output pins
LOW	Source Lane0(p) → DP0_INP Source Lane0(n) → DP0_INN	DP0_OUTP → Sink Lane0(p) DP0_OUTN → Sink Lane0(n)
	Source Lane1(p) → DP1_INP Source Lane1(n) → DP1_INN	DP1_OUTP → Sink Lane1(p) DP1_OUTN → Sink Lane1(n)
	Source Lane2(p) → DP2_INP Source Lane2(n) → DP2_INN	DP2_OUTP → Sink Lane2(p) DP2_OUTN → Sink Lane2(n)
	Source Lane3(p) → DP3_INP Source Lane3(n) → DP3_INN	DP3_OUTP → Sink Lane3(p) DP3_OUTN → Sink Lane3(n)
HIGH	Source Lane3(p) → DP0_INP Source Lane3(n) → DP0_INN	DP0_OUTP → Sink Lane3(p) DP0_OUTN → Sink Lane3(n)
	Source Lane2(p) → DP1_INP Source Lane2(n) → DP1_INN	DP1_OUTP → Sink Lane2(p) DP1_OUTN → Sink Lane2(n)
	Source Lane1(p) → DP2_INP Source Lane1(n) → DP2_INN	DP2_OUTP → Sink Lane1(p) DP2_OUTN → Sink Lane1(n)
	Source Lane0(p) → DP3_INP Source Lane0(n) → DP3_INN	DP3_OUTP → Sink Lane0(p) DP3_OUTN → Sink Lane0(n)

Table 8. HPD configuration

HPD	PTN3816 device state
LOW	Deep power saving state
HIGH	Operational mode (D3 or D0 mode depending on AUX command or high-speed traffic)

Table 9. Flat gain configuration

FG2	FG1	Flat gain (dB) of individual DP lanes			
		Lane 3	Lane 2	Lane 1	Lane 0
LOW	LOW	0.7	0.7	0.7	0.7
LOW	OPEN	0.7	0.7	0.7	-0.7
LOW	HIGH	0.7	0.7	-0.7	0.7
OPEN	LOW	0.7	0.7	-0.7	-0.7
OPEN	OPEN	0.7	-0.7	0.7	0.7

Table 9. Flat gain configuration*...continued*

FG2	FG1	Flat gain (dB) of individual DP lanes			
		Lane 3	Lane 2	Lane 1	Lane 0
OPEN	HIGH	0.7	-0.7	-0.7	0.7
HIGH	LOW	-0.7	0.7	0.7	0.7
HIGH	OPEN	-0.7	-0.7	0.7	0.7
HIGH	HIGH	-0.7	-0.7	-0.7	-0.7

7.4 Control flow

The HPD pin of PTN3816 overrides all other control inputs/signals. This input pin can be changed dynamically at any time based on Source-sink connectivity status. After POR, PTN3816 checks the HPD pin. If it is LOW, PTN3816 defaults to Deep power saving state and if it is HIGH, the device goes into normal operating mode (and held in D3 mode) waiting for AUX communication or DP high speed traffic. The signal detector at high speed input determines whether the DP signal crosses the LoS threshold level. The AUX communication exchanged between DP source and sink is monitored by PTN3816 and the mode change (D3←→D0) is affected accordingly.

The configuration pins – EQ1, EQ2, FG1, FG2 and OSL can be changed dynamically at any time.

In deep power saving state, PTN3816 line drivers and input receive paths are terminated to ground with hi-ohmic resistors.

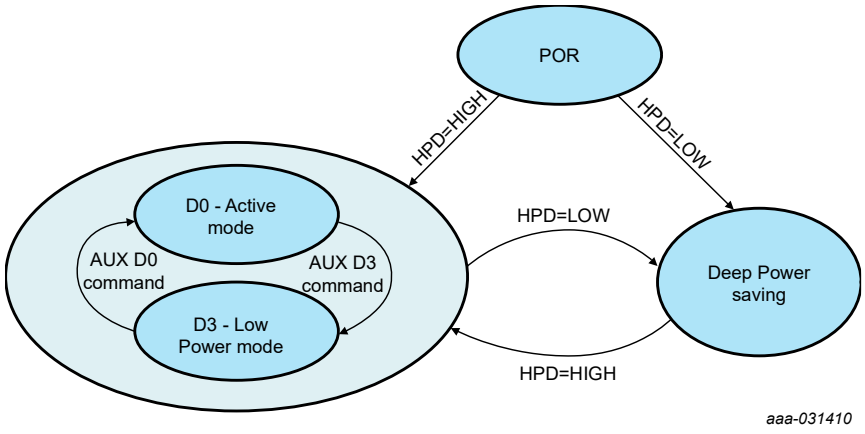


Figure 3. Control flow and state transition diagram

The HPD signal is debounced for 100 ms (min) for HIGH to LOW transitions. With this, when HPD goes LOW due to display sink disconnect will trigger PTN3816 to transition to Deep power saving state. The IRQ_HPD event (≤2 ms duration) does not impact the operational state of PTN3816.

7.5 Signal detectors

PTN3816 implements Loss of (High-speed) Signal detector aka LOS detector (LoS threshold of 45 mVppd typ) – this function is meant to detect the presence of high-speed signaling at the high-speed input pins. Based on LOS detector output, PTN3816

implements power management to optimizes current consumption under DP (D0 vs D3) mode and especially under electrical Idle conditions.

7.6 Application scenarios

PTN3816 can be used in different system applications – source side DP redriver, sink side DP redriver or as a DP redriver in a dongle/dock as shown in Figure 4 and Figure 5 below.

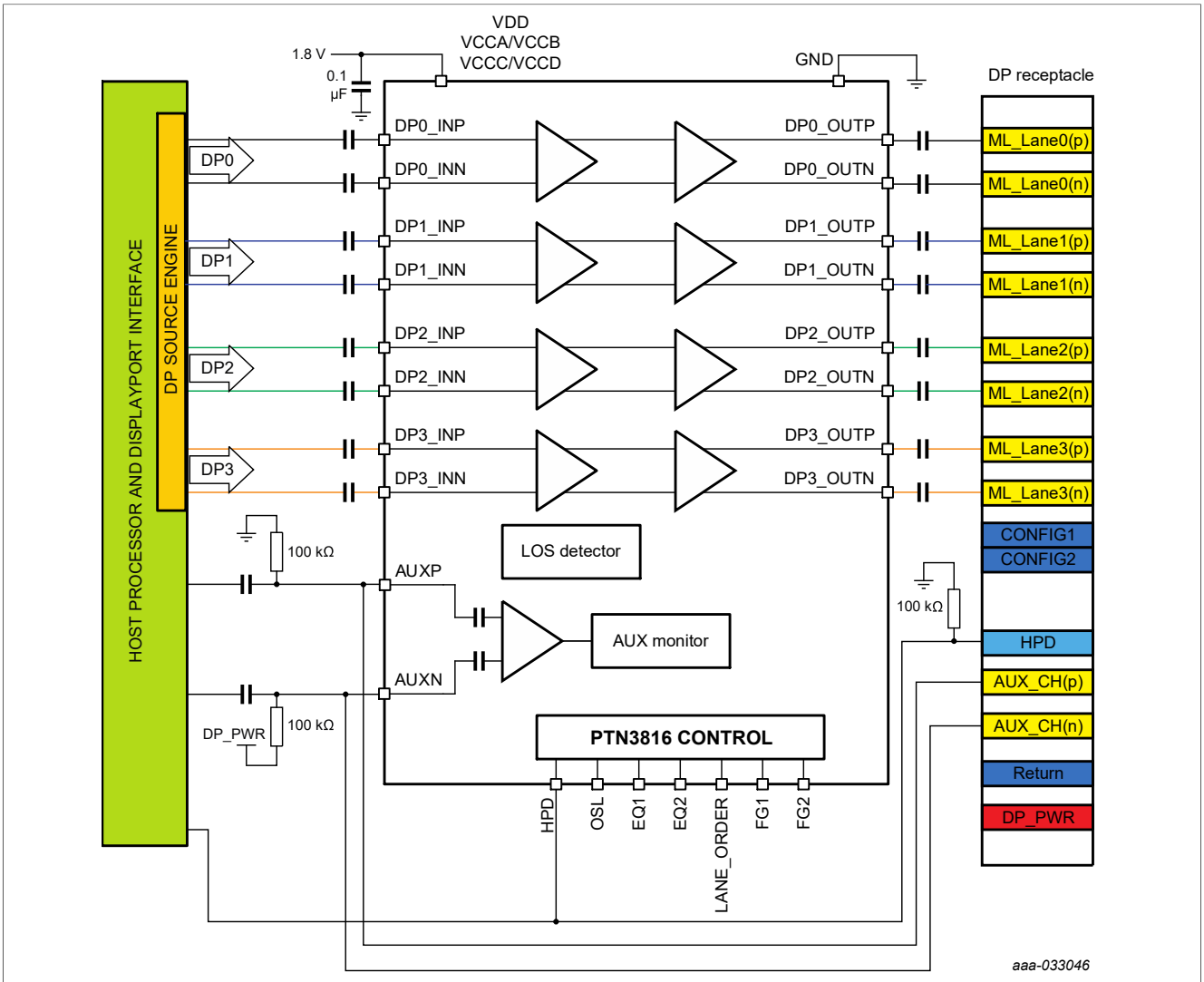


Figure 4. Connection illustration when PTN3816 in DP source side application

Figure 4 shows PTN3816 usage in DP source side application. In this configuration, upstream side of PTN3816 is connected to host processor and downstream side is connected to DP receptacle.

PTN3816 controls can be configured in the platform to suit the application needs.

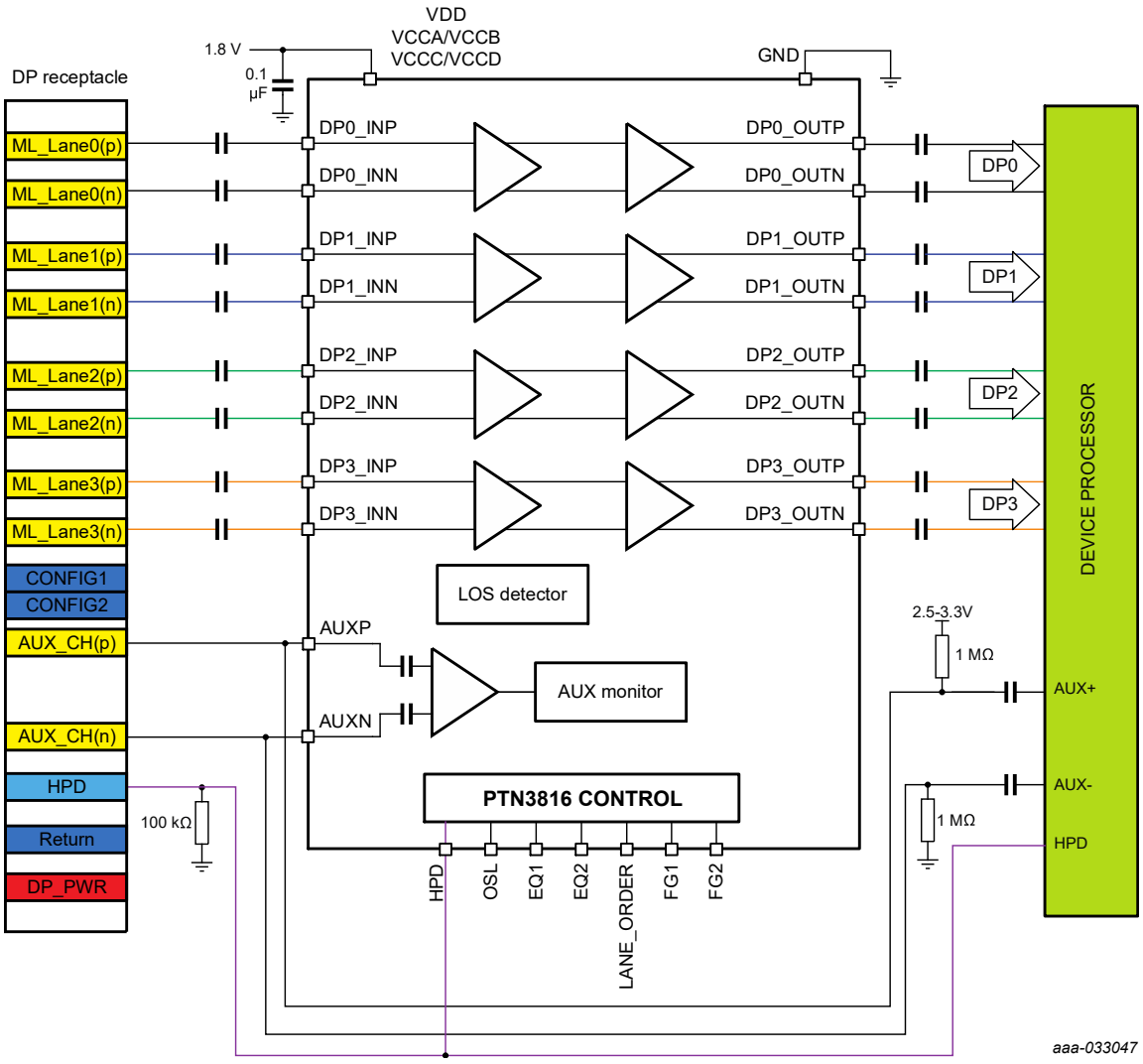


Figure 5. Connection illustration when PTN3816 in DP Sink side application

Figure 5 shows PTN3816 being used in DP sink side application. In this configuration, downstream side of PTN3816 is connected to device processor while the upstream side is connected to DP receptacle.

8 Limiting values

Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 10. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Unique Identifier
V_{DD}[1]	Supply voltage	1.8 V digital supply voltage	-0.5	-	+2.2	V	LTC-VOL-PRIO1-001
V_{CCXX}[1]	Supply voltage for high-speed channels	VCCA, VCCB, VCCC, VCCD	-0.5	-	+2.2	V	LTC-VOL-PRIO1-002
V_I[1]	Input voltage	EQ1, EQ2, FG1, FG2, OSL, HPD, LANE_ ORDER, AUXP/N pins	-0.5	-	+3.6	V	LTC-VOL-PRIO1-005
		High-speed pins	-0.5	-	+2.5	V	LTC-VOL-PRIO1-006
T_{stg}	Storage temperature		-65	-	150	°C	LTC-TMP-PRIO1-007
V_{esd}	Electro Static Discharge	HBM[2] for High-speed and AUX pins	1500	-		V	LTC-VOL-PRIO1-008
		HBM for other control pins	1500	-		V	LTC-VOL-PRIO1-009
		CDM[3] for High-speed and AUX pins	1000	-		V	LTC-VOL-PRIO1-010
		CDM for other control pins	1000	-		V	LTC-VOL-PRIO1-011
$R_{th(j-a)}$	Thermal resistance from junction to ambient environment	JEDEC still air test environment	-	40.6	-	°C/W	LTC-RES-PRIO2-012
$R_{th(j-c)}$	Thermal resistance from junction to case		-	16.8	-	°C/W	LTC-RES-PRIO2-013
$R_{th(j-b)}$	Thermal resistance from junction to board	FR4 PCB material and with center pad soldered with recommended solder pad structure	-	19.7	-	°C/W	LTC-RES-PRIO2-014

[1] All voltage values, except differential voltages, are with respect to network ground terminal.

[2] Human Body Model: ANSI/EOS/ESD-S5.1-1994, standard for ESD sensitivity testing, Human Body Model – Component level; Electrostatic Discharge Association, Rome, NY, USA.

[3] Charged Device Model: ANSI/EOS/ESD-S5.3-1-1999, standard for ESD sensitivity testing, Charged Device Model – Component level; Electrostatic Discharge Association, Rome, NY, USA

9 Recommended operating conditions

Over operating free-air temperature range (unless otherwise noted). Typical values are specified for 1.8 V and 25 °C operating temperature.

Table 11. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Unique Identifier
V_{DD}	Supply voltage for digital circuitry	VDD pin	1.7	1.8	1.9	V	ROC-VOL-PRIO1-001
V_{CC}	Supply voltage for high-speed lanes	VCCA, VCCB, VCCC and VCCD pins	1.7	1.8	1.9	V	ROC-VOL-PRIO1-002
V_I	Input voltage	EQ1, EQ2, OSL, AUXP/N, LANE_ ORDER, HPD, FG1 and FG2 pins	-0.3		3.6	V	ROC-VOL-PRIO1-003
		High-speed Data pins	-0.3		V_{CC}+0.3	V	ROC-VOL-PRIO1-005
T_{amb}	Ambient temperature	Operating in free air	-20	-	85	°C	ROC-TMP-PRIO1-008

10 Characteristics

10.1 Device characteristics

Table 12. Device characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Unique Identifier
V_{GND_VCC} noise	Noise voltage from DUT (50 Hz to 1 MHz) GND noise/bounce with V_{CC} as the reference point	DUT only and No bypass cap during testing Test recommendations: Battery powered DUT with V_{CCx} pin as the reference power plan and measure the GND pin ground bounce; measured by power rail probe		18		mVpp	DEV-VOL-PRIO2-001
	Noise voltage (1 MHz to 10 MHz)			18		mVpp	DEV-VOL-PRIO2-002
	Noise voltage (10 MHz to 5 GHz)				10	mVpp	DEV-VOL-PRIO1-003
CMRR	Common Mode Rejection Ratio Δ(Vcm,rx)/Δ(Vout_diff)	10 MHz to 1 GHz		30		dB	DEV-DB-PRIO2-004
PSRR	Power Supply Rejection Ratio Δ(VCC)/Δ(Vout_diff)	10 MHz to 200 MHz		41		dB	DEV-DB-PRIO2-005
$t_{Startup}$	Start-up time	Between supply voltage exceeding 1.4 V and sampling of EQ1/EQ2/ OSL/FG1/FG2 pin			3	ms	DEV-TIM-PRIO1-006
t_{rcfg}	Reconfiguration time	Any channel configuration pin change (from one setting to another setting) to specified operating characteristics. Device is supplied with valid supply voltage. This includes control pin changes	-	-	50	µs	DEV-TIM-PRIO1-009
$t_{hold\text{-}port}$	Hold time for data on the control pins after VDD ramps up	hold time for determining channel control changes	2.5	3		ms	DEV-TIM-PRIO1-015
$t_{HPD(EN\text{-}DIS)}$	Disable time to turn off high speed data channels when HPD goes LOW	Applicable when HPD is getting deasserted (HIGH to LOW transition).	95	100	105	ms	DEV-TIM-PRIO1-066
$t_{HPD(DIS\text{-}EN)}$	Enable time to turn on the high speed data channels when HPD goes HIGH	Applicable when HPD is getting asserted (LOW to HIGH transition).	8	10	25	µs	DEV-TIM-PRIO1-067
t_{PD}	Differential Propagation Delay	Differential propagation delay between 50 % level at input and output of High-speed pins		70	90	ps	DEV-TIM-PRIO1-011

Table 12. Device characteristics*...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Unique Identifier
Gp	Peaking gain (compensation at 10 GHz, 5 GHz and 4.05 GHz, relative to gain at 100 MHz; sinusoidal input of 100 mVppd); EQ2 = No connect, EQ1 = No connect, FGx = HIGH	10 GHz		20		dB	DEV-DB-PRIO2-016
		5 GHz		12.1		dB	DEV-DB-PRIO1-017
		4.05 GHz		10.2		dB	DEV-DB-PRIO1-018
Gp,var	Peaking gain variation over Gp at 10 GHz		-2.3		+2.3	dB	DEV-DB-PRIO2-019
OSL_{100M}	-1 dB compression point of output swing at 100 MHz	OSL = No connect		650		mVppd	DEV-VOL-PRIO2-024
		OSL = LOW		800		mVppd	DEV-VOL-PRIO2-025
		OSL = HIGH		950		mVppd	DEV-VOL-PRIO2-026
OSL_{4G}	-1 dB compression point of output swing at 4.05 GHz	OSL = No connect		650		mVppd	DEV-VOL-PRIO2-070
		OSL = LOW		800		mVppd	DEV-VOL-PRIO2-071
		OSL = HIGH		950		mVppd	DEV-VOL-PRIO2-072
OSL_{10G}	-1 dB compression point of output swing at 10 GHz	OSL = No connect		650		mVppd	DEV-VOL-PRIO2-032
		OSL = LOW		800		mVppd	DEV-VOL-PRIO2-033
		OSL = HIGH		950		mVppd	DEV-VOL-PRIO2-034
V_{noise_in}	Input referred noise	100 MHz to 15 GHz; Peaking gain of 10.2 dB at 10 GHz and OSL 950 mVppd		0.8		mV_{rms}	DEV-VOL-PRIO2-035
		100 MHz to 15 GHz; Peaking gain of 17.3 dB at 10 GHz and OSL 950 mVppd		1		mV_{rms}	DEV-VOL-PRIO2-036
V_{noise_out}	Output referred noise	100 MHz to 15 GHz; Peaking gain of 10.2 dB at 10 GHz and OSL 950 mVppd		2.0		mV_{rms}	DEV-VOL-PRIO2-037
		100 MHz to 15 GHz; Peaking gain of 17.3 dB at 10 GHz and OSL 950 mVppd		2.0		mV_{rms}	DEV-VOL-PRIO2-038
V_{LOS}	Loss of Signal detector threshold level	Applicable to high speed lanes		45		mVppd	DEV-VOL-PRIO2-042
I_{DD}	Supply current All 4 DP lanes are active	-1 dB compression point at 950 mVppd		250	270	mA	DEV-CUR-PRIO1-044
		-1 dB compression point at 800 mVppd		225	260	mA	DEV-CUR-PRIO1-045
		-1 dB compression point at 650 mVppd		200	240	mA	DEV-CUR-PRIO1-046

Table 12. Device characteristics...*continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Unique Identifier
	Supply current 2 DP lanes are active	-1 dB compression point at 950 mVppd		125	140	mA	DEV-CUR-PRIO1-048
		-1 dB compression point at 800 mVppd		110	130	mA	DEV-CUR-PRIO1-049
		-1 dB compression point at 650 mVppd		115	120	mA	DEV-CUR-PRIO1-050
	Supply current 1 DP lane is active	-1 dB compression point at 950 mVppd		62	75	mA	DEV-CUR-PRIO1-052
		-1 dB compression point at 800 mVppd		57	70	mA	DEV-CUR-PRIO1-053
		-1 dB compression point at 650 mVppd		52	65	mA	DEV-CUR-PRIO1-054
	Supply current	Power saving mode (DP D3 mode)		3.2		mA	DEV-CUR-PRIO2-059
		Deep Power-saving state (HPD = LOW)		10		µA	DEV-CUR-PRIO2-060
$Xtak_{oo}$	Far end crosstalk between two output drivers (between any two DP lane outputs)	Applies at 10 GHz		-34		dB	DEV-DB-PRIO2-065

Note: For DisplayPort interface, One lane means one differential pair/channel

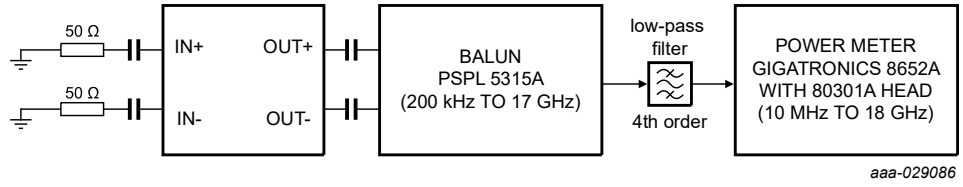


Figure 6. Noise test configuration

10.2 Input AC/DC characteristics

Table 13. Input AC/DC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Unique Identifier
$C_{ac\_coupling}$	AC coupling capacitance	Applicable for high speed input pins	75		265	nF	INC-CAP-PRIO1-001
$T_{Discharge}$	Discharge time				250	ms	INC-TIM-PRIO1-003
$R_{in\text{-}DC}$	Input DC common mode impedance		21		34	Ω	INC-RES-PRIO1-004
$V_{RX\text{-}CM\text{-}AC\text{-}PP}$	RX AC common mode voltage tolerance	A single tone injection at 120 MHz is a stress test			300	mVpp	INC-VOL-PRIO1-005
		A single tone injection at 400 MHz is another stress test			100	mVpp	INC-VOL-PRIO1-006
$R_{IN\text{-}DIFF\text{-}DC}$	DC Differential Impedance		90		131	Ω	INC-RES-PRIO1-007
$V_{IP\text{-}DC\text{-}CM}$	DC biasing/common mode voltage	Biasing on high speed input pins		1.8		V	INC-VOL-PRIO2-008
$V_{RX\text{-}DIFF\text{-}PP}$	DisplayPort Input voltage (peak to peak differential signal)	At high speed input pins	45		1400	mVppd	INC-VOL-PRIO1-013
$V_{voltage\_jump}$	Maximum voltage jump on input pin side measured before AC coupling capacitors	Applicable during power-on/power-off, transition from low power to active state and vice versa	-0.3	-	1	V	INC-VOL-PRIO1-009
$RL_{DD11,\ IN}$	Input differential mode Return Loss	100 MHz to 10.3 GHz		15		dB	INC-DB-PRIO2-014
$RL_{CC11,\ IN}$	Input common mode Return Loss	100 MHz to 10.3 GHz		12		dB	INC-DB-PRIO2-015

10.3 Output AC/DC characteristics

Table 14. Output AC/DC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Unique Identifier
$C_{ac\_coupling}$	AC coupling capacitance	Applicable on high speed output	75		265	nF	OUC-CAP-PRIO1-013
R_{OP-DC}	Output DC common mode Impedance		21		34	Ω	OUC-RES-PRIO1-001
$R_{OP-DIFF-DC}$	Output Differential Impedance		89		131	Ω	OUC-RES-PRIO1-002
$V_{OP-DC-CM}$	DC biasing/common mode voltage on high speed pins	-1 dB Compression point at 950 mVppd		1.2		V	OUC-VOL-PRIO2-003
		-1 dB Compression point at 800 mVppd		1.3		V	OUC-VOL-PRIO2-004
		-1 dB Compression point at 650 mVppd		1.4		V	OUC-VOL-PRIO2-005
$V_{TX-CM-AC-PP\_ACTIVE}$	Output AC Common mode output voltage in active state	Device input fed with differential signal			20	mVpp	OUC-VOL-PRIO1-007
$V_{TX-IDLE-DIFF-AC-pp}$	Output AC differential output voltage	When link is in electrical idle			10	mVppd	OUC-VOL-PRIO1-008
$V_{voltage\_jump}$	Maximum voltage jump on output pin side measured after AC coupling capacitors	Applicable during power-on/power-off, transition from low power to active state and vice versa	-0.3	-	1	V	OUC-VOL-PRIO1-009
$RL_{DD11, OP}$	Output differential mode Return Loss	100 MHz to 10.3 GHz		18		dB	OUC-DB-PRIO2-011
$RL_{CC11, OP}$	Output common mode Return Loss	100 MHz to 10.3 GHz		12		dB	OUC-DB-PRIO2-012

10.4 AUX monitor characteristics

Table 15. AUX monitor characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Unique Identifier
V_I	Bias Voltage at the pin	AUXP/AUXN pins	0		3.6	V	AUX-VOL-PRIO1-001
r_{AUX}	AUX bit rate			1		Mbps	AUX-FRQ-PRIO2-002
$V_{AUX\text{-}AC\text{-}DIFF\text{-}pp}$	AUX AC differential peak-to-peak	AUXP/AUXN pins	0.27		1.38	Vppd	AUX-VOL-PRIO1-003
I_{IL}	Leakage current at the pin	Pin voltage 3.6 V			19	µA	AUX-CUR-PRIO1-004
I_{bck}	Back current sunk from pin to powered down supply	V_{DD} = 0 V, Pin voltage = 3.6 V			27	µA	AUX-CUR-PRIO1-005
Z_{in}	AUX monitor differential input impedance	Over frequency range of interest DC to 50 MHz		1		MΩ	AUX-RES-PRIO2-006
C_{Aux}	AUX AC coupling capacitance		75		200	nF	AUX-CAP-PRIO1-007

All S-parameter measurements are with respect to 100 Ω differential impedance reference and 50 Ω single-ended impedance reference.

10.5 Input characteristics of binary configuration pin – HPD, LANE_ORDER

Table 16. Binary control input characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Unique Identifier
V_{IH}	High level voltage	LANE_ORDER pin	$0.7*V_{DD}$	-	$V_{DD}+0.3$	V	BIN-VOL-PRIO1-001
V_{IL}	Low level voltage	LANE_ORDER pin	-	-	$0.25*V_{DD}$	V	BIN-VOL-PRIO1-002
$V_{Lo\ to\ Hi}$	HPD plug detection threshold	HPD pin	2	-	3.6	V	BIN-VOL-PRIO1-007
$V_{Hi\ to\ Lo}$	HPD unplug detection threshold	HPD pin	-	-	0.8	V	BIN-VOL-PRIO1-008
I_{IL}	Leakage current at the pin	VDD = 1.8 V, Pin voltage = 3.6 V			14	µA	BIN-CUR-PRIO1-003
		VDD = 1.8 V, Pin voltage = 1.8 V			1.5	µA	BIN-CUR-PRIO1-004
I_{bck}	Back current sunk from pin to powered down supply	VDD = 0, Pin voltage = 3.6 V			24	µA	BIN-CUR-PRIO1-005
C_{pin}	Maximum allowed capacitance at the pin				10	pF	BIN-CAP-PRIO1-006

10.6 Input characteristics of ternary configuration pins - EQ1, EQ2, OSL, FG1 and FG2

Table 17. Ternary control input characteristics (external system voltage V_{SYS}= 1.7 V to 3.6 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Unique Identifier
V_{IH}	High level voltage	External pull-up 1 kΩ resistor to V_{SYS}	0.8*V_{DD}		V_{SYS}	V	TER-VOL-PRIO1-001
V_{IM}	Unconnected or open condition		0.35*V_{DD}		0.45*V_{DD}	V	TER-VOL-PRIO1-002
V_{IL}	Low level voltage	External pull-down 1 kΩ resistor to GND			0.15*V_{DD}	V	TER-VOL-PRIO1-003
I_{IL}	Leakage current when pin is not active	VDD = 1.8 V, Pull-up resistor connected to V_{SYS} = 3.6 V			15	µA	TER-CUR-PRIO1-004
		VDD = 1.8 V, Pull-up resistor connected to V_{SYS} = 1.8 V			1	µA	TER-CUR-PRIO1-005
	Leakage current when pin is active	VDD = 1.8 V, Pull-up resistor connected to V_{SYS} = 3.6 V			80	µA	TER-CUR-PRIO1-006
		VDD = 1.8 V, Pull-up resistor connected to V_{SYS} = 1.8 V	-25		35	µA	TER-CUR-PRIO1-007
I_{bck}	Back current sunk from pin to powered down supply	VDD = 0, Pin voltage = 3.6 V			20	µA	TER-CUR-PRIO1-008
R_{pu}	Internal pull-up resistance			120		kΩ	TER-RES-PRIO2-009
R_{pd}	Internal pull-down resistance			80		kΩ	TER-RES-PRIO2-010
C_{pin}	Maximum allowed capacitance at the pin				10	pF	TER-CAP-PRIO1-011

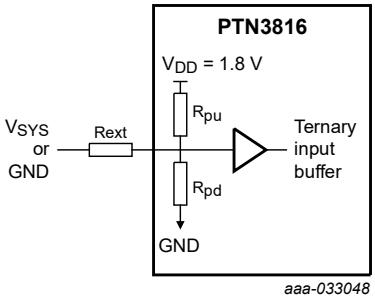


Figure 7. Ternary GPIO input buffer setting

11 Package outline

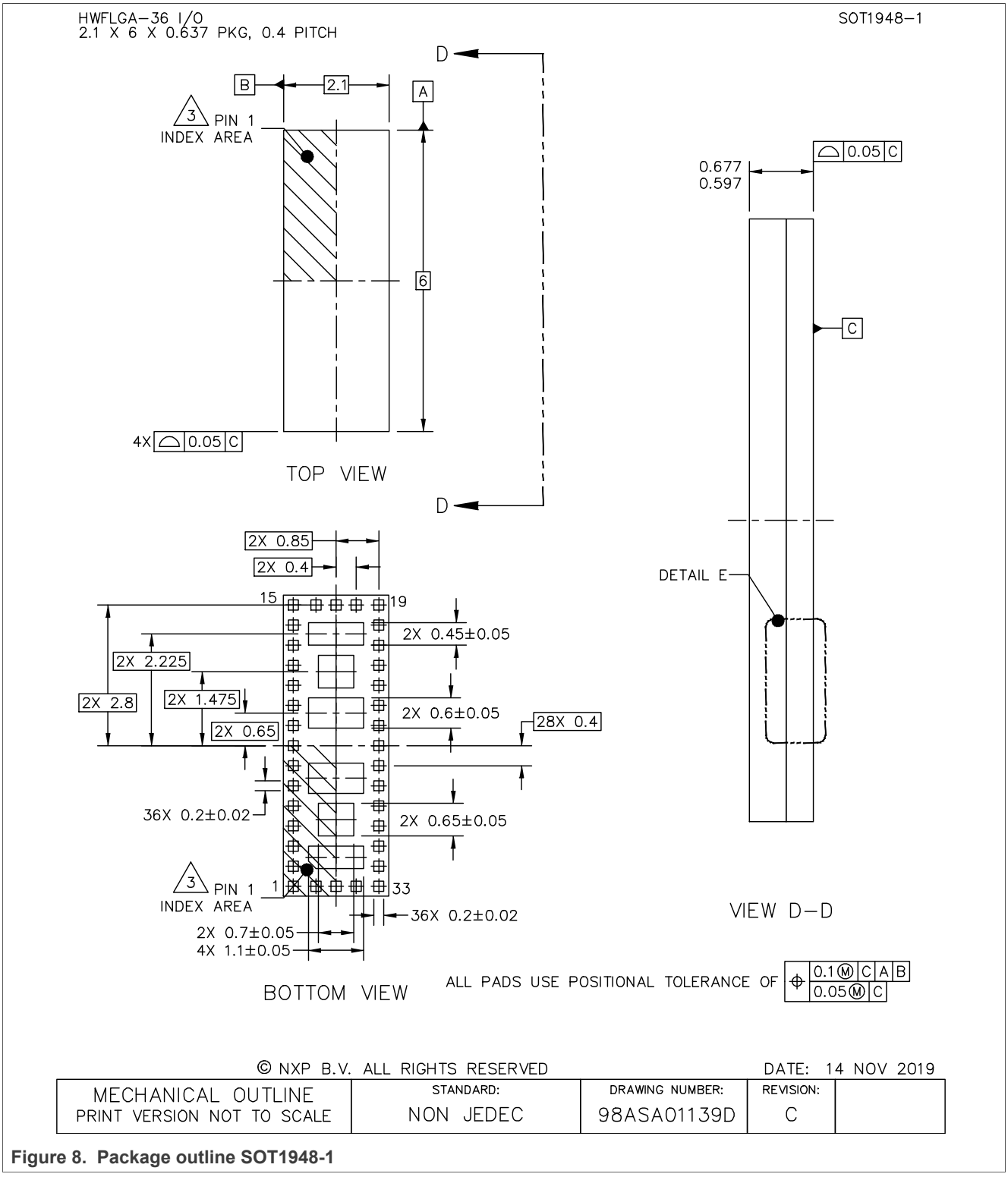


Figure 8. Package outline SOT1948-1

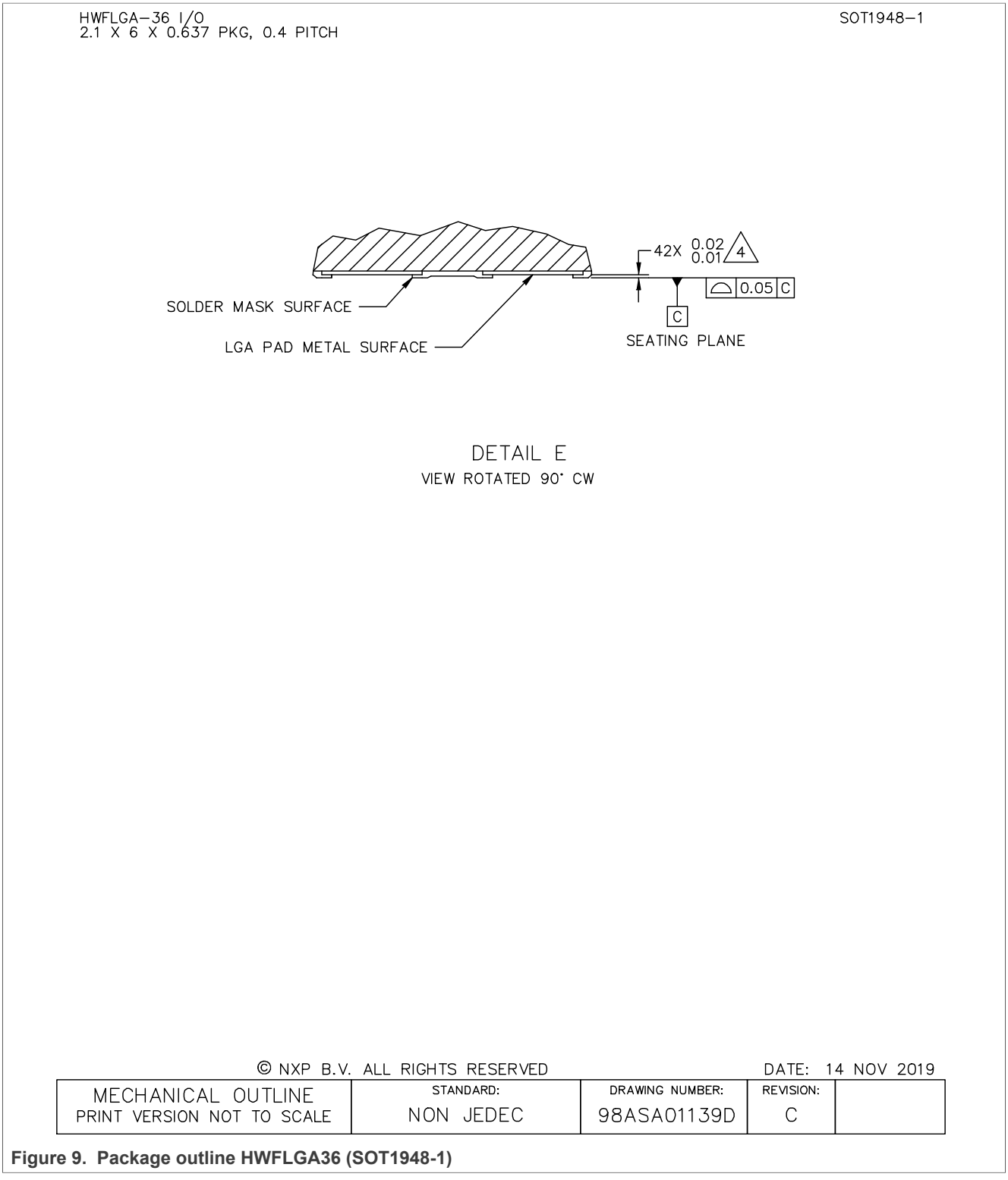


Figure 9. Package outline HWFLGA36 (SOT1948-1)

Figure 10. Package outline note HWFLGA36 (SOT1948-1)

12 Packing information

12.1 SOT1948-1; HWFLGA36; reel dry pack, SMD, 13" Q1 standard product orientation ordering code (12NC) ending 019

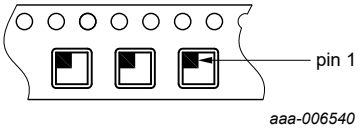
12.1.1 Dimensions and quantities

Table 18. Dimensions and quantities

Reel dimensions d × w (mm)[1]	SPQ/PQ (pcs)[2]	Reels per box
330 × 12	7000	1

[1] d = reel diameter; w = tape width.
[2] Packing quantity dependent on specific product type. View ordering and availability details at NXP order portal, or contact your local NXP representative.

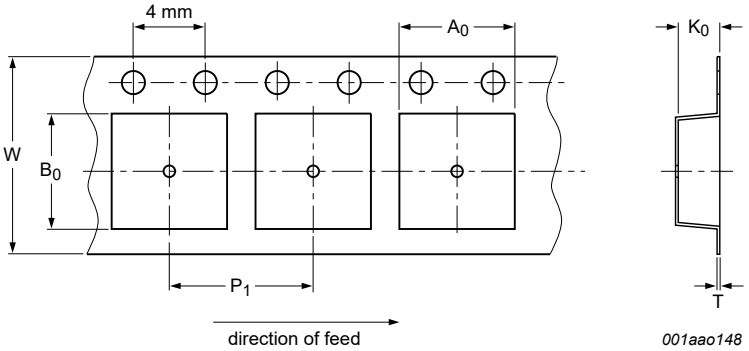
12.1.2 Product orientation



Pin 1 is in quadrant 1.

Figure 11. Product orientation in carrier tape

12.1.3 Carrier tape dimensions



Not drawn to scale.

Figure 12. Carrier tape dimensions

Table 19. Carrier tape dimensions

In accordance with IEC 60286-3/EIA-481.

A_0 (mm)	B_0 (mm)	K_0 (mm)	T (mm)	P_1 (mm)	W (mm)
2.30 ± 0.05	6.30 ± 0.05	0.85 +.1/-.05	0.30 ± 0.05	8 ± 0.1	12 +0.3/-0.1

13 Soldering

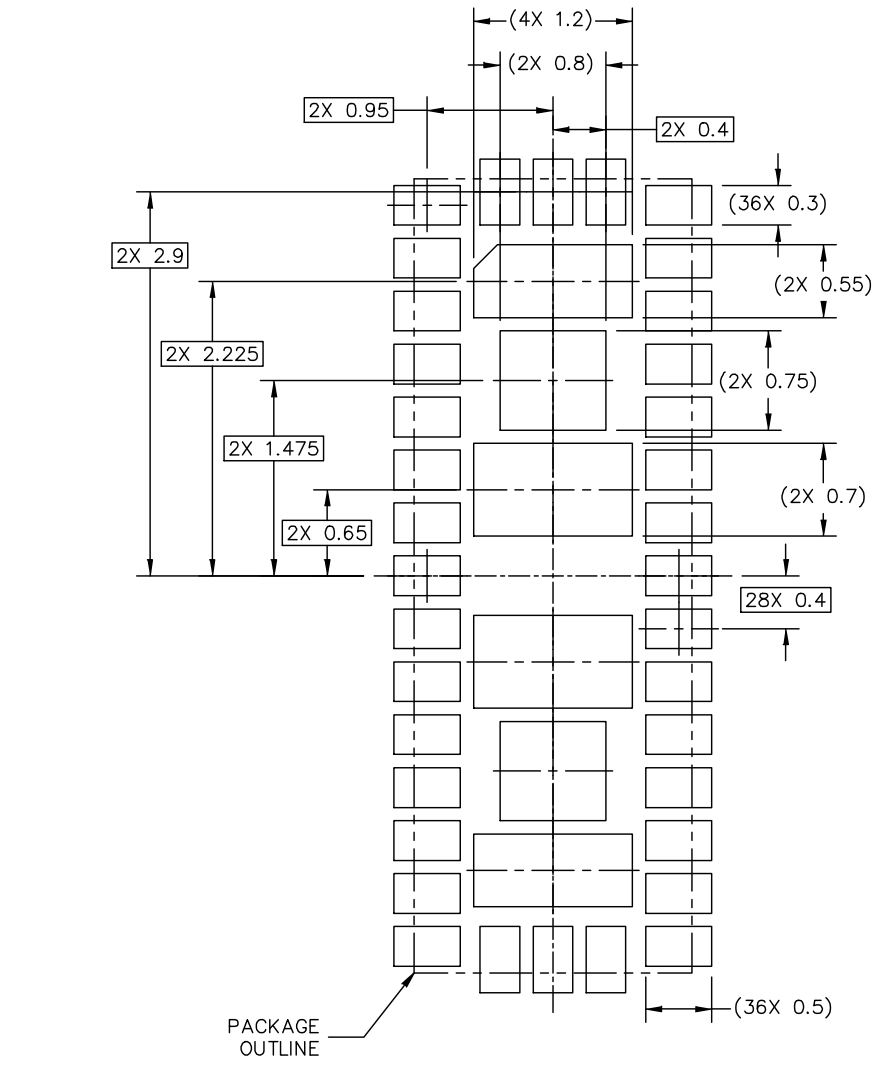


Figure 13. Reflow soldering footprint for SOT1948-1

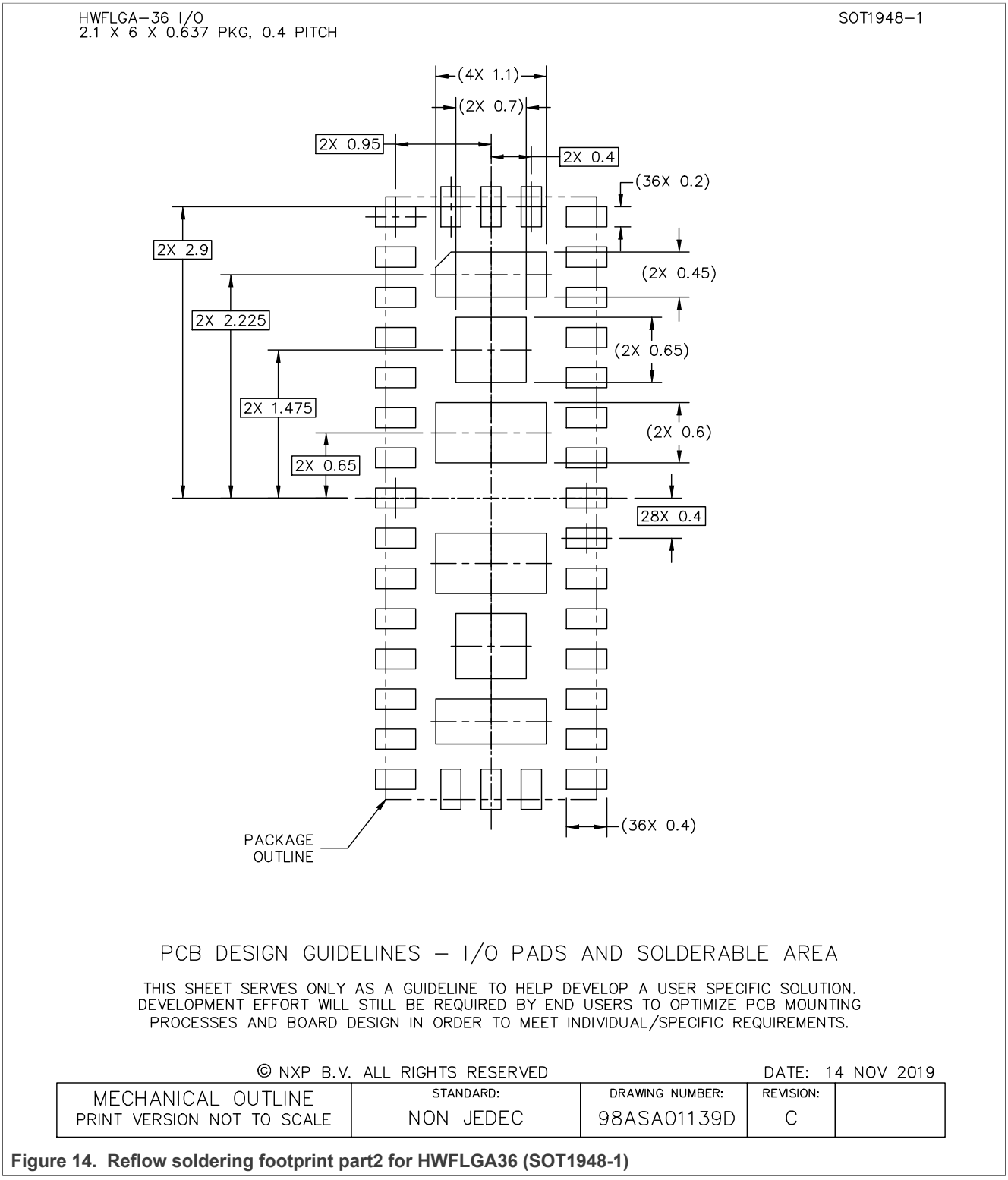


Figure 14. Reflow soldering footprint part2 for HWFLGA36 (SOT1948-1)

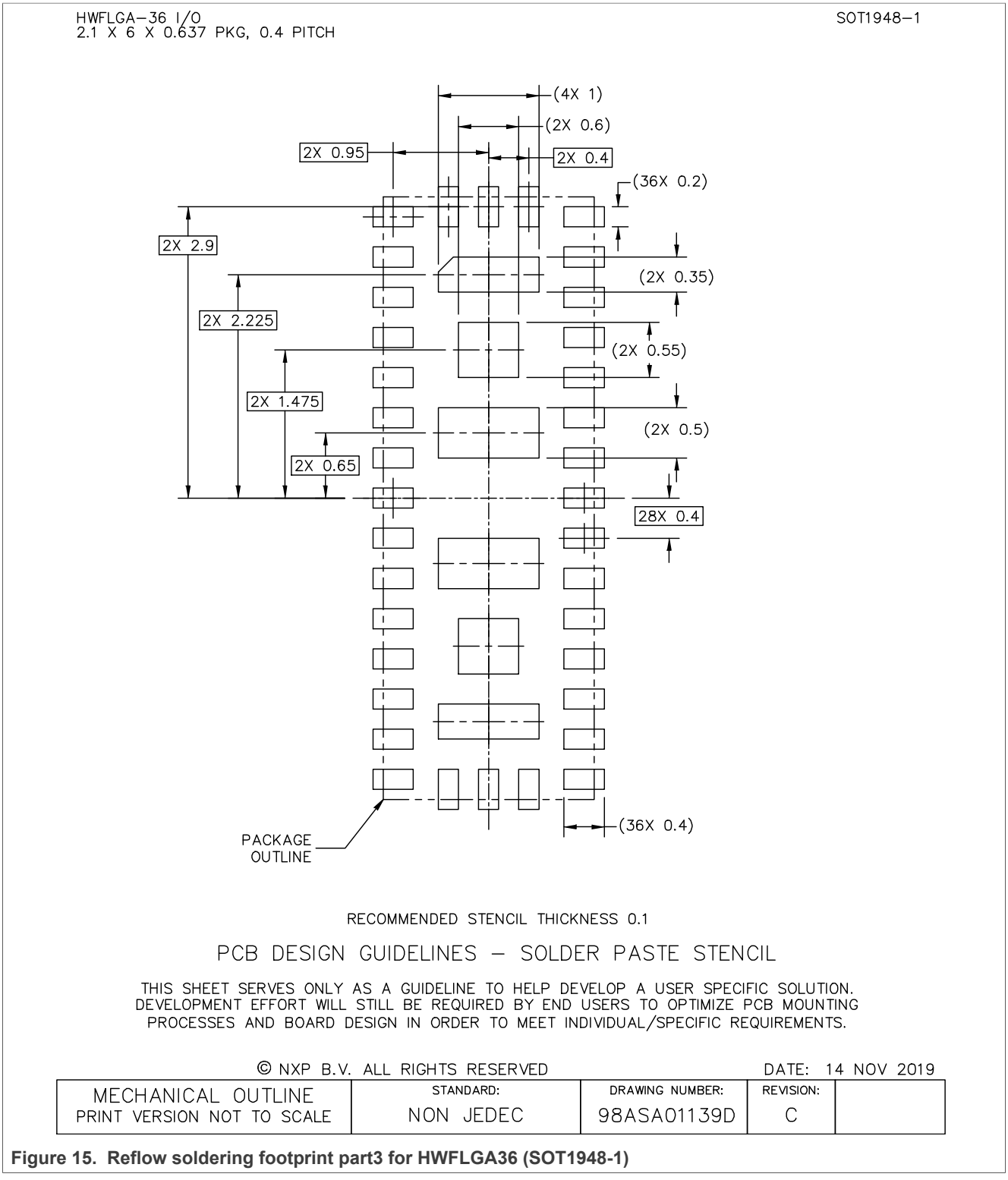


Figure 15. Reflow soldering footprint part3 for HWFLGA36 (SOT1948-1)

14 Abbreviations

Table 20. Abbreviations

Acronym	Description
AUX	Auxiliary channel of DisplayPort standard
CDM	Charged Device Model
DFP	Downstream Facing Port
DP	DisplayPort
Gbps	Giga bits per second
HBM	Human Body Model
HPD	Hot Plug Detect signaling of DisplayPort standard
NC	No Connect
OS	Output Swing
OSL	Output Swing Linearity level
Rx	Receiver
SI	Signal Integrity
TX	Transmitter
UFP	Upstream Facing Port

15 Revision history

Table 21. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PTN3816 v1.0	20210607	Product data sheet	-	-

16 Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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