

PUMB11

PNP/PNP resistor-equipped double transistor; R1 = 10 k Ω , R2 = 10 k Ω

1 October 2022

Product data sheet

1. General description

PNP/PNP double Resistor-Equipped Transistor (RET) in a very SOT363 (SC-88) Surface-Mounted Device (SMD) plastic package.

NPN/PNP complement: PUMD3
NPN/NPN complement: PUMH11

2. Features and benefits

- 100 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- · Reduces component count
- Reduces pick and place costs

3. Applications

- · Low current peripheral drivers
- · Control of IC inputs
- · Replaces general-purpose transistors in digital applications

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit	
Per transistor	Per transistor							
V _{CEO}	collector-emitter voltage	open base		-	-	-50	V	
Io	output current			-	-	-100	mA	
R1	bias resistor 1 (input)		[1]	7	10	13	kΩ	
R2/R1	bias resistor ratio		[1]	0.8	1	1.2		

[1] See "Section 11: Test information" for resistor calculation and test conditions.



PNP/PNP resistor-equipped double transistor; R1 = 10 k Ω , R2 = 10 k Ω

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	GND1	GND (emitter) TR1		O1 I2 GND2
2	I1	input (base) TR1		
3	O2	output (collector) TR2		R1 R2
4	GND2	GND (emitter) TR2		TR2
5	12	input (base) TR2		R2 R1
6	01	output (collector) TR1	1 1 2 3 TSSORE (SOT262)	
			TSSOP6 (SOT363)	GND1 I1 O2
				006aaa212

6. Ordering information

Table 3. Ordering information

Type number	Package				
	Name	Version			
PUMB11		plastic, surface-mounted package; 6 leads; 0.65 mm pitch; 2.1 mm x 1.25 mm x 0.95 mm body	SOT363		

7. Marking

Table 4. Marking codes

Type number	Marking code[1]
PUMB11	B%1

[1] % = placeholder for manufacturing site code

PNP/PNP resistor-equipped double transistor; R1 = 10 k Ω , R2 = 10 k Ω

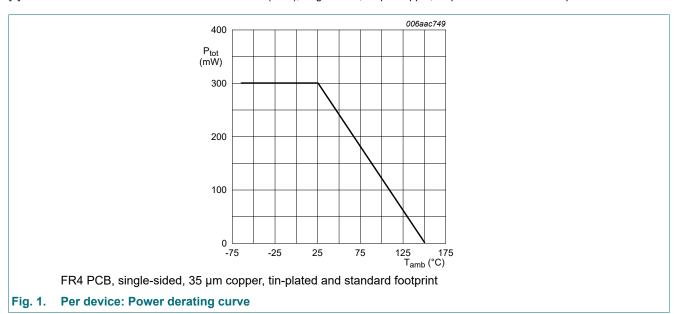
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transiste	or		,	'	'	
V _{CBO}	collector-base voltage	open emitter		-	-50	V
V _{CEO}	collector-emitter voltage	open base		-	-50	V
V_{EBO}	emitter-base voltage	open collector		-	-10	V
V _I	input voltage	positive		-	10	V
		negative		-	-40	V
Io	output current			-	-100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	200	mW
Per device						
P _{tot}	total power dissipation	T _{amb} = 25 °C	[1]	-	300	mW
Tj	junction temperature			-	150	°C
T _{amb}	ambient temperature			-65	150	°C
T _{stg}	storage temperature			-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided, 35 µm copper, tin-plated and standard footprint.



PNP/PNP resistor-equipped double transistor; R1 = 10 k Ω , R2 = 10 k Ω

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	625	K/W
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	417	K/W

[1] Device mounted on an FR4 PCB, single-sided, 35 µm copper, tin-plated and standard footprint.

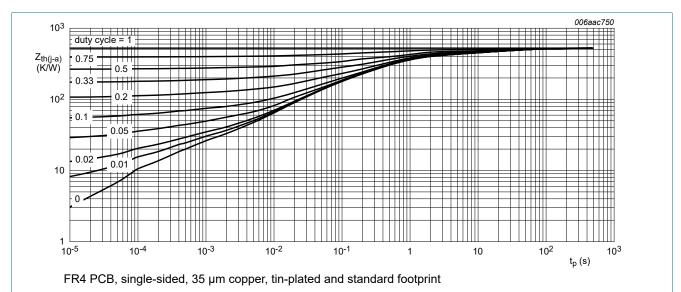


Fig. 2. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

PNP/PNP resistor-equipped double transistor; R1 = 10 k Ω , R2 = 10 k Ω

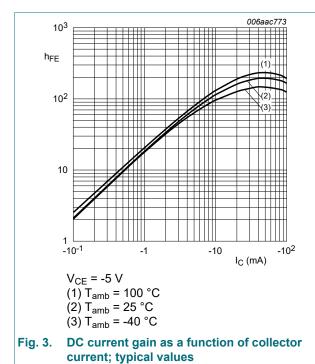
10. Characteristics

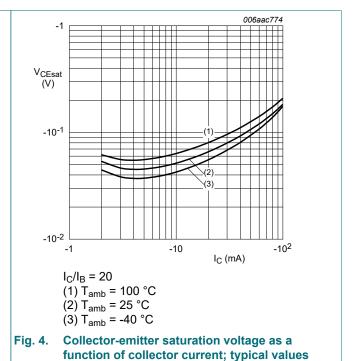
Table 7. Characteristics

 T_{amb} = 25 °C unless otherwise specified.

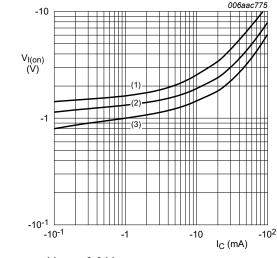
Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Per transist	or		<u> </u>				
V _{(BR)CBO}	collector-base breakdown voltage	I _C = -100 μA; I _E = 0 A	= -100 μA; l _E = 0 A		-	-	V
V _{(BR)CEO}	collector-emitter breakdown voltage	I _C = -2 mA; I _B = 0 A		-50	-	-	V
I _{CBO}	collector-base cut-off current	V _{CB} = -50 V; I _E = 0 A		-	-	-100	nA
I _{CEO} collector-emitter cut-off		V _{CE} = -30 V; I _B = 0 A		-	-	-1	μΑ
	current	V _{CE} = -30 V; I _B = 0 A; T _j = 150 °C		-	-	-5	μΑ
I _{EBO}	emitter-base cut-off current	V _{EB} = -5 V; I _C = 0 A		-	-	-400	μΑ
h _{FE}	DC current gain	V _{CE} = -5 V; I _C = -5 mA		-30	-	-	
V _{CEsat}	collector-emitter saturation voltage	$I_C = -10 \text{ mA}; I_B = -0.5 \text{ mA}$		-	-	-100	mV
V _{I(off)}	off-state input voltage	V _{CE} = -5 V; I _C = -100 μA		-	-1.1	-0.8	V
V _{I(on)}	on-state input voltage	V _{CE} = -0.3 V; I _C = -10 mA		-2.5	-1.8	-	V
R1	bias resistor 1 (input)		[1]	7	10	13	kΩ
R2/R1	bias resistor ratio		[1]		1	1.2	
C _c	collector capacitance	V_{CB} = -10 V; I_{E} = 0 A; i_{e} = 0 A; f = 1 MHz		-	-	3	pF
f _T	transition frequency	V _{CE} = -5 V; I _C = -10 mA; f = 100 MHz	[2]	-	180	-	MHz

- [1] See "Section 11: Test information" for resistor calculation and test conditions.
- [2] Characteristics of built-in transistor



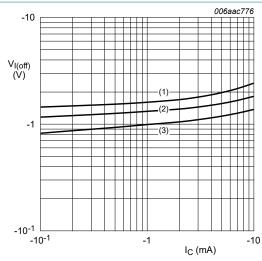


PNP/PNP resistor-equipped double transistor; R1 = 10 k Ω , R2 = 10 k Ω



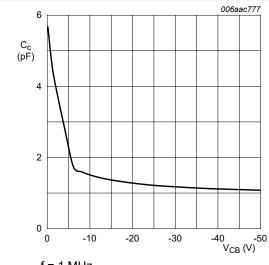
V_{CE} = -0.3 V (1) T_{amb} = -40 °C (2) T_{amb} = 25 °C (3) T_{amb} = 100 °C

Fig. 5. On-state input voltage as a function of collector | Fig. 6. current; typical values



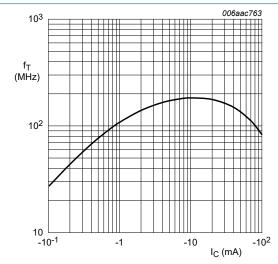
V_{CE} = -5 V (1) T_{amb} = -40 °C (2) T_{amb} = 25 °C (3) T_{amb} = 100 °C

Off-state input voltage as a function of collector current; typical values



f = 1 MHz T_{amb} = 25 °C

Fig. 7. Collector capacitance as a function of collectorbase voltage; typical values



f = 100 MHz

 $T_{amb} = 25 \, ^{\circ}C$

 $V_{CE} = -5 V$

Transition frequency as a function of collector Fig. 8. current; typical values of built-in transistor

PNP/PNP resistor-equipped double transistor; R1 = 10 k Ω , R2 = 10 k Ω

11. Test information

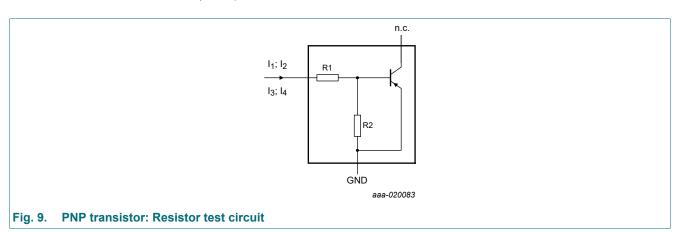
Resistor calculation

· Calculation of bias resistor 1 (R1)

$$R_1 = \frac{V(I_2) - V(I_1)}{I_2 - I_1}$$

· Calculation of bias resistor ratio (R2/R1)

$$\frac{R2}{R1} = \frac{V(I4) - V(I3)}{R1 \cdot (I4 - I3)} - 1$$

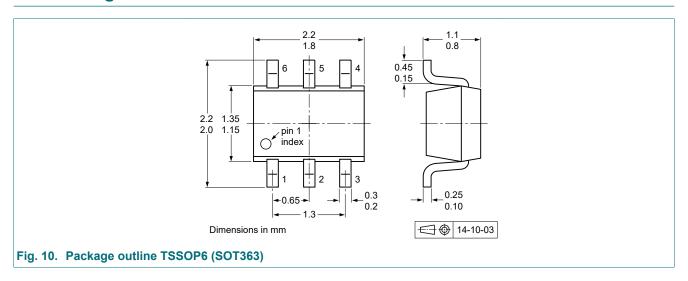


Resistor test conditions

Table 8. Resistor test conditions

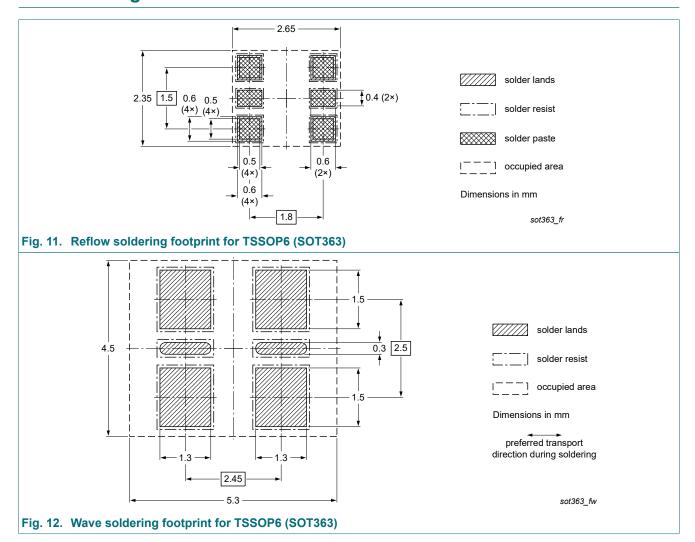
Table 6. Resist	tuble of Resistor test conditions						
PUMB11	R1 (kΩ)	R2 (kΩ)	Test conditions				
			I ₁	l ₂	l ₃	14	
TR1 (PNP)	10	10	-350 μΑ	-450 μA	350 μΑ	450 µA	
TR2 (PNP)	10	10	-350 μΑ	-450 μA	350 μΑ	450 μΑ	

12. Package outline



PNP/PNP resistor-equipped double transistor; R1 = 10 k Ω , R2 = 10 k Ω

13. Soldering



PNP/PNP resistor-equipped double transistor; R1 = 10 k Ω , R2 = 10 k Ω

14. Revision history

Table 9. Revision history

Table 3. Kevision msto		I	I		
Data sheet ID	Release date	Data sheet status	Change notice	Supersedes	
PUMB11 v.5	20221001	Product data sheet	-	PEMB11_PUMB11 v.4	
Modifications:	 The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Family data sheet reduced to single type data sheet. Product changed to non-automotive qualification. Please refer to nexperia.com for automotiv (-Q) product alternative(s). Packing information is removed. 				
PEMB11_PUMB11 v.4	20111130	Product data sheet	-	PEMB11_PUMB11 v.3	
PEMB11_PUMB11 v.3	20031003	Product data sheet	-	PUMB11 v.2	
PUMB11 v.2	20010913	Preliminary specification	-	PUMB11 v.1	
PUMB11 v.1	20000808	Product specification	-	-	

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15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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