QPA1000

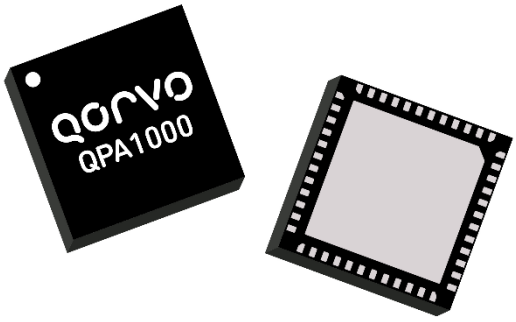
2.8 – 3.2 GHz 50 Watt GaN Amplifier

Product Description

Qorvo's QPA1000 is a high-power, S-band amplifier fabricated on Qorvo's QGaN25 0.25 um GaN on SiC production process. Covering 2.8 – 3.2 GHz, the QPA1000 typically provides 47 dBm of saturated output power and 22 dB of large-signal gain while achieving 58 % power-added efficiency.

The QPA1000 can also support a variety of operating conditions to best support system requirements. With good thermal properties, it can support a range of bias voltages and will perform well under pulse applications. The QPA1000 is matched to 50 ohms with integrated DC blocking caps on both I/O ports. It is ideal for use in both commercial and military radar systems.

Lead-free and RoHS compliant.

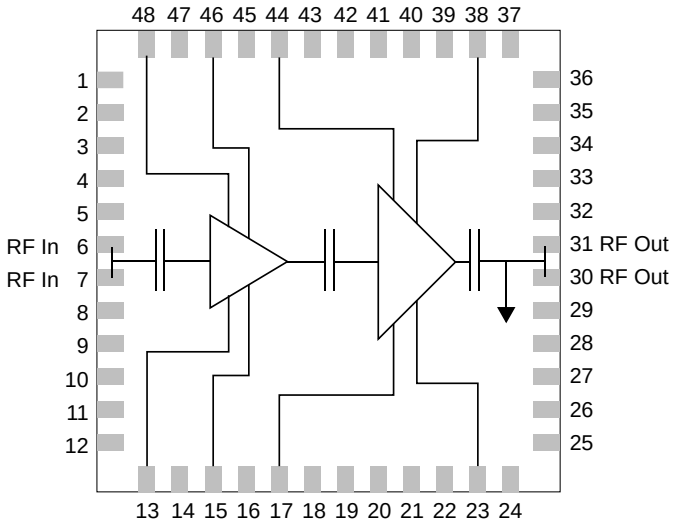


Product Features

- Frequency Range: 2.8 – 3.2 GHz
- Pout: 47 dBm (P_{IN} = 25 dBm)
- Large Signal Gain: 22 dB (P_{IN} = 25 dBm)
- PAE: 58 % (P_{IN} = 25 dBm)
- Bias: V_D = 25 V, I_{DQ} = 200 mA, V_G = −2.8 V (Typ)
- Supports Long Pulse Operation
- Package Dimensions: 7.0 x 7.0 x 0.85 mm

Performance is typical across frequency. Please reference electrical specification table and data plots for more details.

Functional Block Diagram



Applications

- Military Radar
- Commercial Radar

Ordering Information

Part	Description
QPA1000	2.8–3.2 GHz 50 W GaN Power Amplifier
QPA1000EVB	QPA1000 Evaluation Board

Absolute Maximum Ratings

Parameter	Value / Range
Drain Voltage (V_D)	40 V
Drain Current (I_{D1}/I_{D2})	0.77 / 3.84 A
Gate Voltage Range	−8 to 0 V
Gate Current (I_G)	See plot page 9
Dissipated Power (P_{DISS})[1]	44.25 W
Input Power (50 Ω, 85 °C)	33 dBm
Input Power (9:1 VSWR, 85 °C)	33 dBm
Mounting Temperature (30 seconds)	260 °C
Storage Temperature	−55 to 150 °C

Note:
[1] T_{BASE} = 85 °C, T_{CH} = 225 °C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter	Value
Drain Voltage	25 V
Drain Current (quiescent, I_{DQ})	200 mA
Drain Current (under drive, I_D)	3.7 A
Gate Voltage	-2.8 V
Operating Temperature Range	−40 to 85 °C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

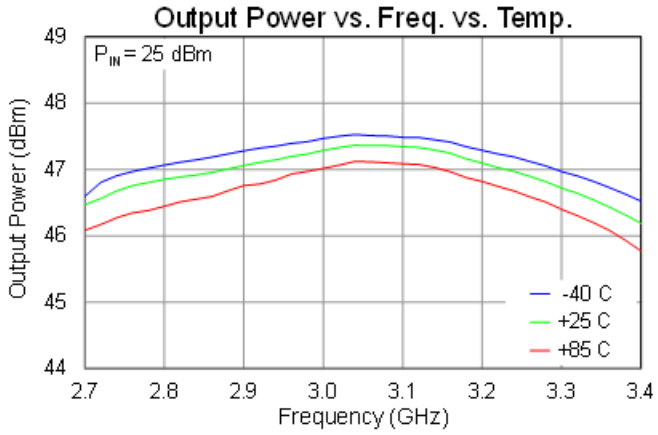
Electrical Specifications

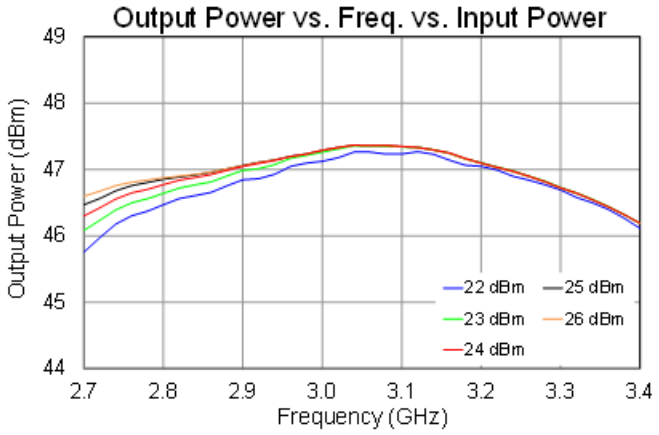
Test conditions, unless otherwise noted: 25 °C, V_D = 25 V, I_{DQ} = 200 mA, Pulse Width = 100 us, Duty Cycle = 10%

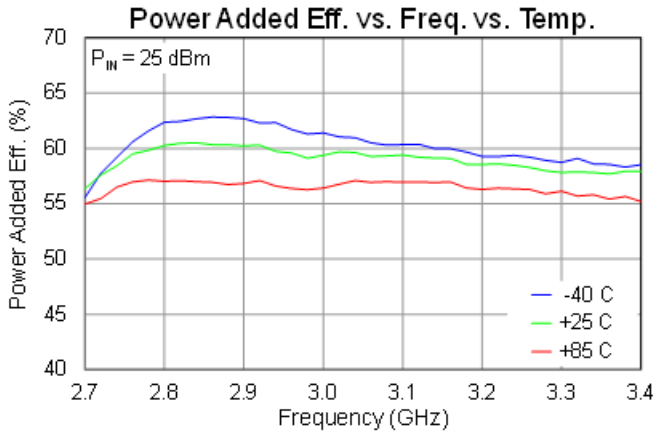
Parameter	Min	Typ	Max	Units
Operational Frequency Range	2.8	3.0	3.2	GHz
Output Power (P_{IN} = 25 dBm)	46	47		dBm
PAE (P_{IN} = 25 dBm)	50	58		%
Small Signal Gain		25		dB
Input Return Loss		11		dB
Output Return Loss		13		dB
2nd Harmonic		−27		dBc
3rd Harmonic		−43		dBc
Output Power Temperature Coefficient		−0.004		dBm/°C
Recommended Operating Drain Voltage			25	V

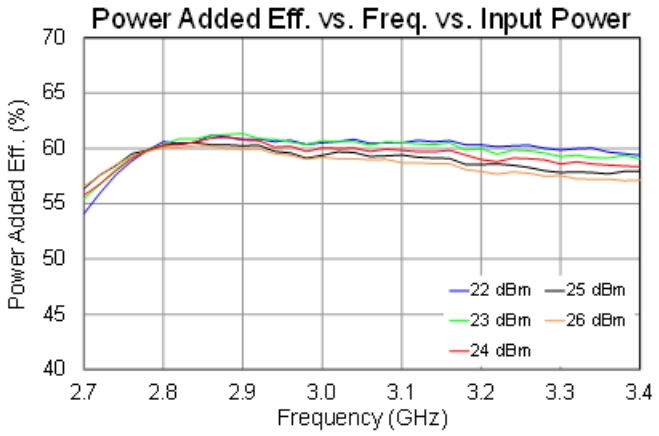
Performance Plots – Large Signal (Pulsed)

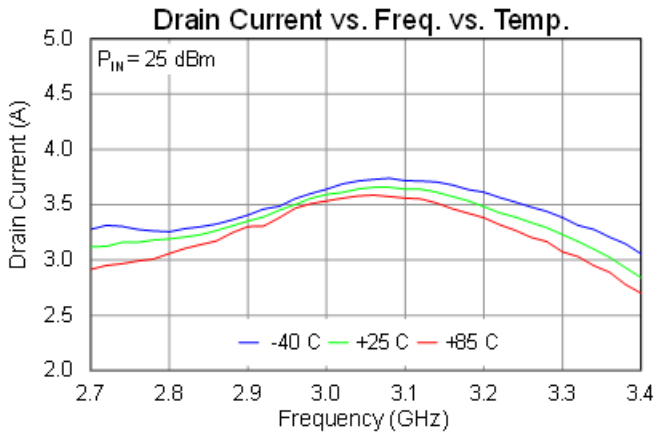
Test conditions unless otherwise noted: Temp. = 25 °C, V_D = 25 V, I_{DQ} = 200 mA, PW = 100 us, Duty Cycle = 10%

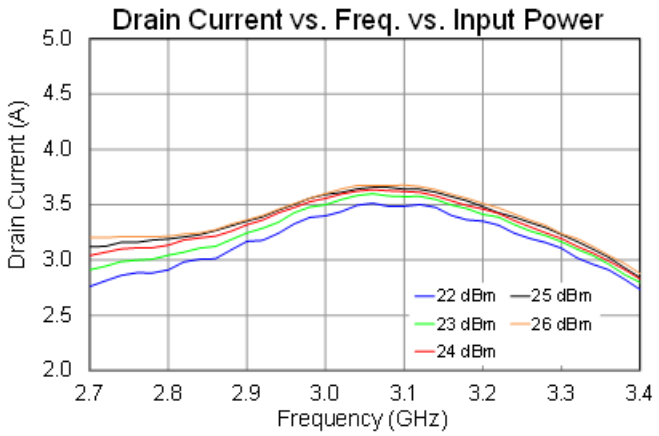






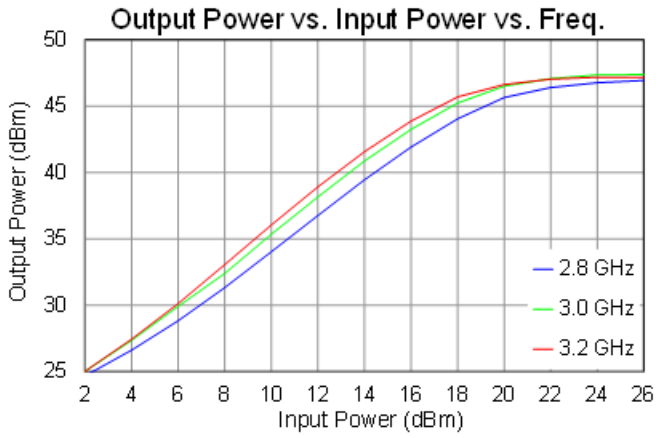


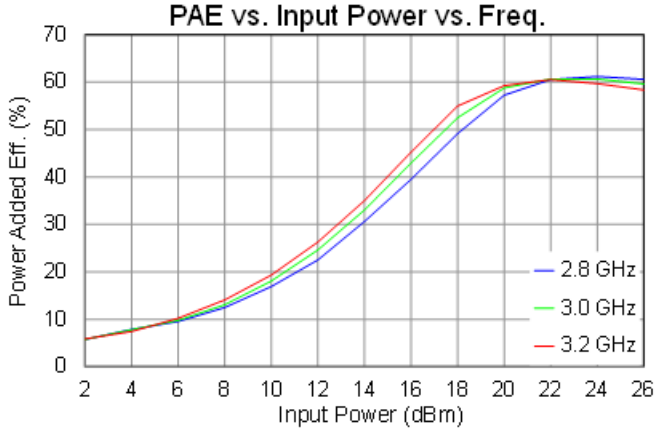


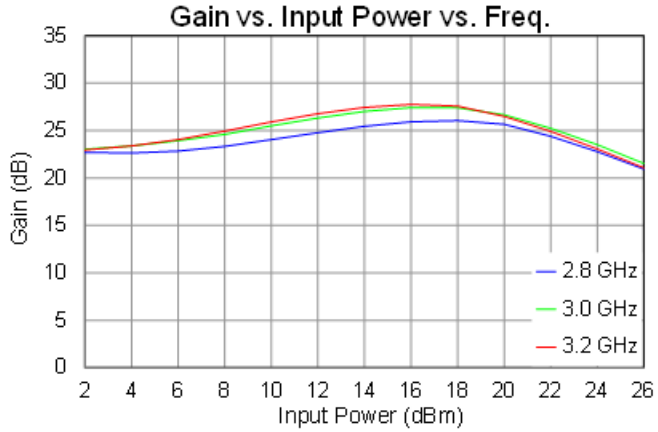


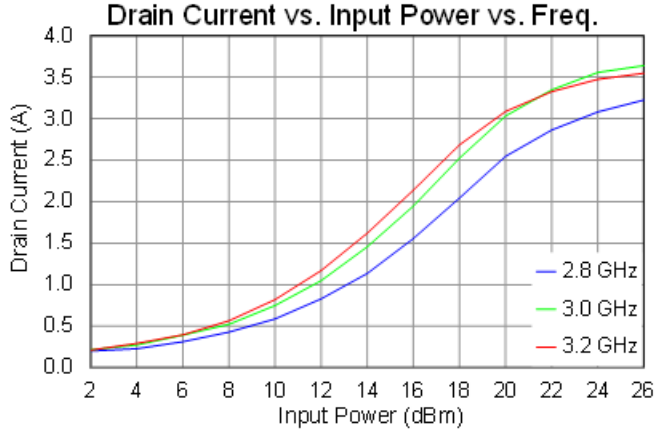
Performance Plots – Large Signal (Pulsed)

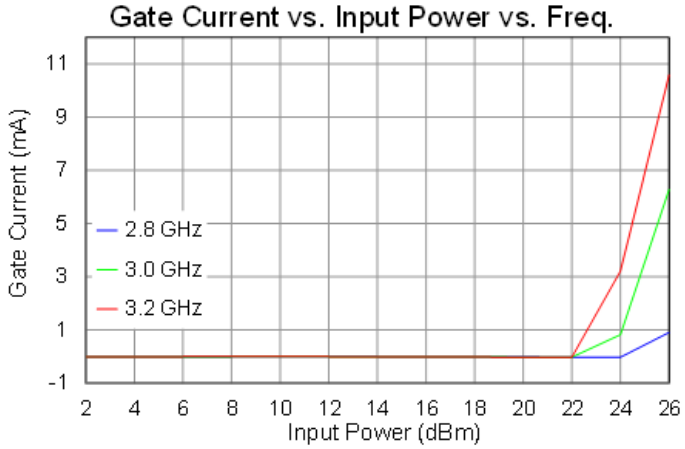
Test conditions unless otherwise noted: Temp. = 25 °C, V_D = 25 V, I_{DQ} = 200 mA, PW = 100 us, Duty Cycle = 10%





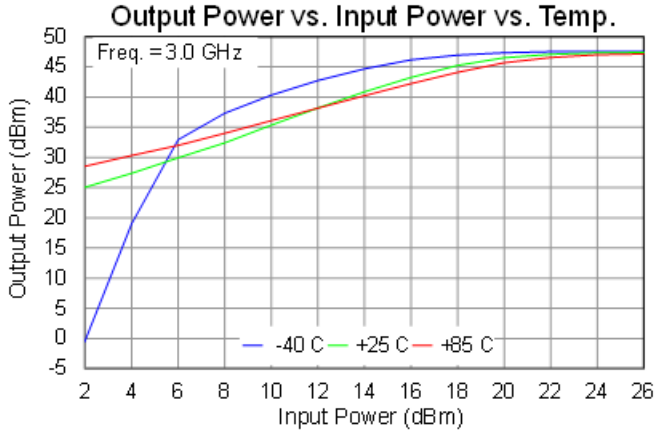


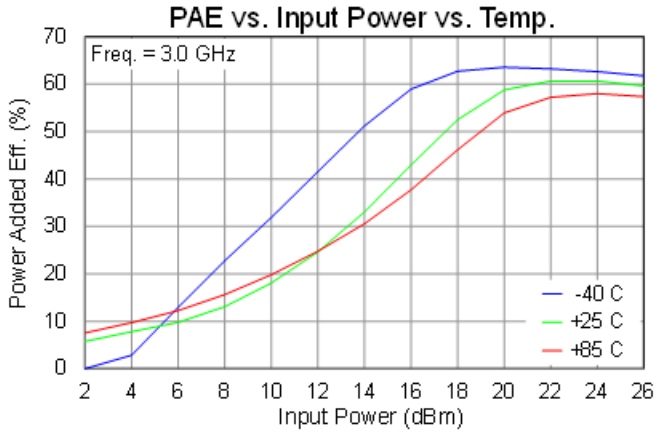


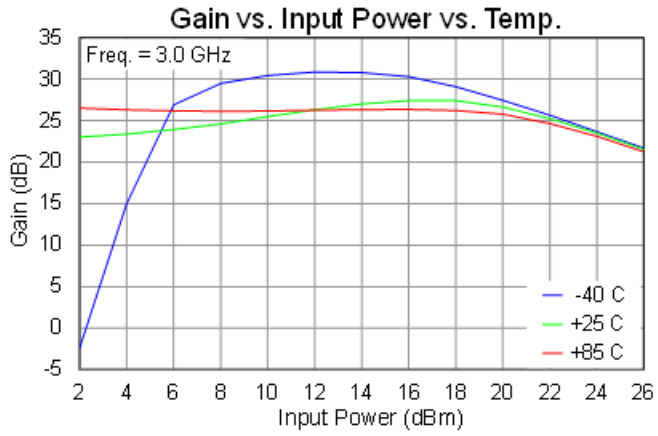


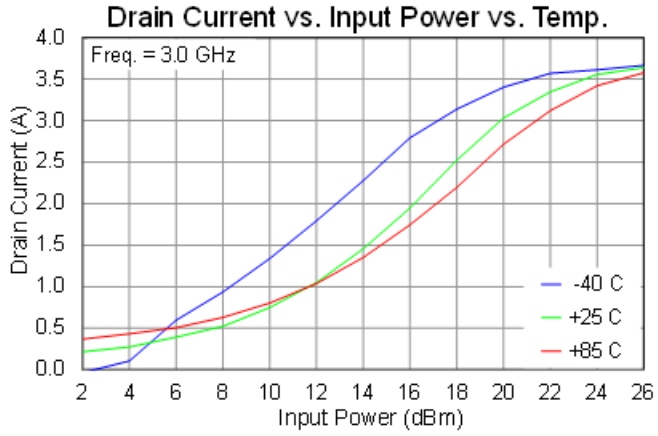
Performance Plots – Large Signal (Pulsed)

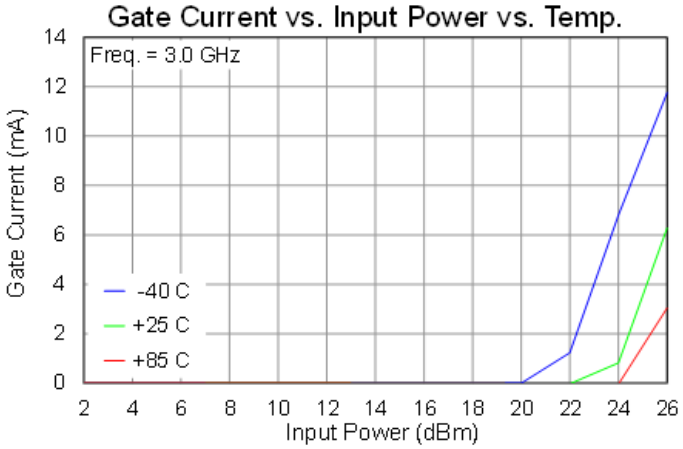
Test conditions unless otherwise noted: Temp. = 25 °C, V_D = 25 V, I_{DQ} = 200 mA, PW = 100 us, Duty Cycle = 10%





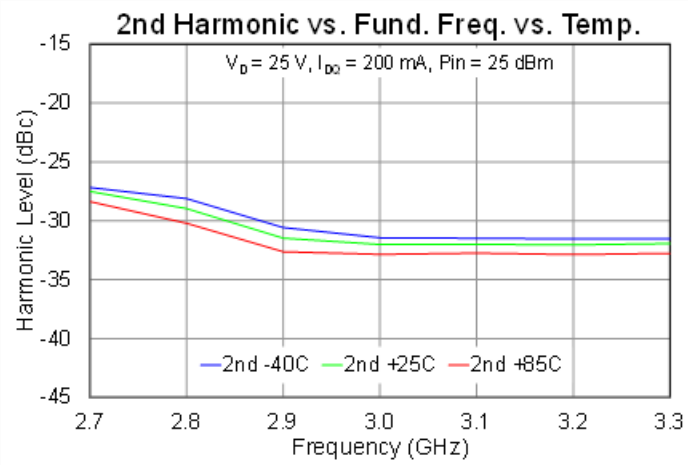


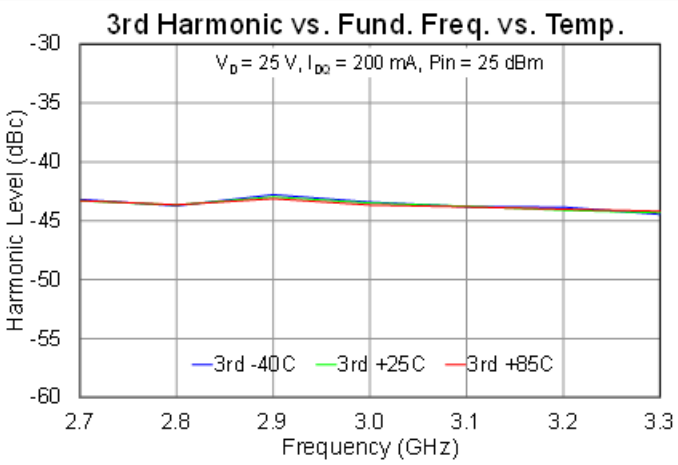


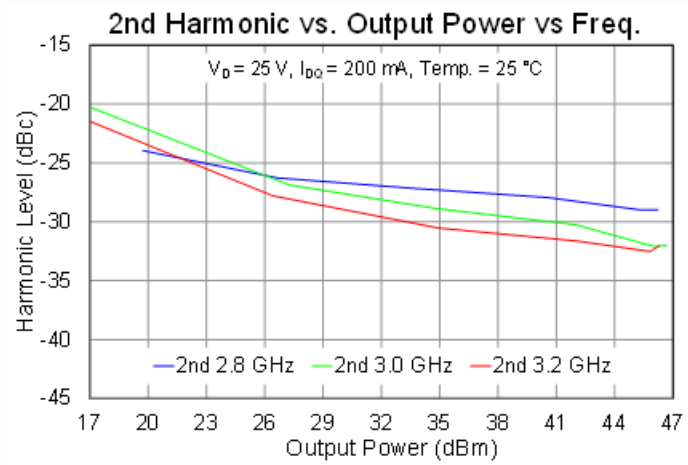


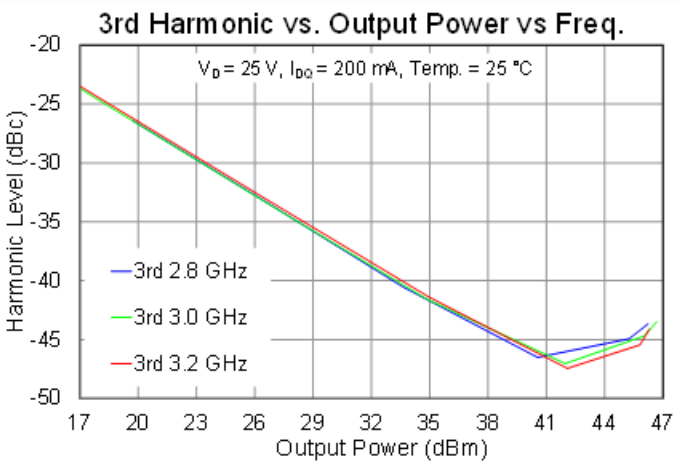
Performance Plots – Harmonics

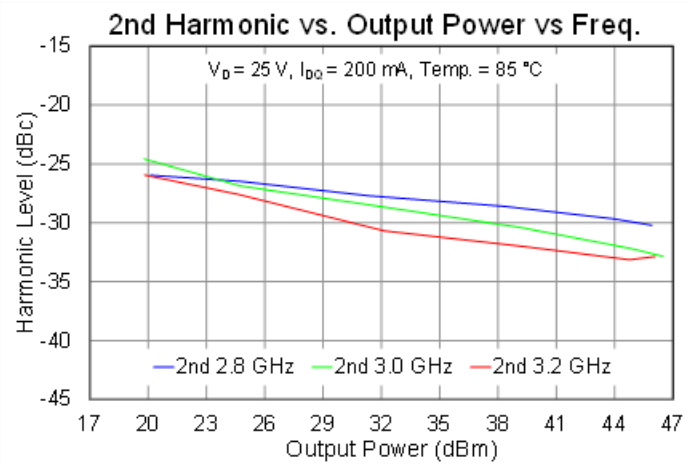
Test conditions unless otherwise noted: Temp. = 25 °C, V_D = 25 V, I_{DQ} = 200 mA, PW = 100 us, Duty Cycle = 10%

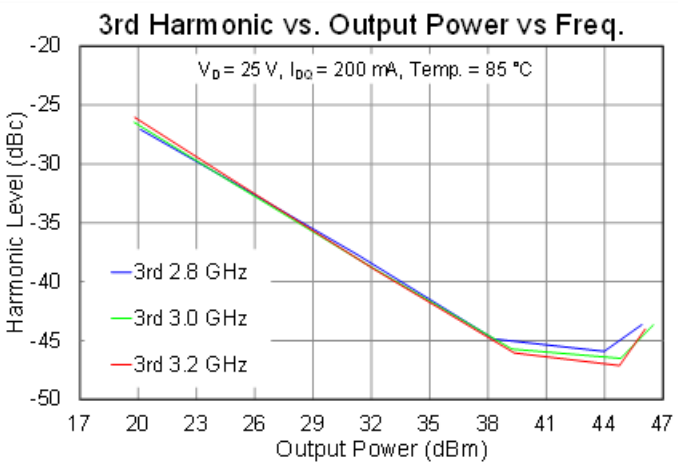








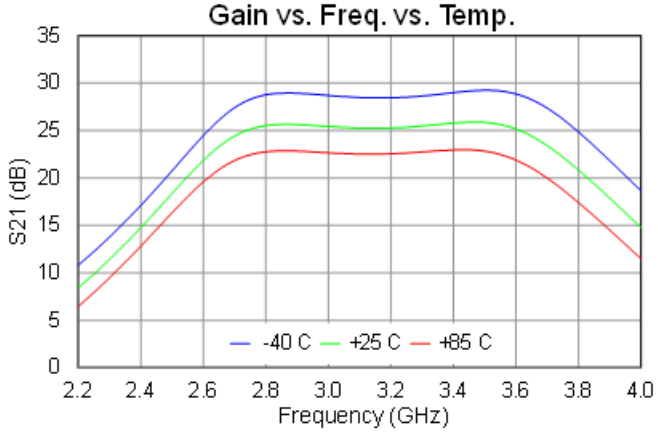




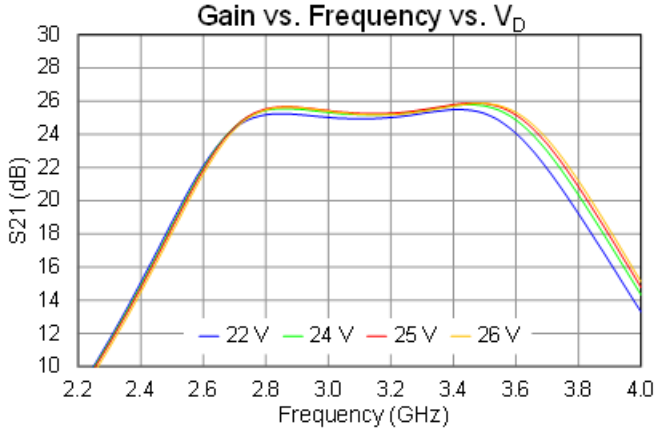
Performance Plots – Small Signal

Test conditions unless otherwise noted: Temp. = 25 °C, V_D = 25 V, I_{DQ} = 200 mA

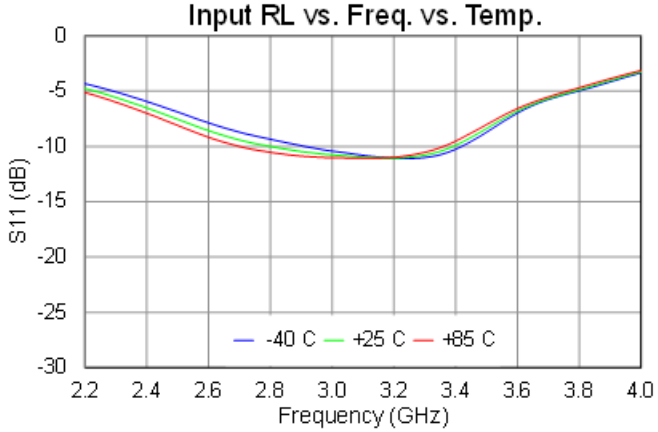
Gain vs. Freq. vs. Temp.



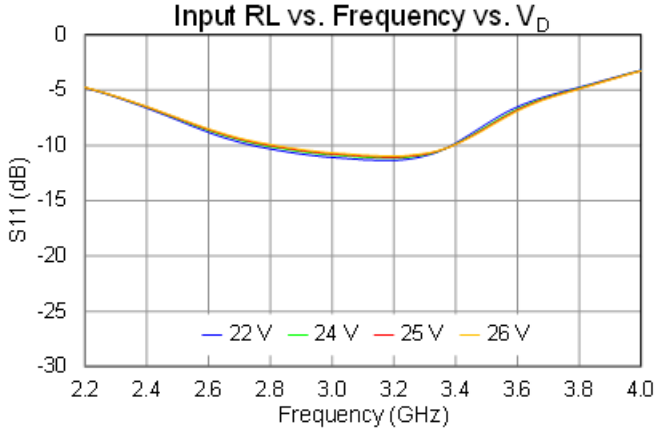
Gain vs. Frequency vs. V_D



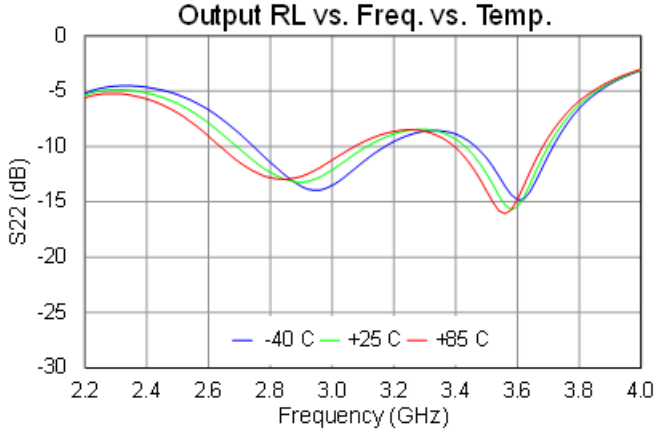
Input RL vs. Freq. vs. Temp.



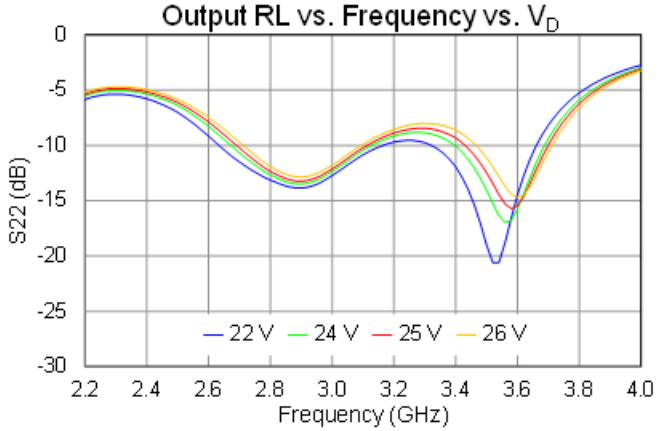
Input RL vs. Frequency vs. V_D



Output RL vs. Freq. vs. Temp.

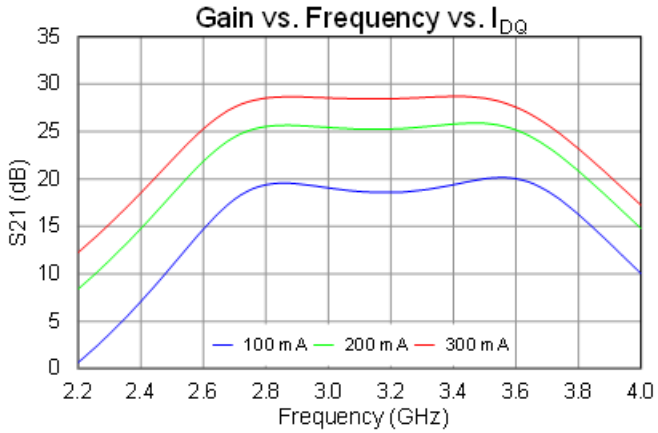


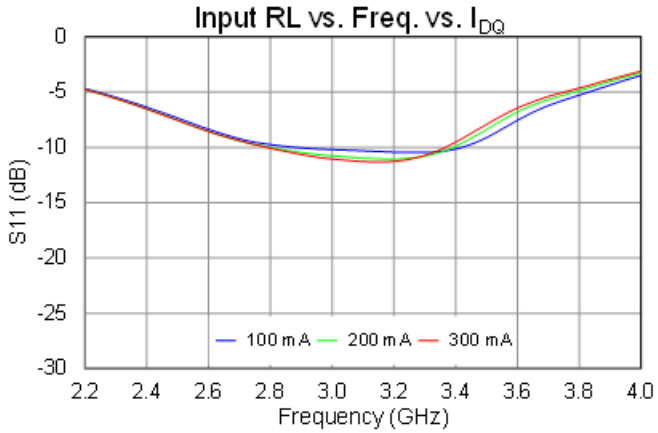
Output RL vs. Frequency vs. V_D

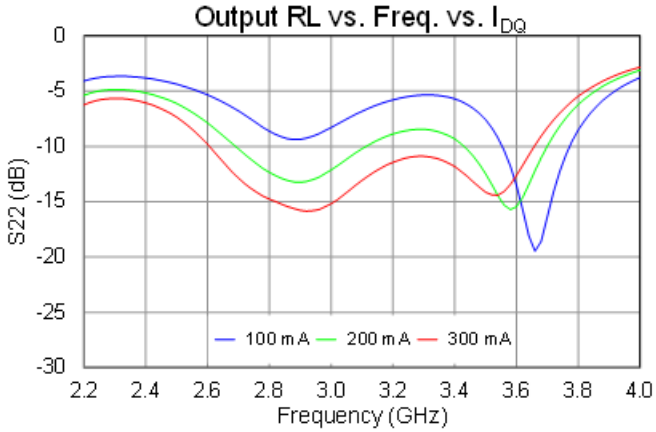


Performance Plots – Small Signal

Test conditions unless otherwise noted: Temp. = 25 °C, V_D = 25 V, I_{DQ} = 200 mA





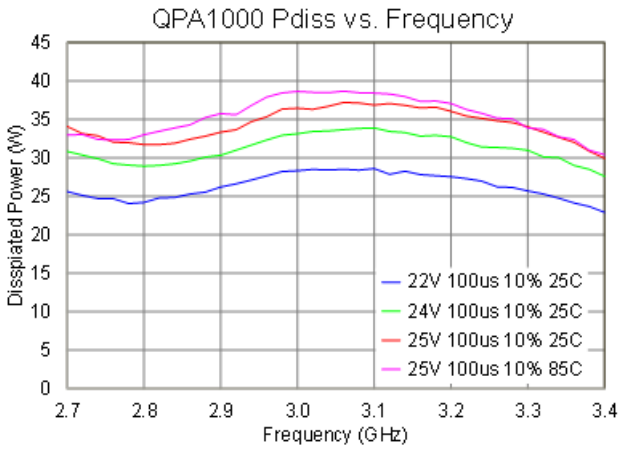


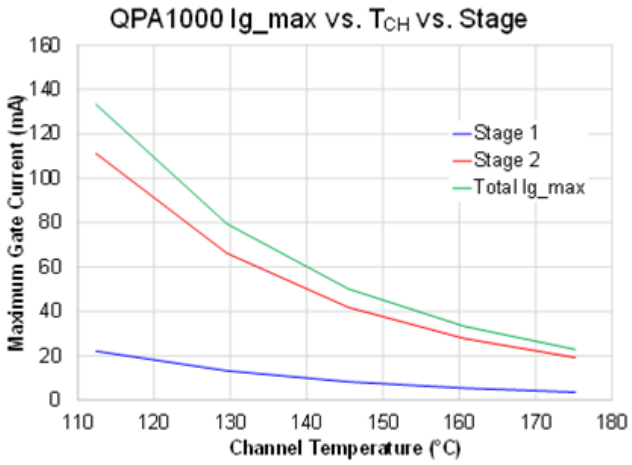
Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	T_{base} = 85°C V_D = 25 V, I_{DQ} = 200 mA P_{DISS} = 5.0 W	0.6	°C/W
Channel Temperature (T_{CH}) (Quiescent)		88	°C
Thermal Resistance (θ_{JC}) (1)	T_{base} = 85°C, V_D = 25 V, I_{DQ} = 200 mA, Freq = 2.8 GHz, I_{D_Drive} = 3.6 A, P_{IN} = 26 dBm, P_{OUT} = 46.6 dBm, P_{DISS} = 33.9 W, PW = 100 us, DC = 10%	0.65	°C/W
Channel Temperature (T_{CH}) (Under RF drive)		107	°C
Thermal Resistance (θ_{JC}) (1)	T_{base} = 85°C, V_D = 25 V, I_{DQ} = 200 mA, Freq = 3.1 GHz, I_{D_Drive} = 3.8 A, P_{IN} = 26 dBm, P_{OUT} = 47.1 dBm, P_{DISS} = 39.4 W, PW = 100 us, DC = 10%	0.66	°C/W
Channel Temperature (T_{CH}) (Under RF drive)		111	°C

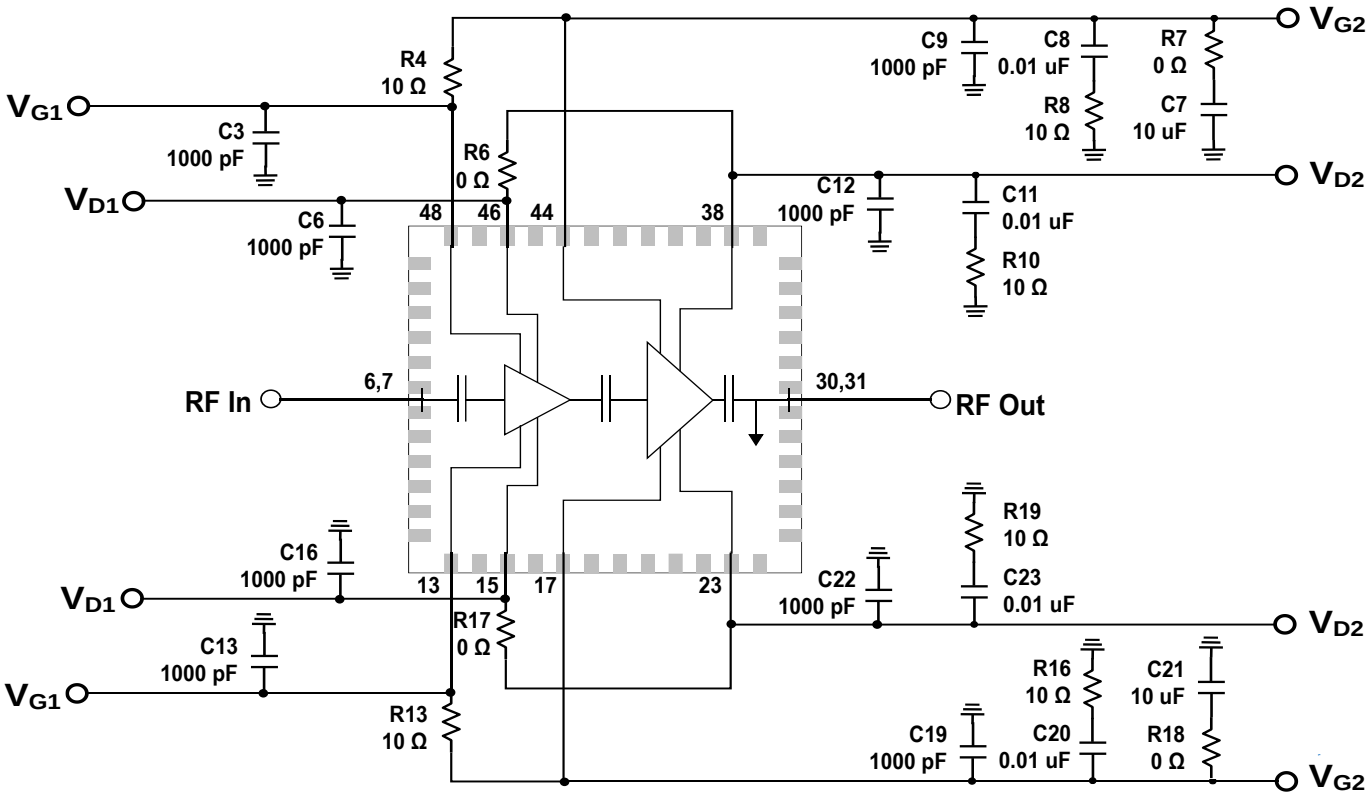
Notes:
1. Thermal resistance measured to back of package.
2. Refer to the following document: GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates

Power Dissipation and Maximum Gate Current





Applications Circuit



Notes:

1. V_G and V_D must be biased from both sides (top and bottom).

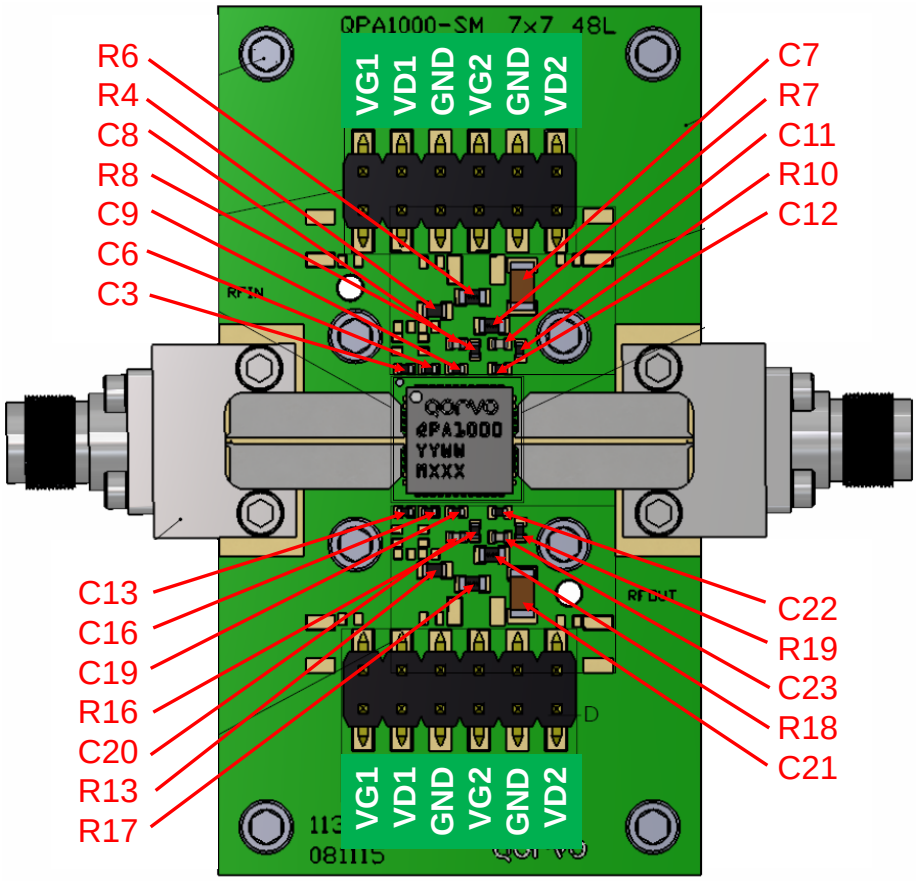
Bias Up Procedure

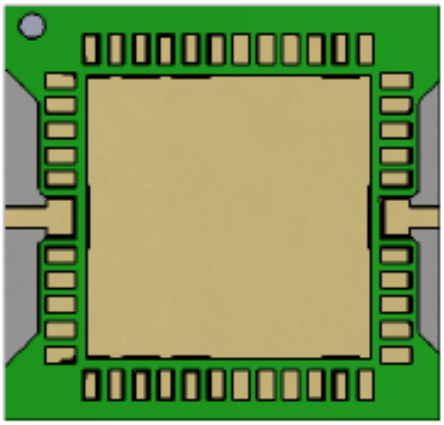
1. Set I_D limit to 6000 mA, I_G limit to 40 mA
2. Set V_G to −6.0 V
3. Set V_D +25 V
4. Adjust V_G more positive until I_{DQ} = 200 mA
5. Apply RF signal

Bias Down Procedure

1. Turn off RF supply
2. Reduce V_G to −6.0 V. Ensure I_{DQ} ~ 0 mA
3. Set V_D to 0 V
4. Turn off V_D supply
5. Turn off V_G supply

Evaluation Board and Mounting Detail





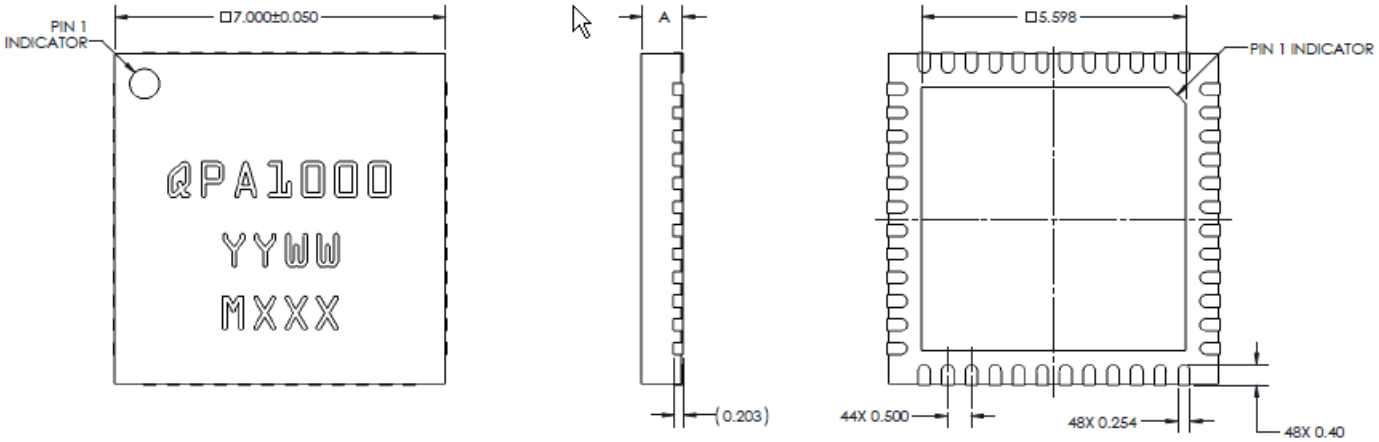
Mounting Detail

RF Layer is 0.008” thick Rogers Corp. RO40003C (εr = 3.35). Metal layers are 0.5 oz. copper. The microstrip line at the connector interface is optimized for the Southwest Microwave end launch connector 1092-02A-5.

Bill of Materials

Ref. Des.	Component	Value	Manuf.	Part Number
C7, C21	Surface Mount Cap.	CAP, 1206, 10uF, 20%, 50V, 20%, X5R	Various	
C3, C6, C9, C12, C13, C16, C19, C22	Surface Mount Cap.	CAP, 0402, 1000pF, 10%, 100V, X7R	Various	
C8, C11, C20, C23	Surface Mount Cap.	CAP, 0402, 0.01uF, ±10%, 50V, X7R	Various	
R8, R10, R16, R19	Surface Mount Res.	RES, 10 OHM ± 5% 0402	Various	
R4, R13	Surface Mount Res.	RES, 10 OHM 1/10W ± 5% 0603	Various	
R6, R7, R16, R18	Surface Mount Res.	RES, 0 OHM 5% 0603	Various	

Mechanical Information



		QFN
A	MAX.	0.900
	NOM.	0.850
	MIN.	0.800

NOTES:
PACKAGE METAL BASE AND LEADS ARE GOLD PLATED.

PART MARKING:
QPA1000: PART NUMBER
YY: PART ASSY YEAR
WW: PART ASSY WEEK
MXXX: LOT NUMBER

DIMENSIONS IN MM

Pin Description

Pin Number	Symbol	Description
1-5, 8-12, 14, 16, 18-22, 24-29, 32-37, 39-43, 45, 47	NC	No connection. Can be grounded on PCB if desired.
6, 7	RF Input	50 Ohm RF input. Pad is capacitively coupled to block on-chip DC voltages.
13, 48	V_{G1}	1st Stage Gate Voltage; bias network is required; must be biased from both sides (V_{G1} and V_{G2} can be tied together in application)
15, 46	V_{D1}	1st Stage Drain Voltage; bias network is required; must be biased from both sides (V_{D1} and V_{D2} can be tied together in application)
17, 44	V_{G2}	2nd Stage Gate Voltage; bias network is required; must be biased from both sides (V_{G1} and V_{G2} can be tied together in application)
23, 38	V_{D2}	2nd Stage Drain Voltage; bias network is required; must be biased from both sides (V_{D1} and V_{D2} can be tied together in application)
30, 31	RF Output	50 Ohm RF output. Pad is capacitively coupled to block on-chip DC voltages. Pad is DC grounded.
49	GND	Ground connection.

Recommended Soldering Temperature Profile