QPA1010

7.9 – 11.0 GHz 15 W GaN Power Amplifier

Product Description

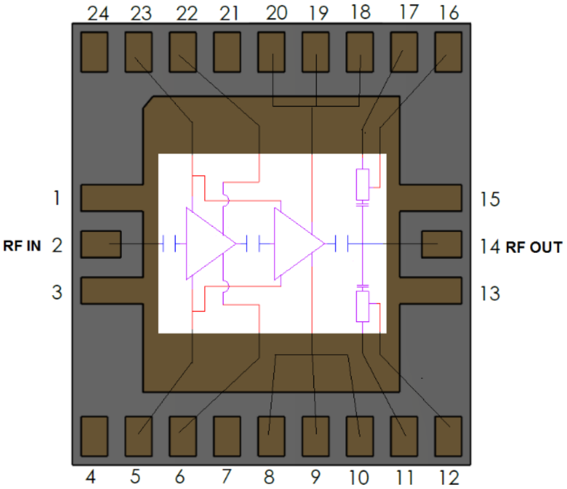
Qorvo's QPA1010 is a X-band high power MMIC amplifier fabricated on Qorvo's production 0.15um GaN on SiC process (QGaN15). The QPA1010 operates from 7.9 – 11 GHz and typically provides 15 W saturated output power with power-added efficiency of 38% and large-signal gain of 18 dB. This combination of wideband performance provides the flexibility designers are looking for to improve system performance while reducing size and cost.

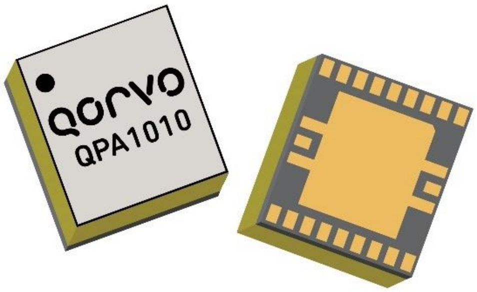
QPA1010 can also support a variety of operating conditions to best support system requirements. With good thermal properties, it can support a range of bias voltages and will perform well under both CW and pulse operations.

The QPA1010 is matched to 50Ω with integrated DC blocking capacitors on both RF I/O ports simplifying system integration. The wideband performance and operational flexibility allow it support satellite communication and data links, as well as, military and commercial radar systems.

Lead-free and RoHS compliant.

Functional Block Diagram





24-Lead 4.5 x 5.0 x 1.72 mm Air Cavity Laminate Package

Product Features

- Frequency Range: 7.9 – 11 GHz
- P_{OUT}: 42 dBm at P_{IN} = 24 dBm
- PAE: 38 % at P_{IN} = 24 dBm
- Large Signal Gain: 18 dB at P_{IN} = 24 dBm
- Small Signal Gain: 25 dB
- Integrated Power Detector
- Bias: V_D = 24 V, I_{DQ} = 600 mA
- Pulsed V_D: PW =100 µS, DC = 10%
- Package Dimensions: 4.5 x 5.0 x 1.72 mm

Performance is typical across frequency. Please reference electrical specification table and data plots for more details.

Applications

- Satellite Communications
- Data Links
- Military and Commercial Radar

Ordering Information

Part No.	Description
QPA1010	7.9 – 11 GHz 15 W GaN Power Amplifier
QPA1010S2	Samples (2 pcs. pack)
QPA1010PCB4B01	Evaluation Board

Absolute Maximum Ratings

Parameter	Value / Range
Drain Voltage (V_D)	29.5 V
Gate Voltage Range (V_G)	−8 to 0V
Drain Current (I_{D1}/I_{D2})	672 mA / 1440 mA
Gate Current (I_G)	See chart, pg. 21
Power Dissipation (P_{DISS}), 85°C, CW	38 W
Input Power (P_{IN}), CW, 50Ω, V_D=28 V, I_{DQ}=600 mA, 85 °C	30 dBm
Input Power (P_{IN}), CW, VSWR 3:1, V_D=28 V, I_{DQ}=600 mA 85 °C	30 dBm
Mounting Temperature (30 seconds)	260 °C
Storage Temperature	−55 to 150 °C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter	Value / Range
Drain Voltage (V_D)	24 V
Drain Current (I_{DQ})	600 mA
Gate Voltage Range (V_G)	-2.9 to -1.5 V
Temperature (T_{BASE})	-40 to +85 °C

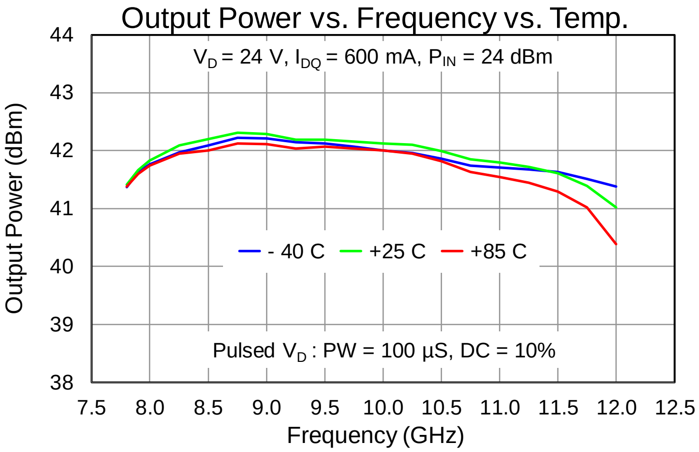
Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

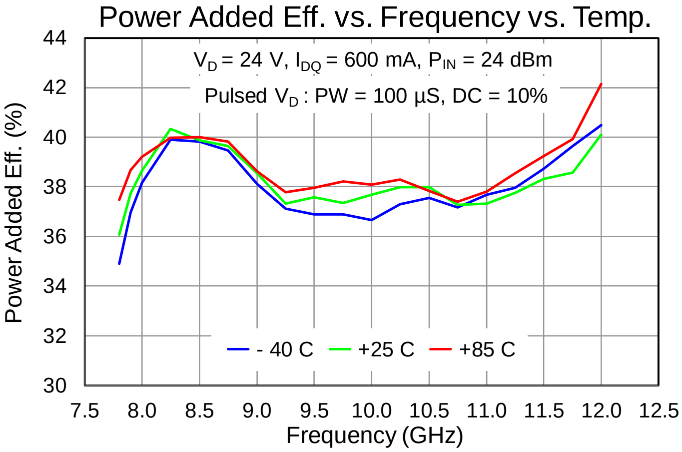
Electrical Specifications

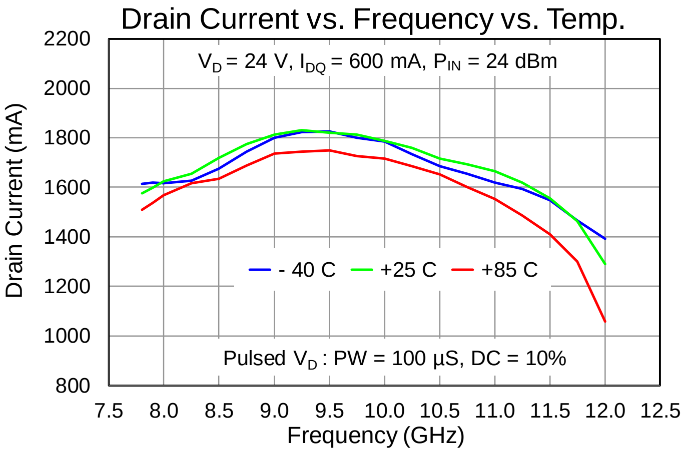
Parameter		Min	Typ	Max	Units
Operational Frequency Range		7.9		11	GHz
Output Power (P_{IN} = 24 dBm)	7.9 GHz		41.7		dBm
	9.0 GHz		42.3		dBm
	11.0 GHz		41.8		dBm
	12.0 GHz		41.0		dBm
Power Added Efficiency (P_{IN} = 24 dBm)	7.9 GHz		37.7		%
	9.0 GHz		38.6		%
	11.0 GHz		37.3		%
	12.0 GHz		40.1		%
3rd Order Intermodulation Level (P_{OUT}/Tone= 35 dBm)	7.9 GHz		−21		dBc dBc dBc
	10.0 GHz		−21		
	11.0 GHz		−22		
	12.0 GHz		−21		
Small Signal Gain	7.9 GHz		27.9		dB
	9.0 GHz		27.8		dB
	11.0 GHz		26.0		dB
	12.0 GHz		21.1		dB
Input Return Loss	7.9 GHz		17		dB
	9.0 GHz		22		dB
	11.0 GHz		21		dB
	12.0 GHz		10		dB
Output Return Loss	7.9 GHz		11		dB
	9.0 GHz		11		dB
	11.0 GHz		18		dB
	12.0 GHz		7		dB
Output Power Temperature Coefficient (25 – 85 °C) (P_{IN} = 24 dBm)			−0.003		dB/°C
Small Signal Gain Temperature Coefficient (25 – 85 °C)			−0.044		dB/°C
Gate Leakage (Vd=10V, Vg=−4.0V, all gates together)		−6.6	−3.0	−0.0001	mA
Recommended Voltage Operations			24	28	V

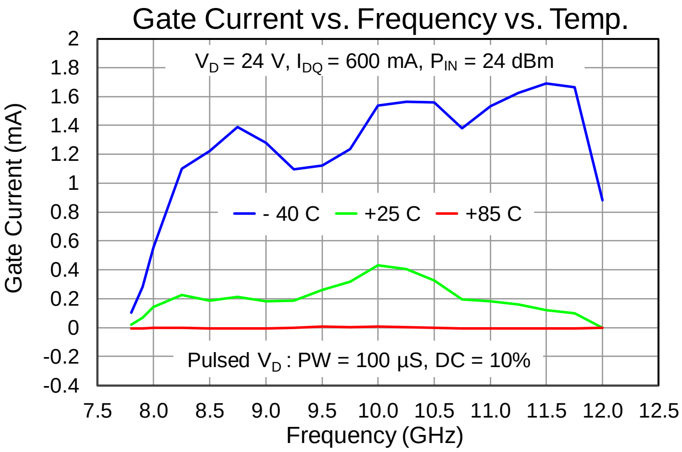
Test conditions, unless otherwise noted: 25 °C, Pulsed V_D: PW = 100 µS, DC = 10%, V_D = 24 V, I_{DQ} = 600 mA, V_G = −1.8 V Typical

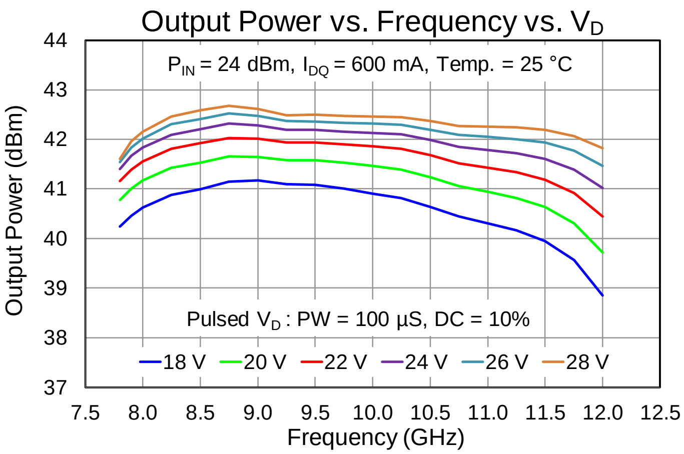
Performance Plots – Large Signal (Pulsed)

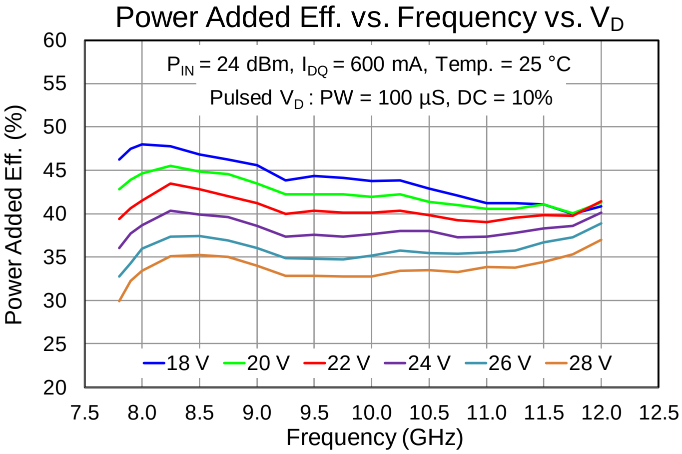

Output Power vs. Frequency vs. Temp.


Power Added Eff. vs. Frequency vs. Temp.

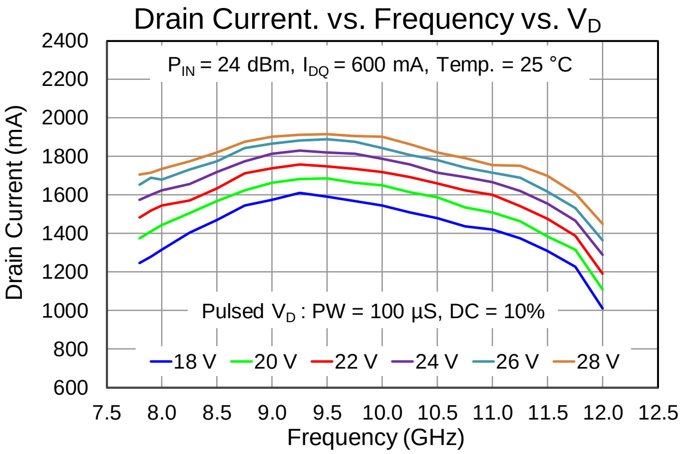

Drain Current vs. Frequency vs. Temp.

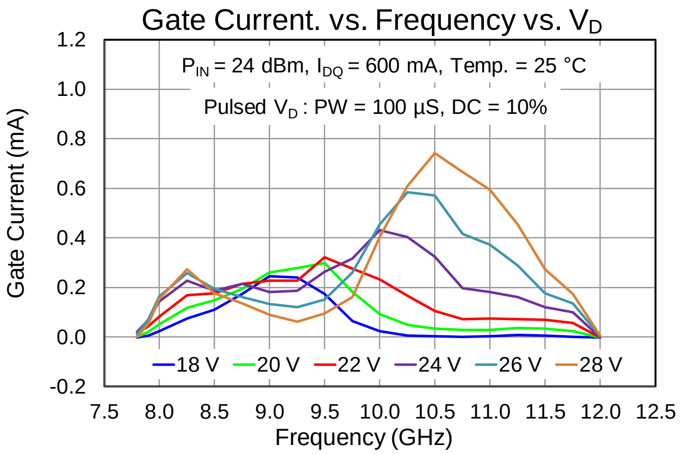

Gate Current vs. Frequency vs. Temp.

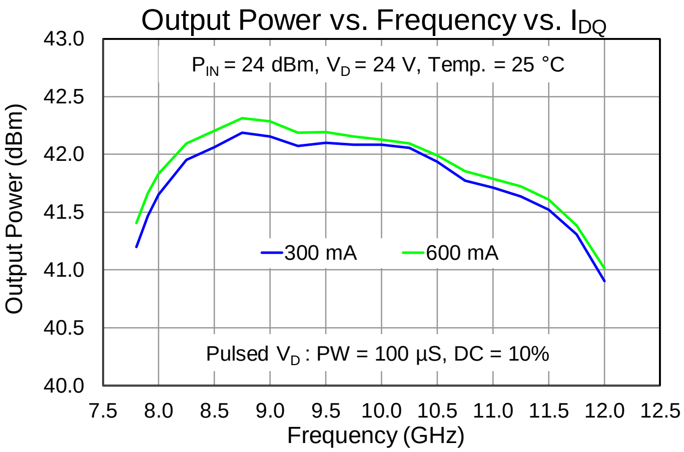

Output Power vs. Frequency vs. V_D

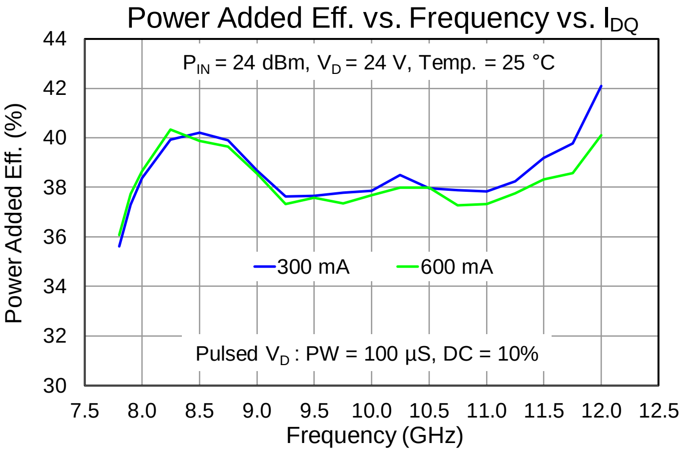

Power Added Eff. vs. Frequency vs. V_D

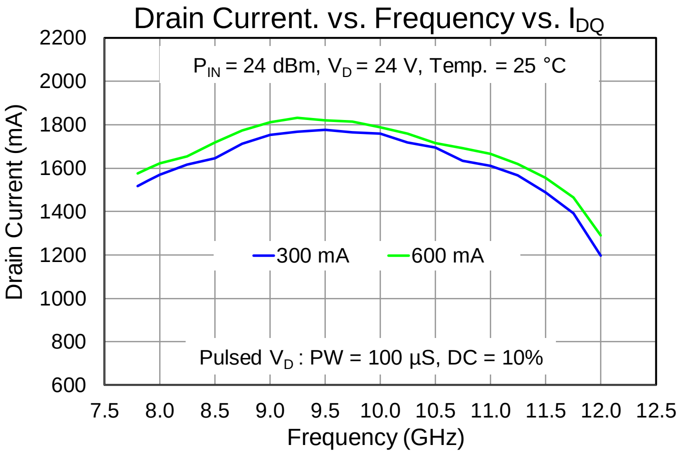
Performance Plots – Large Signal (Pulsed)

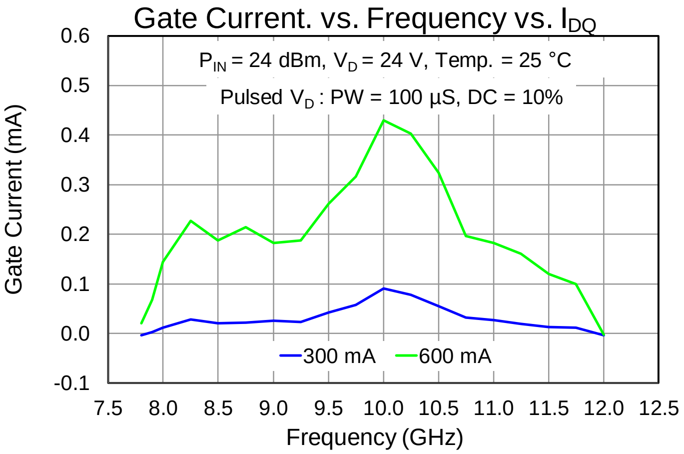






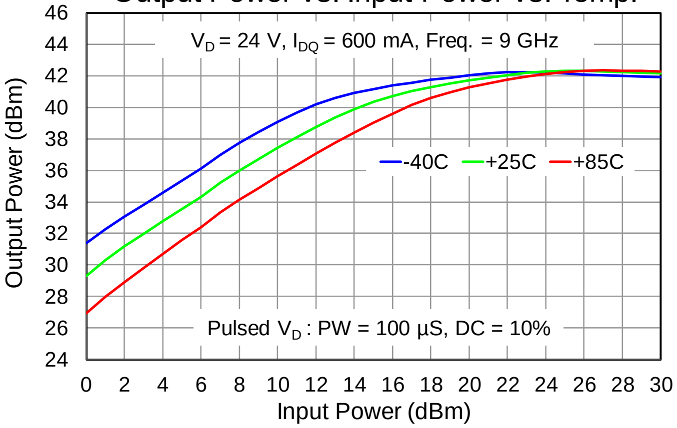




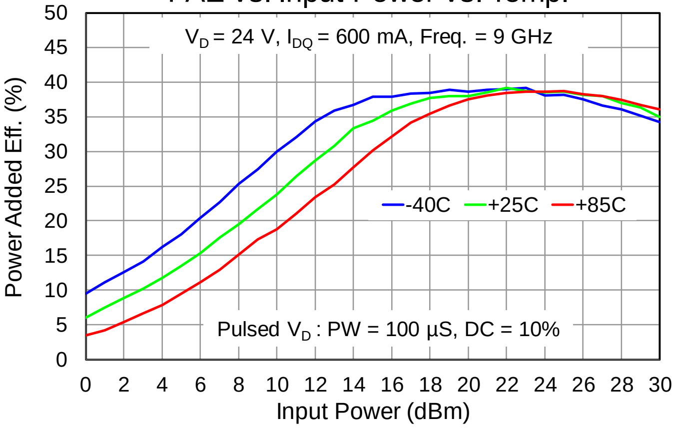


Performance Plots – Large Signal (Pulsed)

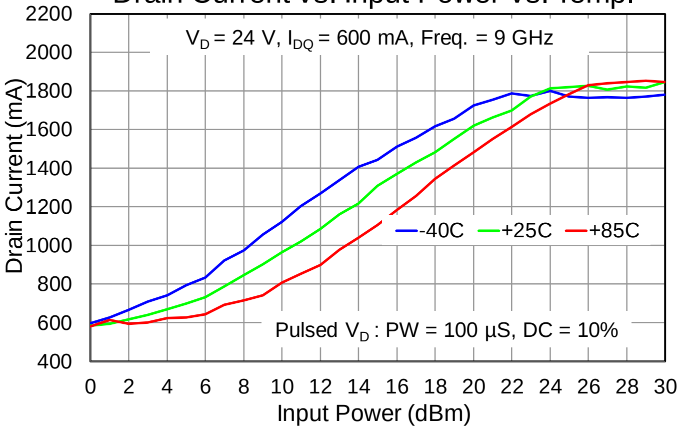
Output Power vs. Input Power vs. Temp.



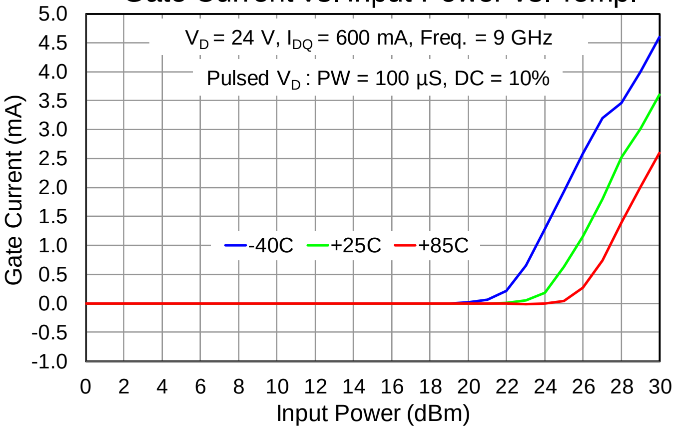
PAE vs. Input Power vs. Temp.



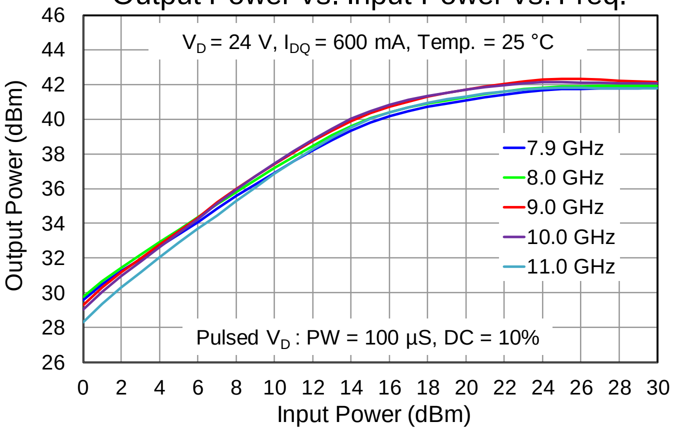
Drain Current vs. Input Power vs. Temp.



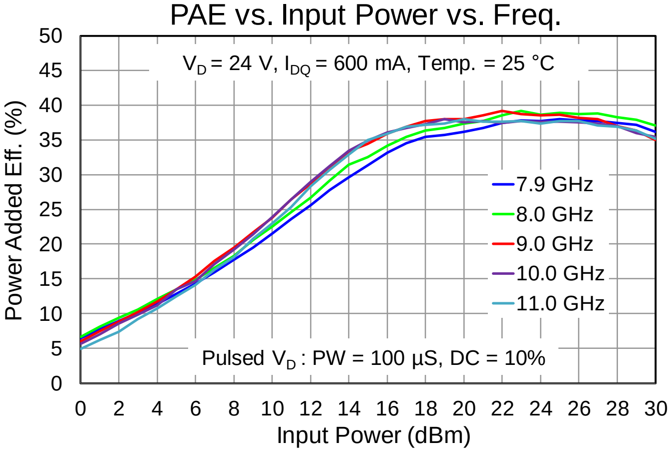
Gate Current vs. Input Power vs. Temp.



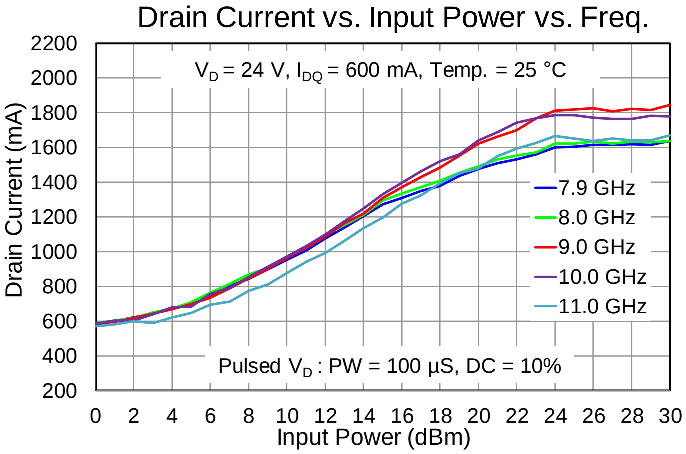
Output Power vs. Input Power vs. Freq.

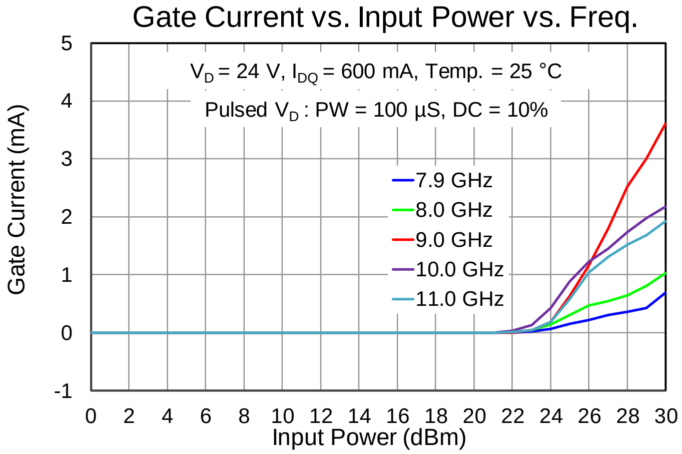


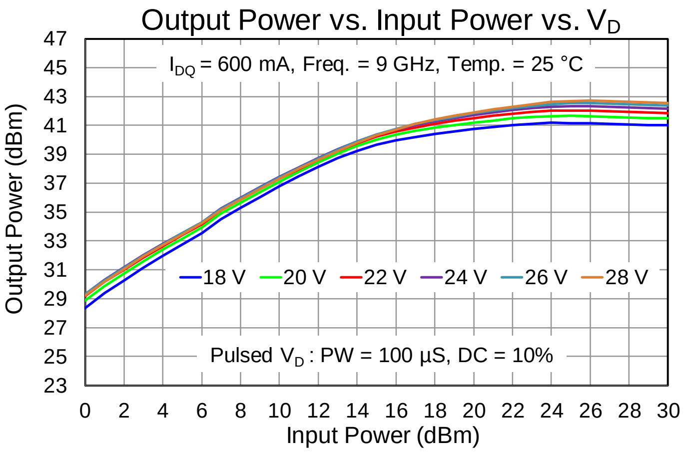
PAE vs. Input Power vs. Freq.

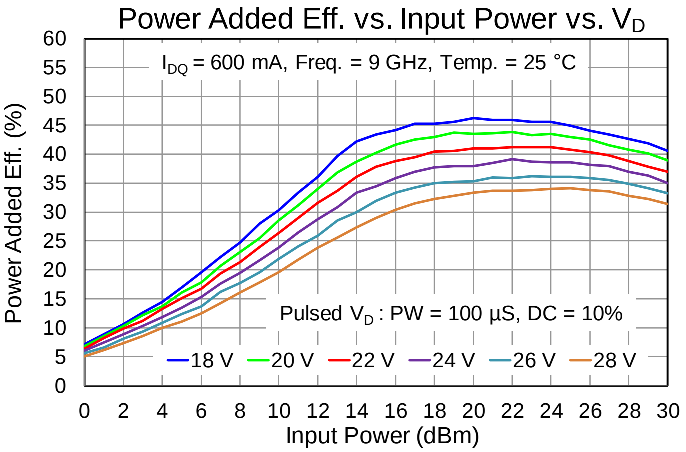


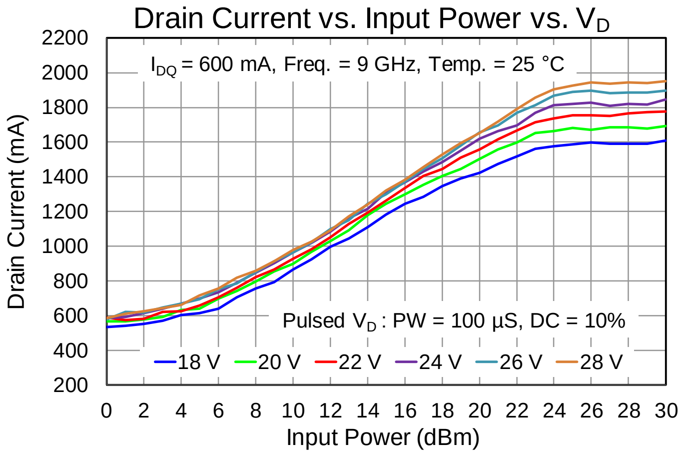
Performance Plots – Large Signal (Pulsed)

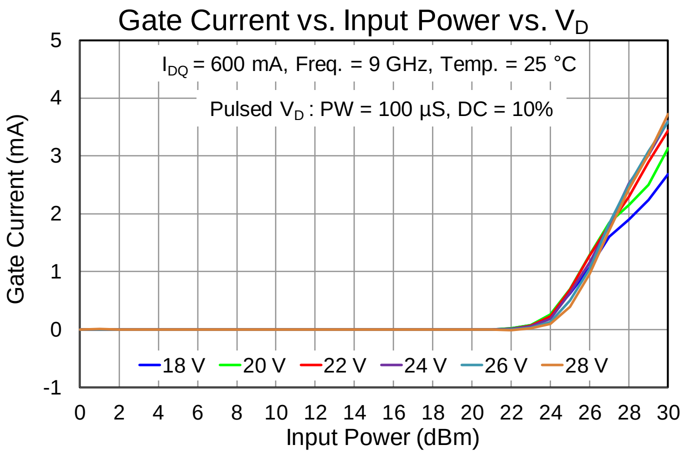




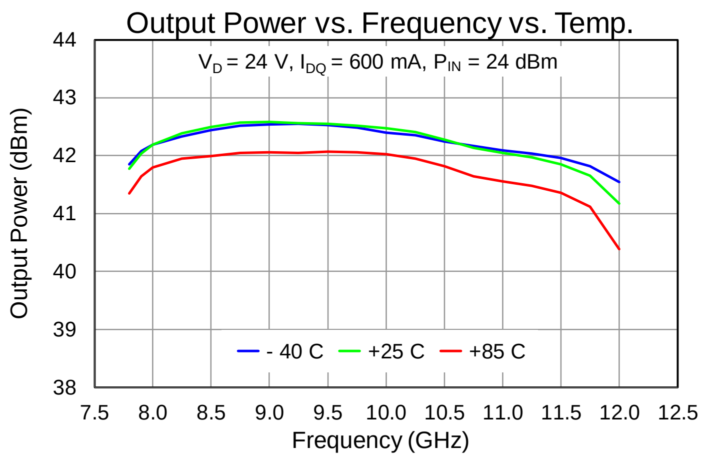


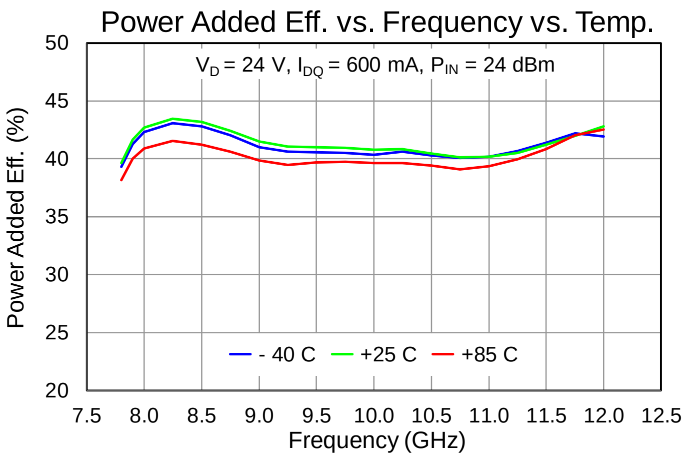


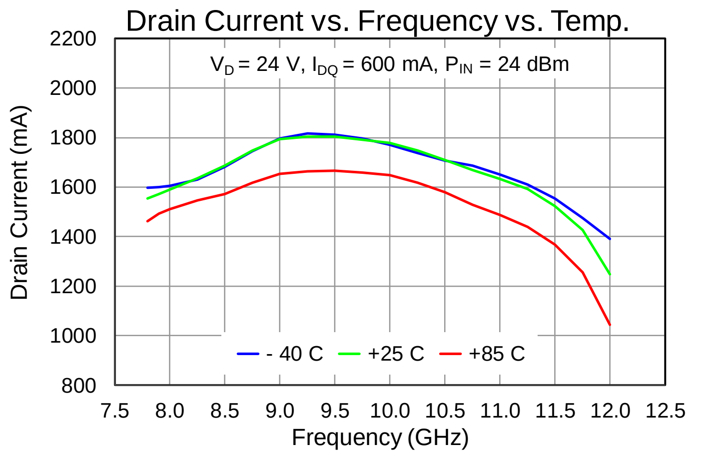


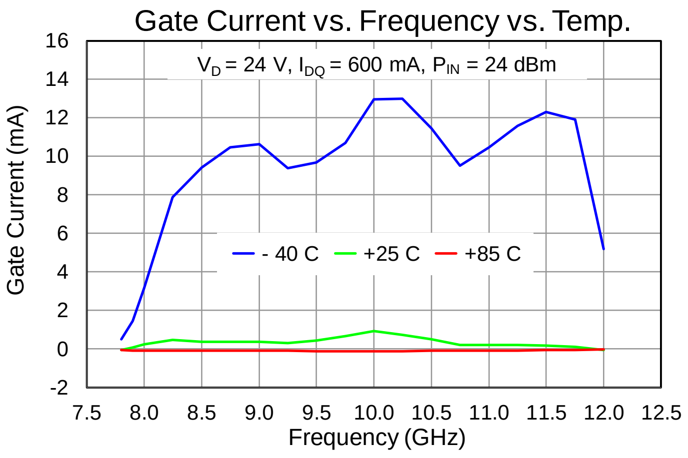


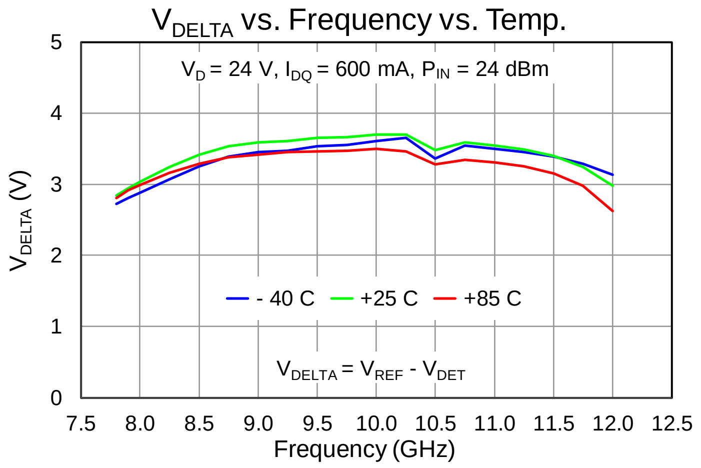
Performance Plots – Large Signal (CW)



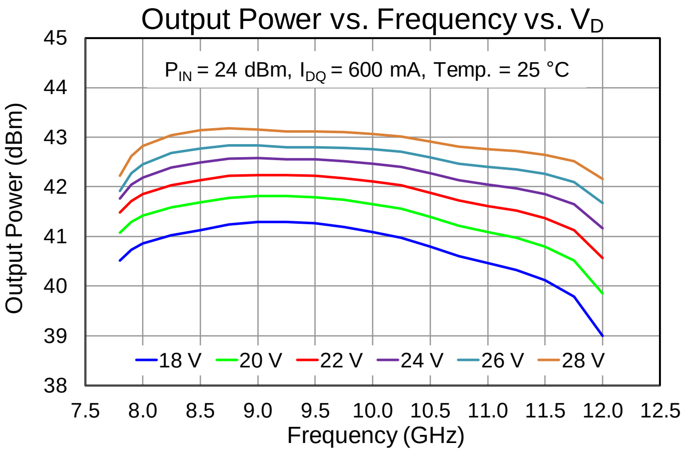


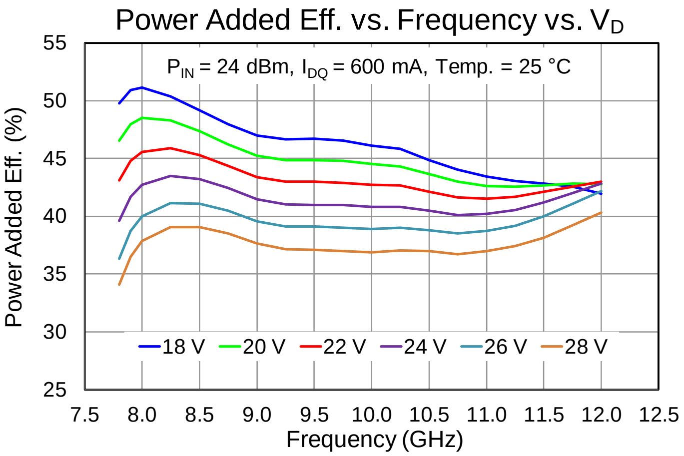


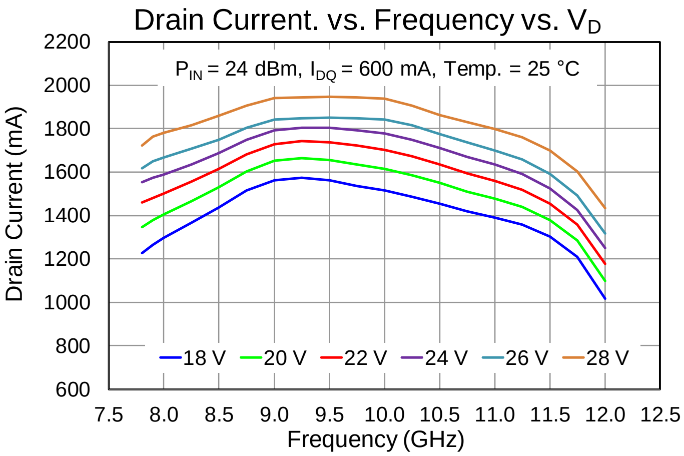


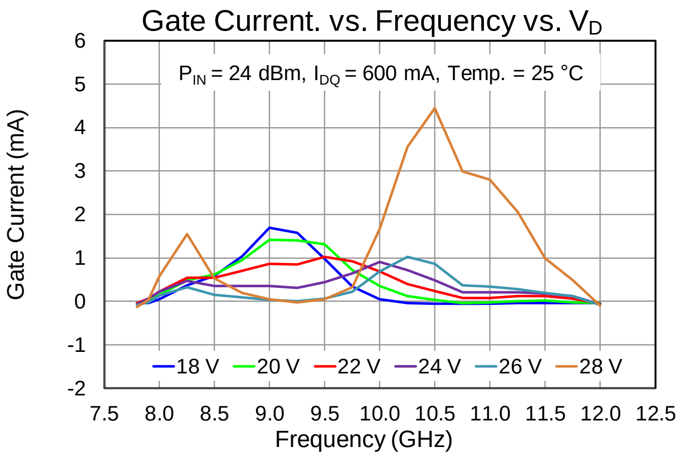


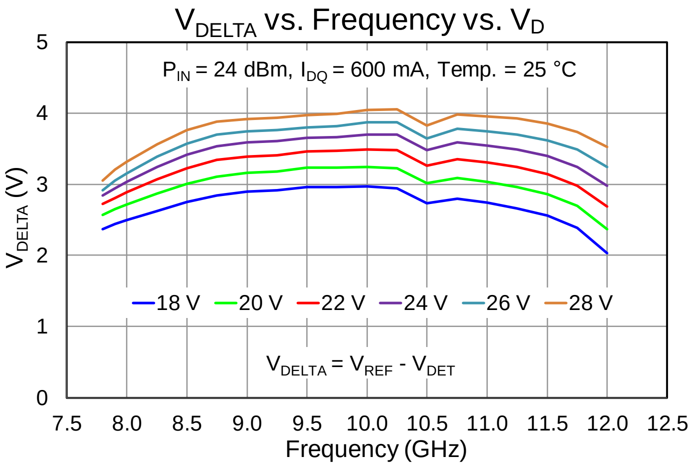
Performance Plots – Large Signal (CW)



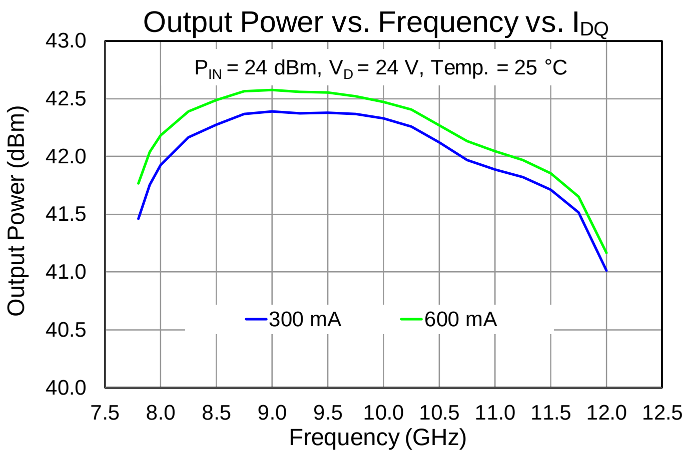


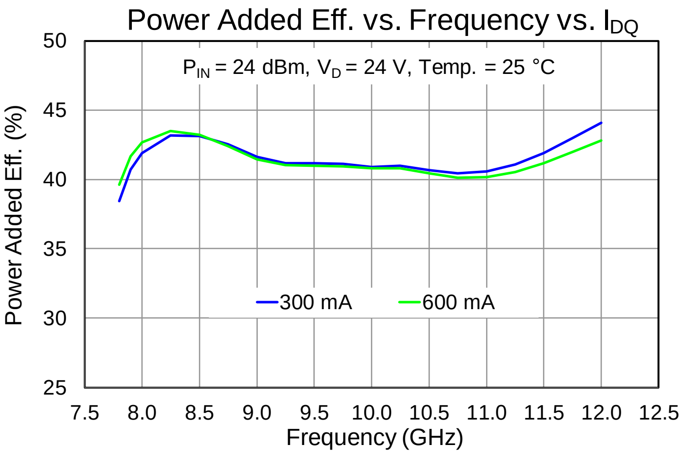


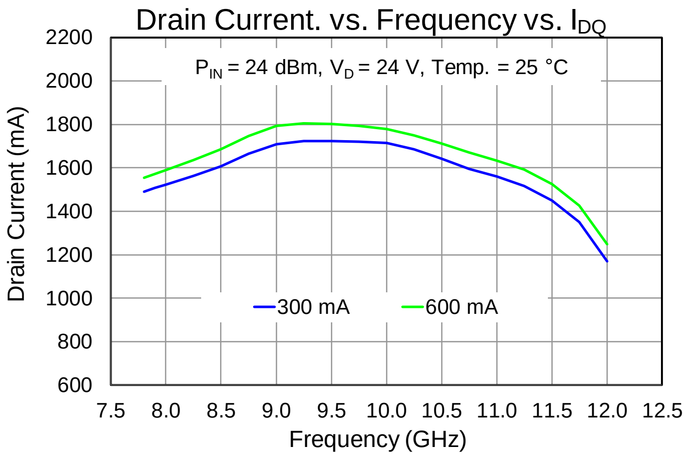


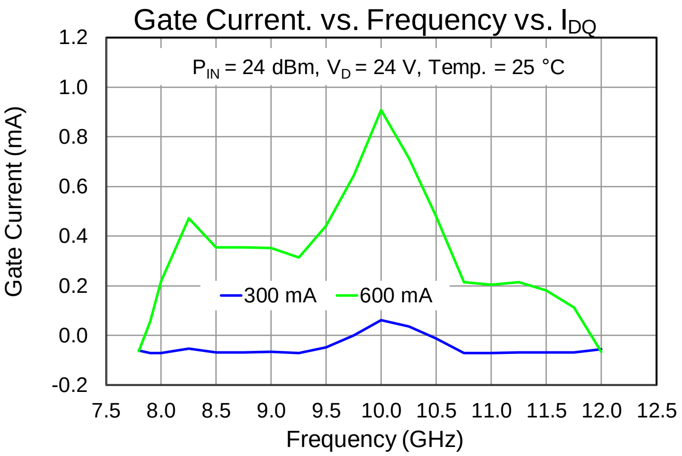


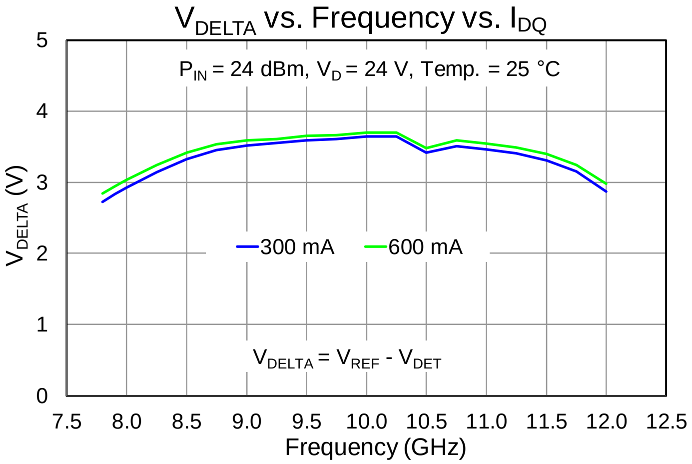
Performance Plots – Large Signal (CW)



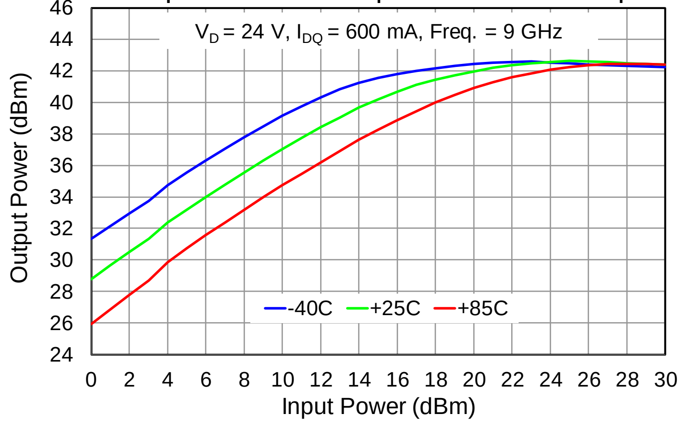


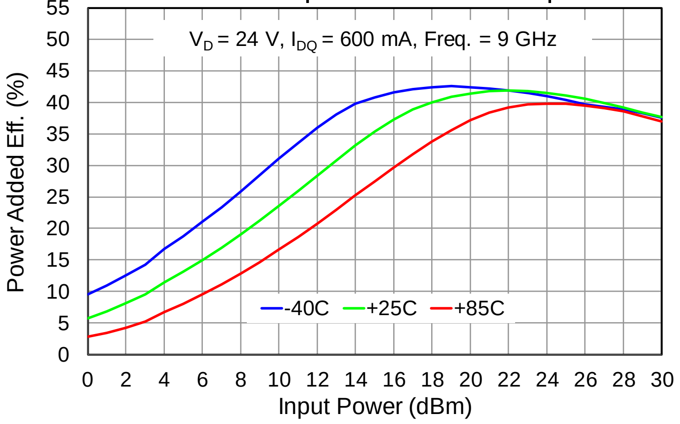


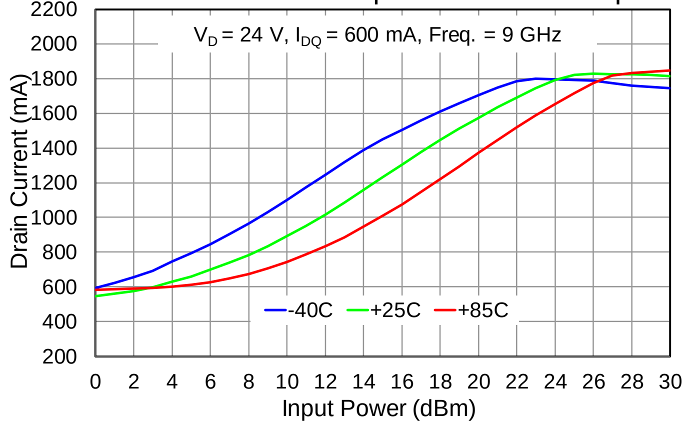


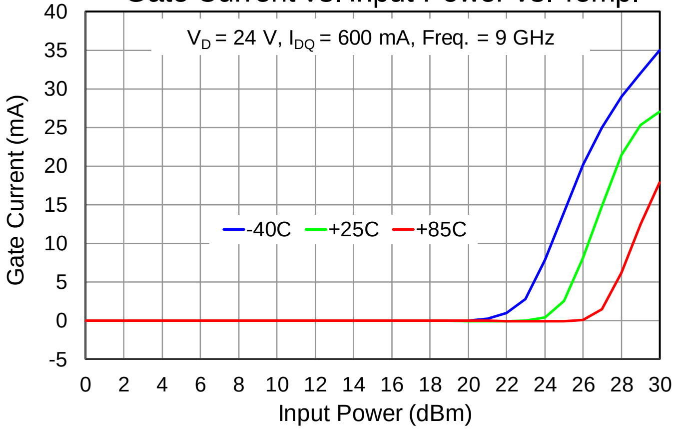


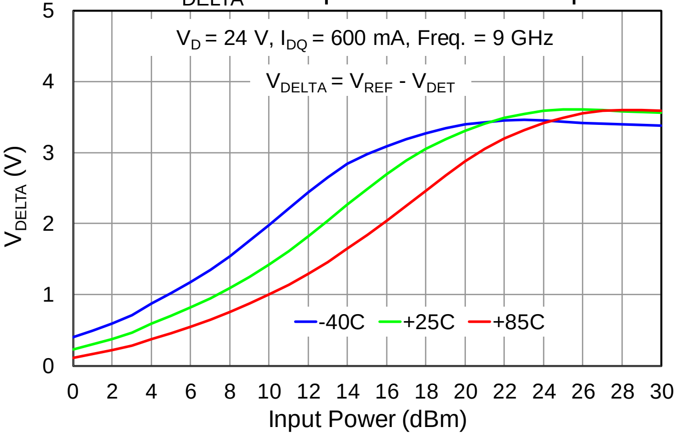
Performance Plots – Large Signal (CW)


Output Power vs. Input Power vs. Temp.

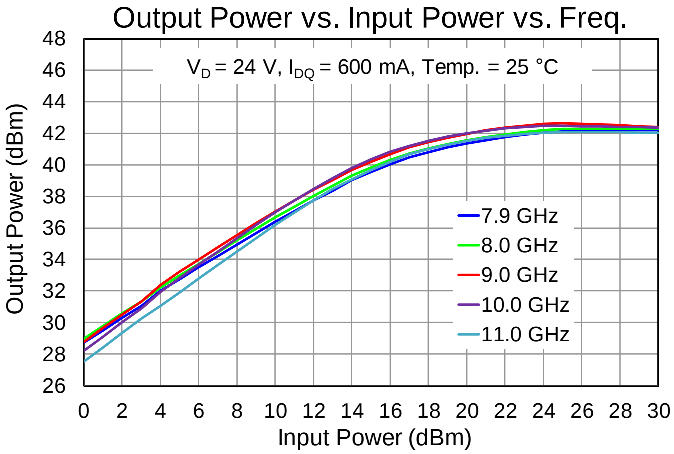

PAE vs. Input Power vs. Temp.

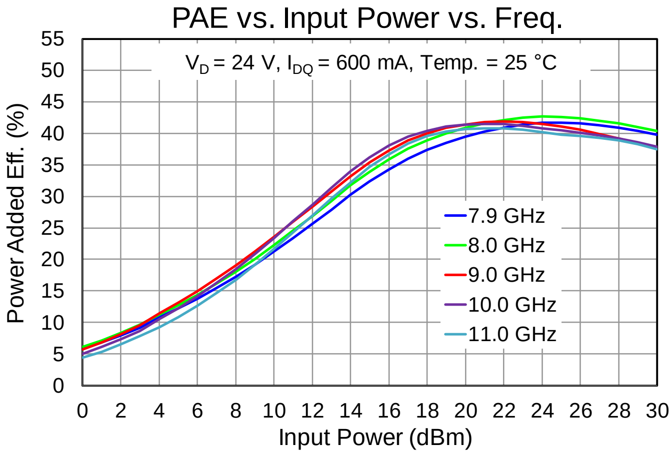

Drain Current vs. Input Power vs. Temp.

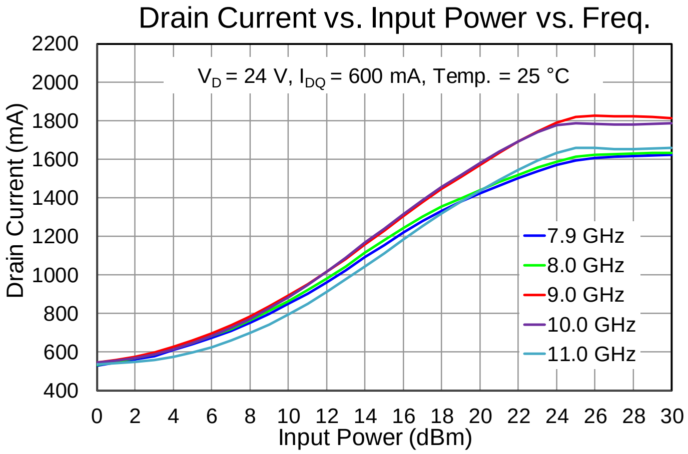

Gate Current vs. Input Power vs. Temp.

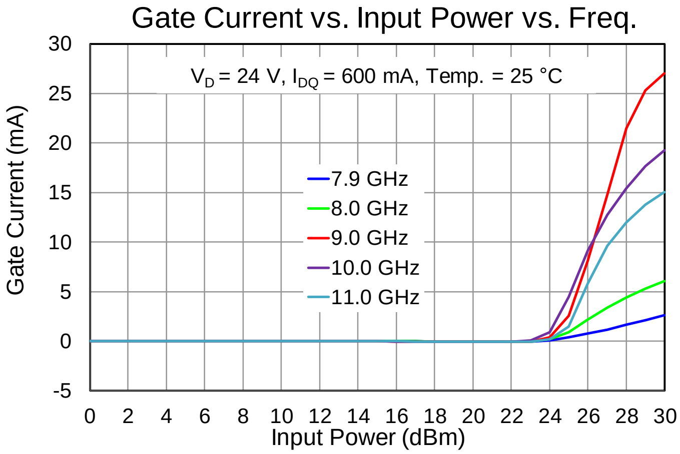

V_{DELTA} vs. Input Power vs. Temp.

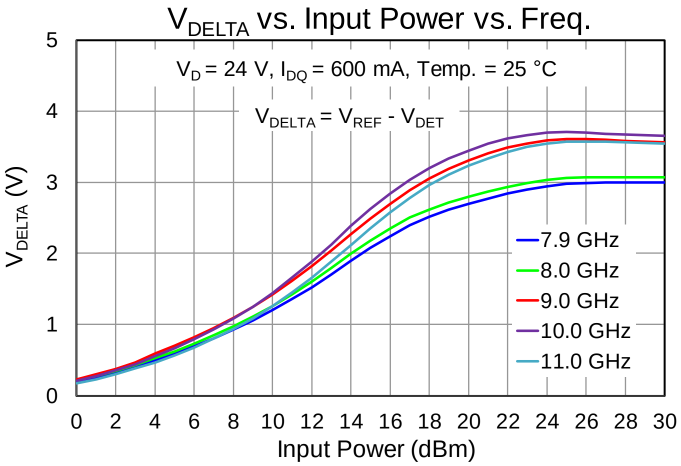
Performance Plots – Large Signal (CW)



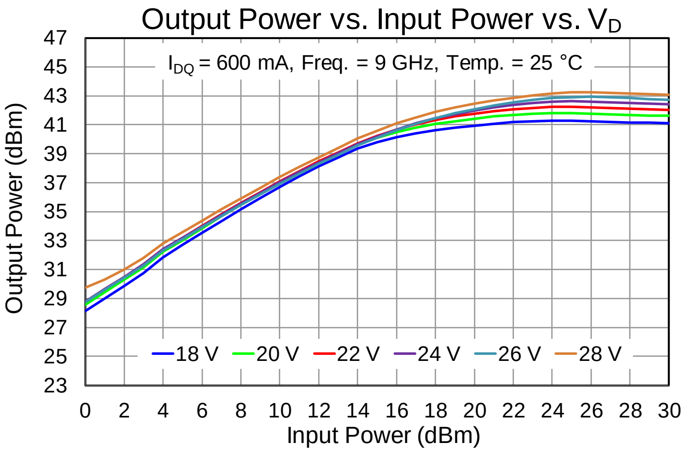


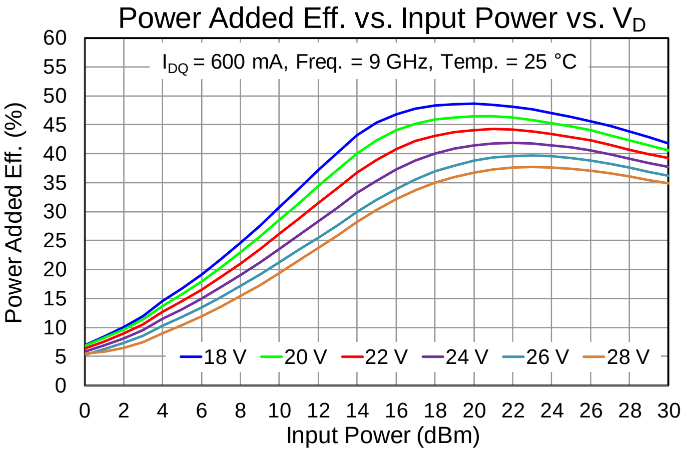


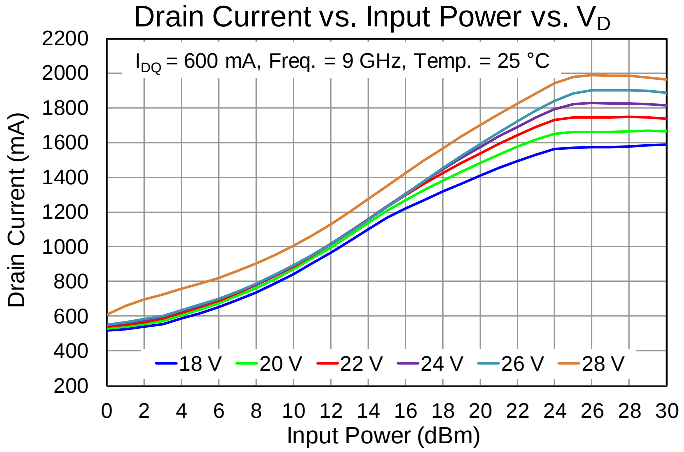


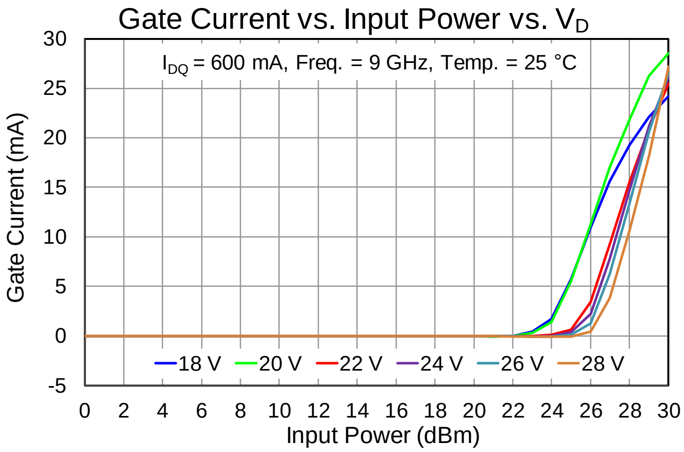


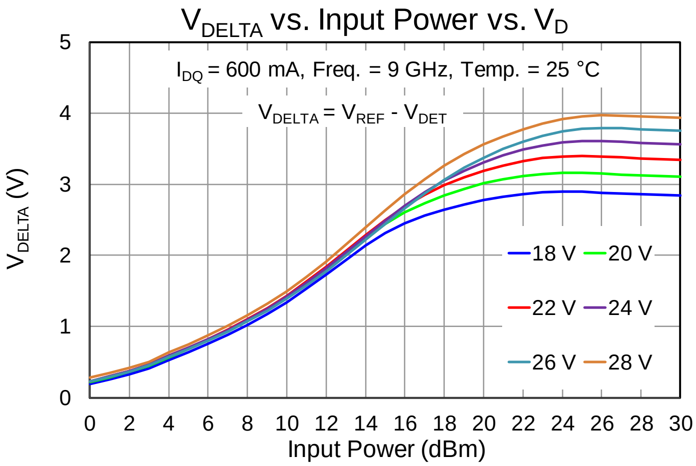
Performance Plots – Large Signal (CW)



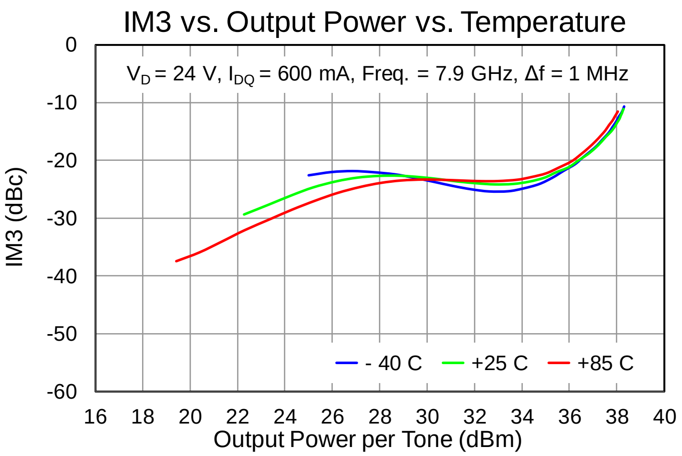


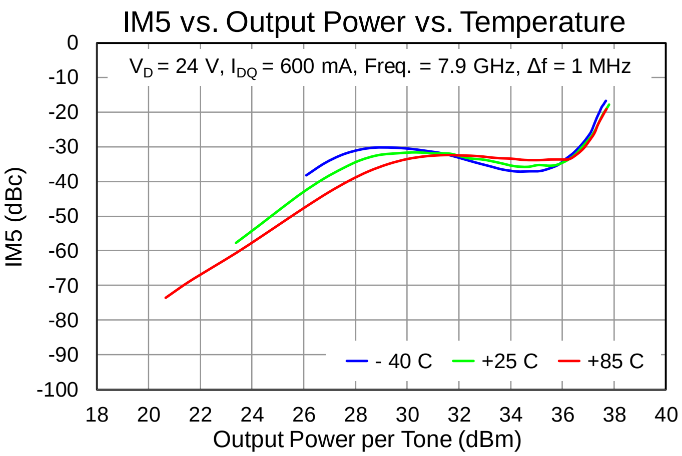


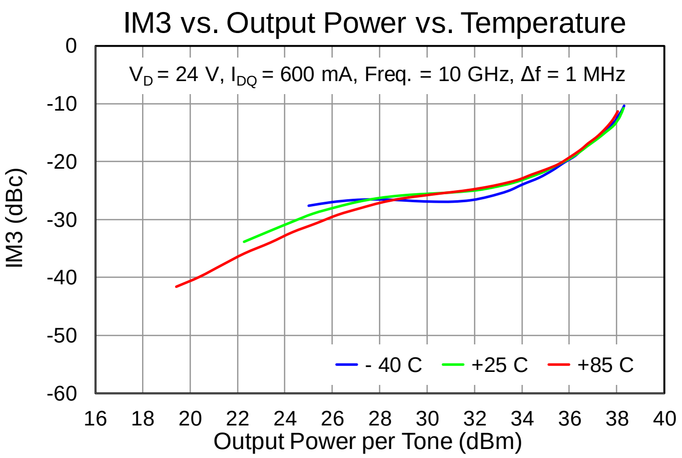


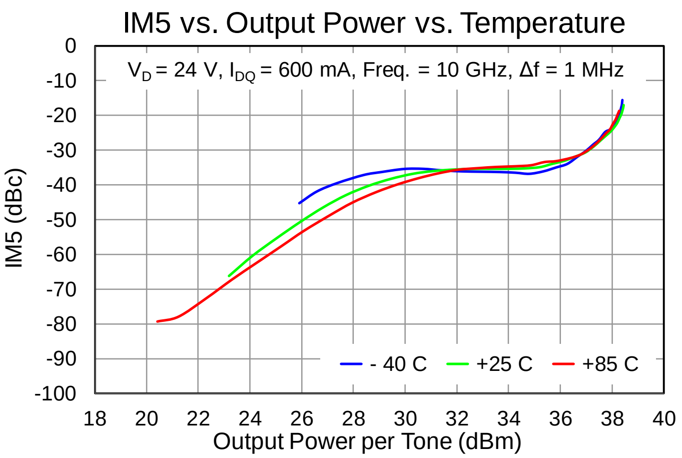


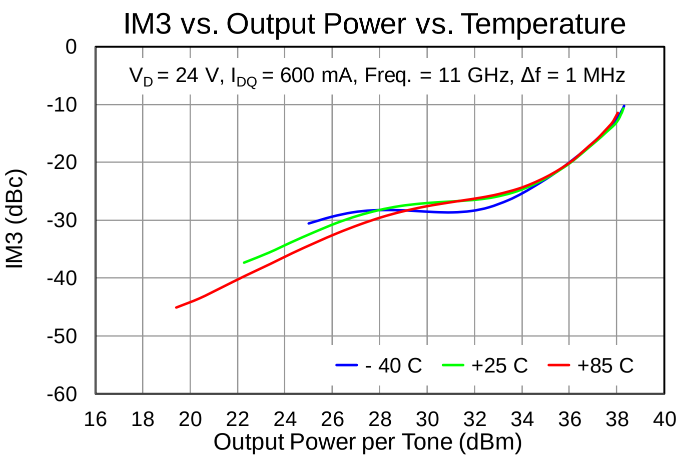
Performance Plots – Linearity

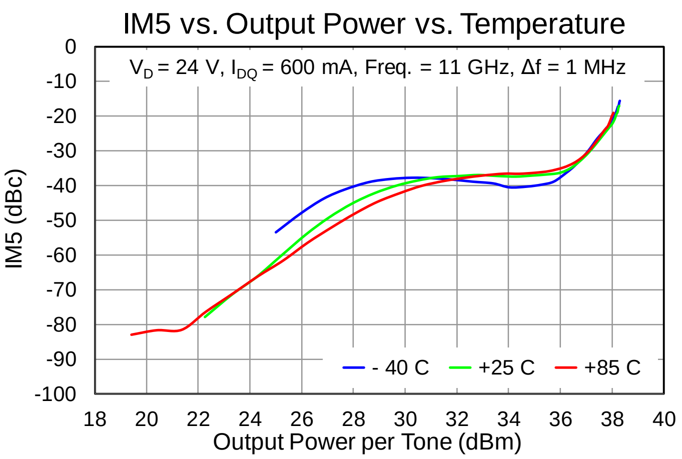




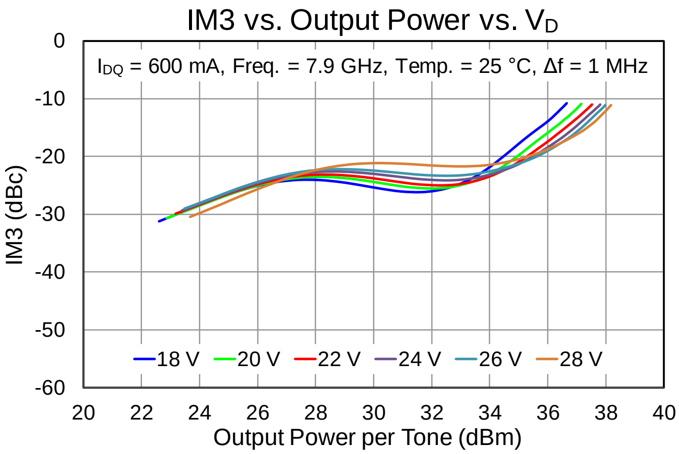


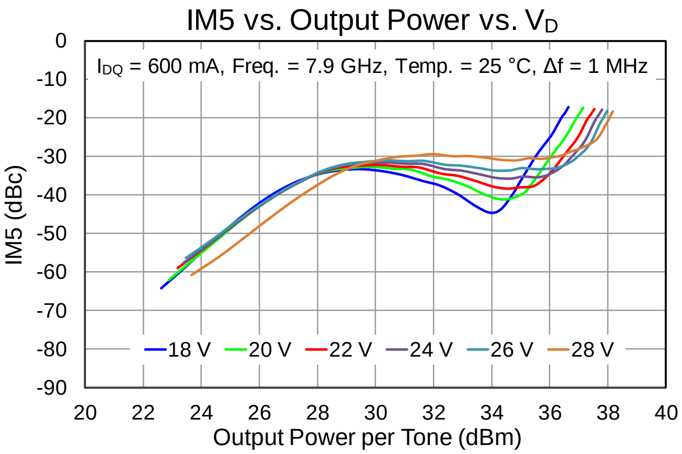


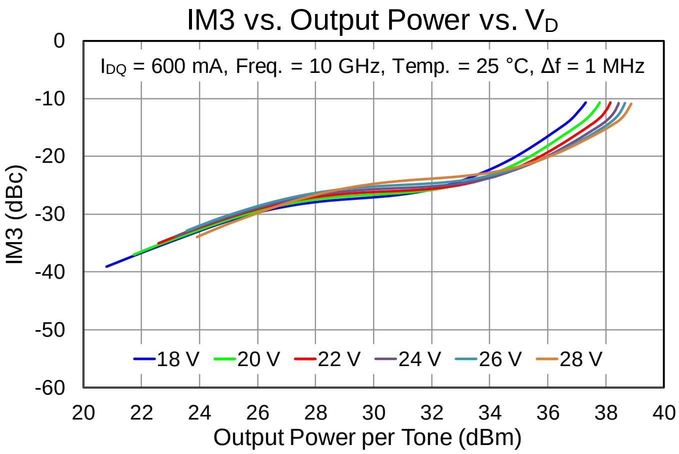


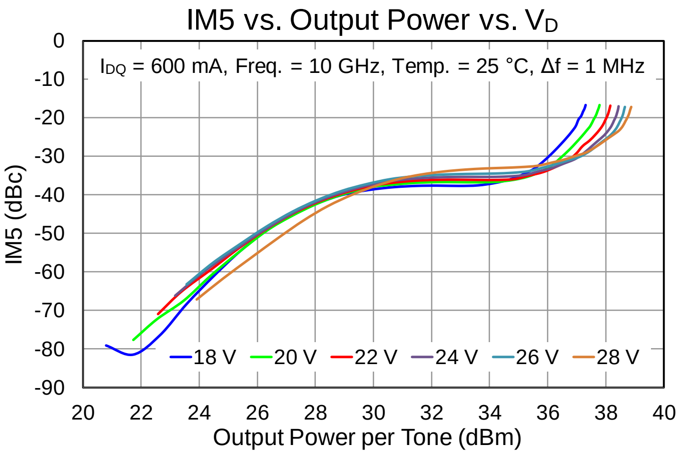


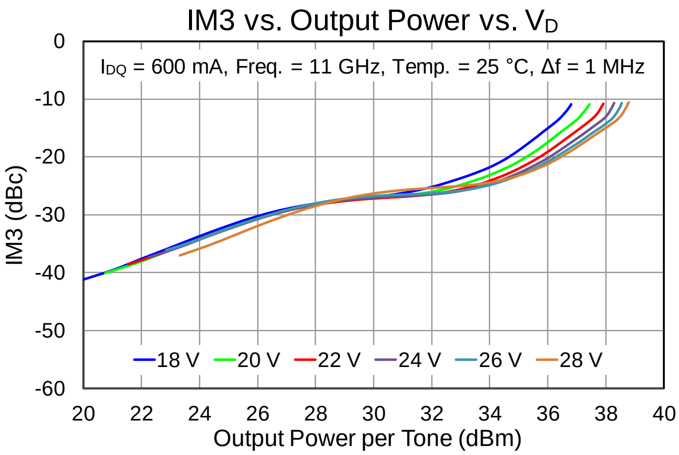
Performance Plots – Linearity

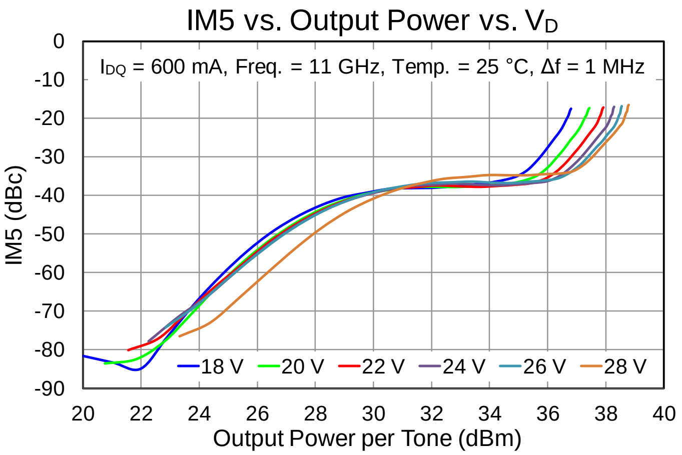




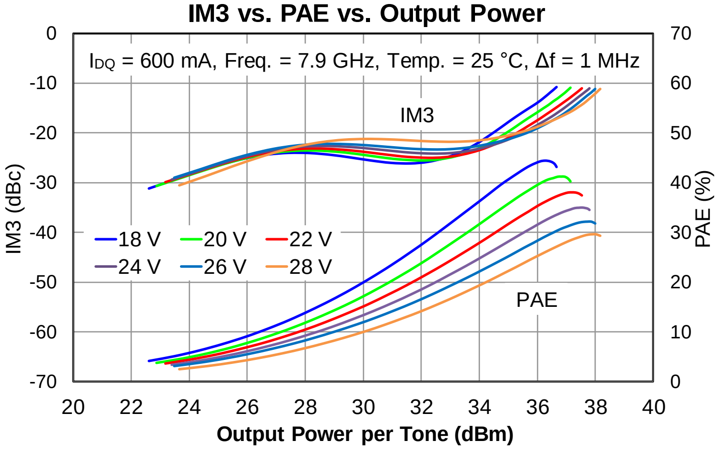




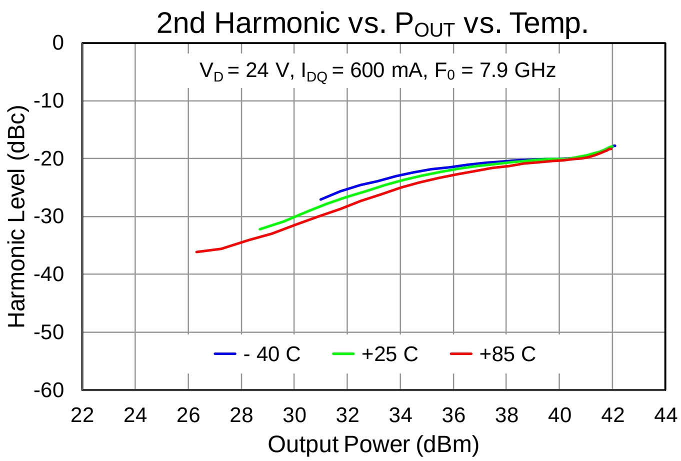


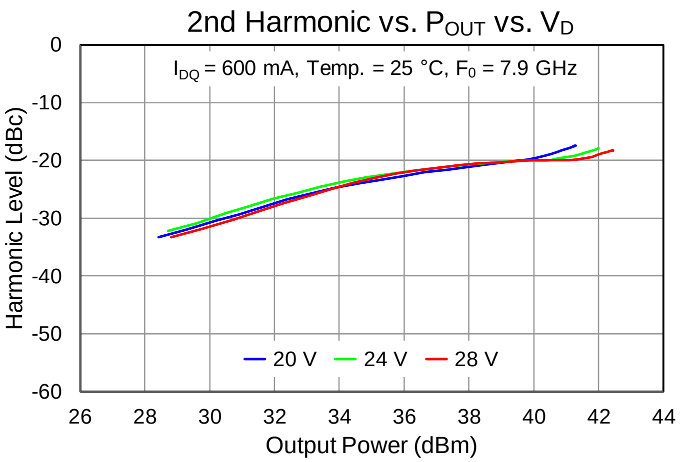


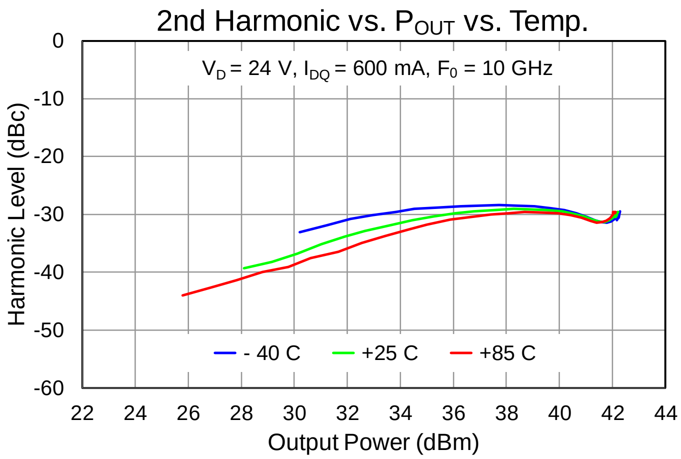
Performance Plots – Linearity

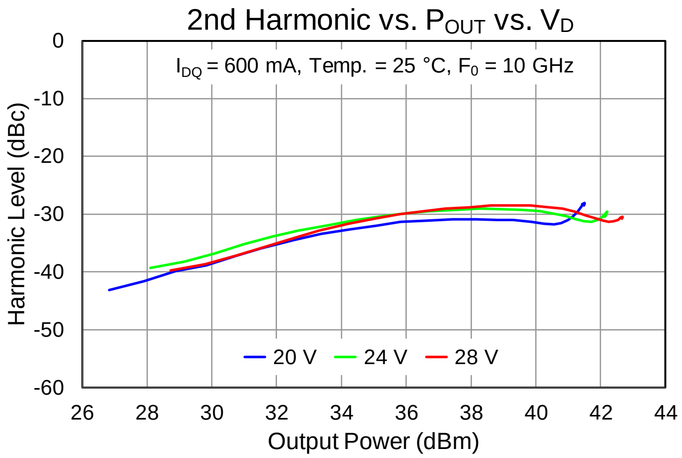


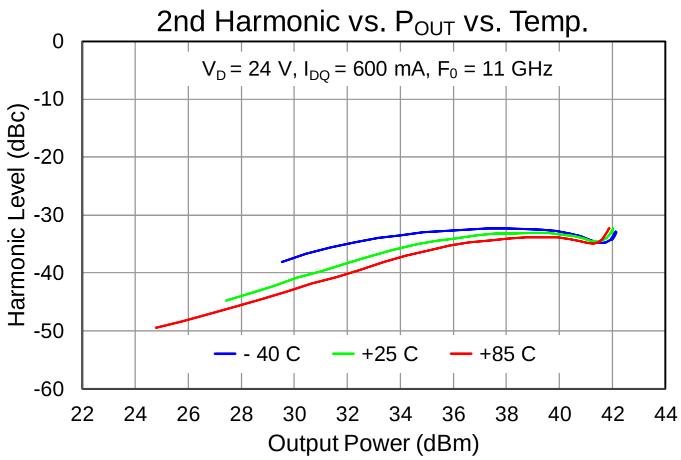
Performance Plots – Harmonics

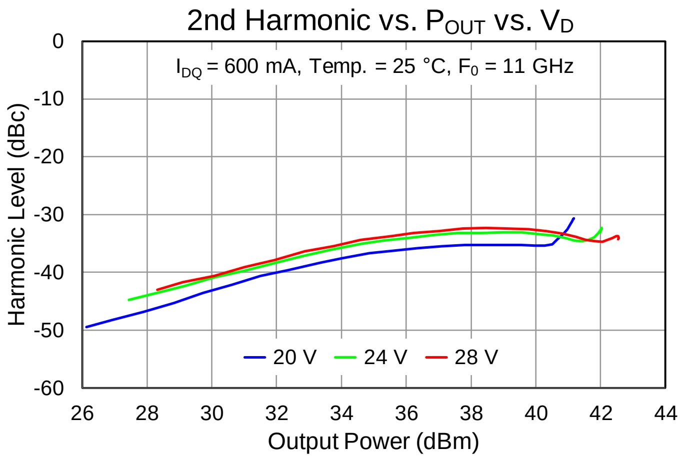

2nd Harmonic vs. P_{OUT} vs. Temp.


2nd Harmonic vs. P_{OUT} vs. V_D

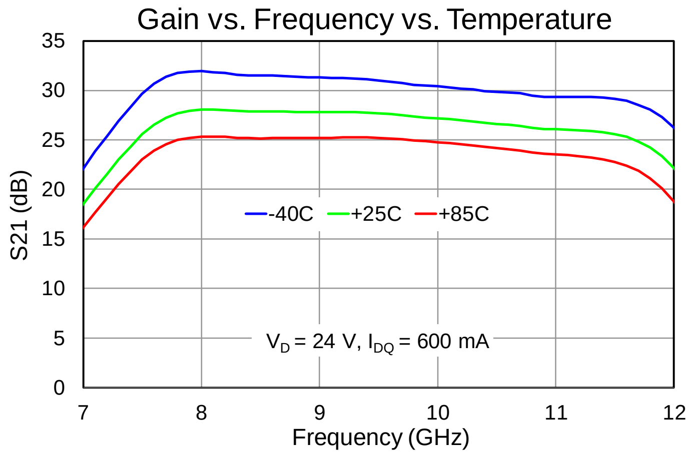

2nd Harmonic vs. P_{OUT} vs. Temp.

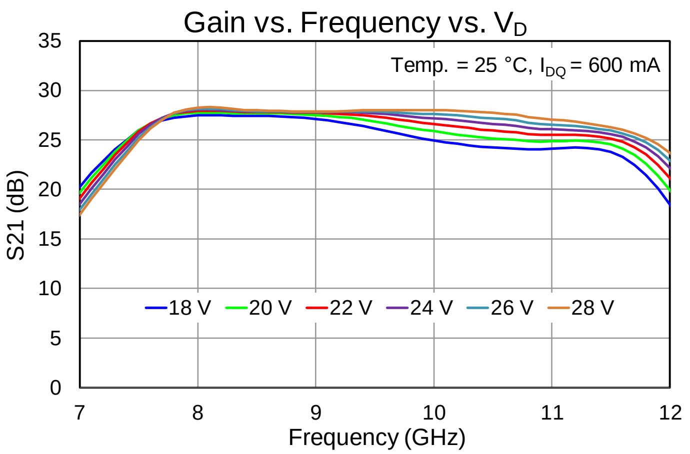

2nd Harmonic vs. P_{OUT} vs. V_D

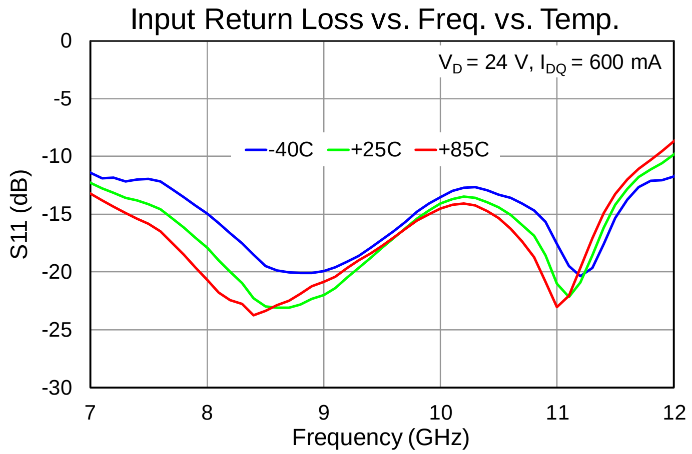

2nd Harmonic vs. P_{OUT} vs. Temp.

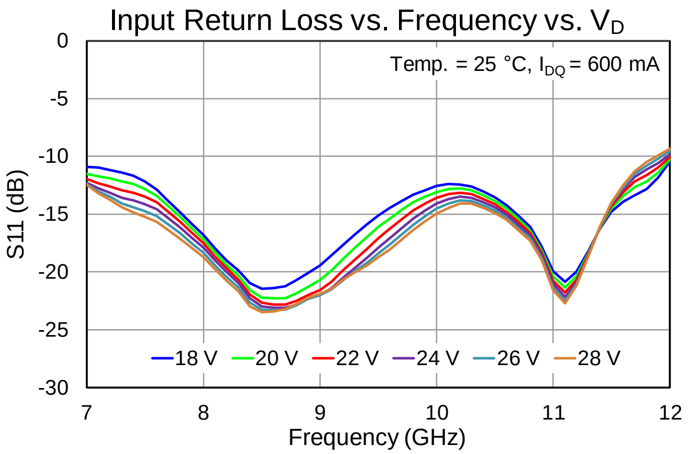

2nd Harmonic vs. P_{OUT} vs. V_D

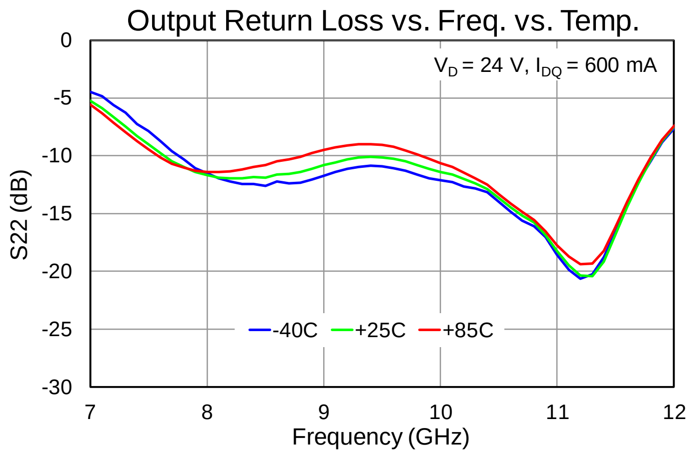
Performance Plots – Small Signal

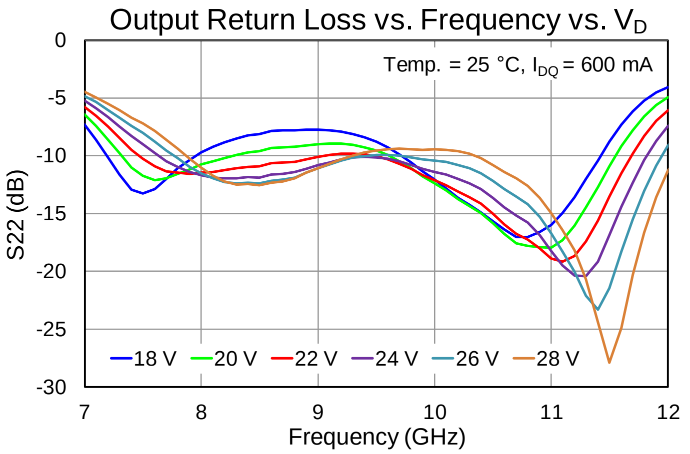

Gain vs. Frequency vs. Temperature


Gain vs. Frequency vs. V$_D$

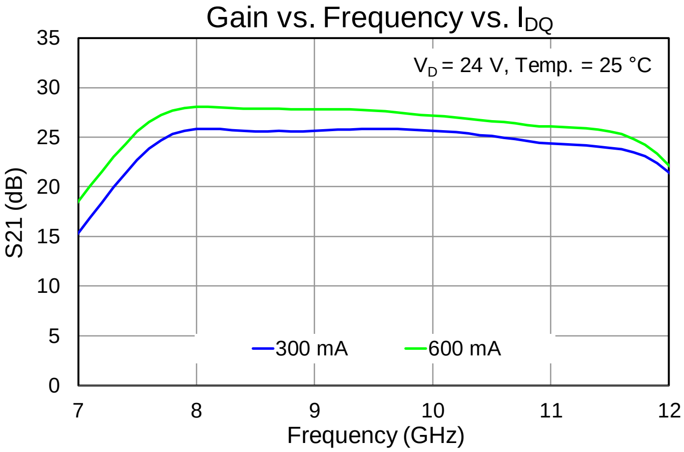

Input Return Loss vs. Freq. vs. Temp.

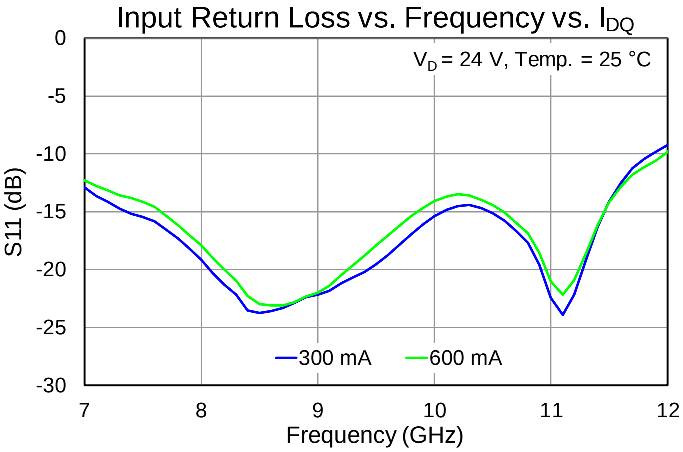

Input Return Loss vs. Frequency vs. V$_D$

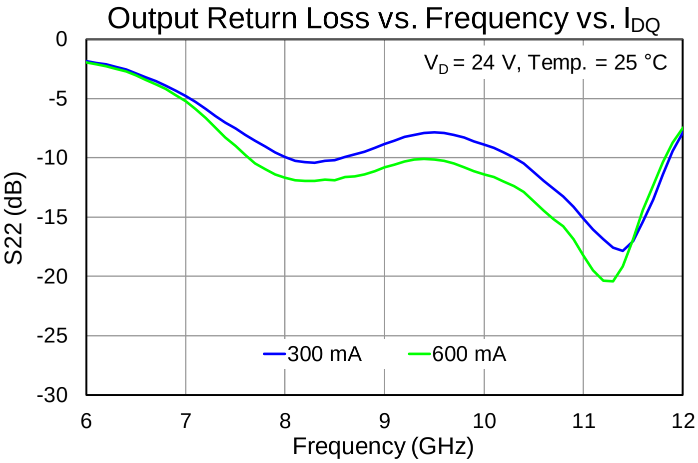

Output Return Loss vs. Freq. vs. Temp.


Output Return Loss vs. Frequency vs. V$_D$

Performance Plots – Small Signal







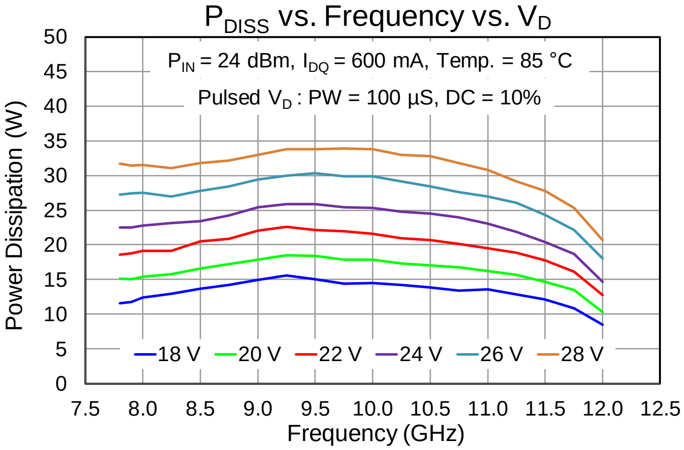
Thermal and Reliability Information

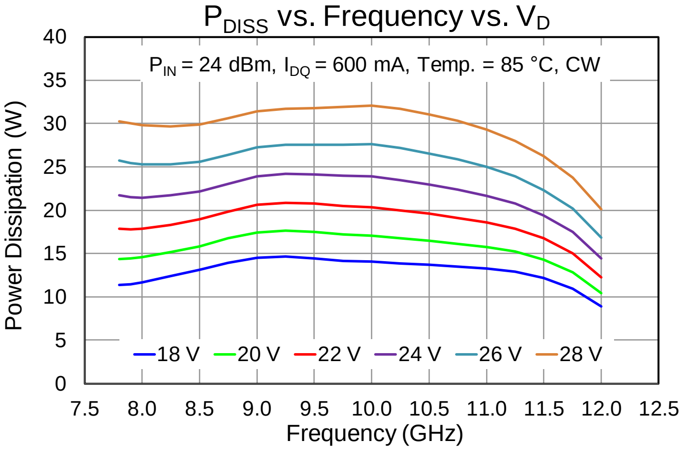
Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	T_{BASE} = 85 °C, V_D = +24 V, I_{DQ} = 600 mA, Pulsed V_D (100 us/10%), Freq = 9.25 GHz, P_{IN} = 24 dBm, I_{D_Drive} = 1.7 A, P_{OUT} = 42 dBm, P_{DISS} = 25.9 W	2.503	°C/W
Channel Temperature (T_{CH}) (Under RF drive) (2)		149.8	°C
Thermal Resistance (θ_{JC}) (1)	T_{BASE} = 85°C, V_D = +24V, I_{DQ} = 600 mA, CW, P_{DISS} = 14.4 W	2.860	°C/W
Channel Temperature (T_{CH}) (No RF) (2)		126.2	°C
Thermal Resistance (θ_{JC}) (1)	T_{BASE} = 85 °C, V_D = +24 V, I_{DQ} = 600 mA, CW, Freq = 9.25 GHz, P_{IN} = 24 dBm, I_{D_Drive} = 1.7 A, P_{OUT} = 42 dBm, P_{DISS} = 24.2 W	2.704	°C/W
Channel Temperature (T_{CH}) (Under RF drive) (2)		150.4	°C
Thermal Resistance (θ_{JC}) (1)	T_{BASE} = 85 °C, V_D = +20 V, I_{DQ} = 600 mA, Pulsed V_D (100 us/10%), Freq = 9.25 GHz, P_{IN} = 24 dBm, I_{D_Drive} = 1.6 A, P_{OUT} = 41.3 dBm, P_{DISS} = 18.5 W	1.896	°C/W
Channel Temperature (T_{CH}) (Under RF drive) (2)		120.1	°C
Thermal Resistance (θ_{JC}) (1)	T_{BASE} = 85°C, V_D = +20V, I_{DQ} = 600 mA, CW, P_{DISS} = 12 W	2.807	°C/W
Channel Temperature (T_{CH}) (No RF) (2)		118.7	°C
Thermal Resistance (θ_{JC}) (1)	T_{BASE} = 85 °C, V_D = +20 V, I_{DQ} = 600 mA, CW, Freq = 9.25 GHz, P_{IN} = 24 dBm, I_{D_Drive} = 1.56 A, P_{OUT} = 41.4 dBm, P_{DISS} = 17.7 W	2.552	°C/W
Channel Temperature (T_{CH}) (Under RF drive) (2)		130.2	°C

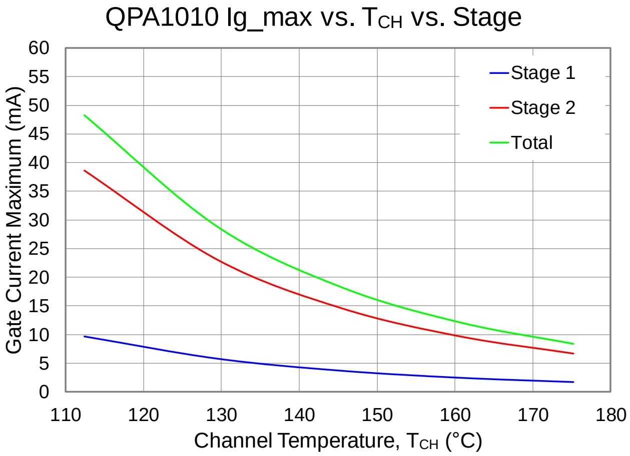
Notes:

1. Thermal resistance is referenced to the package backside T_{BASE}
2. IR scan equivalent. Refer to the following document: GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates

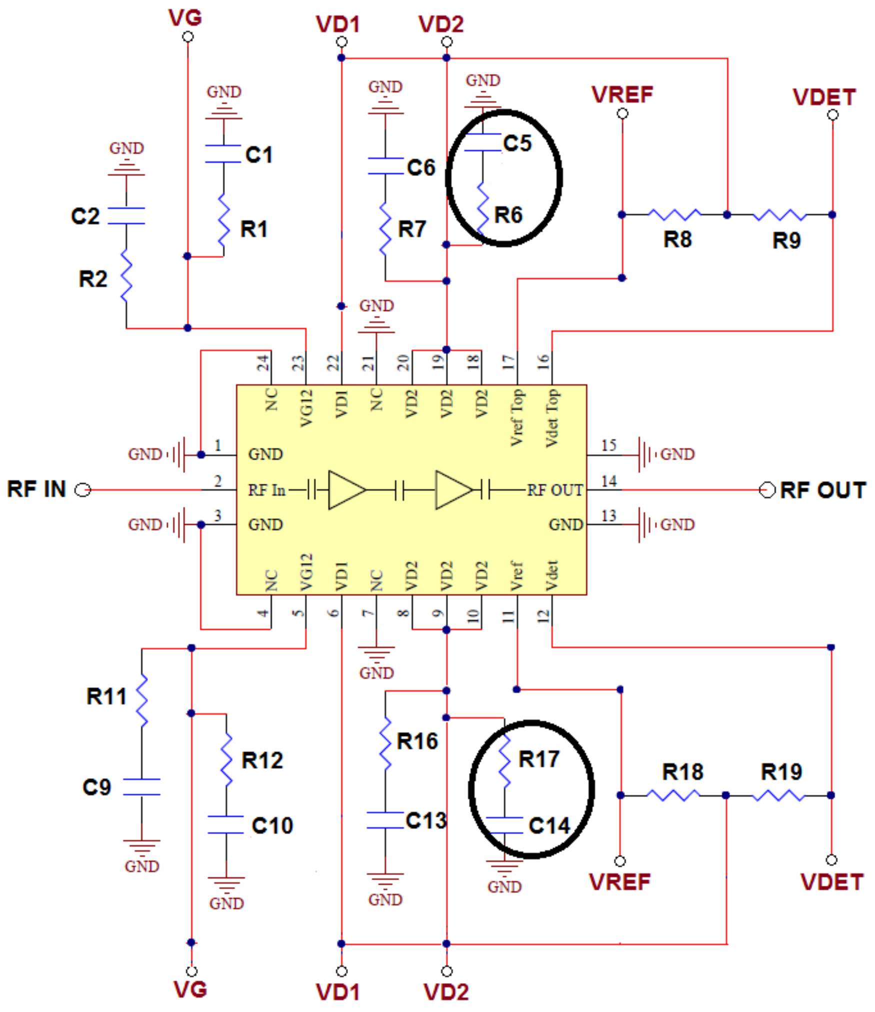
Power Dissipation and Maximum Gate Current







Applications Circuit for Linear and Pulsed Operations



Note: $V_{DELTA} = V_{REF} - V_{DET}$

- QPA1010 can be biased from either the top side or bottom side.
- V_{D1} and V_{D2} need to be tied together.
- V_{D1} / V_{D2} and V_{REF} / V_{DET} have to be on the same side for V_{DELTA} to work.
- Bypassing components required for the side(s) being biased.
- The extra bias components (R6, R17, C5 and C14) are required for optimum linearity.

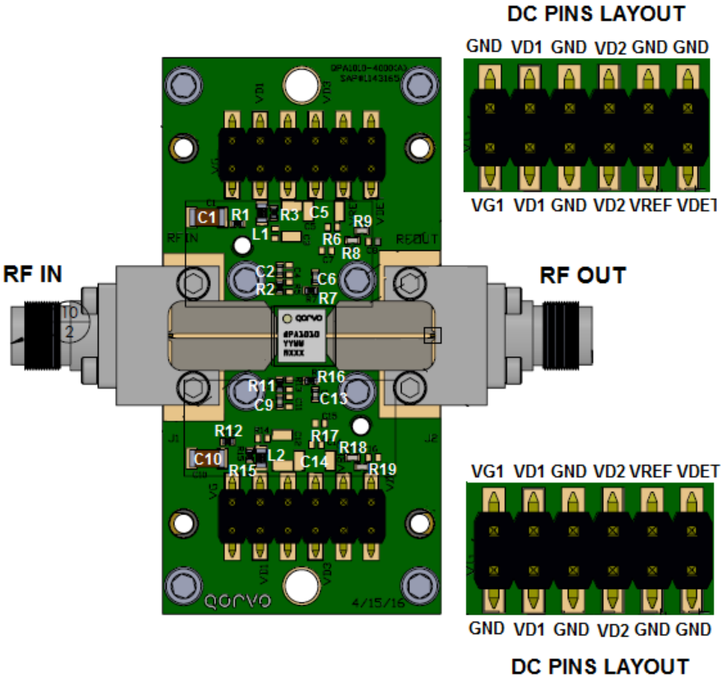
Bias Up Procedure

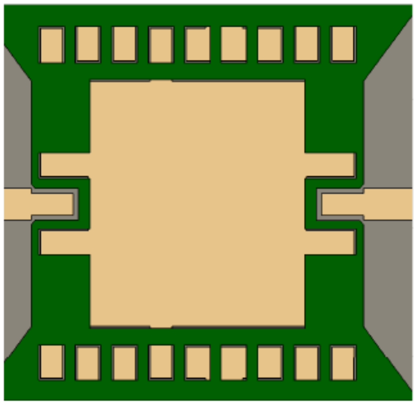
1. Set I_D limit to 2000 mA, I_G limit to 20 mA
2. Apply −5 V to V_G
3. Apply +24 V to V_D; ensure I_{DQ} is approx. 0 mA
4. Adjust V_G until I_{DQ} = 600 mA (V_G ~ −1.8 V Typ.).
5. Turn on RF supply

Bias Down Procedure

1. Turn off RF supply
2. Reduce V_G to −5 V; ensure I_{DQ} is approx. 0 mA
3. Set V_D to 0 V
4. Turn off V_D supply
5. Turn off V_G supply

Evaluation Board (EVB) Layout Assembly for Pulsed Operation





MOUNTING DETAIL

Note: PCB is a multilayer

1. All 4 metal thicknesses are 0.5 oz
2. Upper core 1 is Rogers 4003C, 8 mil thick
3. Lower core 2 is 370HR, 6 mil thick
4. Prepreg is an epoxy coated glass fabric
5. Total finished PCB thickness is 25 ±3 mil
6. This EVB uses a copper-coined PCB for optimum thermal management under high dissipation long pulse and/or CW conditions

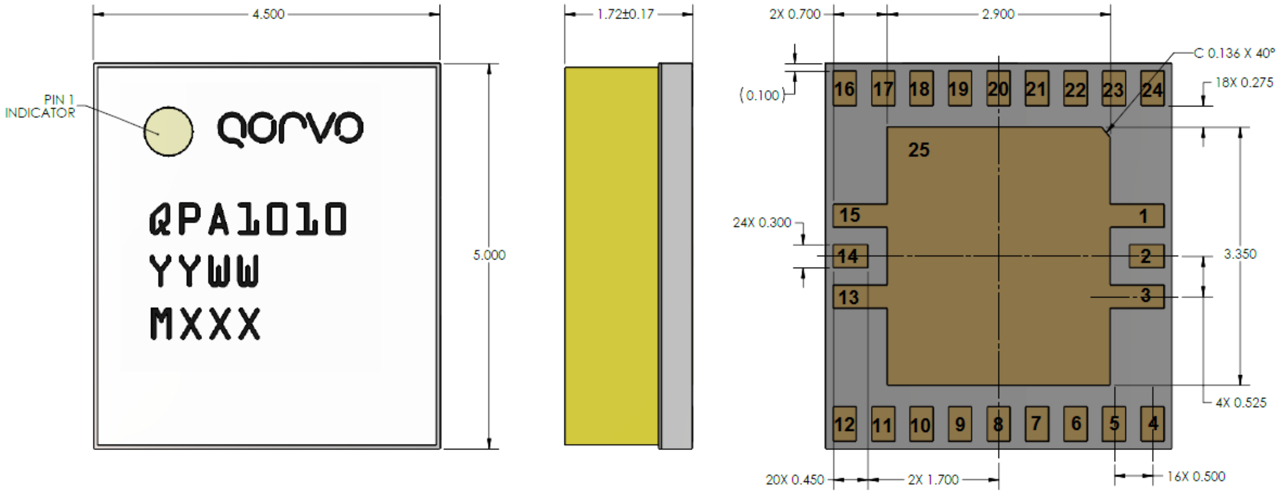
Bill of Materials for EVB

Reference Des.	Value	Description	Manuf.	Part Number
C1, C5, C10, C14	10 uF	CAP, 1206, 50 V, 20 %, X5R	Various	–
C2, C6, C9, C13	0.01 uF	CAP, 0402, 50 V, 10 %, X7R	Various	–
R1, R12	5.1 Ohm	RES, 0402, 50V, 5 %, SMT	Various	–
R2, R3, R6, R7, R11, R15, R16, R17 (1)	0 Ohm	RES, 0402, 5 %, SMD	Various	–
R8, R9, R18, R19	25.5 K Ohm	RES, 0402, 1/16W, 1%, 0402	Various	–
L1, L2 (1)	0 Ohm	RES, 0603, 1/10 W	Various	–

Note:

1. These components are acting as the jumpers for this EVB.

Mechanical Information



Units: millimeters
Tolerances: unless specified
x.xx = ± 0.25
x.xxx = ± 0.100
Materials:
Base: Laminate
Lid: FR4
All metalized features are gold plated
Part is epoxy sealed
Marking:
QPA1010: Part number
YY: Part Assembly year
WW: Part Assembly week
MXXX: Batch ID

Pin Description

Pad No.	Symbol	Description
1, 3, 13, 15, 25 (pad)	GND	Ground. Must be grounded on the PCB. Conductive filled vias recommended for least inductance and improved thermal performance
2	RF_{IN}	RF Input; matched to 50 Ω; DC blocked
4, 7, 21, 24	N/C	Not connected internally. Recommended to be grounded
5, 23	V_{G1-2}	Stage 1-2 Gate Voltage. Bias network is required; see recommended Application Information above on page 22
6, 22	V_{D1}	Stage 1 Drain Voltage. Bias network is required; see recommended Application Information above on page 22
8 – 10, 18 - 20	V_{D2}	Stage 2 Drain voltage; Bias network is required; see recommended Application Information above on page 22
11, 17	V_{REF}	Reference voltage
12, 16	V_{DET}	Detector voltage
14	RF_{OUT}	RF Output; matched to 50 Ω; DC blocked

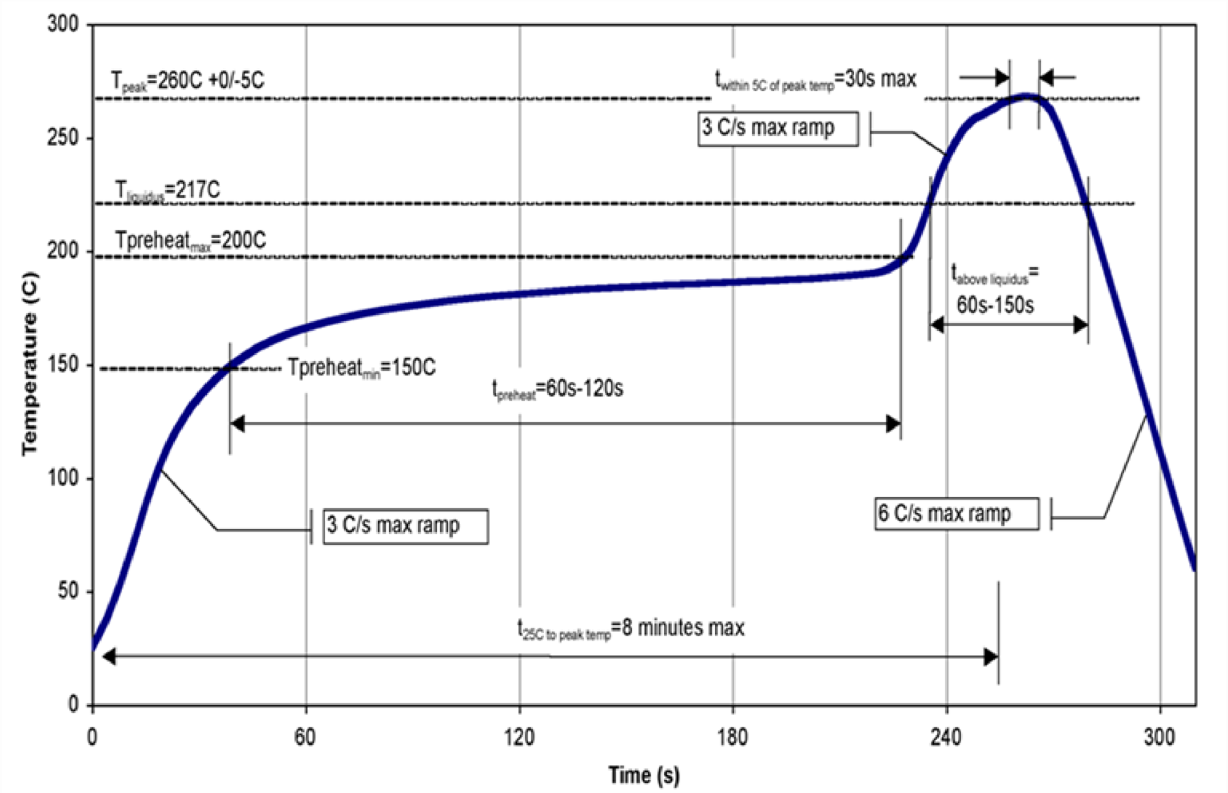
Assembly Notes

Compatible with lead-free soldering processes with 260°C peak reflow temperature.

This package is air-cavity and non-hermetic, and therefore cannot be subjected to aqueous washing. The use of no-clean solder to avoid washing after soldering is highly recommended.

Contact plating: Ni-Au

Solder rework not recommended



Recommended Soldering Temperature Profile