QPA2237

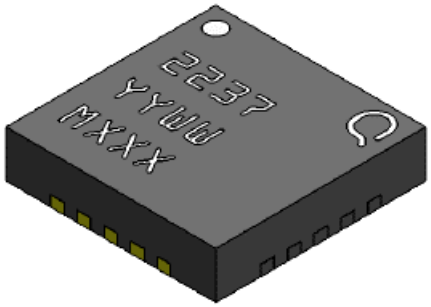
0.03 – 2.5 GHz 10 W GaN Power Amplifier

Product Description

Qorvo's QPA2237 is a wideband amplifier fabricated on Qorvo's production 0.25um GaN on SiC process. The QPA2237 operates from 0.03 – 2.5 GHz and provides 10W of saturated output power with 13 dB of large signal gain and 52% power-added efficiency.

The QPA2237 is available in a low-cost, surface-mount, 20 lead, 4x4 OVM QFN. It is ideally suited to support both radar and communication applications across defense and commercial markets as well as electronic warfare. The QPA2237 is fully matched to 50Ω at both RF ports allowing for simple system integration. DC blocks are required on both RF ports and the drain voltage must be injected through an off chip bias-tee on the RF output port.

Lead-free and RoHS compliant.



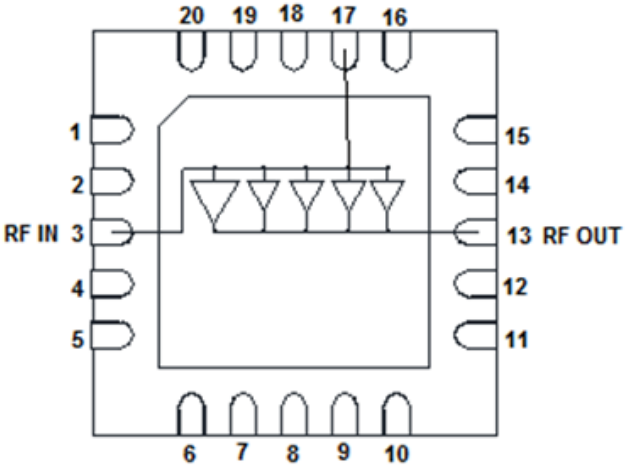
QFN 4x4 mm 20L

Product Features

- Frequency Range: 0.03 – 2.5 GHz
- P_{SAT}: 40 dBm at P_{IN} = 27 dBm
- PAE: 52%
- Large Signal Gain: 13 dB
- Small Signal Gain: 18.5 dB
- Input Return Loss: 9 dB
- Output Return Loss: 9.5 dB
- Bias: V_D = 32 V, I_{DQ} = 360 mA
- Wideband Flat Power
- Package Dimensions: 4.0 x 4.0 x 0.85 mm

Performance is typical across frequency. Please reference electrical specification table and data plots for more details.

Functional Block Diagram



Applications

- Commercial and military radar
- Communications
- Electronic Warfare

Ordering Information

Part No.	Description
QPA2237	0.03 – 2.5 GHz 10 W GaN Power Amplifier
QPA2237EVBP01	Evaluation Board

Electrical Specifications

Test conditions unless otherwise noted: 25 °C, V_D = +32 V, I_{DQ} = 360 mA, CW.

Parameter		Min	Typ	Max	Units
Operational Frequency Range		0.03	–	2.5	GHz
Output Power @ P_{IN} = 27 dBm	Frequency = 0.05 GHz	39.5	40.5	–	dBm
	Frequency = 1.25 GHz	39.5	40.1	–	
	Frequency = 2.5 GHz	39.5	40.4	–	
Power Added Efficiency @ P_{IN} = 27 dBm	Frequency = 0.05 GHz	48	65	–	%
	Frequency = 1.25 GHz	48	48.5	–	
	Frequency = 2.5 GHz	48	57	–	
Small Signal Gain	Frequency = 0.05 GHz	–	22.5	–	dB
	Frequency = 1.25 GHz	–	20	–	
	Frequency = 2.5 GHz	–	19	–	
Input Return Loss	Frequency = 0.05 GHz	–	9	–	dB
	Frequency = 1.25 GHz	–	13	–	
	Frequency = 2.5 GHz	–	13	–	
Output Return Loss	Frequency = 0.05 GHz	–	10	–	dB
	Frequency = 1.25 GHz	–	11	–	
	Frequency = 2.5 GHz	–	16	–	
Gate Leakage (V_D=30V, V_G=−5.0V)		−2.4	–	–	mA
Small Signal Gain Temperature Coefficient		–	−0.017	–	dB/°C
Output Power Temperature Coefficient		–	−0.004	–	dBm/°C
Recommended Operating Voltage:		–	32	36	V

Recommended Operating Conditions

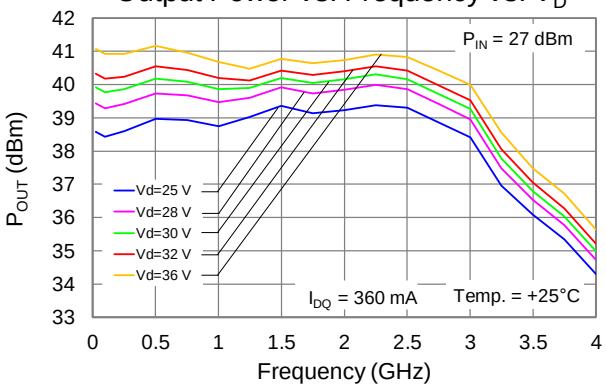
Parameter	Value / Range
Drain Voltage (V_D)	+32 V
Drain Current (I_{DQ})	360 mA
Temperature (T_{BASE})	−40 to 85 °C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

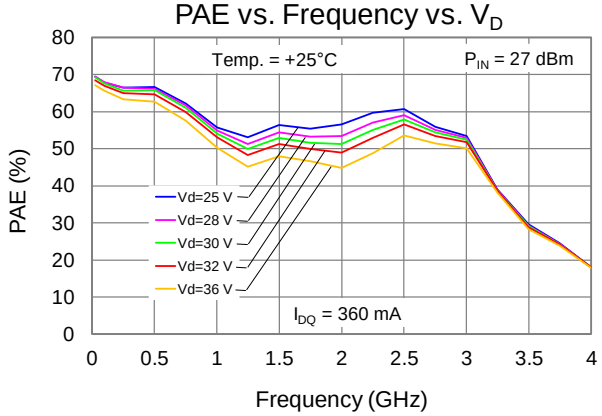
Performance Plots – Large Signal (CW)

The plots reflect performance measured with an external coaxial bias tee and DC blocks
(See application circuit on page 11)

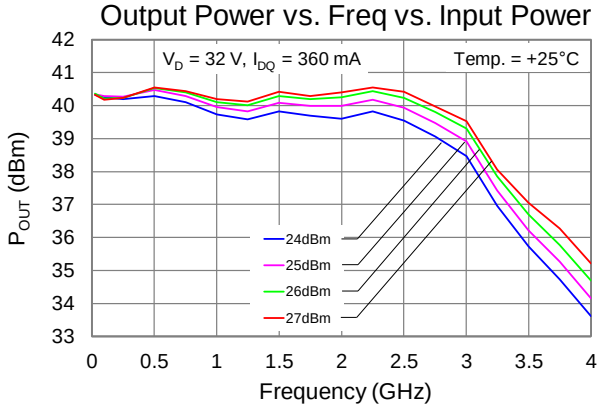
Output Power vs. Frequency vs. V_D



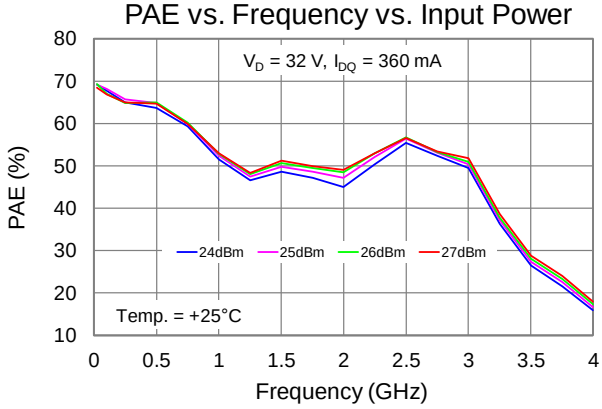
PAE vs. Frequency vs. V_D



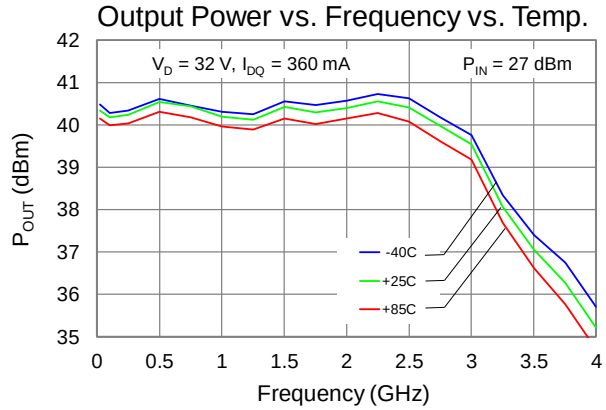
Output Power vs. Freq vs. Input Power



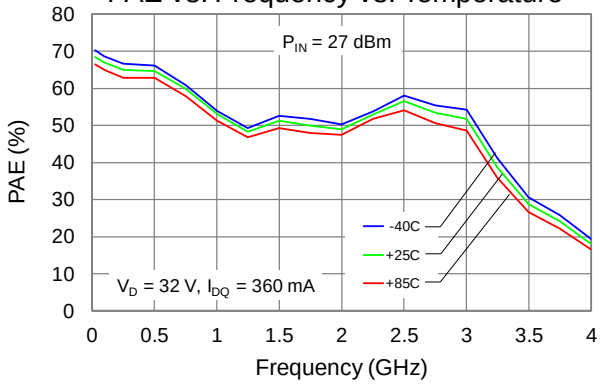
PAE vs. Frequency vs. Input Power



Output Power vs. Frequency vs. Temp.



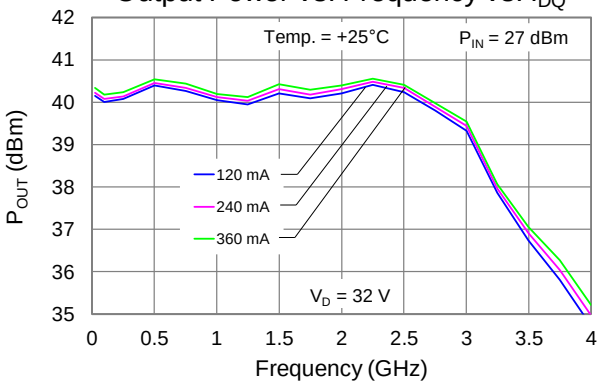
PAE vs. Frequency vs. Temperature



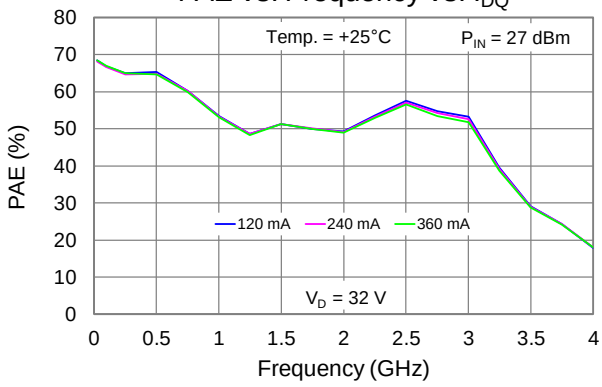
Performance Plots – Large Signal (CW)

The plots reflect performance measured with an external coaxial bias tee and DC blocks
(See application circuit on page 11)

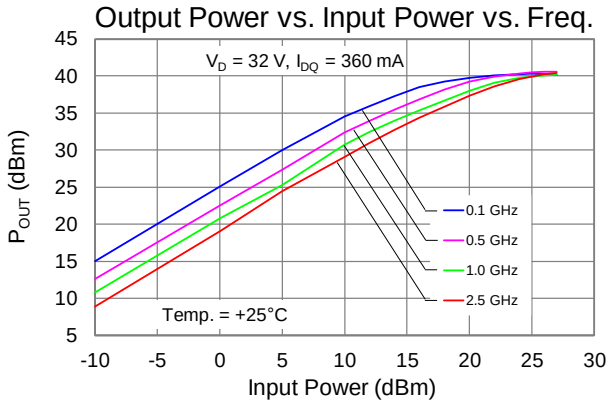
Output Power vs. Frequency vs. I_{DQ}



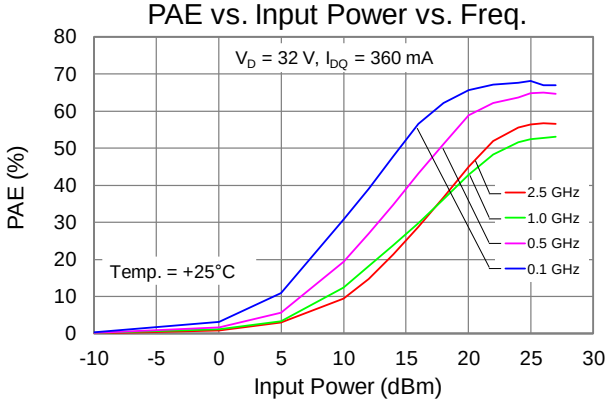
PAE vs. Frequency vs. I_{DQ}



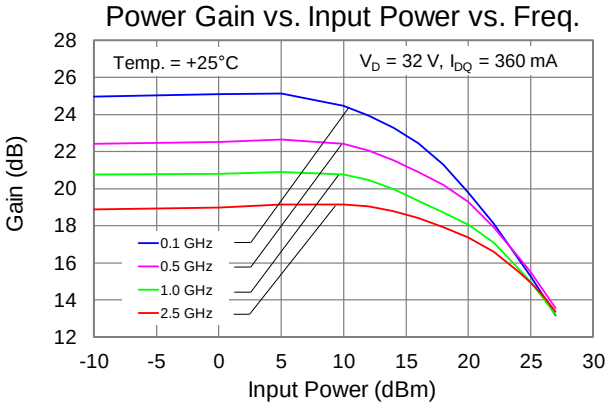
Output Power vs. Input Power vs. Freq.



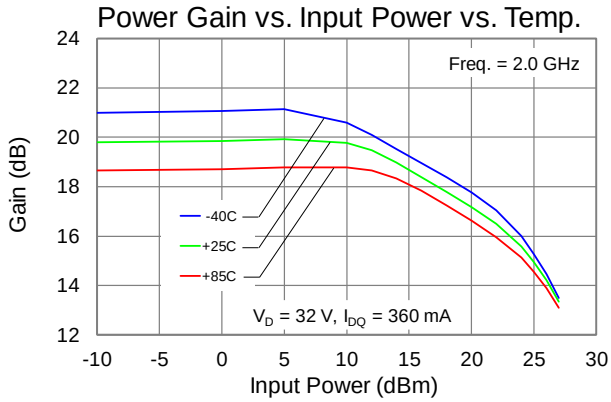
PAE vs. Input Power vs. Freq.



Power Gain vs. Input Power vs. Freq.

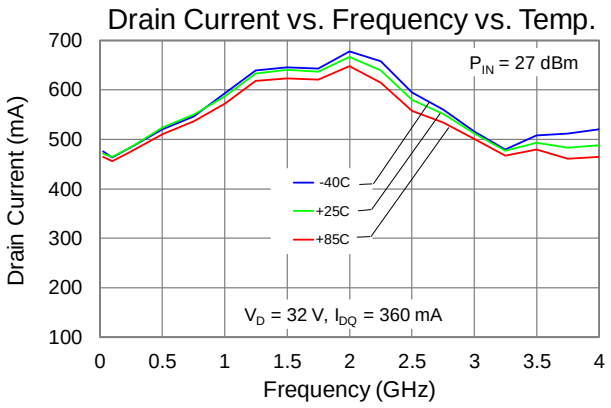


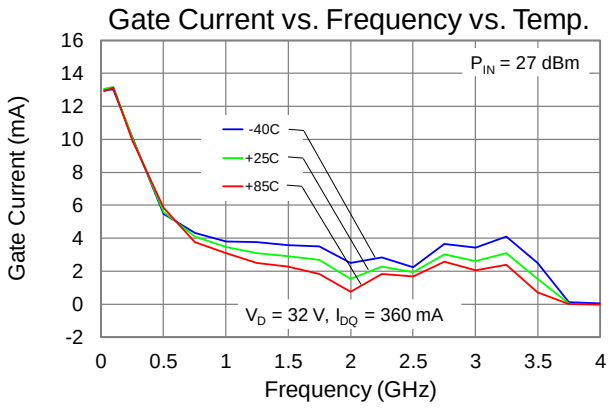
Power Gain vs. Input Power vs. Temp.

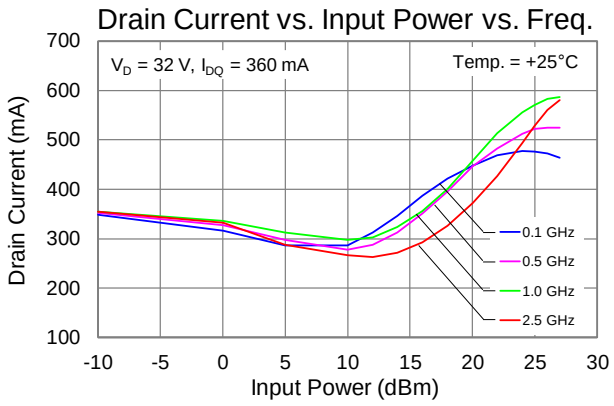


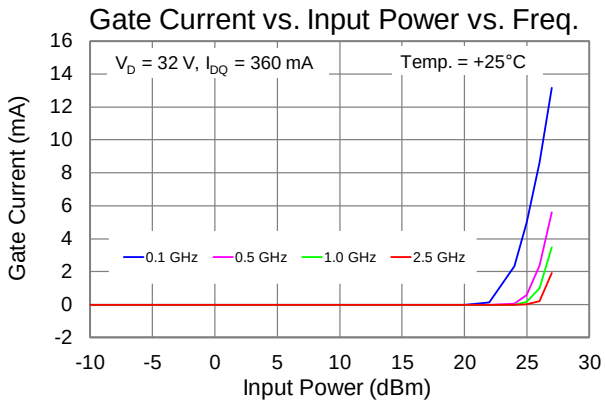
Performance Plots – Large Signal (CW)

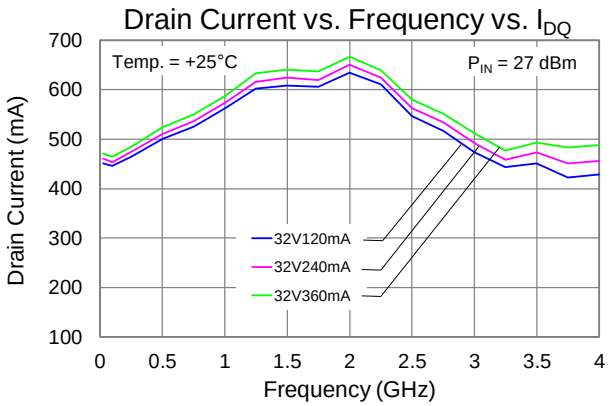
The plots reflect performance measured with an external coaxial bias tee and DC blocks
(See application circuit on page 11)

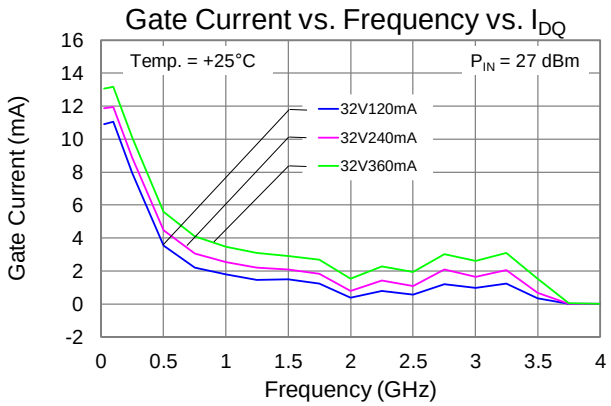








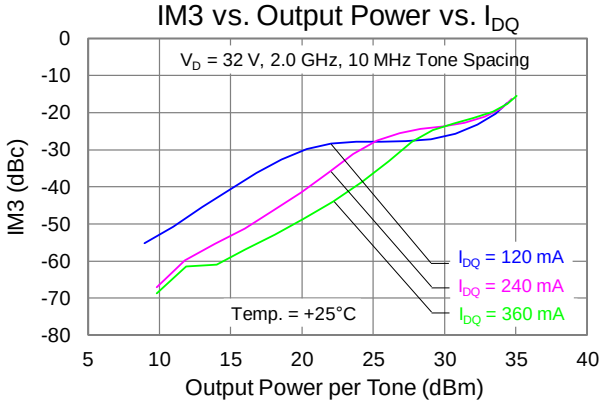




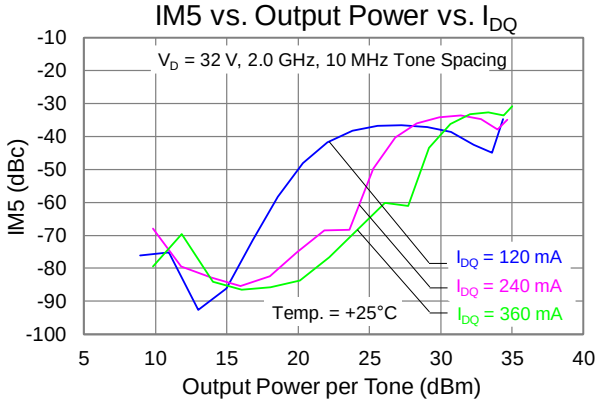
Performance Plots – Linearity

The plots reflect performance measured with an external coaxial bias tee and DC blocks
(See application circuit on page 11)

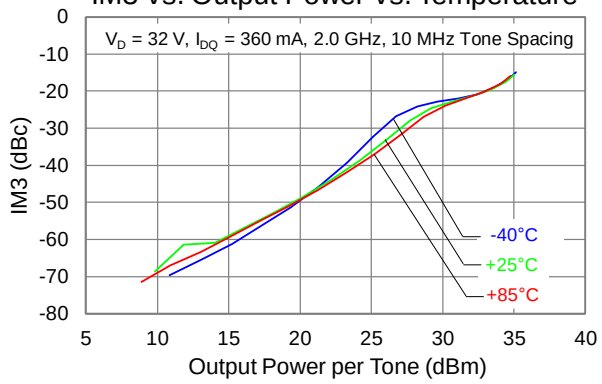
IM3 vs. Output Power vs. I_{DQ}



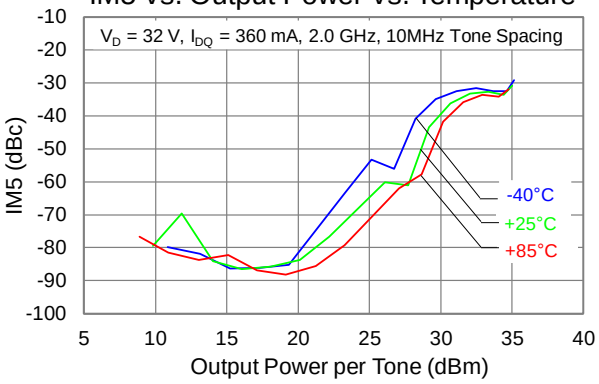
IM5 vs. Output Power vs. I_{DQ}



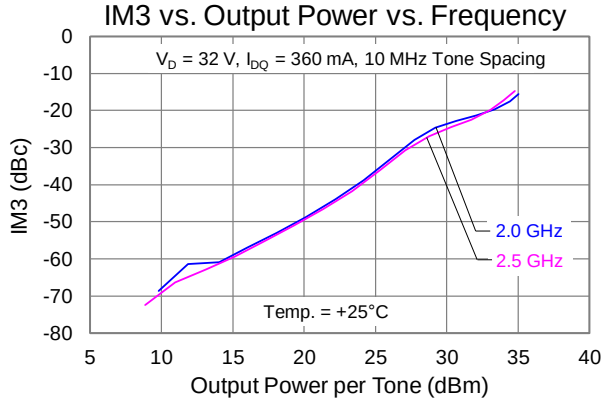
IM3 vs. Output Power vs. Temperature



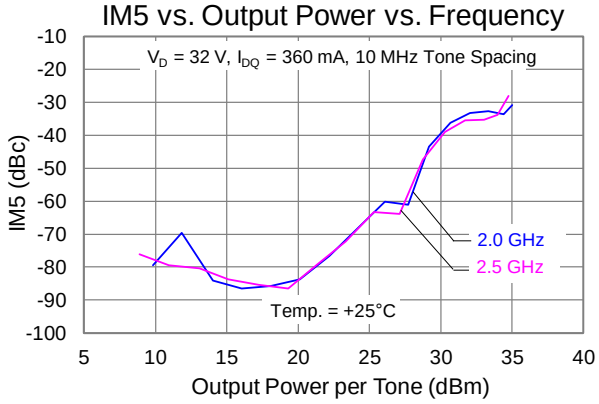
IM5 vs. Output Power vs. Temperature



IM3 vs. Output Power vs. Frequency

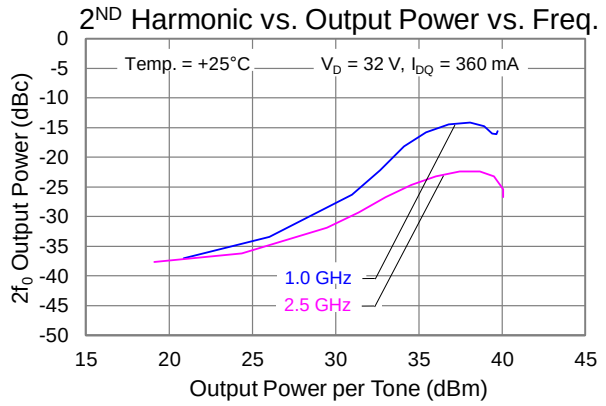


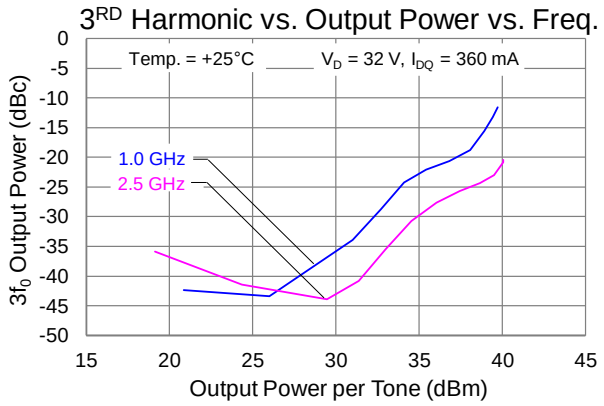
IM5 vs. Output Power vs. Frequency

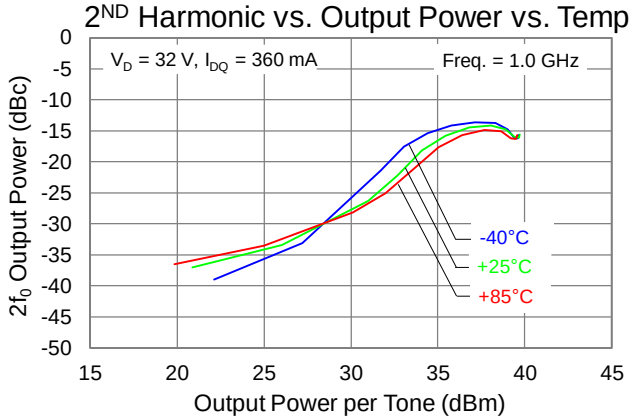


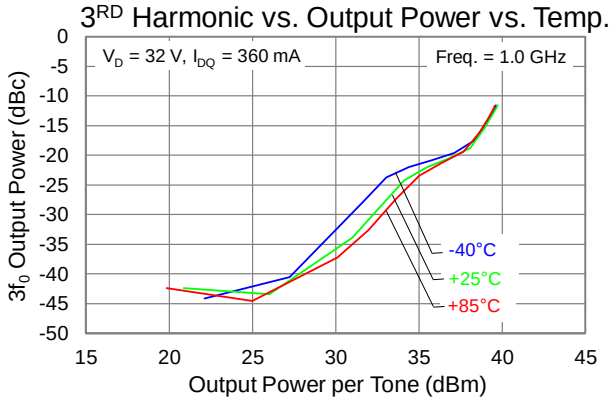
Performance Plots – Linearity

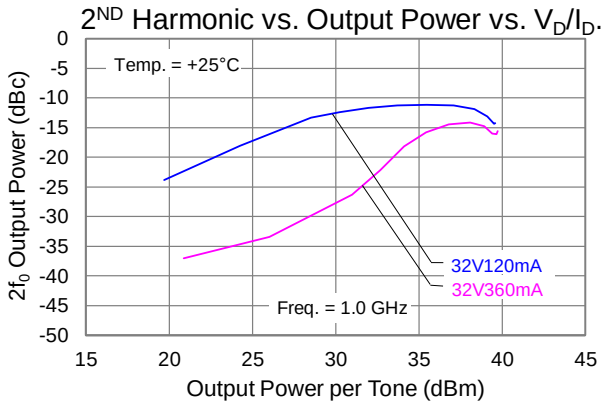
The plots reflect performance measured with an external coaxial bias tee and DC blocks
(See application circuit on page 11)

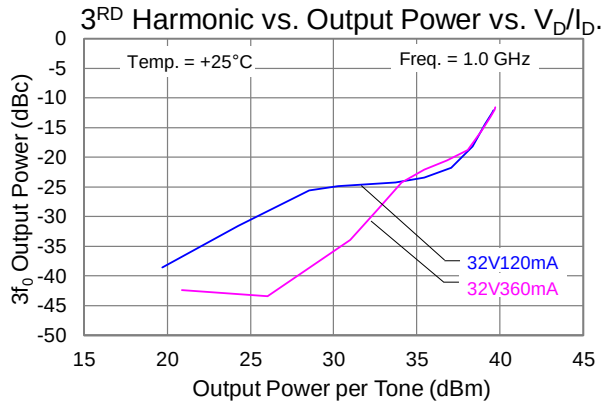








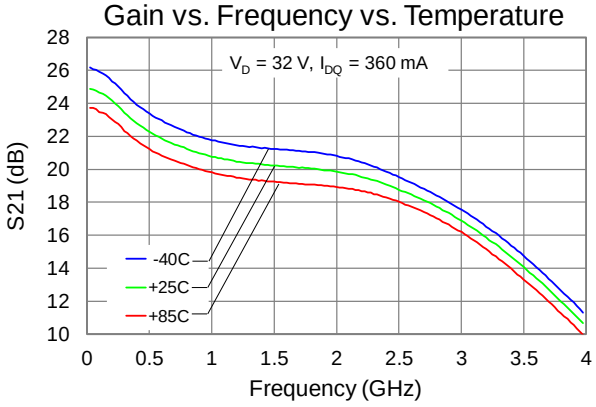




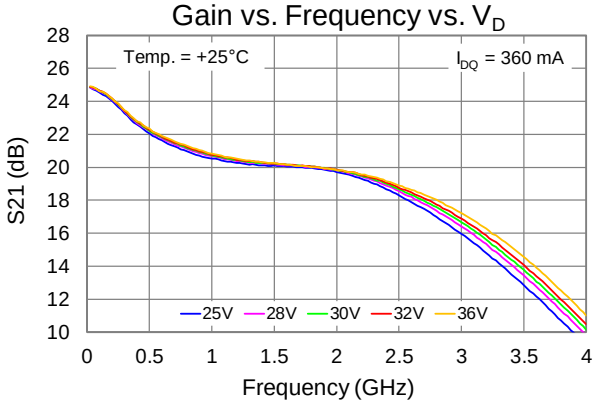
Performance Plots – Small Signal

The plots reflect performance measured with an external coaxial bias tee and DC blocks
(See application circuit on page 11)

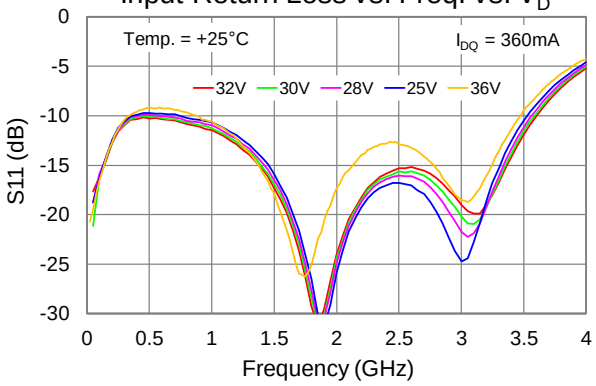
Gain vs. Frequency vs. Temperature



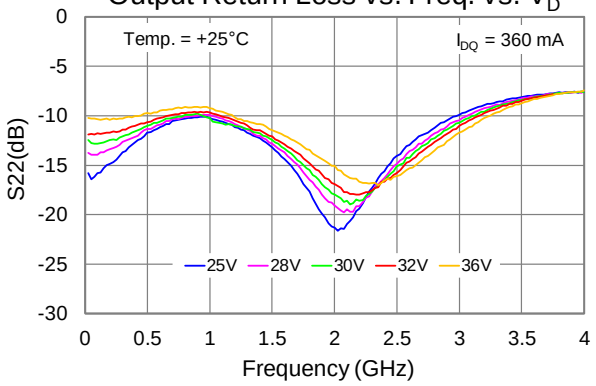
Gain vs. Frequency vs. V_D



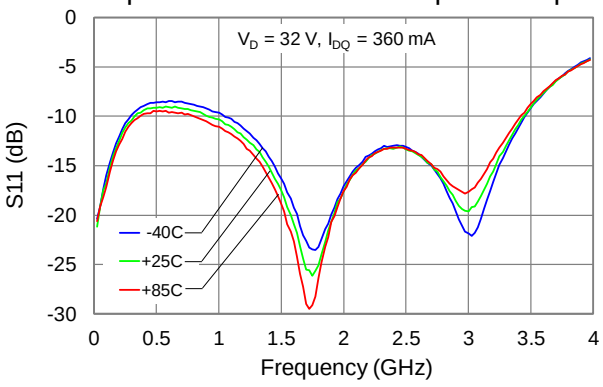
Input Return Loss vs. Freq. vs. V_D



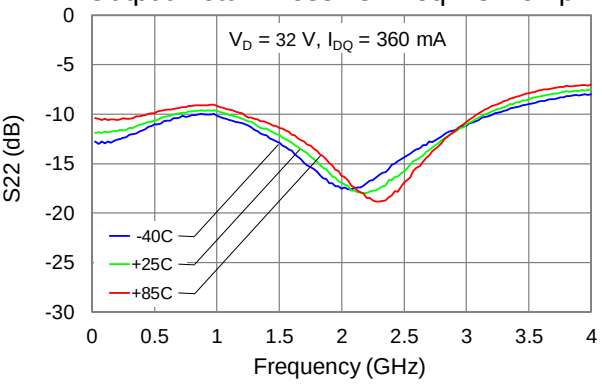
Output Return Loss vs. Freq. vs. V_D



Input Return Loss vs. Freq. vs. Temp.



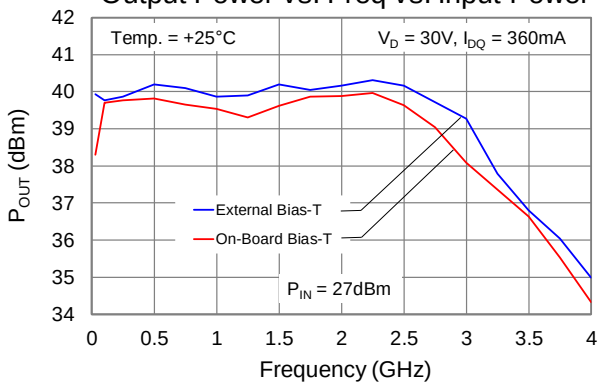
Output Return Loss vs. Freq. vs. Temp.



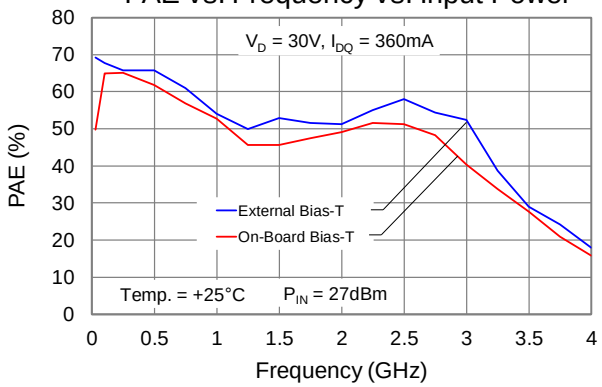
Performance Plots – Large Signal (CW), On-board vs. External Coaxial Bias-T

The plots reflect performance measured with an external coaxial bias tee and DC blocks
(See application circuit on page 11 and 13)

Output Power vs. Freq vs. Input Power



PAE vs. Frequency vs. Input Power

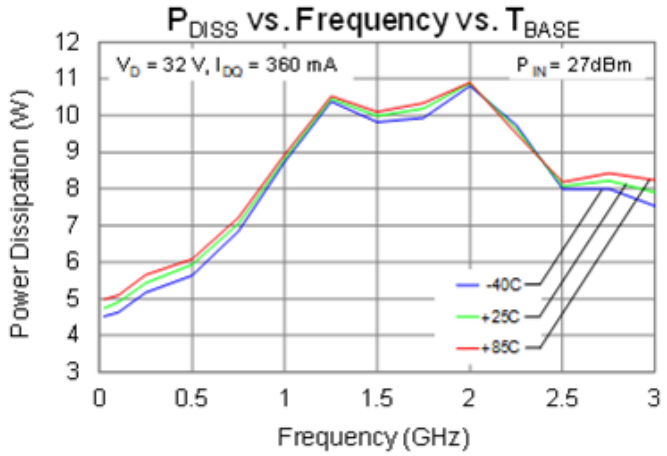


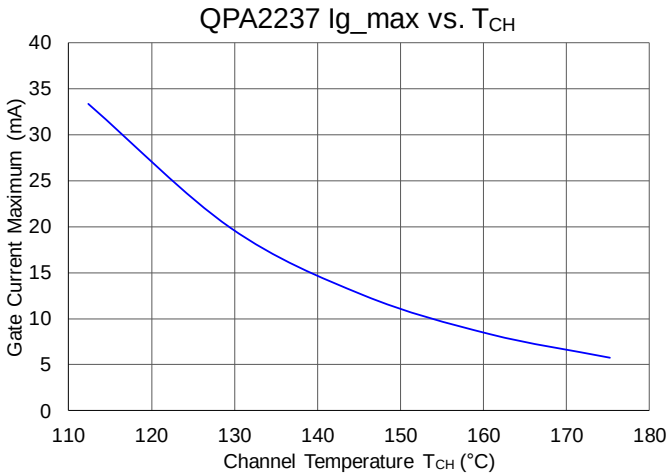
Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	T_{BASE} = 85 °C, V_D = +32 V (CW), Freq = 2.0 GHz P_{IN} = 27 dBm, I_{DQ} = 360 mA, I_{D_Drive} = 648 mA, P_{OUT} = 40 dBm, P_{DISS} = 10.9 W	5.948	°C/W
Channel Temperature (T_{CH}) (Under RF drive) (2)		149.8	°C

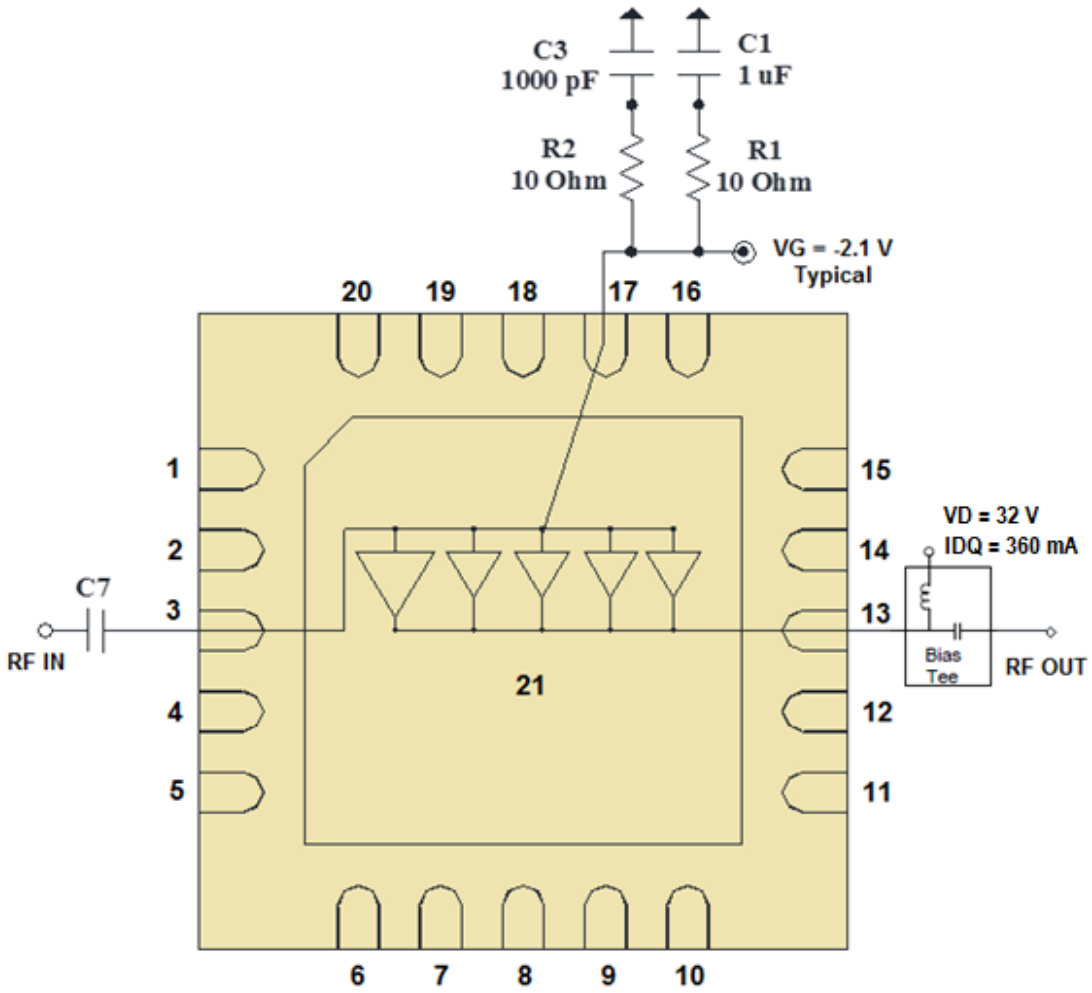
Notes:
1. Thermal resistance referenced to back of package at 85 °C.
2. IR scan equivalent channel temperature. Refer to the following document: GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates

Power Dissipation and Maximum Gate Current





Application Circuit (Coaxial input DC Block and Coaxial Output Bias-T Option)



Notes:

1. Coaxial input DC block (C7) is used for input port (RF In.)
2. External wide bandwidth Bias-Tee is used for output port (RF Out). VD is applied through the output Bias-Tee.
3. Data contained herein taken with this EVB configuration.

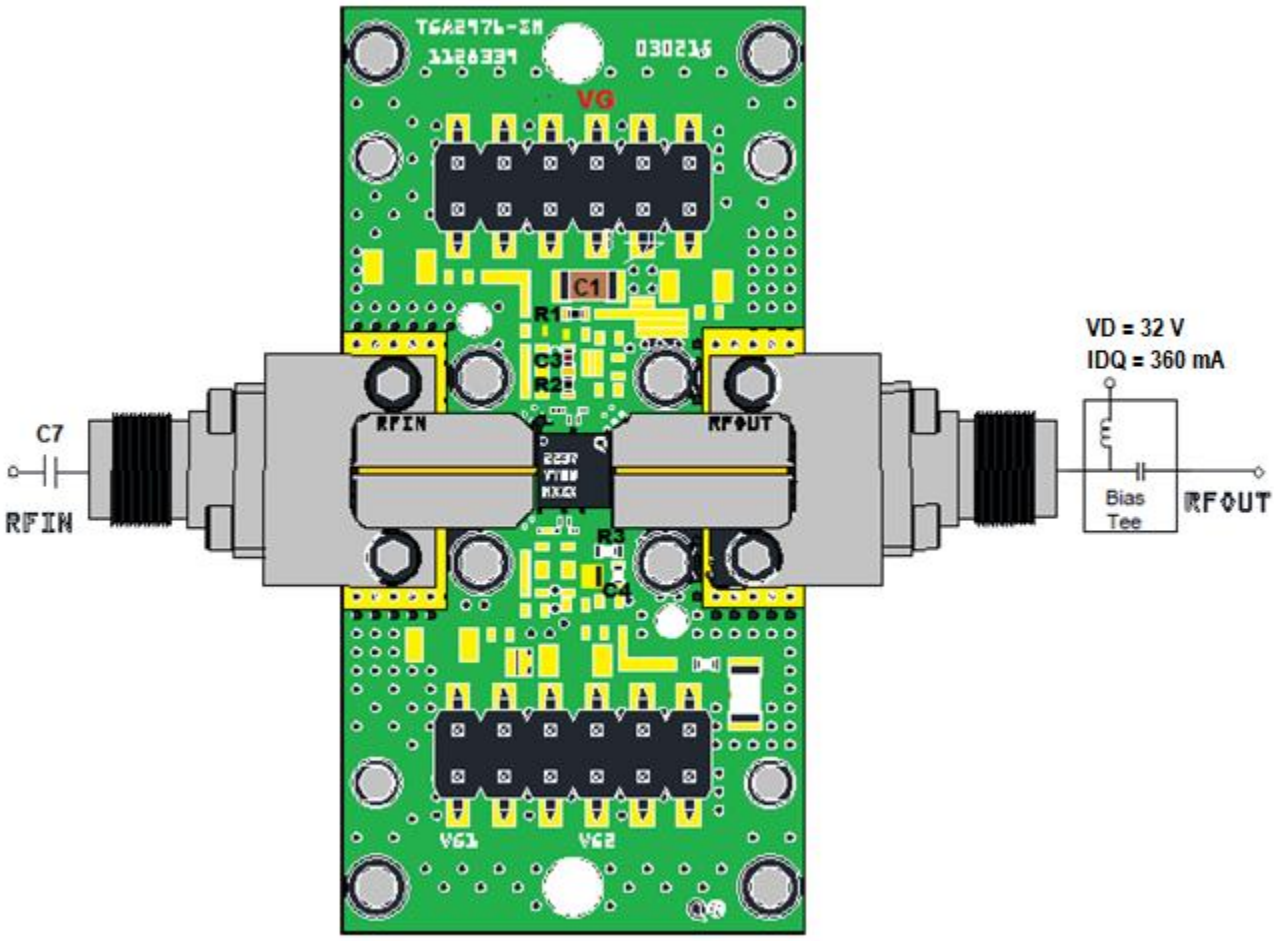
Bias Up Procedure

1. Set I_D limit to 700mA, I_G limit to 15mA
2. Set V_G to -5.0V
3. Set V_D +32V
4. Adjust V_G more positive until I_{DQ} = 360mA (V_G ~ -2.1V Typical)
5. Apply RF signal

Bias Down Procedure

1. Turn off RF signal
2. Reduce V_G to -5.0V. Ensure I_{DQ} ~ 0mA
3. Set V_D to 0V
4. Turn off V_D supply
5. Turn off V_G supply

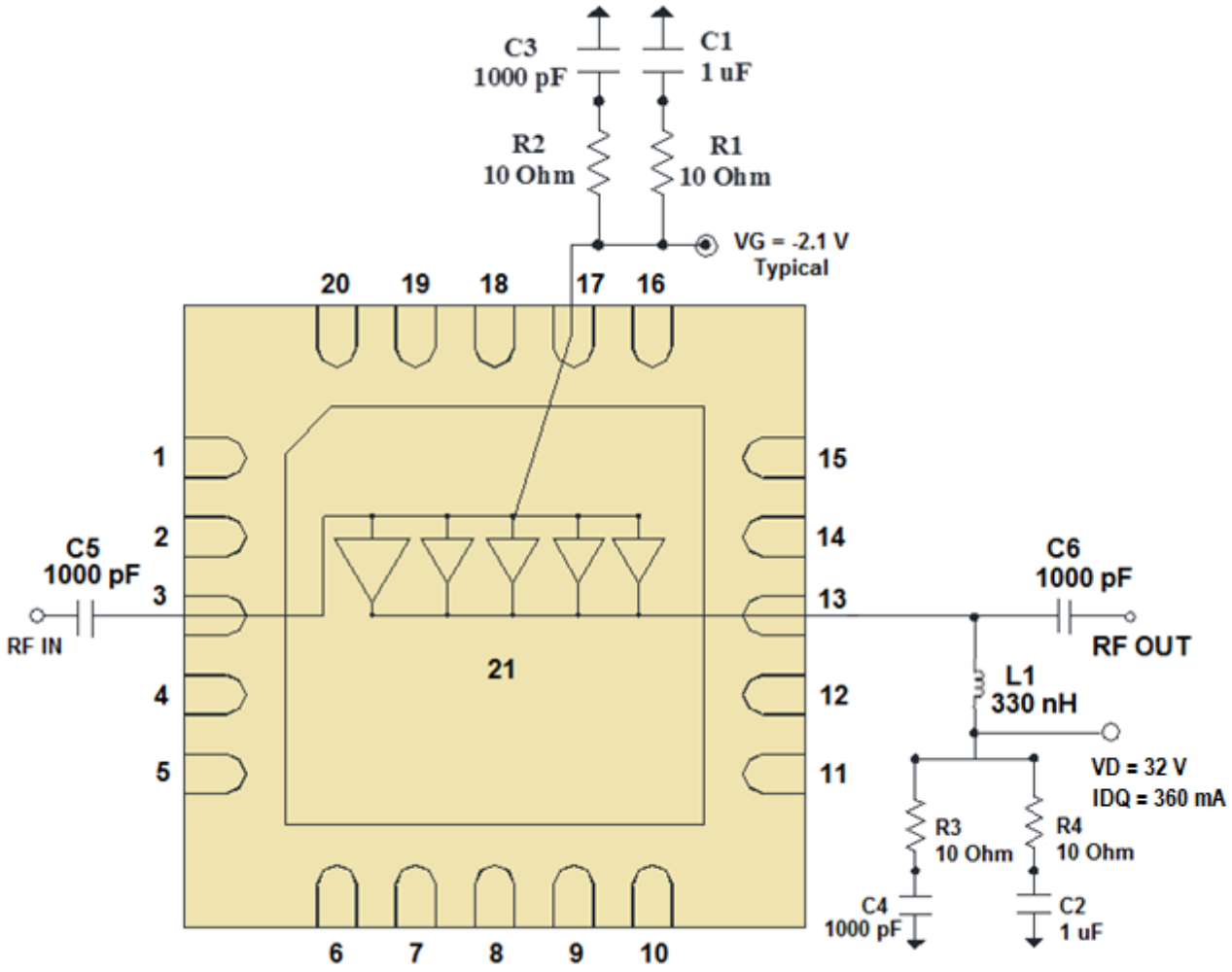
EVB Layout (Coaxial input DC Block and Coaxial Output Bias-T Option)



Bill of Materials

Reference Des.	Value	Description	Manuf.	Part Number
C1	1 uF	Cap, 1206, 50V, 5%, X7R	Various	–
C3	1000 pF	Cap, 0402, 100V, 10%, X7R	Various	–
C7		DC Block	Various	–
R1 – R2	10Ω	Res, 0402, 5%, SMD	Various	–

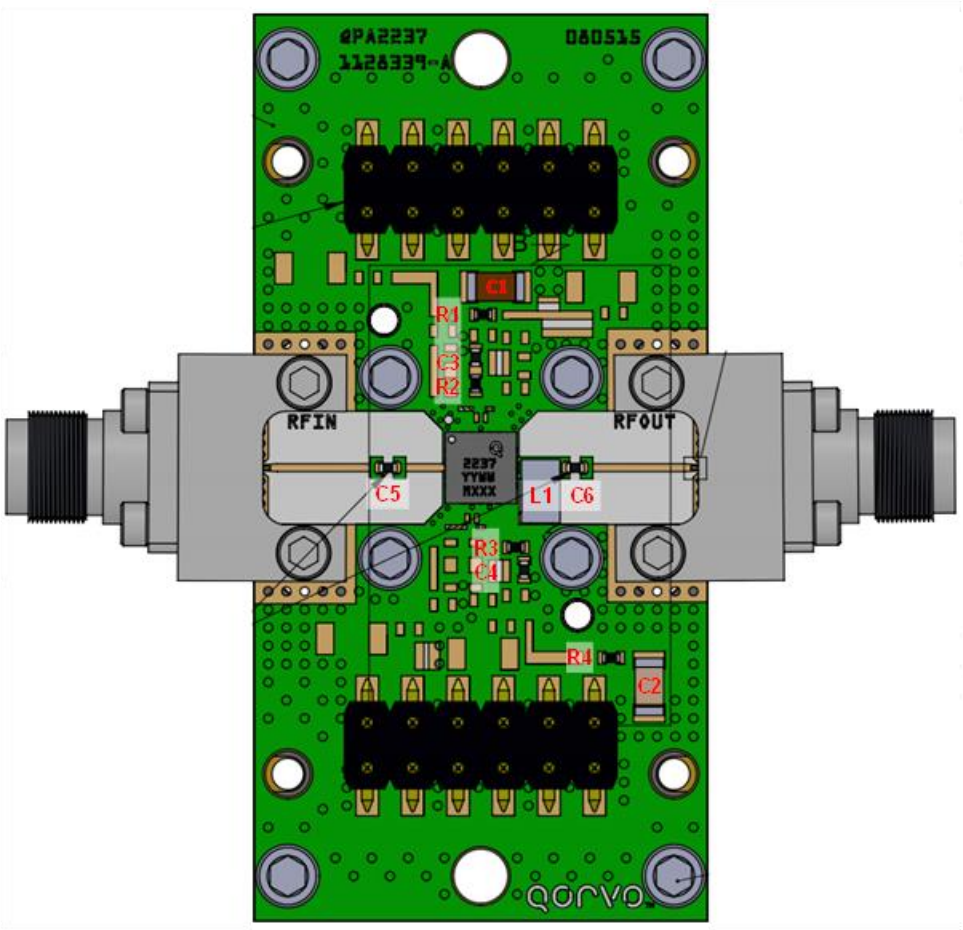
Application Circuit (On-Board DC Blocks and Output Bias-T Option)

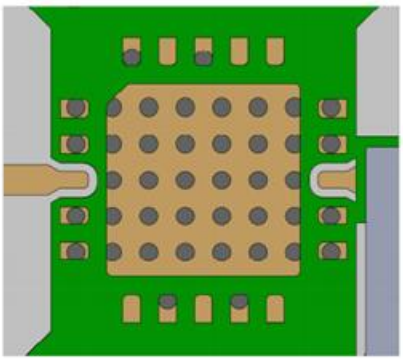


Notes:

1. Performance of the DUT with surface-mount DC blocks and bias tee components may be degraded relative to the coaxial option. These components should be optimized for the desired operational bandwidth.
2. EVBs provided for customer evaluation are provided with this configuration.

EVB Layout (On-Board DC Blocks and Output Bias-T Option)



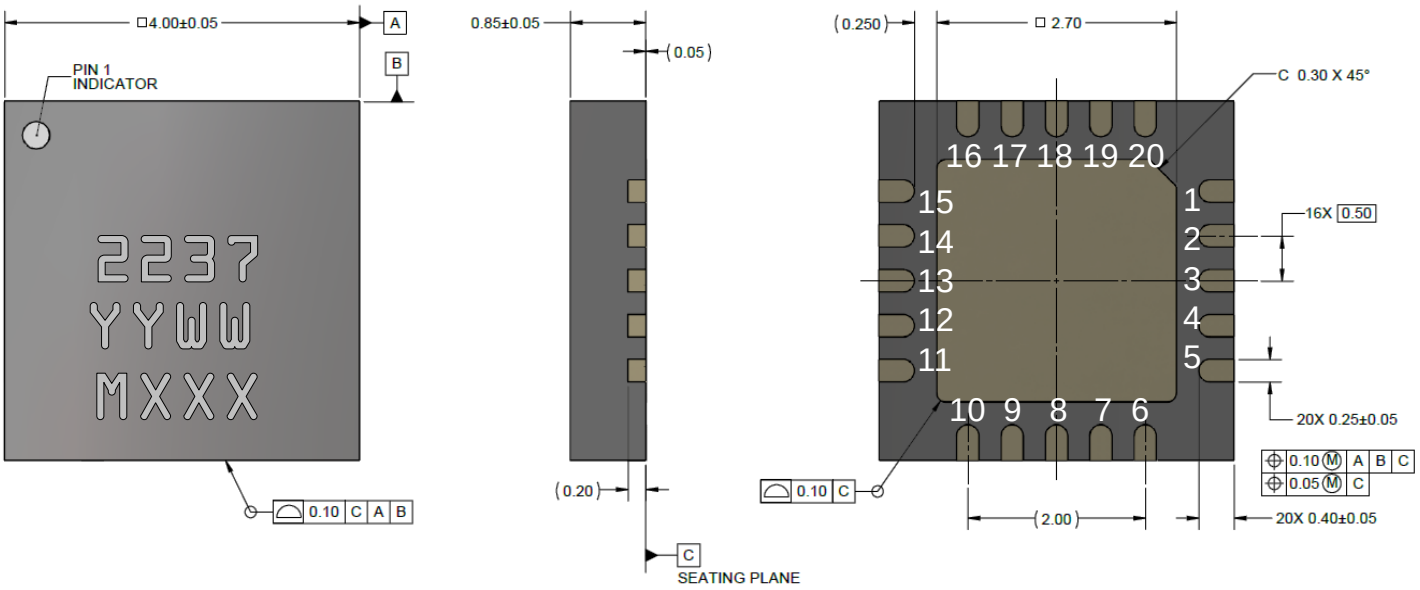


Package Pad Landing Area

Bill of Materials for On-Board Bias-Tee

Reference Des.	Value	Description	Manuf.	Part Number
C1, C2	1 uF	Cap, 1206, 50V, 5%, X7R	Various	–
C3 – C6	1000 pF	Cap, 0402, 100V, 10%, X7R	Various	–
L1	330 nH	Ind, 1206, 850mA, 5%	Various	–
R1 – R4	10Ω	Res, 0402, 5%, SMD	Various	–

Mechanical Information



NOTES (UNLESS OTHERWISE SPECIFIED):
1. ALL DIMENSIONS ARE IN MM
2. PACKAGE LEADS ARE GOLD PLATED
3. PART IS MOLD ENCAPSULATED
4. PART MARKING
   - 2237: PART NUMBER
   - YY: PART ASSEMBLY YEAR
   - WW: PART ASSEMBLY WEEK
   - XXX: BATCH ID

TOLERANCES
.XX = ± .25
.XXX = ± .127
.XXXX = ± .0254

Pin Description

Pin No.	Symbol	Description
1, 2, 4 – 12, 14 – 16, 18 – 20	N/C	No connection
3	RF IN	Input; matched to 50 Ω.
13	RF OUT / V_D	Output and Drain Voltage; matched to 50 Ω.
17	V_G	Gate Voltage, bias network is required; see recommended Application Information on page 11
21	GND	Ground Paddle. Multiple vias should be employed on the PCB to minimize inductance and thermal resistance.

Absolute Maximum Ratings

Parameter	Value / Range
Drain Voltage (V_D)	40 V
Gate Voltage Range (V_G)	-8 to 0 V
Drain Current (I_D)	1.2 A
Gate Current (I_G)	See plot page 10
Power Dissipation (P_{DISS}), 85 °C	19 W
Input Power (P_{IN}), CW, 50 Ω, 85 °C	33 dBm
Input Power (P_{IN}), CW, VSWR 3:1, V_D = 32 V, 85 °C	33 dBm
Max VSWR, CW, P_{IN} = 27 dBm, V_D = 32 V, 85 °C (Load)	10:1
Mounting Temperature (30 Seconds)	260 °C
Storage Temperature	-55 to 150 °C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Soldering Temperature Profile