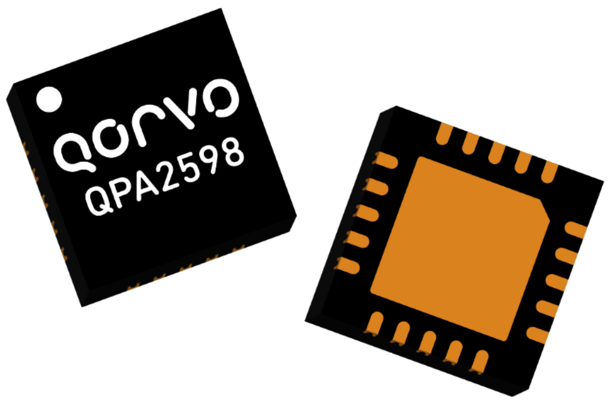
QPA2598

6 – 12 GHz 2.5 W GaN Driver Amplifier

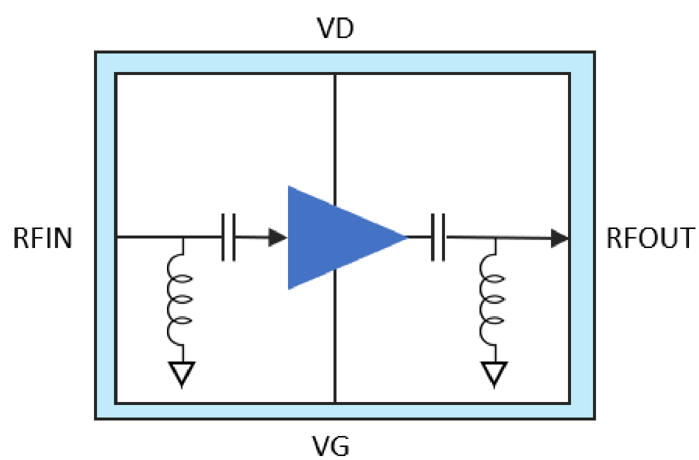
Product Description

Qorvo's QPA2598 is a packaged broadband driver amplifier fabricated on Qorvo's QGaN15 0.15 um GaN on SiC process. Operating from 6 to 12 GHz, the QPA2598 achieves 2.5 W output power with a Power Added Efficiency of 30 % and harmonic suppression of -30dBc. Under nominal bias, it provides 22 dB small signal gain and 16 dB of large signal power gain.

The QPA2598 is available in small form factor 4x4 mm overmold QFN which allows for easy system integration. The QPA2598 is an ideal choice to drive Qorvo's high performing GaN HPAs allowing the user to run both driver and HPA off the same voltage rail.



Functional Block Diagram



Product Features

- Frequency Range: 6 - 12 GHz
- Small Signal Gain: 23 dB (mid-band)
- Pout: 34 dBm (P_{IN} = 18 dBm)
- PAE: 30 % CW
- Power Gain: 16 dB (P_{IN} = 18 dBm)
- Harmonic Suppression -30 dBc (Pin = 18 dBm)
- IM3: - 30 dBc (24 dBm Pout/Tone)
- Input Return Loss: 10 dB
- Output Return Loss: 8 dB
- Bias: V_D = 22 V, I_{DQ} = 55 mA, V_G = - 2.5 V Typical
- Package Dimensions: 4.0 x 4.0 x 0.85 mm

Applications

- Commercial and military radar
- Communications
- Electronic Warfare (EW)

Ordering Information

Part No.	Description
QPA2598	Driver Amplifier, Waffle Pack, Qty 50
QPA2598TR7	Tape and Reel 7 ", Qty 500
QPA2598EVB	QPA2598 Evaluation Board, Qty 1

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Drain Voltage (V_D)		22		V
Drain Current (I_{DQ})		55		mA
Drain Current Under RF Drive (I_{D_DRIVE})		See plots		mA
Gate Voltage (V_G, typical)		−2.5		V
Gate Current Under RF Drive (I_{G_DRIVE})		See plots		mA
Operation Temperature	−40		+85	°C

Electrical performance is measured under conditions noted in the electrical specifications table. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Parameter	Min	Typ	Max	Units
Operational Frequency Range	6		12	GHz
Small Signal Gain (from 6 to 9 GHz)		24		dB
Small Signal Gain (from 10 to 12 GHz)		22		dB
Input Return Loss		-10		dB
Output Return Loss		-8		dB
Output Power (at Pin = 18 dBm)		34		dBm
Power Added Efficiency (at Pin = 18 dBm)		30		%
Power Gain (at Pin = 18 dBm)		16		dB
Harmonic Suppressions (2nd at Pin = 18 dBm)		-30		dBc
IM3 (at Pout/tone = 24 dBm/Tone)		-30		dBc
Small Signal Gain Temperature Coefficient		-0.047		dB/°C
Gate Leakage Current (V_D = 10 V, V_G = -3.7 V)	-1.2	- 0.5	0	mA

Test conditions unless otherwise noted: V_D = +22 V, IDQ= 55 mA, VG = -2.5V typical, CW Mode, 25 °C
Data de-embedded to reference planes

Absolute Maximum Ratings

Parameter	Min Value	Max Value	Units
Drain Voltage (V_D)	-	29.6	V
Gate Voltage Range (V_G)	-8	+1	V
Drain Current (I_D)	-	0.65	A
Gate Current (I_G)	-10	50	mA
Power Dissipation (P_{DISS}), 85 °C	-	9.8	W
Input Power (P_{IN}), CW, 50 Ω, 85 °C,	-	23	dBm
Mounting Temperature (30 Seconds)	-	260	°C
Storage Temperature	-55	150	°C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

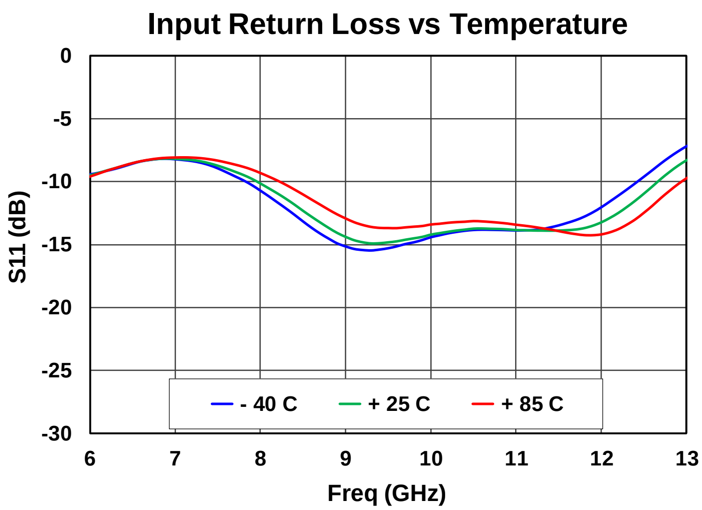
Thermal and Reliability Information

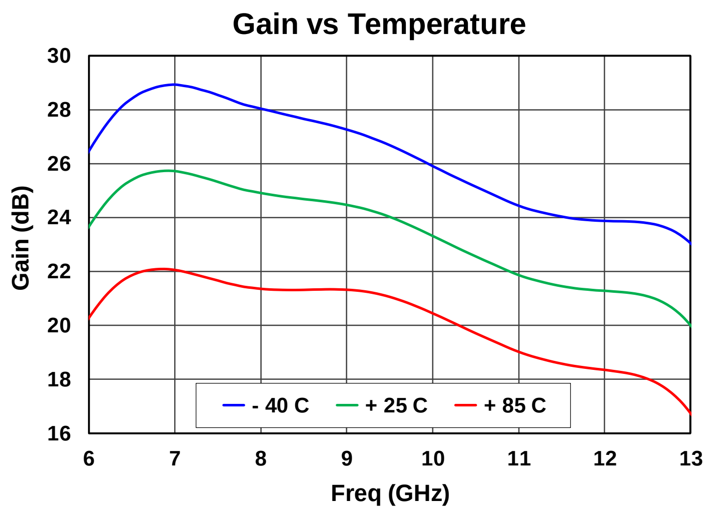
Parameter	Values	Units	Conditions
Under Drive, Thermal Resistance (θ_{JC}) (1,2,3)	10.98	°C/W	T_{BASE} = 85 °C, V_D = +22 V, CW Freq = 10 GHz, I_{D_DRIVE} = 394 mA P_{IN} = +18 dBm, P_{OUT} = +34 dBm, P_{DISS} = 6.18 W
Channel Temperature (T_{CH})	152.86	°C	

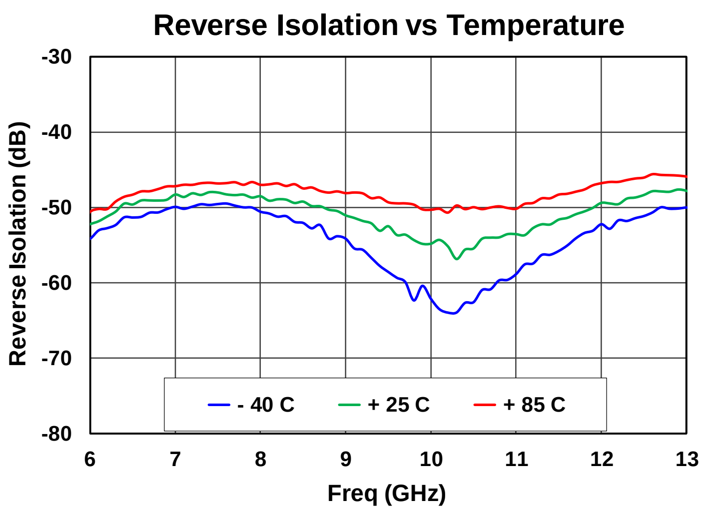
Notes:
1. Thermal resistance is referenced to package backside
2. Base or ambient temperature is 85 ˚C
3. Refer to the following document: GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates

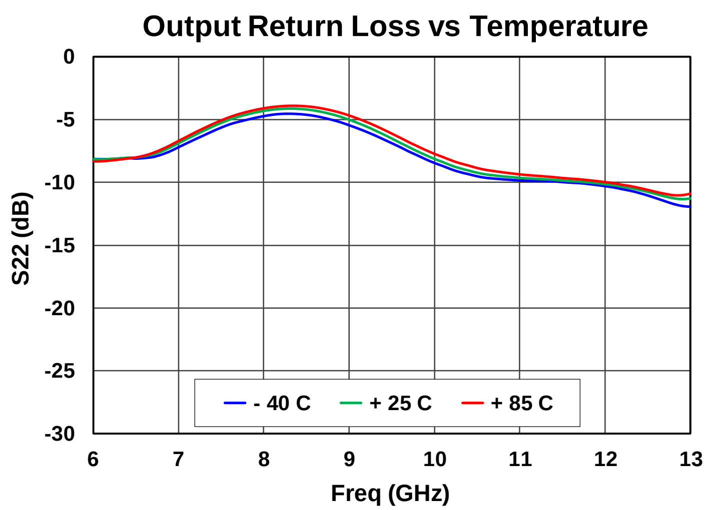
Performance Plots – Small Signal

Test conditions unless otherwise specified: V_D = 22 V, I_{DQ} = 55 mA, V_G = -2.5 V Typical, 25 °C





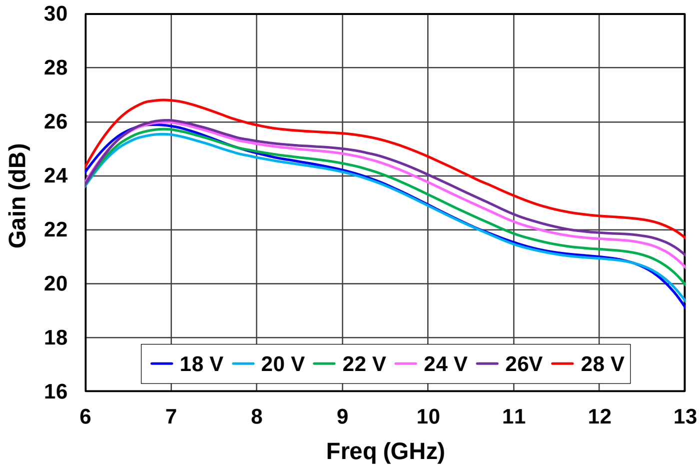




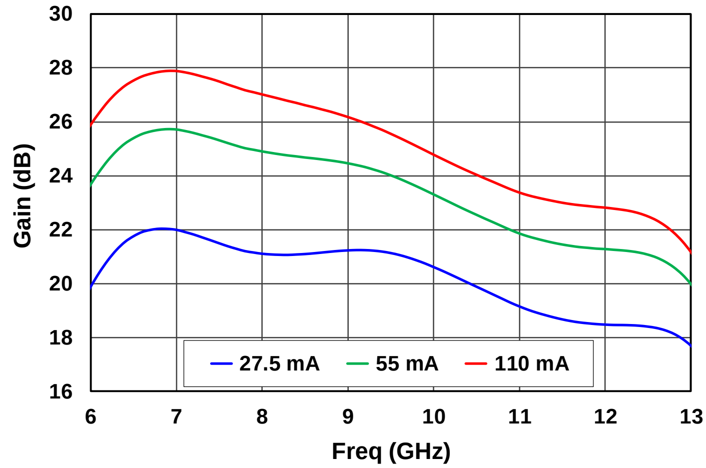
Performance Plots – Small Signal

Test conditions unless otherwise specified: V_D = 22 V, I_{DQ} = 55 mA, V_G = -2.5 V Typical, 25 °C

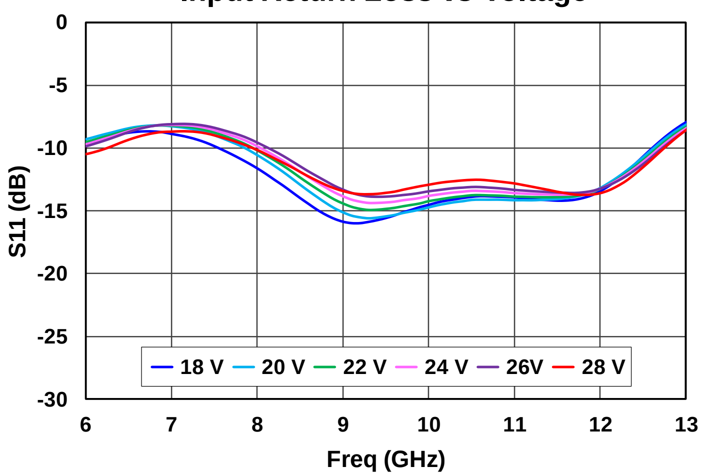
Gain vs Voltage



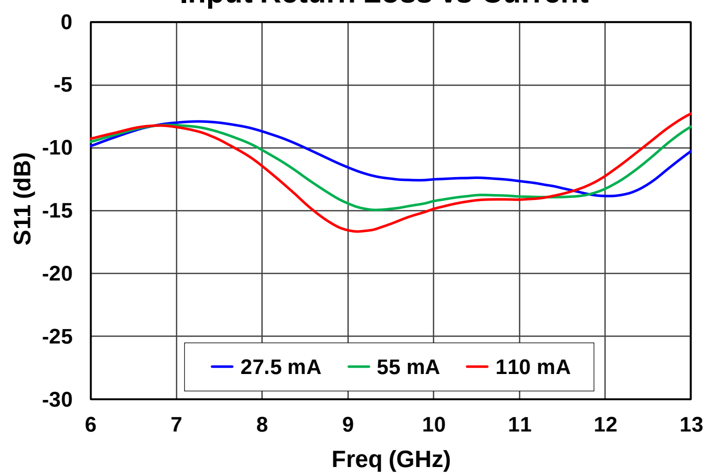
Gain vs Current



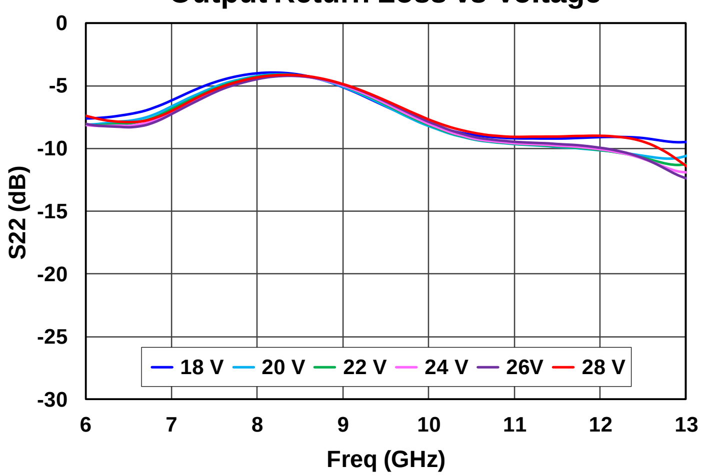
Input Return Loss vs Voltage



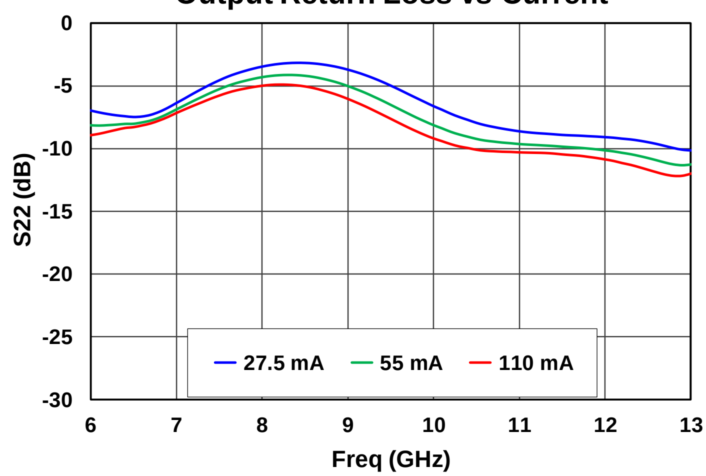
Input Return Loss vs Current



Output Return Loss vs Voltage

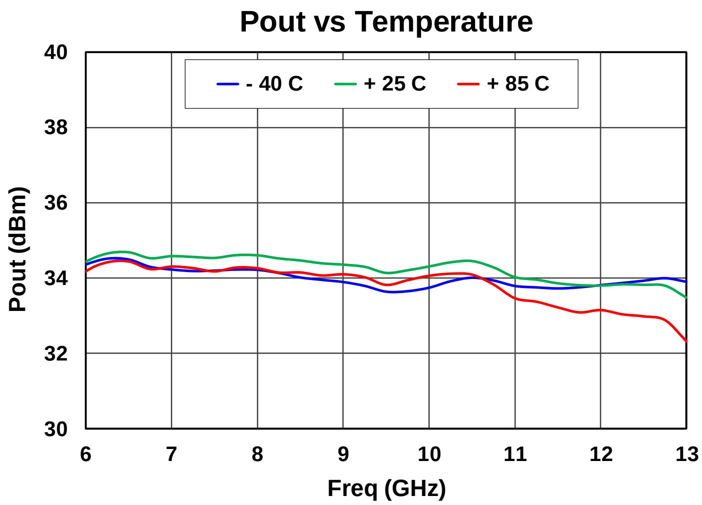


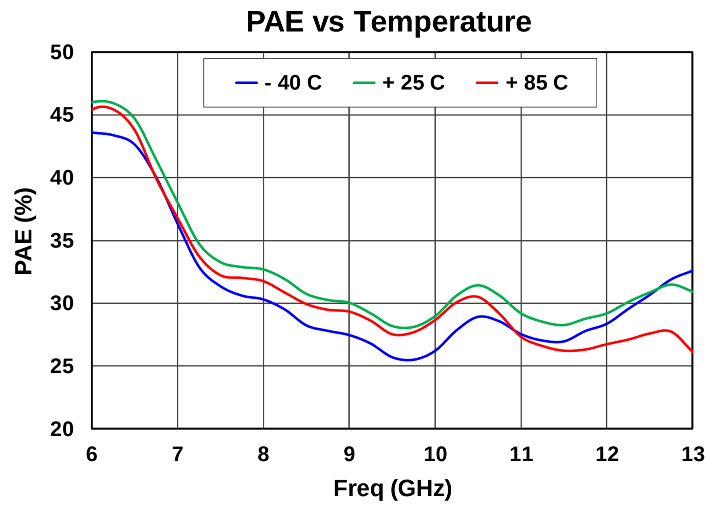
Output Return Loss vs Current

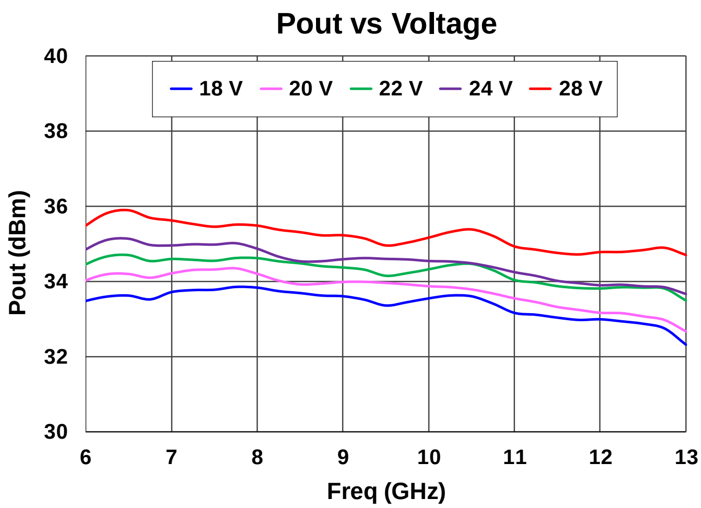


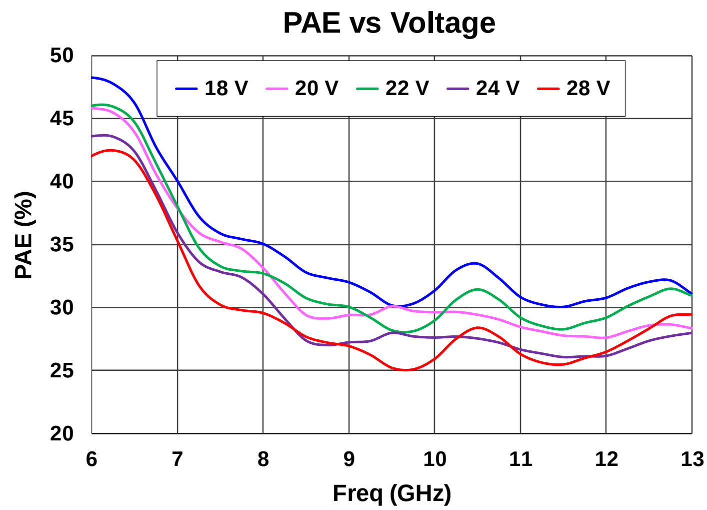
Performance Plots – Large Signal

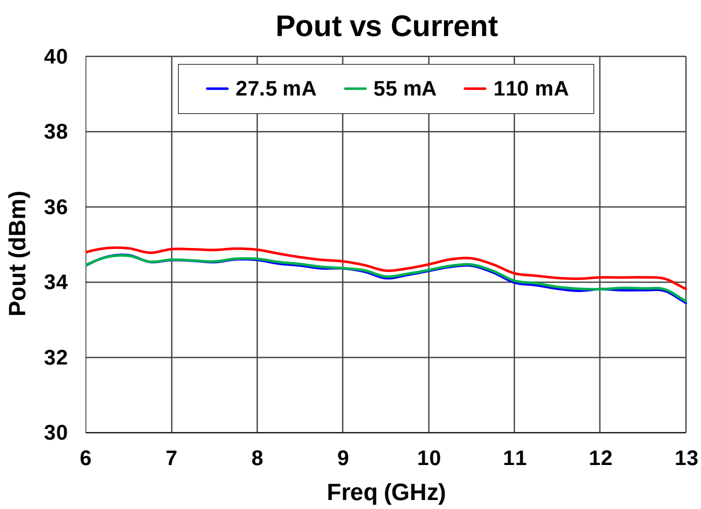
Test conditions unless otherwise specified: V_D = 22 V, I_{DQ} = 55 mA, Pin = 18 dBm, V_G = -2.5 V Typical, CW, 25 °C

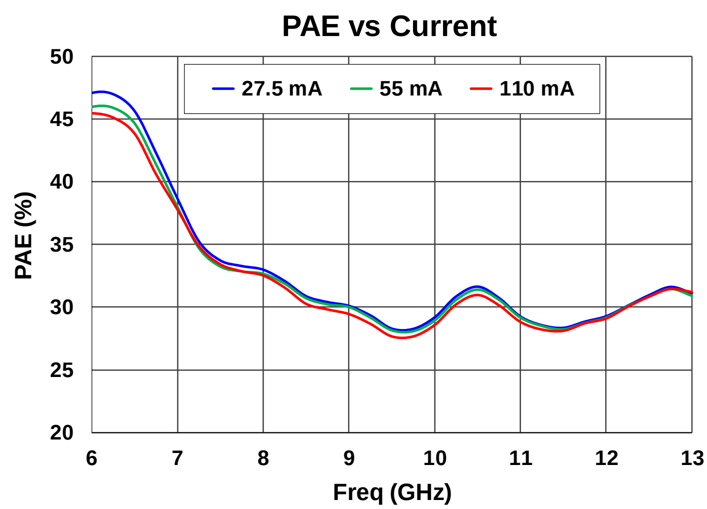






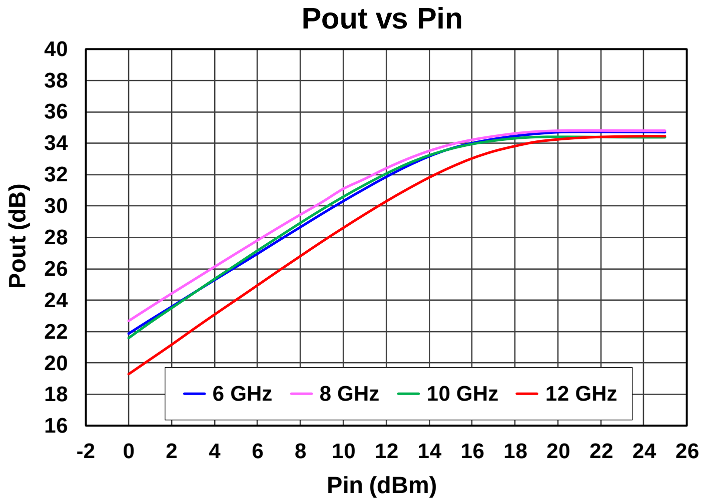


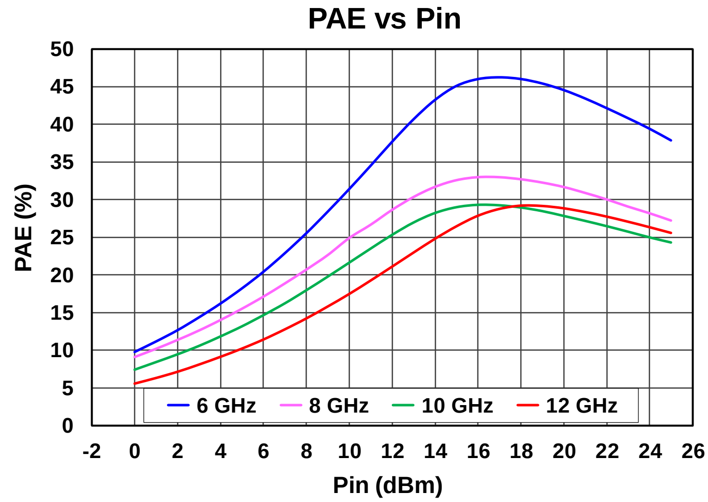


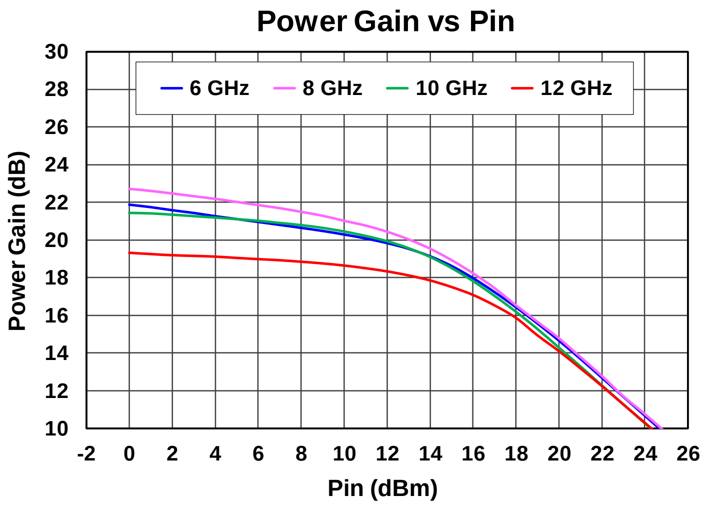


Performance Plots – Large Signal

Test conditions unless otherwise specified: V_D = 22 V, I_{DQ} = 55 mA, V_G = -2.5 V Typical, CW, 25 °C







Performance Plots – Large Signal

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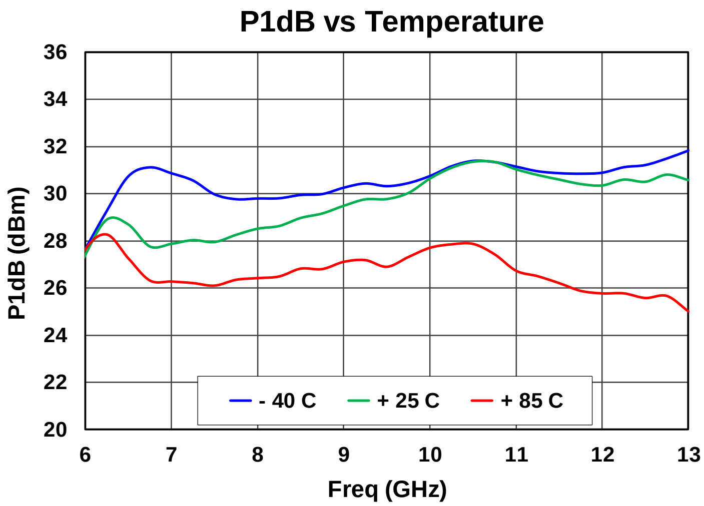
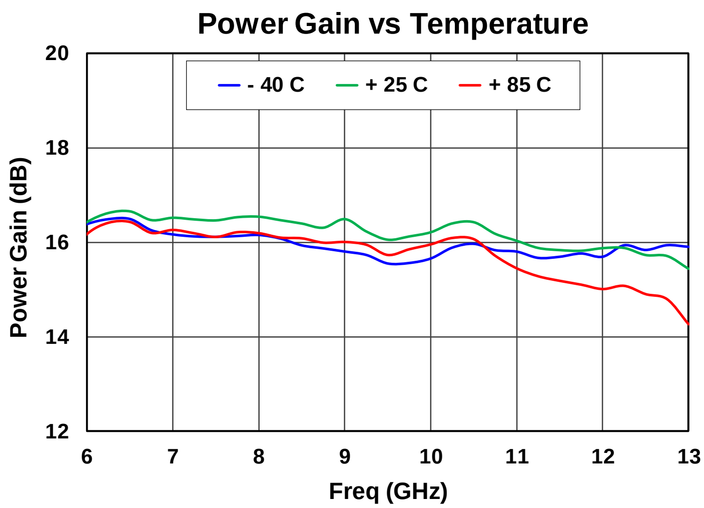
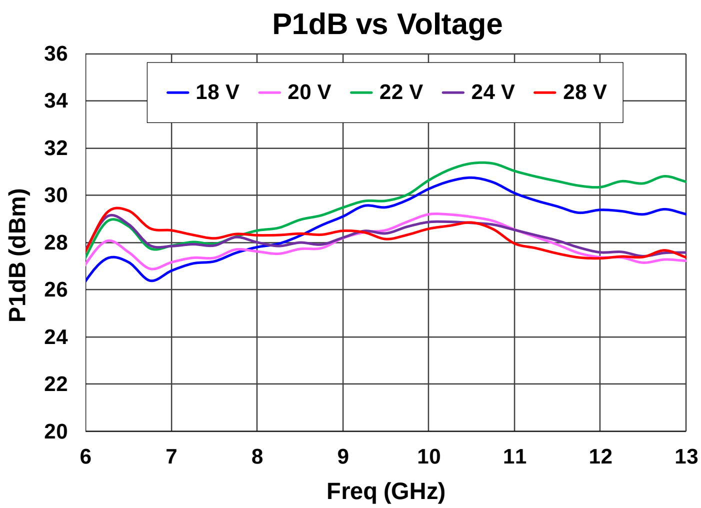
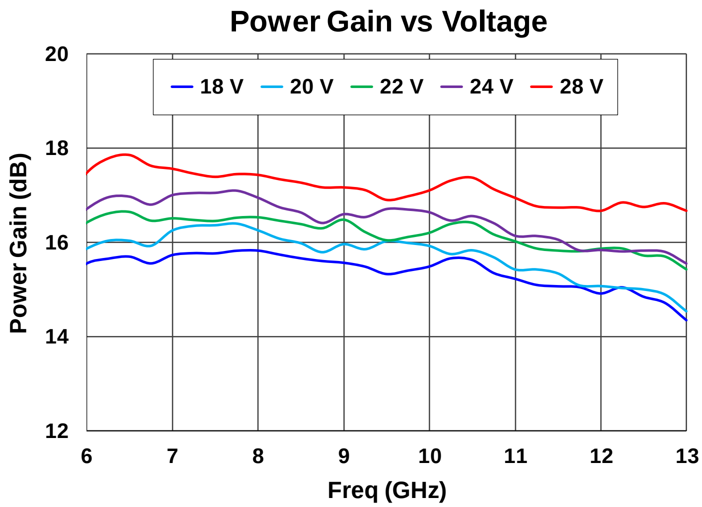
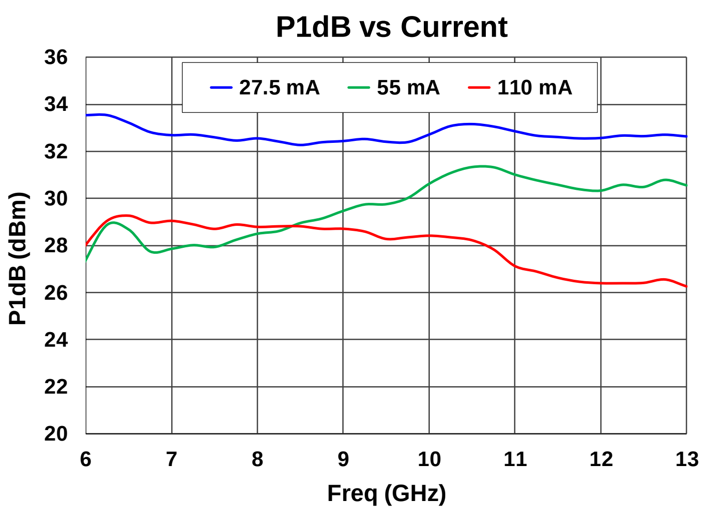
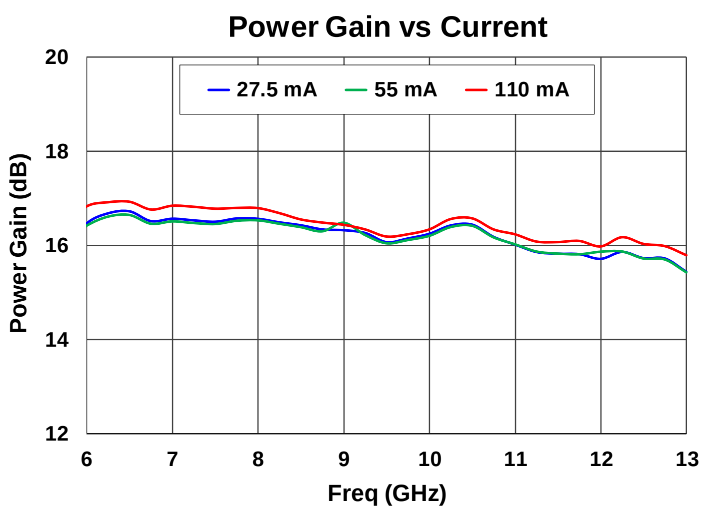








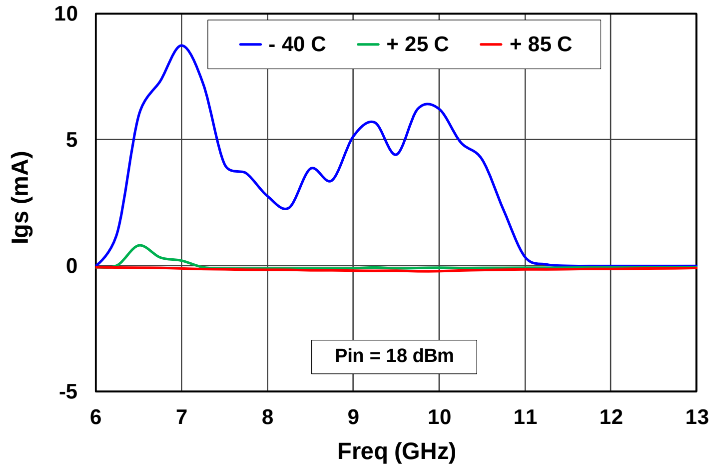




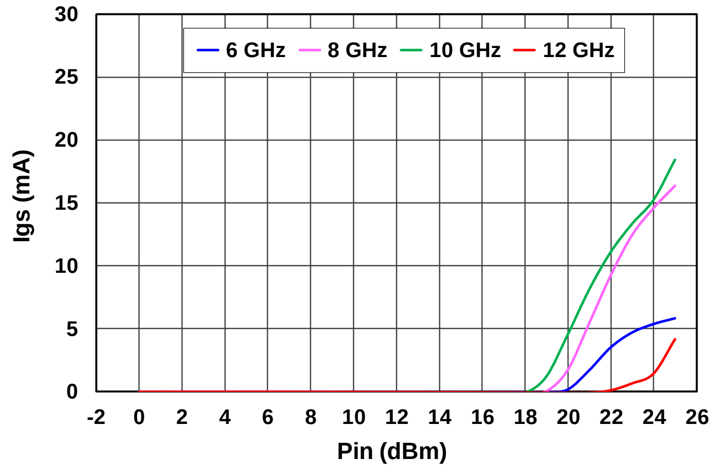
Performance Plots – Large Signal

Test conditions unless otherwise specified: V_D = 22 V, I_{DQ} = 55 mA, V_G = -2.5 V Typical, CW, 25 °C

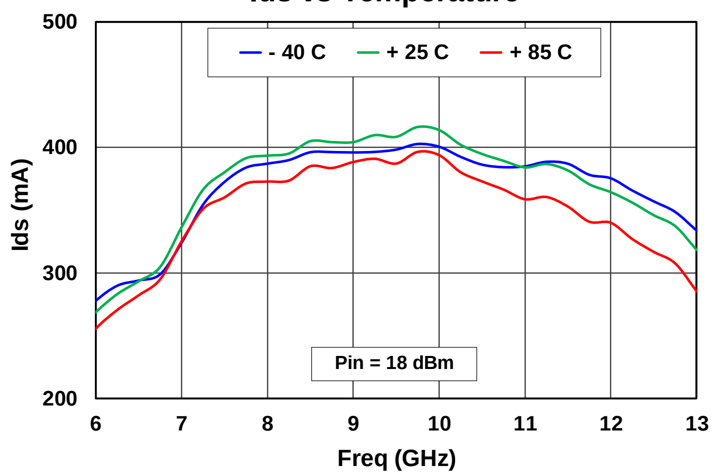
Igs vs Temperature



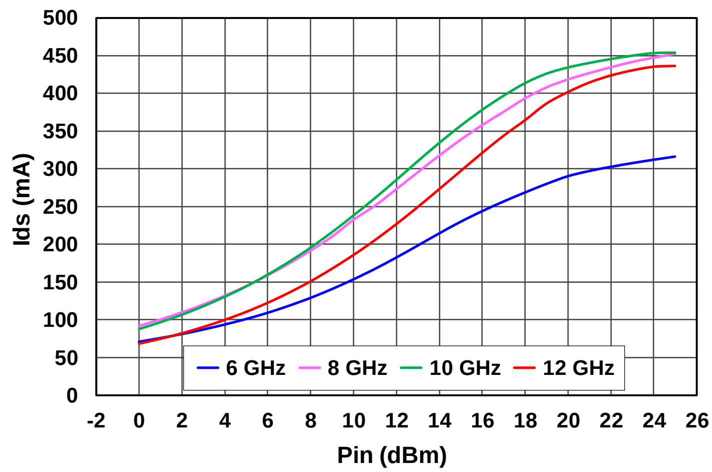
Igs vs Pin



Ids vs Temperature

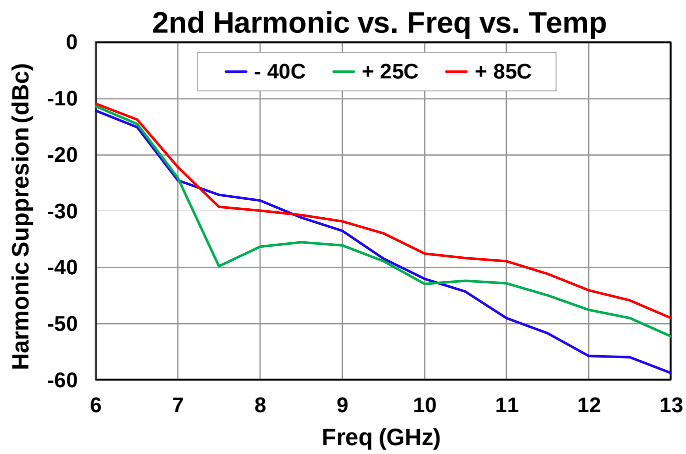


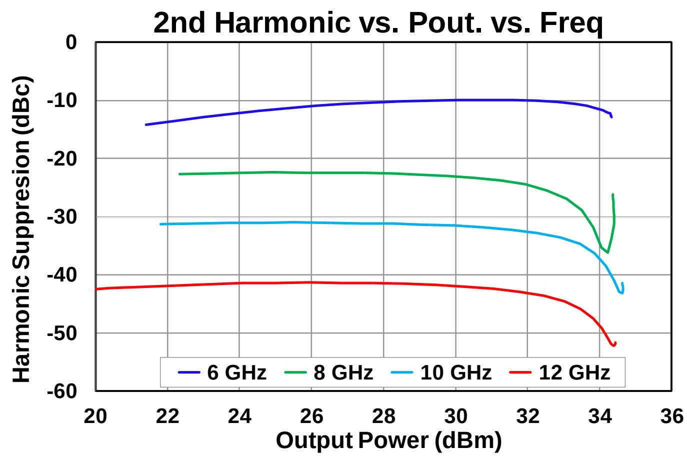
Ids vs Pin

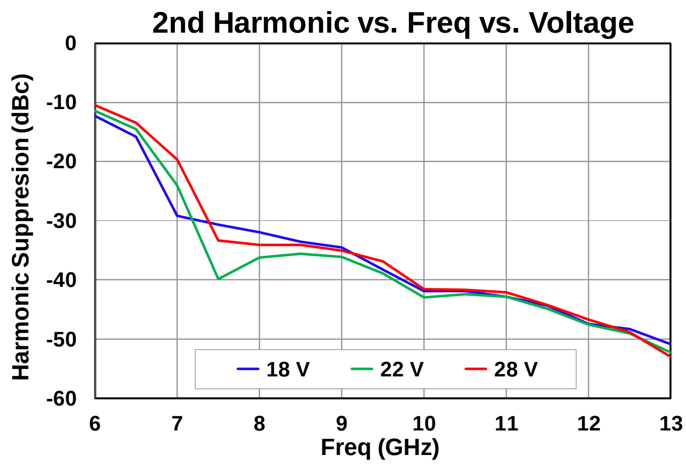


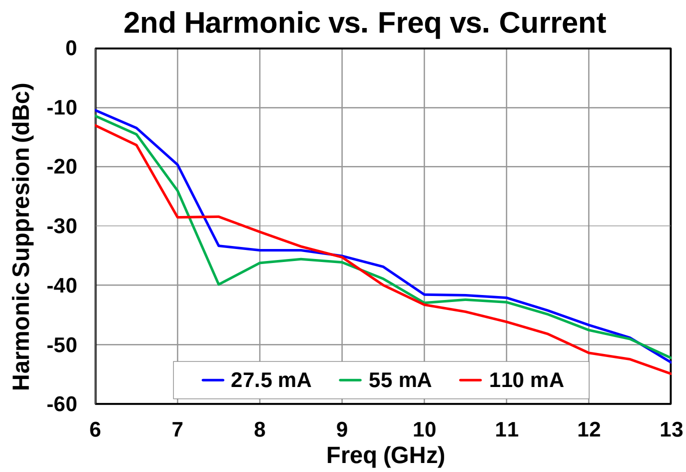
Performance Plots – Harmonics

Test conditions unless otherwise specified: V_D = 22 V, I_{DQ} = 55 mA, V_G = -2.5 V Typical, Pin = 18 dBm, 25 °C



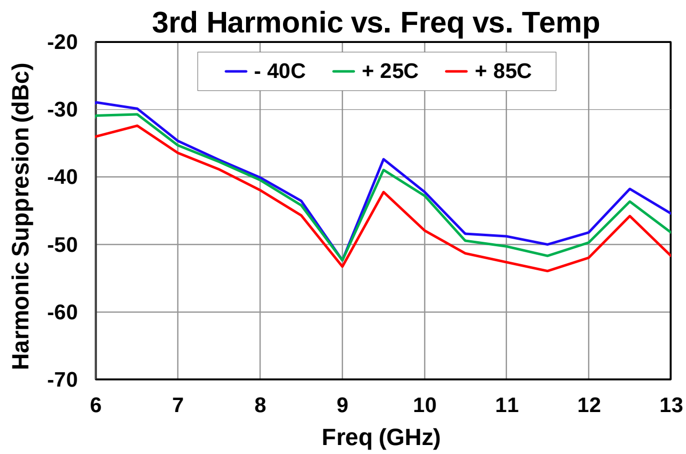


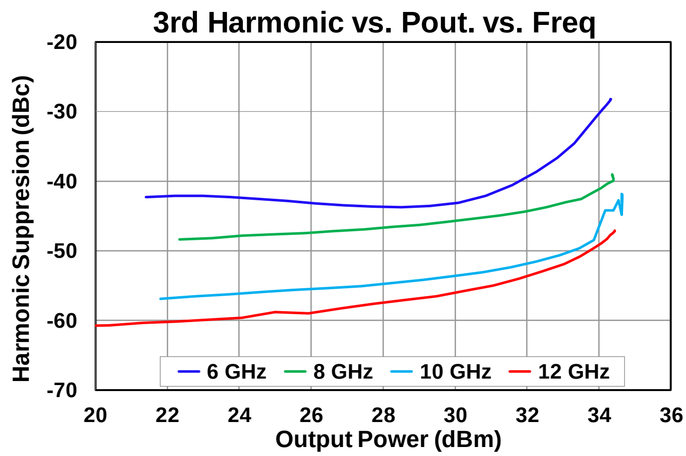


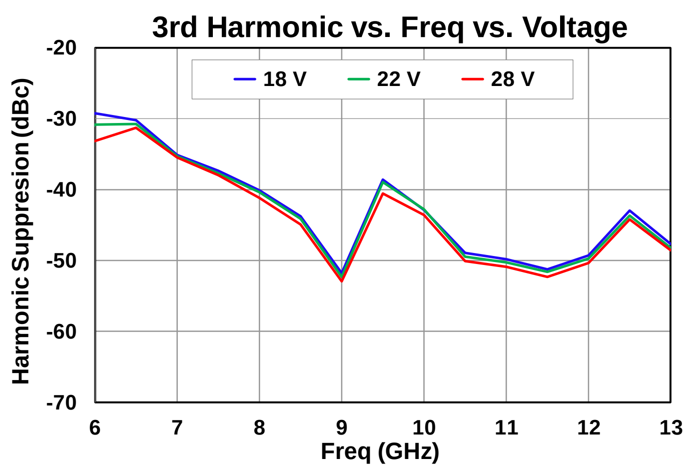


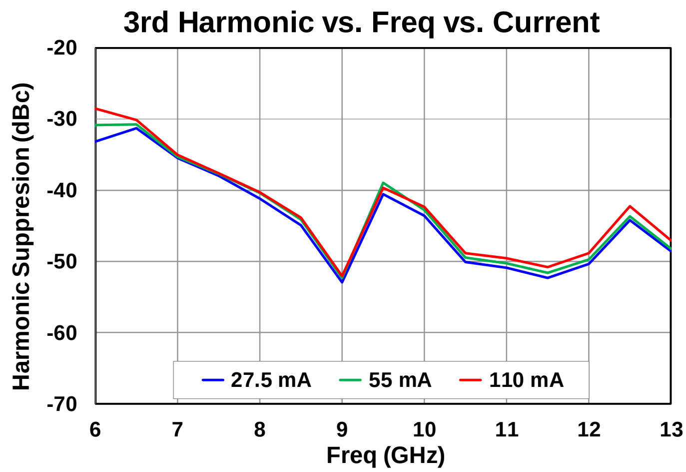
Performance Plots – Harmonics

Test conditions unless otherwise specified: V_D = 22 V, I_{DQ} = 55 mA, V_G = -2.5 V Typical, Pin = 18 dBm, 25 °C



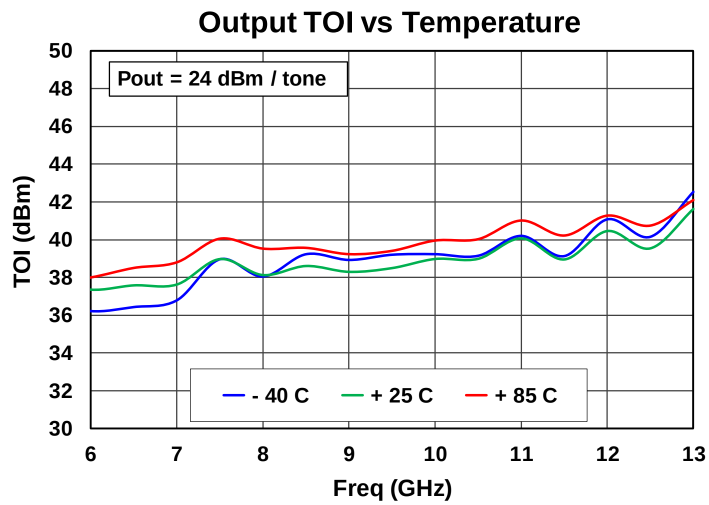


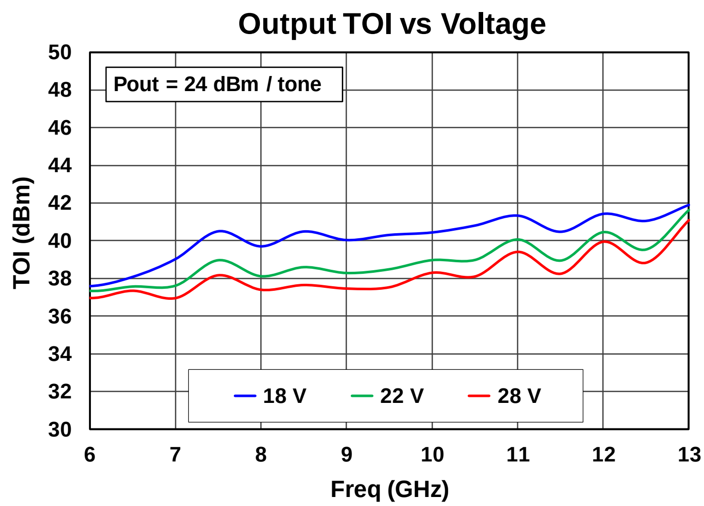


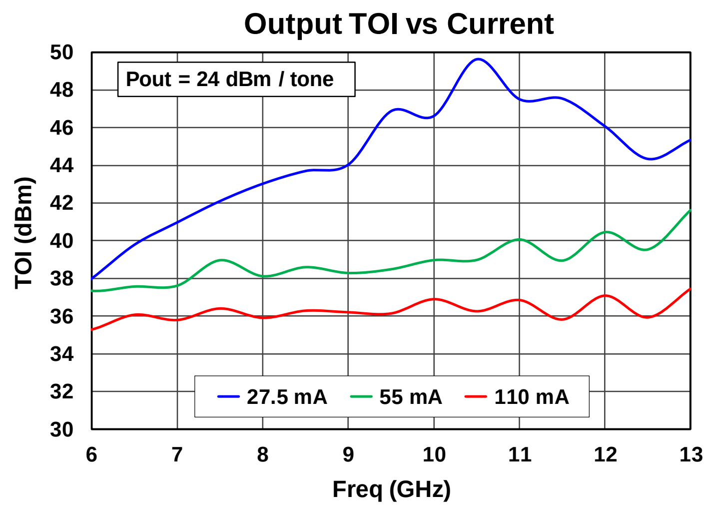


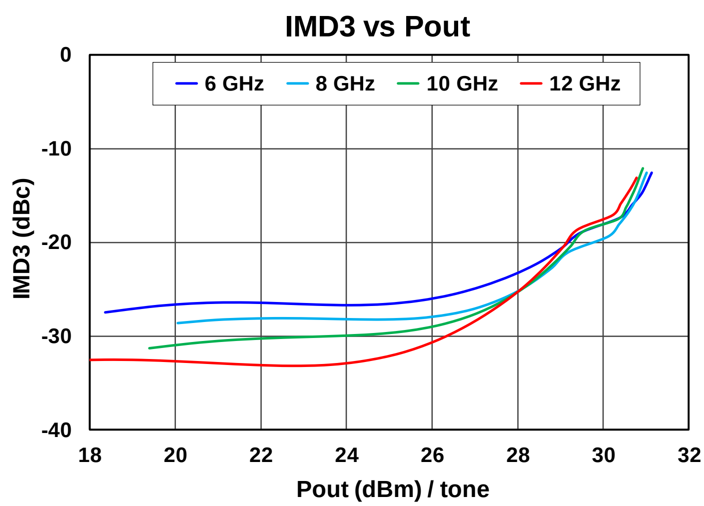
Performance Plots – Linearity

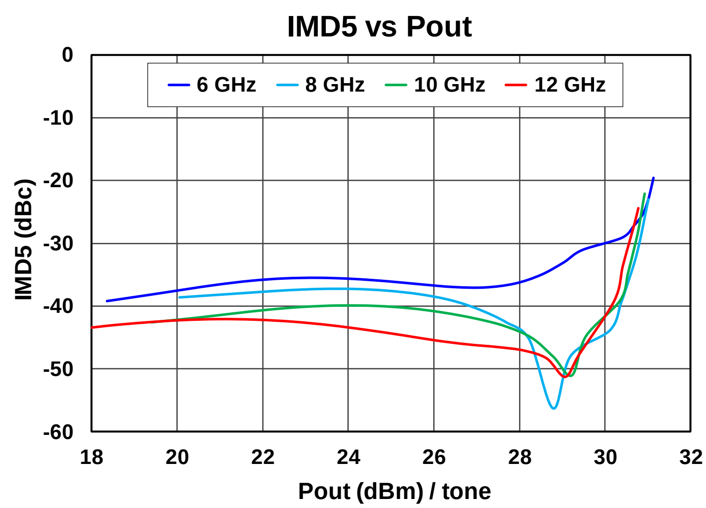
Test conditions unless otherwise specified: V_D = 22 V, I_{DQ} = 55 mA, V_G = -2.5 V Typical, Tone Spacing = 10 MHz, 25 °C



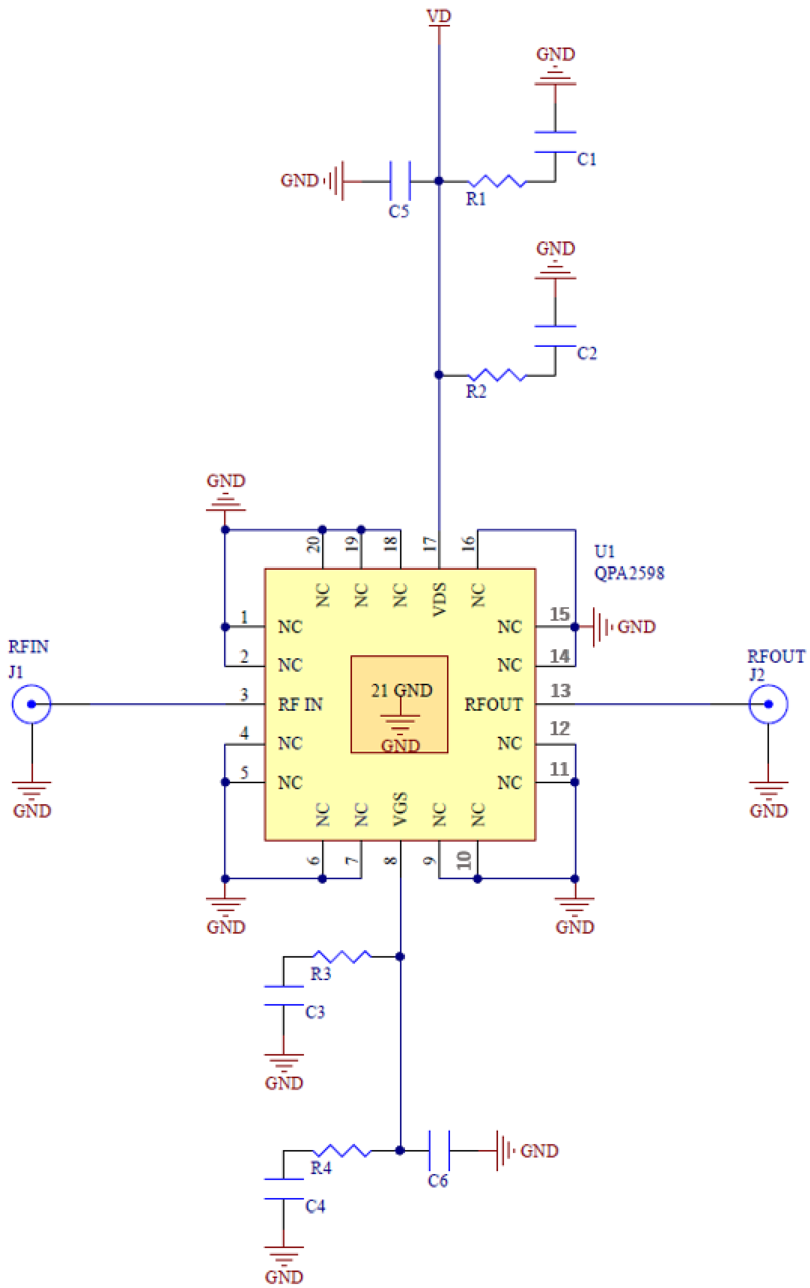








Application Circuit



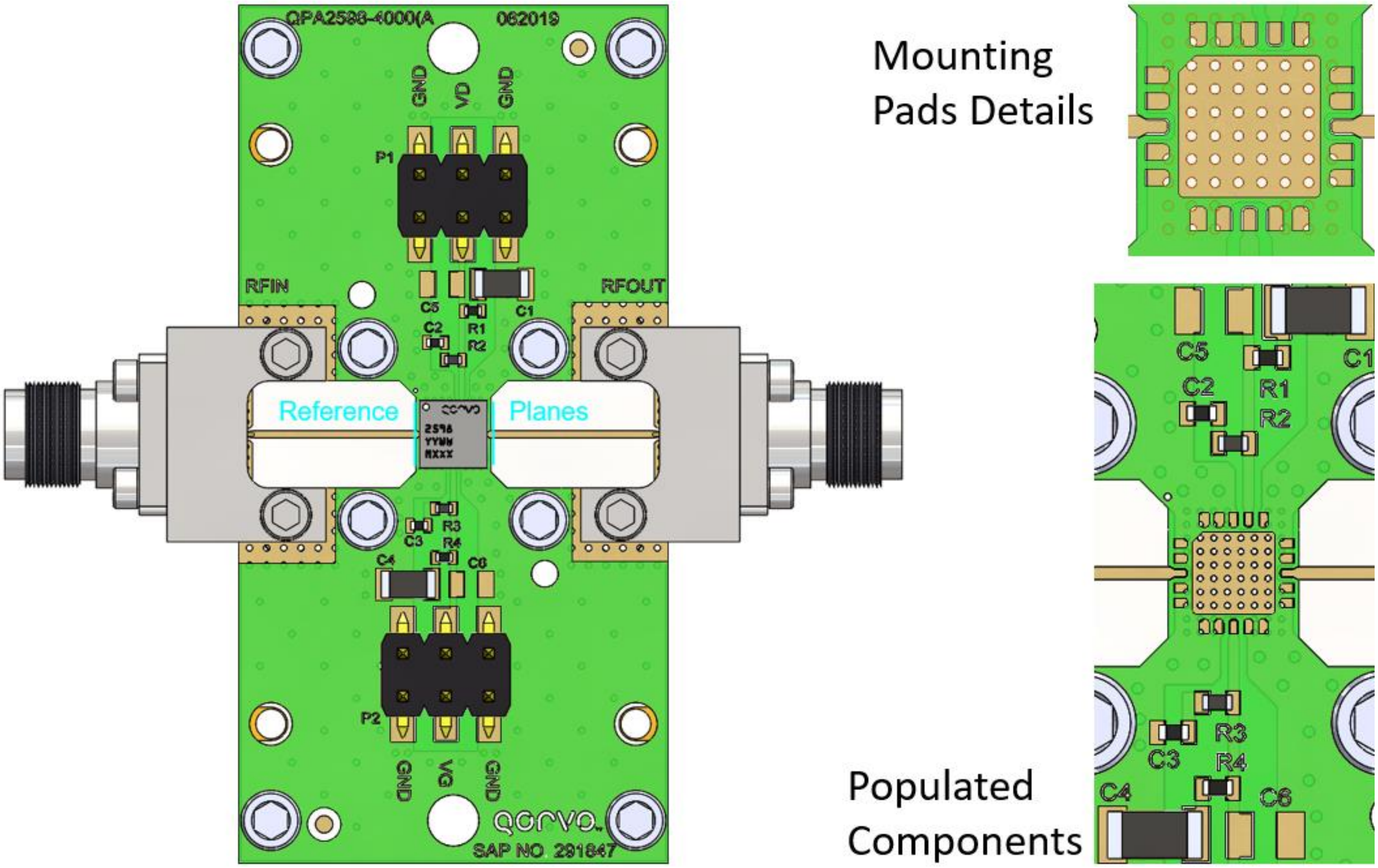
Bias Up Procedure

1. Set I_D limit to 650 mA, I_G limit to 50 mA
2. Apply −5 V to V_G
3. Apply +22 V to V_D; ensure I_{DQ} is approx. 0 mA
4. Adjust V_G until I_{DQ} = 55 mA (V_G ~ −2.5 V Typ.).
5. Turn on RF

Bias Down Procedure

1. Turn off RF
2. Reduce V_G to −5 V; ensure I_{DQ} is approx. 0 mA
3. Set V_D to 0 V
4. Turn off V_D supply
5. Turn off V_G supply

EVB and BOM



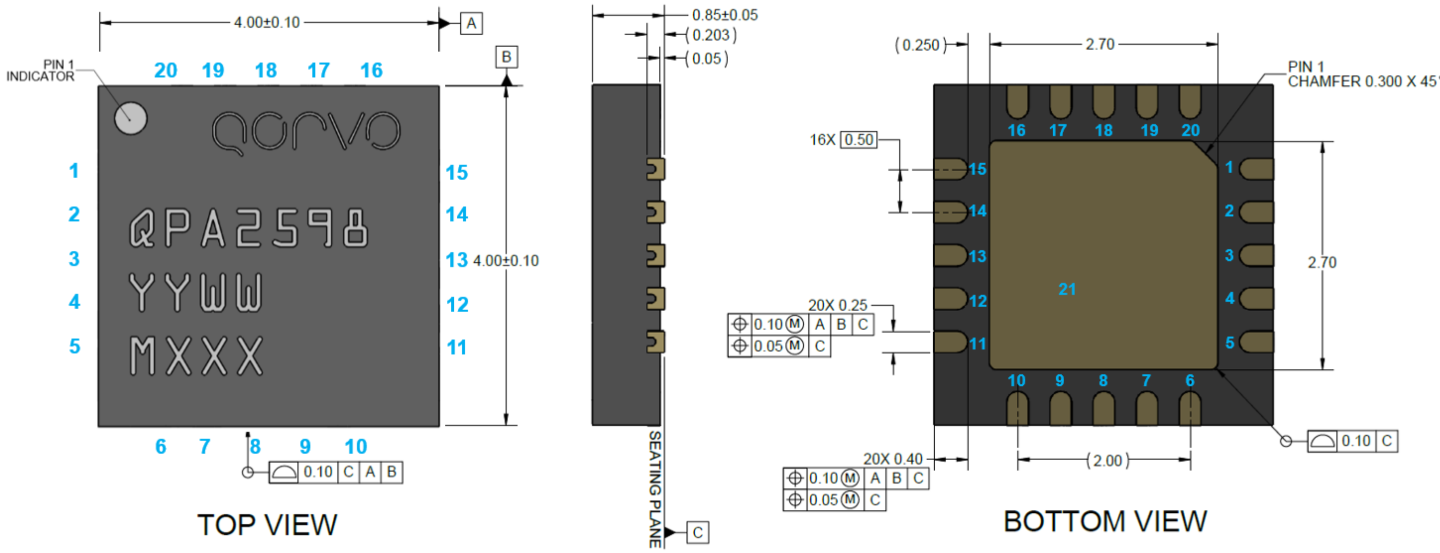
PCB core material is Rogers Corp. RO4003C, RF Layer is 0.008" thick, ε_r = 3.38. Metal layers are 0.5 oz. copper.
The microstrip line at the connector interface is optimized for the Southwest Microwave end launch connector 1092-01A-5.

The trace pattern shown has been developed and tested for optimized assembly at Qorvo. The PCB land pattern has been developed to accommodate lead tolerances. Since processes vary from company to company, careful process development is recommended.

Bill of Materials

Reference Des.	Value	Description	Manuf.	Part Number
C1, C4	10 µF	Cap, 1206, X5R	Various	
C2, C3	1000 pF	Cap, 0402, X7R	Various	
R1, R4	0 Ohms	Resistor, 1/10 W, 0402	Various	
R2, R3	1.8 Ohms	Resistor, 1/10 W, 5%, 0402	Various	
J1, J2	-	2.92 MM RF CONNECTOR	Southwest Microwave	1092-01A-5

Pin Configuration and Description



Dimensions in mm, Package is mold encapsulated with NiPdAu plated leads
Part Marking: QPA2598: Part Number, YY = Part Assembly Year, WW = Part Assembly Week, MXXX = Batch ID

Pin No.	Label	Description
1, 2, 4 - 7, 9 - 12, 14 – 16, 18 - 20	NC	No internal connection, can be grounded
3	RFIN	Input; Matched to 50 Ω; DC grounded
8	V_G	Gate Voltage; Bias network required; see recommended application circuit
13	RFOUT	Output; Matched to 50 Ω; DC grounded
17	V_D	Drain voltage; Bias network is required, see recommended application circuit
21	GND	Slug ground

Solderability

1. Compatible with the latest version of J-STD-020, Lead-free solder, 260 °C.

Recommended Soldering Temperature Profile