QPA2626

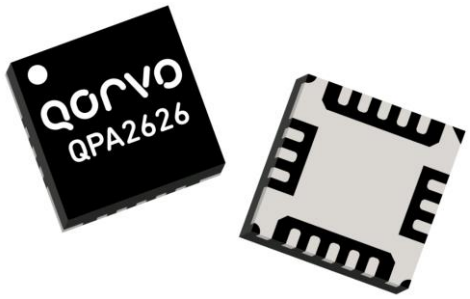
17 – 22 GHz GaAs Low Noise Amplifier

Product Description

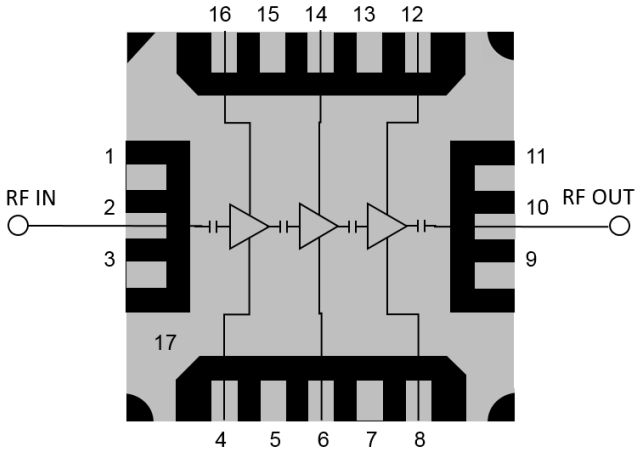
Qorvo's QPA2626 is a packaged, high-performance, low noise amplifier fabricated on Qorvo's production 90nm pHEMT (QPHT09) process. Covering 17 – 22 GHz, the QPA2626 provides 25 dB small signal gain and P1dB of 20 dBm, while supporting a noise figure of 1.3 dB and IM3 levels of −55 dBc (at Pout=0 dBm/tone).

Packaged in a small 4 mm x 4 mm plastic overmold QFN, the QPA2626 is matched to 50 ohms with integrated DC blocking caps on both I/O ports for easy handling and simple system integration.

The QPA2626 high performance and ease of handling makes it ideal for satellite and point to point communication systems.



Functional Block Diagram



Product Features

- Frequency Range: 17 – 22 GHz
- Noise Figure: 1.3 dB
- Small Signal Gain: 25 dB
- P1dB: 20 dBm
- IM3: −55 dBc (@ Pout=0 dBm/tone)
- Bias: V_D = 3.5 V, I_{DQ} = 90 mA, V_G = −0.46 V
- Plastic Overmolded Package
- Package Dimensions: 4.0 x 4.0 x 0.85 mm

Performance is typical across frequency. Please reference electrical specification table and data plots for more details.

Ordering Information

Part	Description
QPA2626TR7	Tape and Reel, 7" reel, Qty 500
QPA2626EVB1	QPA2626 Evaluation Board, Qty 1

Applications

- Satellite Communications
- Point- to - Point Communications

Absolute Maximum Ratings

Parameter	Value	Units
Drain Voltage (V_D)	4.5	V
Drain Current ($I_{D1}/I_{D2}/I_{D3}$)	45/45/160	mA
Gate Voltage Range	-1.3 to 0	V
Gate Current ($I_{G1}/I_{G2}/I_{G3}$ at 125 °C)	5.0/5.0/6.6	mA
RF Input Power (50 Ω, 85 °C)	20	dBm
Channel Temperature, T_{CH}	175	°C
Mounting Temperature (30 seconds)	260	°C
Storage Temperature	−55 to 150	°C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter	Value	Units
Drain Voltage	3.5	V
Drain Current (quiescent, I_{DQ})	90	mA
Drain Current (I_D, Low noise / P_{SAT})	90 / 175	mA
Gate Voltage (typical)	−0.46	V
Operating Temperature Range	−40 to 85	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

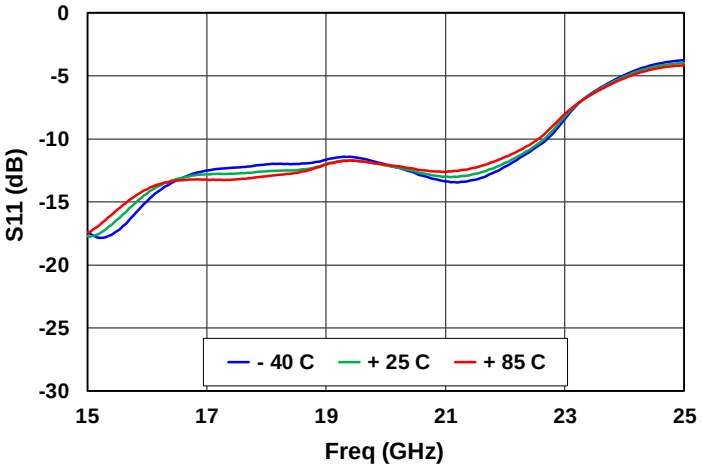
Test conditions, unless otherwise noted: 25 °C, V_D = 3.5 V, I_{DQ} = 90 mA. Data de-embedded to device reference plane.

Parameter	Min	Typical	Max	Units
Frequency	17		22	GHz
Small Signal Gain	22	25		dB
Noise Figure		1.3		dB
1-dB Compression Point		20		dBm
Input Return Loss		12		dB
Output Return Loss		17		dB
3RD Order Intermodulation level (Pout=0 dBm/tone)		−55		dBc
Output TOI (Pout=0 dBm/tone)		28		dBm
Gain Temperature Coefficient		−0.013		dBm/°C

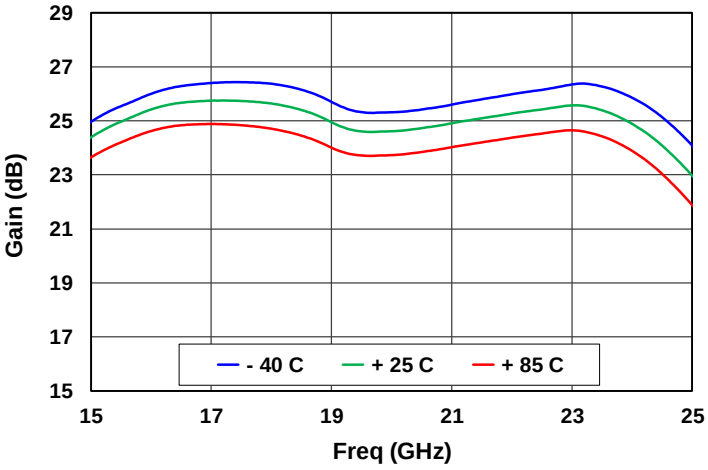
Performance Plots – Small Signal

Test conditions unless otherwise noted: V_D = +3.5V, I_{DQ} = 90 mA, Temp. = +25 °C

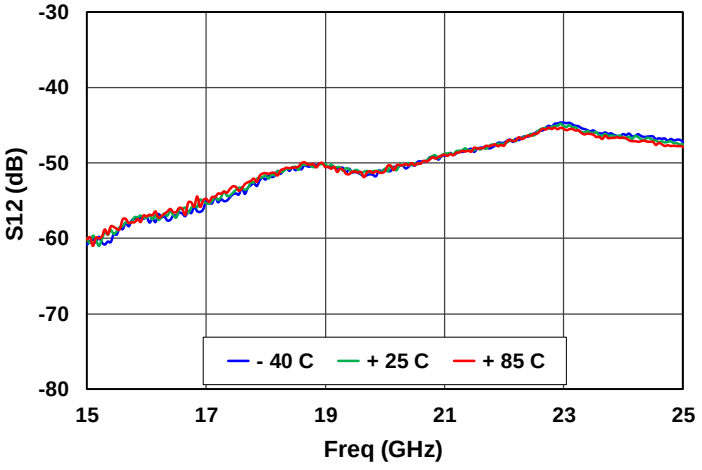
Input Return Loss vs Temperature



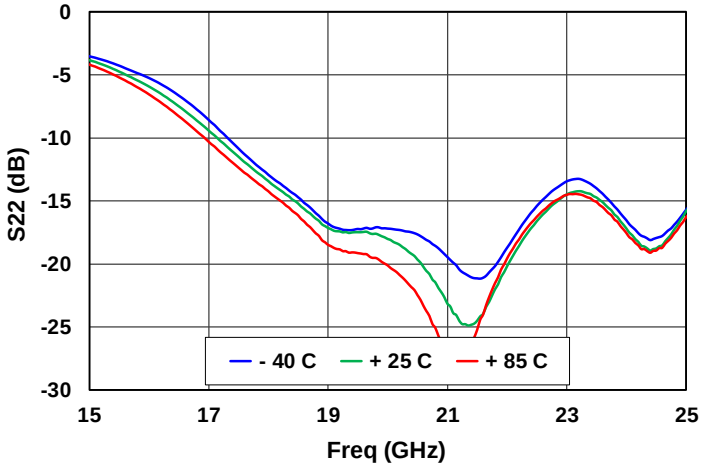
Gain vs Temperature



Reverse Isolation vs Temperature



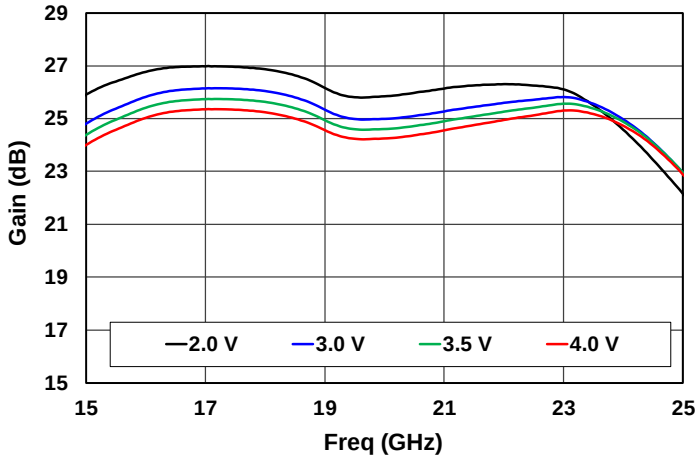
Output Return Loss vs Temperature



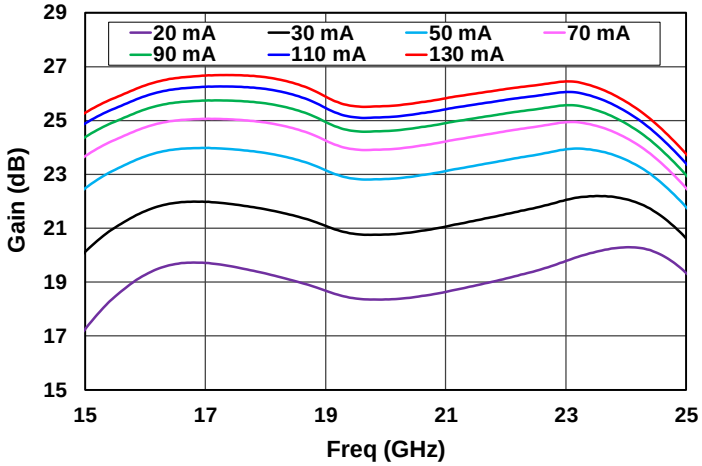
Performance Plots – Small Signal

Test conditions unless otherwise noted: V_D = +3.5V, I_{DQ} = 90 mA, Temp. = +25 °C

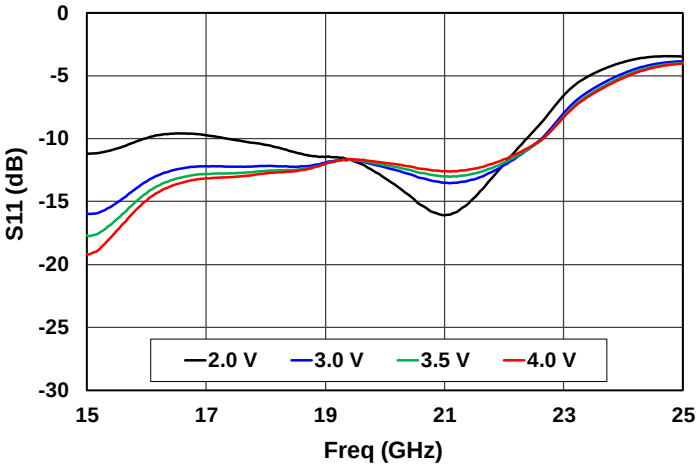
Gain vs Voltage



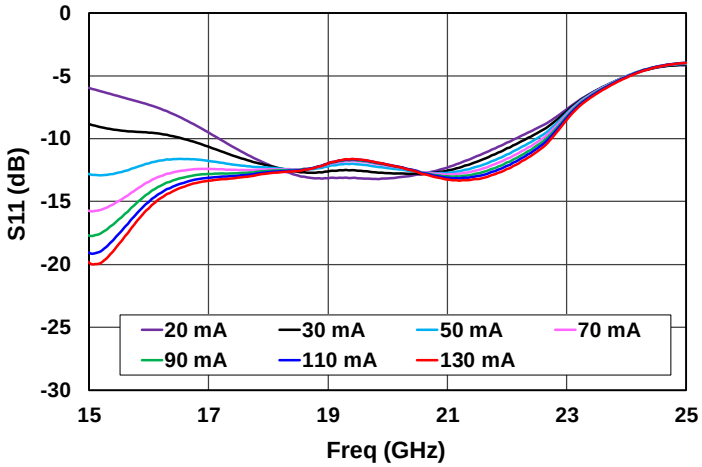
Gain vs Current



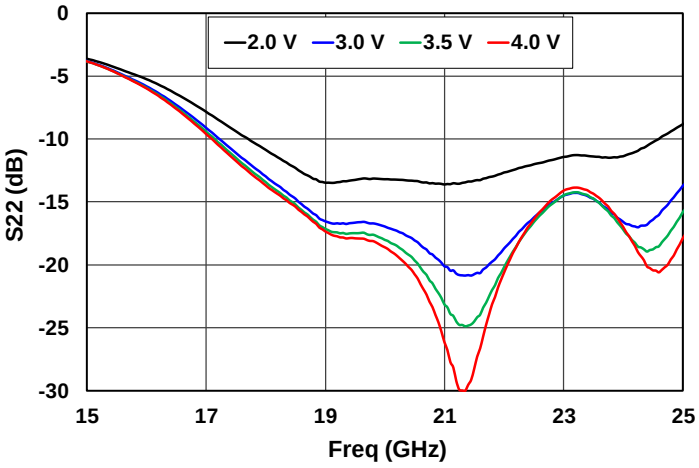
Input Return Loss vs Voltage



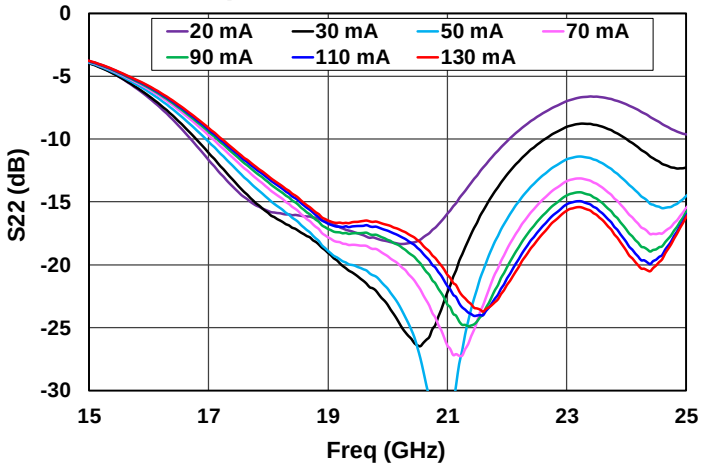
Input Return Loss vs Current



Output Return Loss vs Voltage

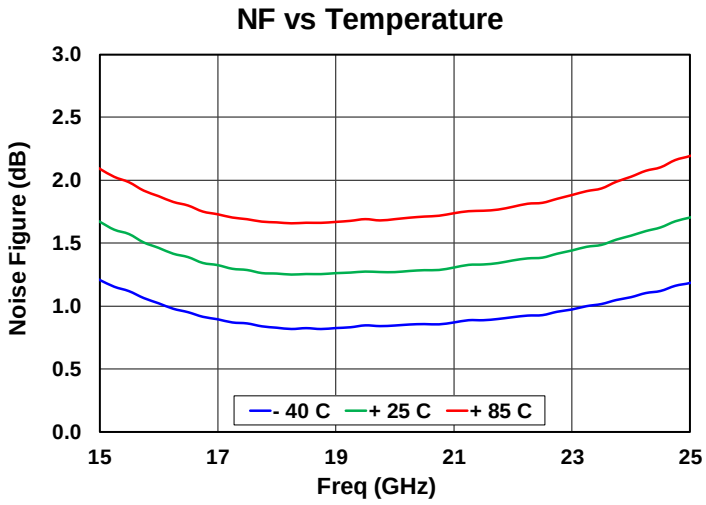


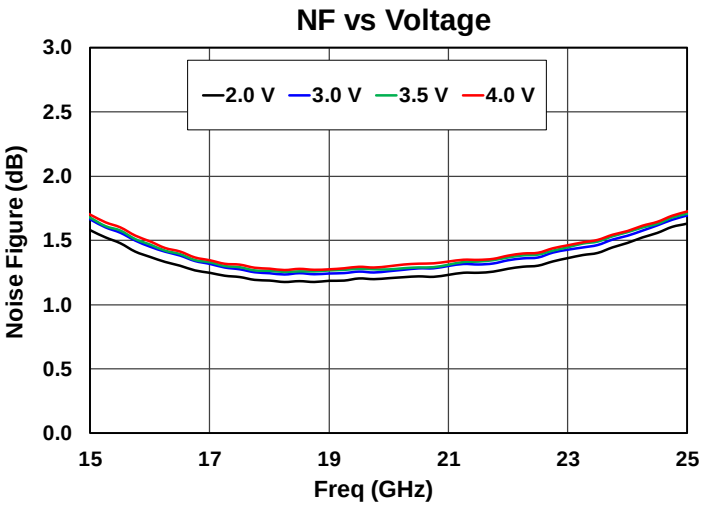
Output Return Loss vs Current

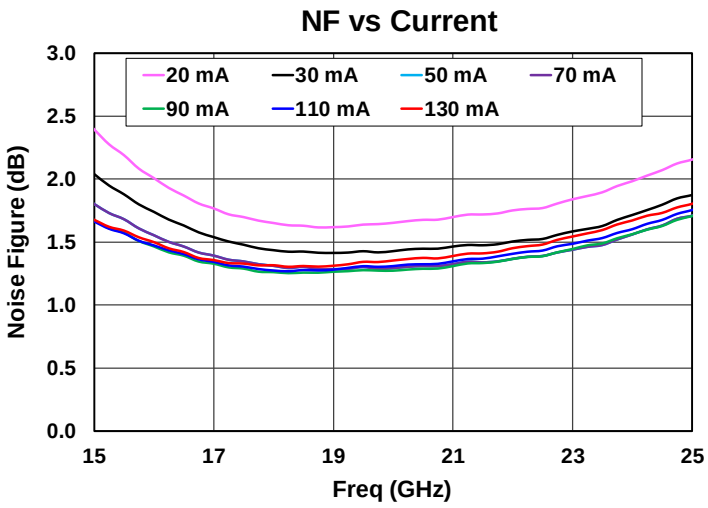


Performance Plots – Small Signal

Test conditions unless otherwise noted: V_D = +3.5V, I_{DQ} = 90 mA, Temp. = +25 °C

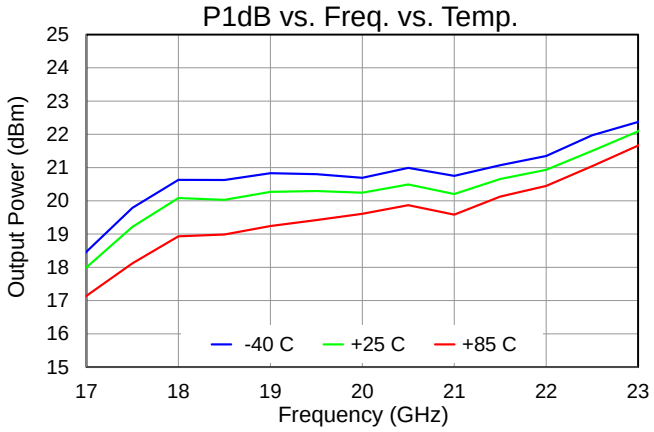


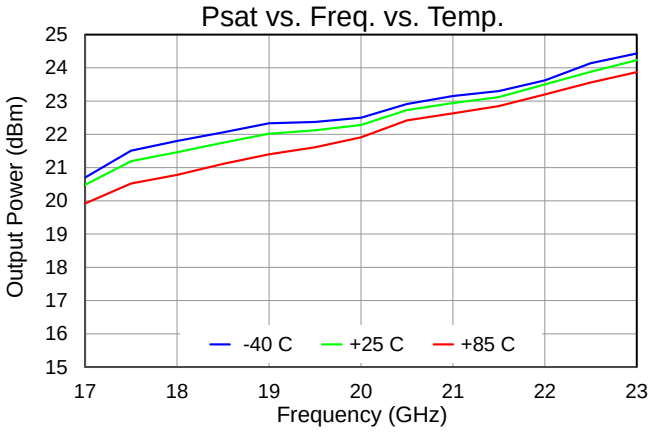


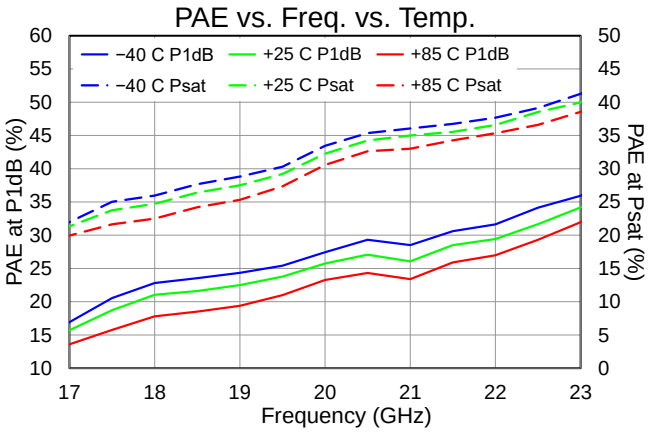


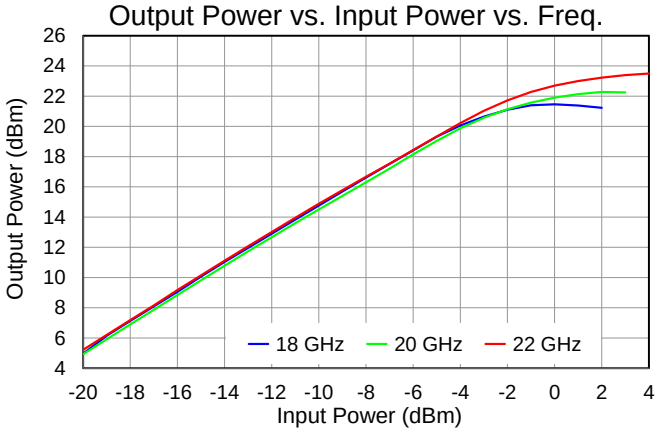
Performance Plots: Large Signal

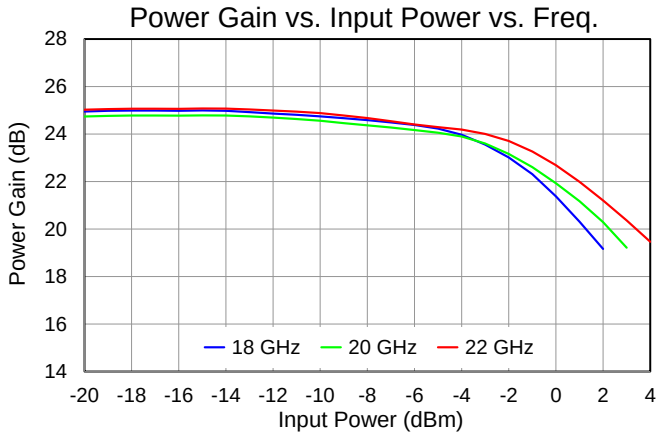
Test conditions unless otherwise noted: Temp. = 25 °C, V_D = 3.5 V, I_{DQ} = 90 mA. Data de-embedded to device reference plane.

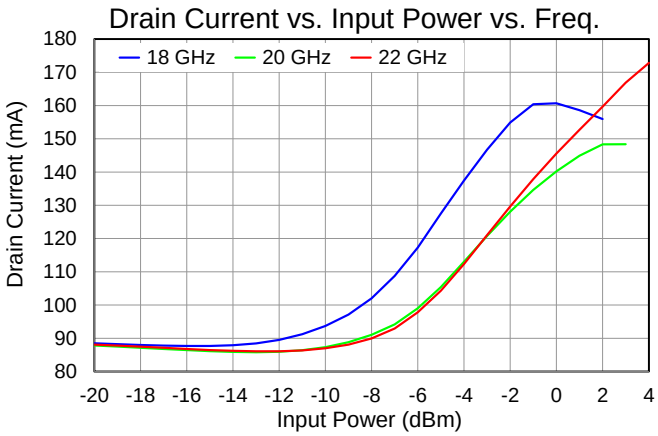








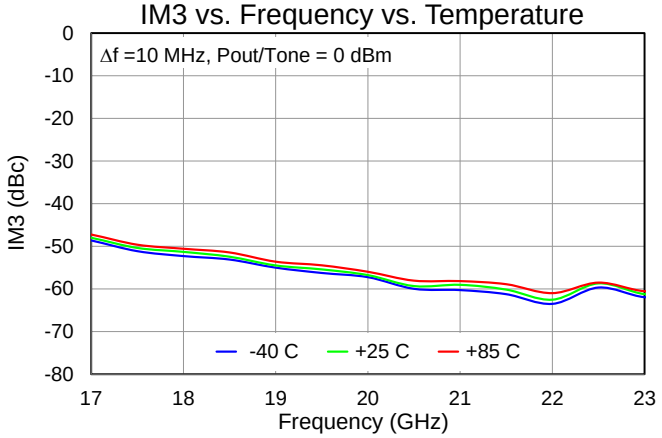




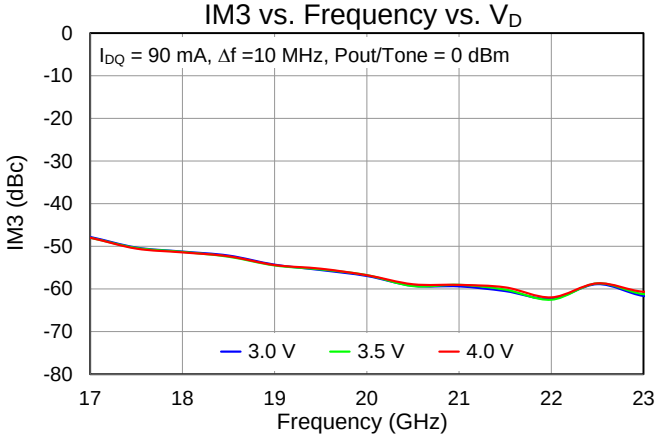
Performance Plots: Linearity

Test conditions unless otherwise noted: Temp. = 25 °C, V_D = 3.5 V, I_{DQ} = 90 mA. Data de-embedded to device reference plane.

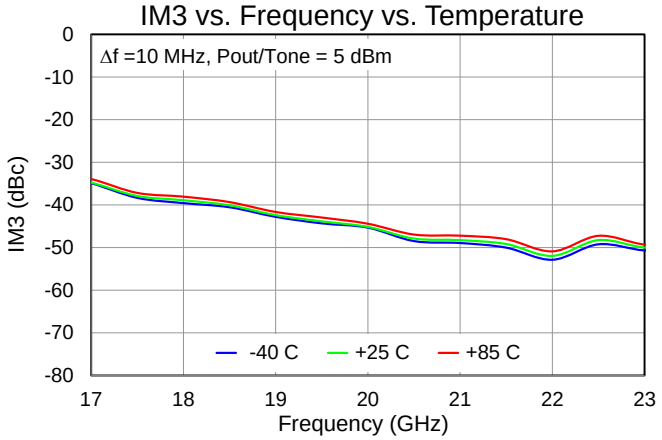
IM3 vs. Frequency vs. Temperature



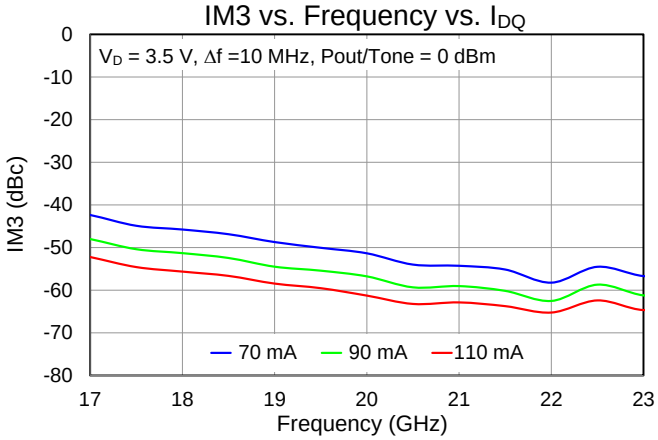
IM3 vs. Frequency vs. V_D



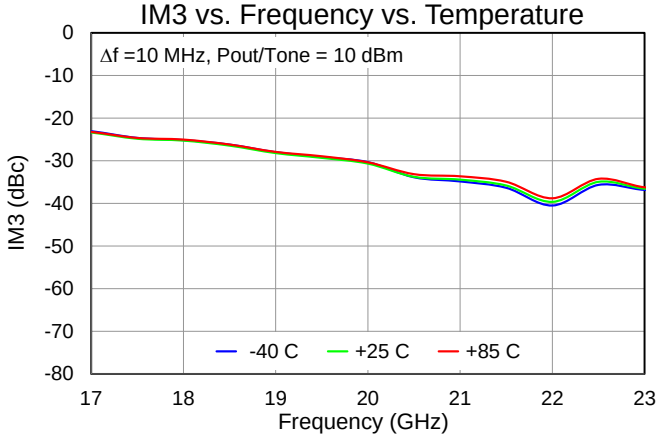
IM3 vs. Frequency vs. Temperature



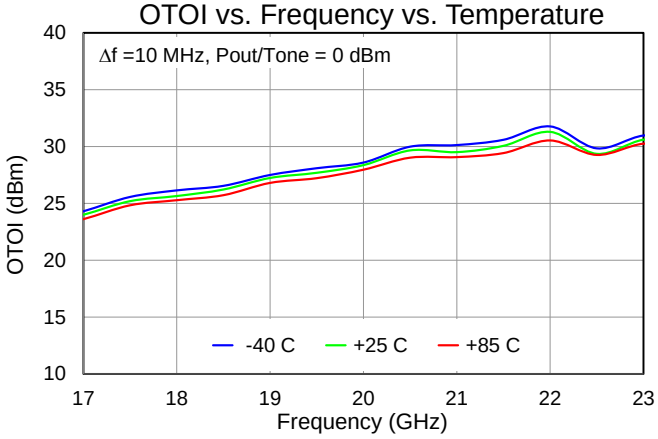
IM3 vs. Frequency vs. I_{DQ}



IM3 vs. Frequency vs. Temperature

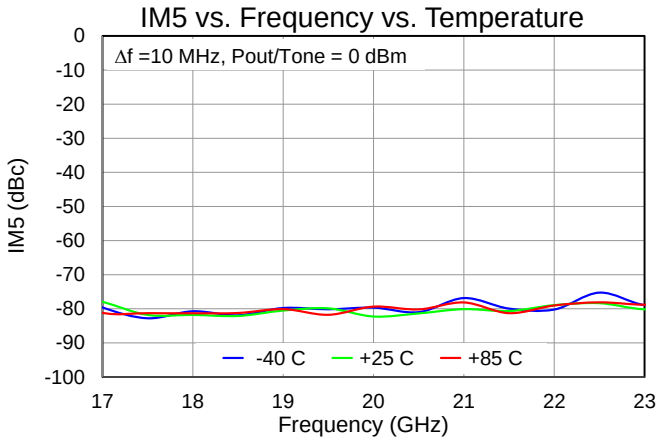


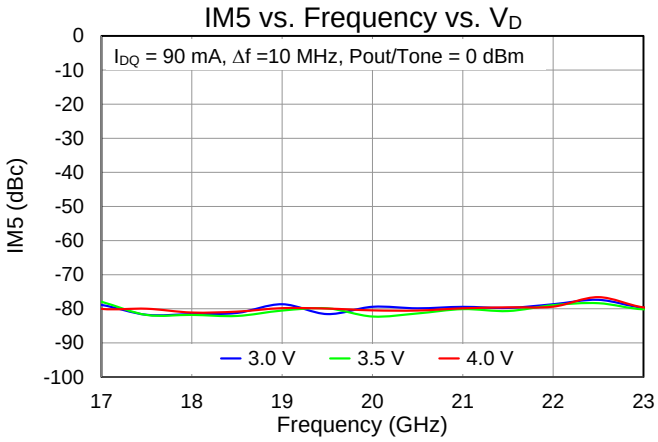
OTOI vs. Frequency vs. Temperature

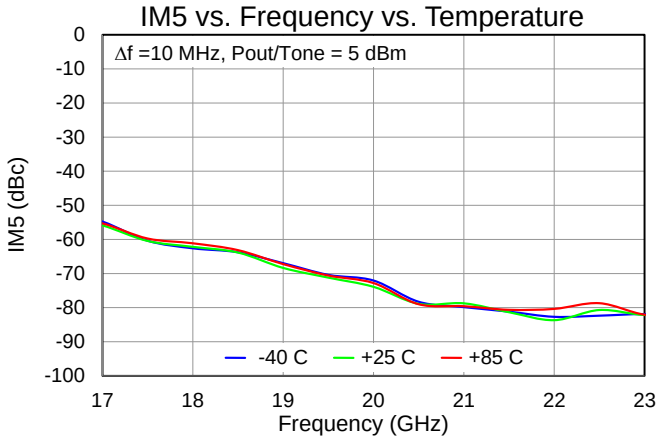


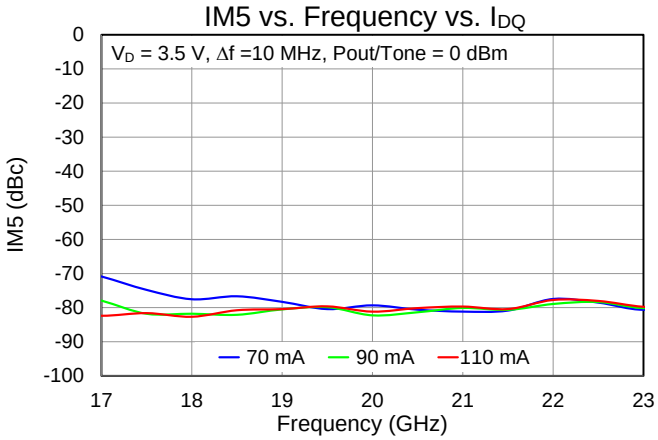
Performance Plots: Linearity

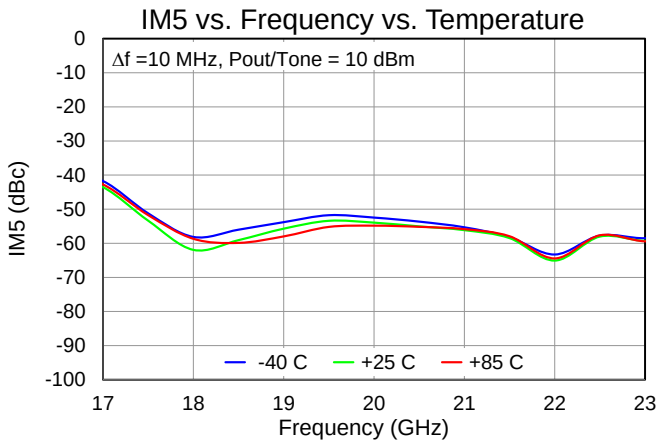
Test conditions unless otherwise noted: Temp. = 25 °C, V_D = 3.5 V, I_{DQ} = 90 mA. Data de-embedded to device reference plane.



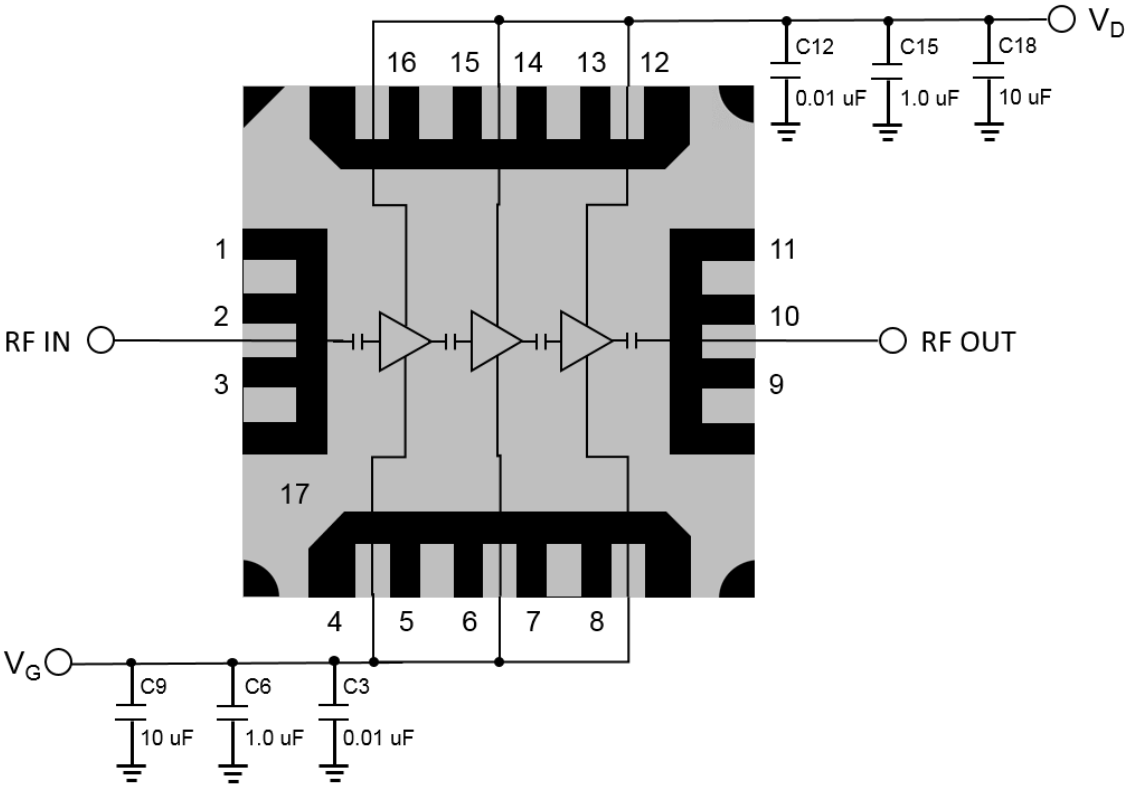








Applications Circuit



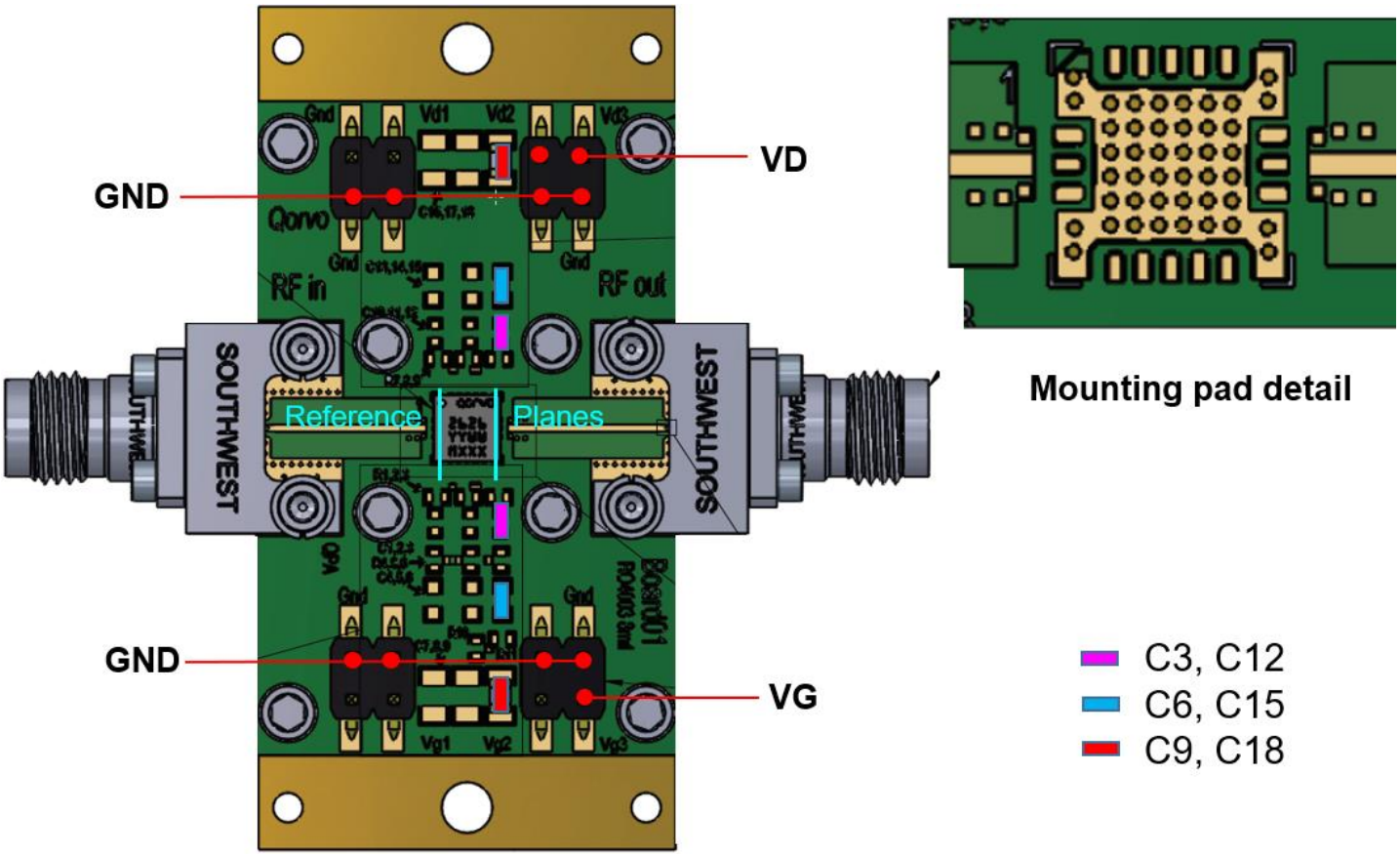
Bias Up Procedure

1. Set I_D limit to 200 mA, I_G limit to 10 mA
2. Set V_G to −1.3 V
3. Set V_D +3.5 V
4. Adjust V_G more positive until I_{DQ} = 90mA (V_G ~ −0.46 V Typical)
5. Apply RF signal

Bias Down Procedure

1. Turn off RF signal
2. Reduce V_G to −1.3 V. Ensure I_{DQ} ~ 0mA
3. Set V_D to 0V
4. Turn off V_D supply
5. Turn off V_G supply

Evaluation Board and Mounting Detail

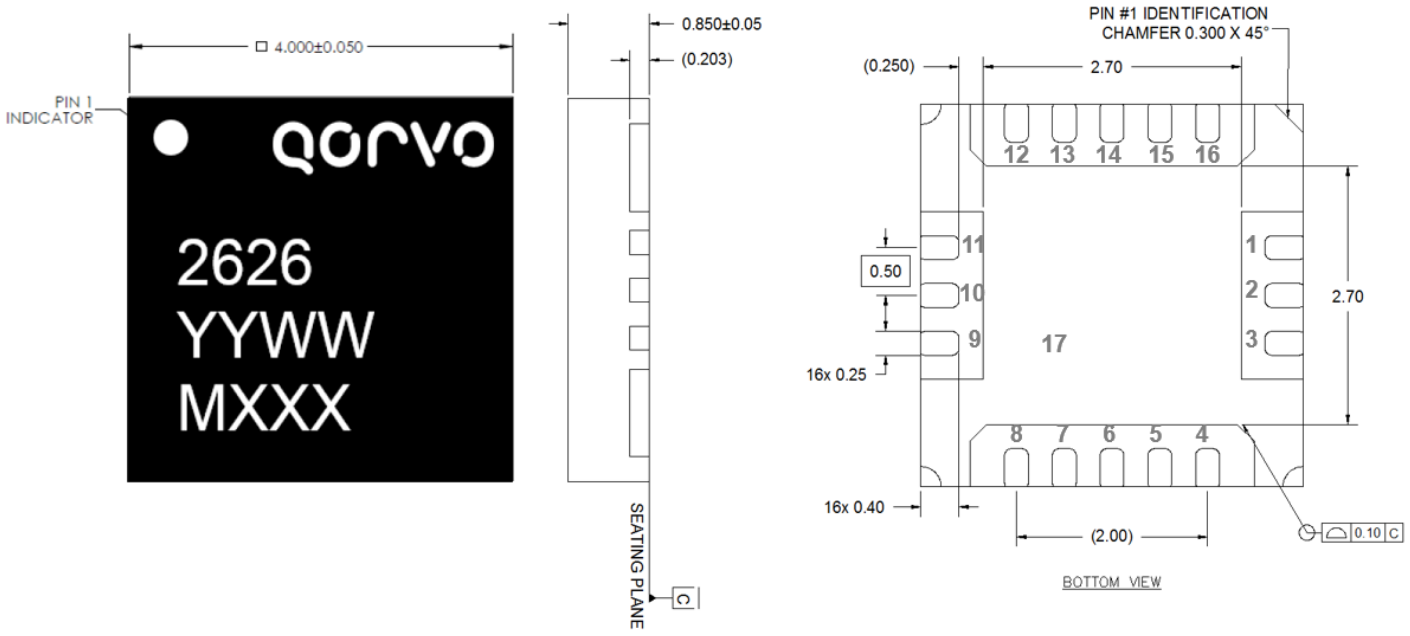


RF Layer is 0.008” thick Rogers Corp. RO4003C (ε_r = 3.35). Metal layers are 0.5 oz. copper. The microstrip line at the connector interface is optimized for the Southwest Microwave end launch connector 1492-04A-5.

All data de-embedded to the device reference plane (shown).

Ref. Des.	Component	Value	Manuf.	Part Number
C3, C12	Surface Mount Cap.	CAP 0.01UF +/-10% 50V 0402 X7R ROHS	Various	
C6, C15	Surface Mount Cap.	CAP 1.0UF +/-10% 16V 0603 X7R ROHS	Various	
C9, C18	Surface Mount Cap.	CAP CER 10UF 10V X7R 10% 0805 TDK ROHS	Various	

Mechanical Drawing & Pad Description



Dimensions in mm, package is mold encapsulated with NiPdAu plated leads

Part Marking: 2626: Part Number; YY = Part Assembly Year; WW = Part Assembly Week; MXXX = Batch ID

Pin Number	Label	Description
1, 3, 9, 11, 17 (slug)	GND	GROUND
2	RF Input	Matched to 50 ohms, DC blocked
4	VG1	Gate Voltage; bias network is required (V_G can be tied together at PCB)
6	VG2	Gate Voltage; bias network is required (V_G can be tied together at PCB)
8	VG3	Gate Voltage; bias network is required (V_G can be tied together at PCB)
10	RF Output	Matched to 50 ohms, DC blocked
12	VD3	Drain Voltage; bias network is required (V_D can be tied together at PCB)
14	VD2	Drain Voltage; bias network is required (V_D can be tied together at PCB)
16	VD1	Drain Voltage; bias network is required (V_D can be tied together at PCB)
5, 7, 13, 15	N/C	No internal connection. Recommend to GND at the PCB level

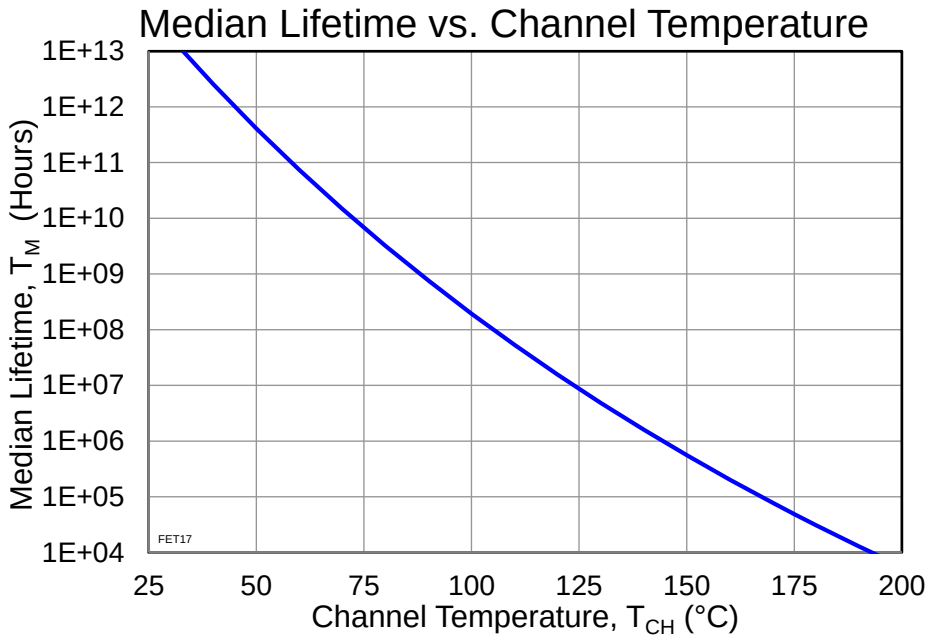
Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	T_{base} = 85°C, V_D = 3.5 V, I_{DQ} = 90 mA Quiescent/Small Signal operation P_{DISS} = 0.315 W	65.1	°C/W
Channel Temperature (T_{CH})		105.5	°C
Median Lifetime (T_M)		1.236E08	Hrs

Notes:
1. Thermal resistance is measured to back of the package.

Median Lifetime

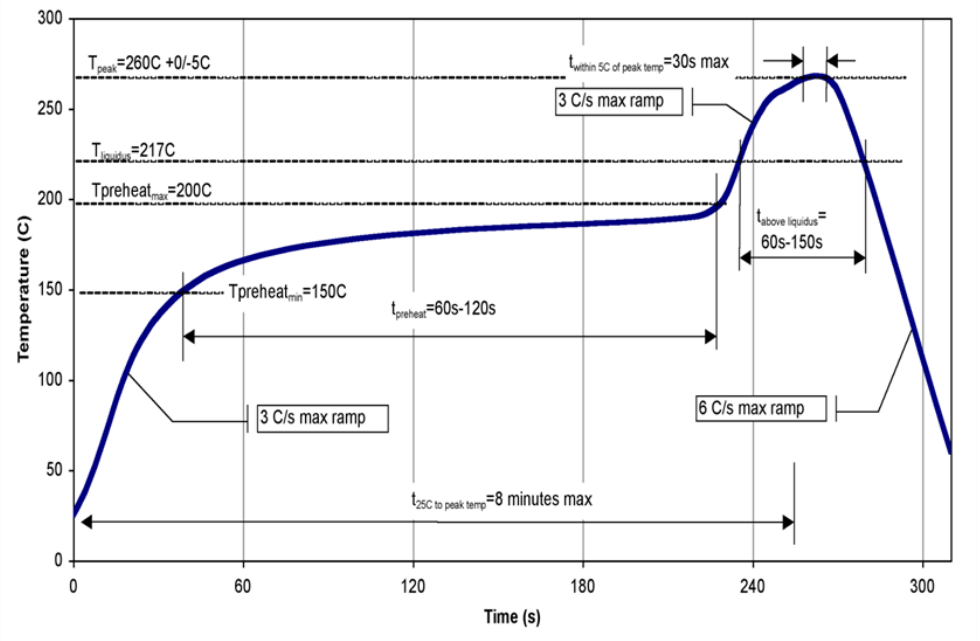
Test Conditions: V_D = 4 V
Failure Criteria = 10% reduction in I_{D_MAX}



Solderability

1. Compatible with the latest version of J-STD-020, Lead-free solder, peak reflow temperature: 260 °C.

Recommended Soldering Temperature Profile



Tape and Reel Information

Standard T/R size = 500 pieces on a 7 inch reel.

Material		Cavity (mm)				Distance Between Centerline (mm)		Carrier Tape (mm)	Cover Carrier (mm)
Vendor	Vendor P/N	Length (A0)	Width (B0)	Depth (K0)	Pitch (P1)	Length direction (P2)	Width Direction (F)	Width (W)	Width (W)
Tek-Pak	QFN0400X 0450C	4.35	4.35	1.1	8.0	2.00	5.50	12.0	9.20