

### Product Overview

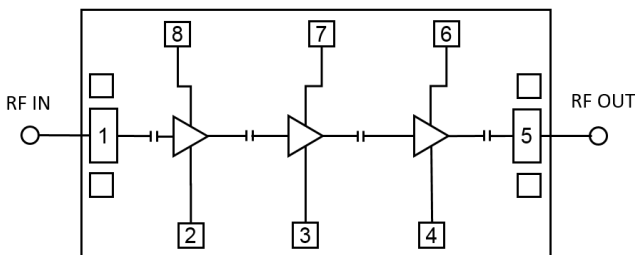
Qorvo's QPA2735D is a high-performance, low noise MMIC amplifier fabricated on Qorvo's production 90 nm pHEMT process (QPHT09). Covering 13 – 20 GHz, the QPA2735D provides 26 dB small signal gain and 1.2 dB noise figure. With a compact size of 2.37 x 0.97 mm, the amplifier can deliver 23 dBm of saturated power with P1dB of 18 dBm. In addition, the device can provide low IMD3 level of -60 dBc at Pout = 0 dBm/tone.

The QPA2735D is matched to 50 ohms with integrated DC blocking caps on both I/O ports for easy handling and simple system integration.

The high performance of the QPA2735D makes it ideal for satellite and point to point communication systems.



### Functional Block Diagram



### Key Features

- Frequency Range: 13 – 20 GHz
- Noise Figure: 1.2 dB (typical)
- Small Signal Gain: 26 dB (typical)
- P1dB: 18 dBm (typical)
- Psat: 23 dBm (typical)
- IMD3: -60 dBc (typical) (Pout=0 dBm/tone)
- Bias: VD = 3.5 V, IDQ = 105 mA, VG = -0.46 V (typical)
- Die Dimensions: 2.37 x 0.97 x 0.10 mm

### Applications

- Satellite Communications
- Point-to-Point Communications

### Ordering Information

Part No.	Description
QPA2735D	13 – 20 GHz Low Noise Amplifier
QPA2735DEVB01	QPA2735D Evaluation Board

## Absolute Maximum Ratings

Parameter	Rating	Units
Drain Voltage ( $V_D$ )	4.5	V
Drain Current ( $I_{D1}/I_{D2}/I_{D3}$ )	96 / 90 / 192	mA
Gate Voltage Range ( $V_G$ )	-1.3 to 0	V
Gate Current ( $I_{G1}/I_{G2}/I_{G3}$ at 125 °C)	5.0 / 5.0 / 6.6	mA
RF Input Power (50 $\Omega$ , 85 °C)	20	dBm
Channel Temperature, $T_{CH}$	175	°C
Mounting Temperature (30 seconds)	260	°C
Storage Temperature	-55 to 150	°C

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

## Recommended Operating Conditions

Parameter	Typical Values	Units
Drain Voltage	3.5	V
Drain Current (quiescent, $I_{DQ}$ )	105	mA
Drain Current ( $I_D$ , Low noise / $P_{SAT}$ )	105 / 175	mA
Gate Voltage (typical)	-0.46	V
Operating Temperature Range	-40 to 85	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

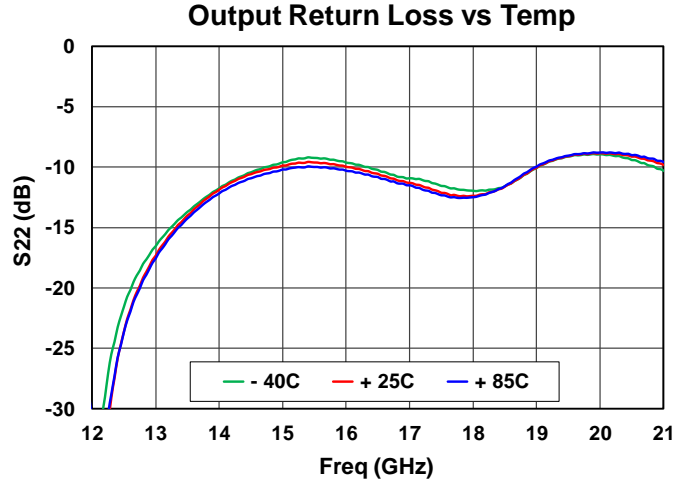
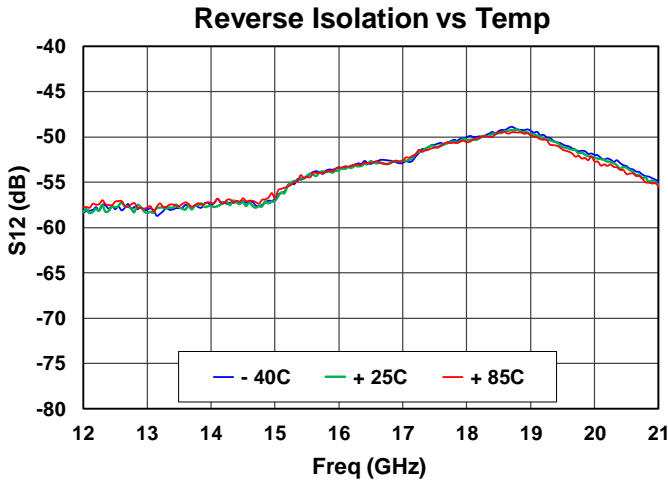
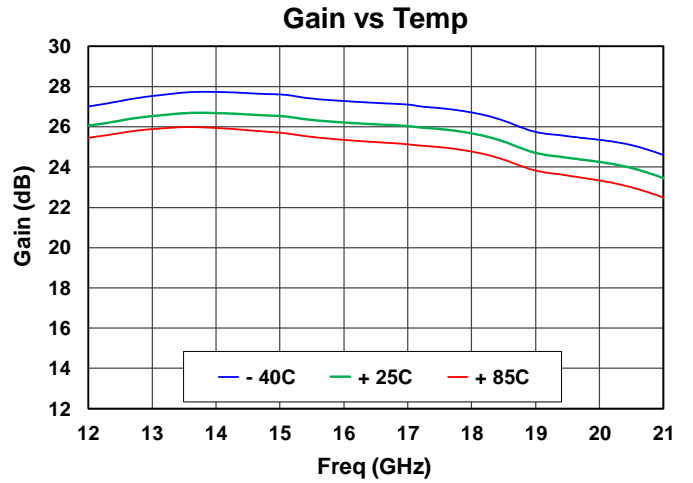
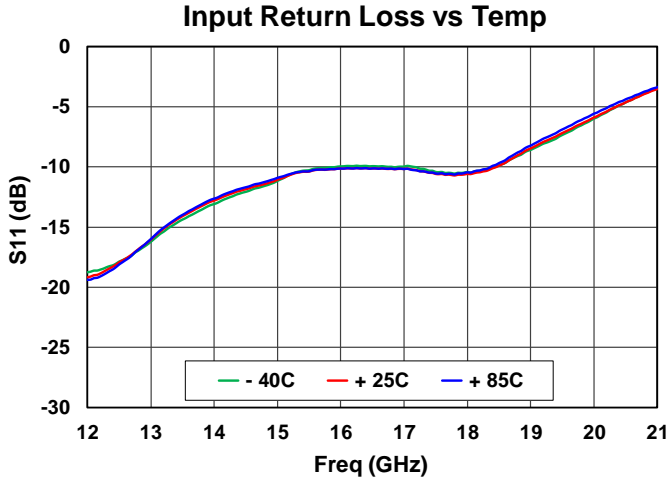
## Electrical Specifications

Test conditions unless otherwise noted:  $V_D = +3.5$  V,  $I_{DQ} = 105$  mA, Temp. = +25 °C. Data de-embedded to MMIC bond wires.

Parameter	Min	Typ	Max	Units
Operating Frequency	13		20	GHz
Small Signal Gain		26		dB
Noise Figure		1.2		dB
Power at 1-dB Compression		18		dBm
Power at Saturation		23		dBm
Input Return Loss		10.0		dB
Output Return Loss		10.0		dB
3 <sup>RD</sup> Order Intermodulation Level ( $P_{OUT} = 0$ dBm / Tone)		-60		dBc
Output TOI ( $P_{out} = 0$ dBm / tone)		30.0		dBm
Gain (S21) Temperature Coefficient		-0.016		dB/°C

Performance Plots – Small Signal

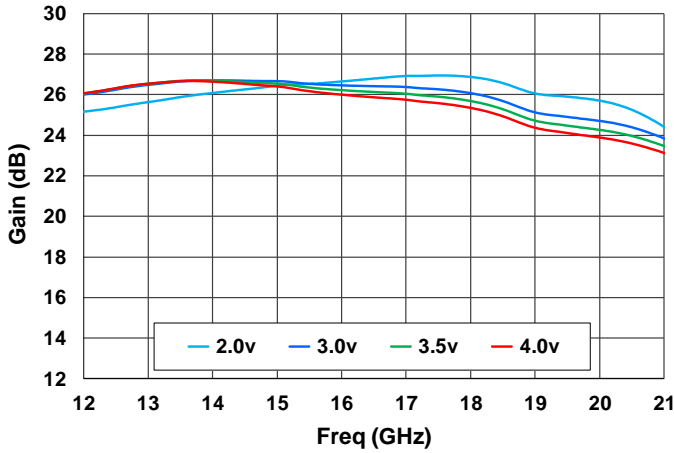
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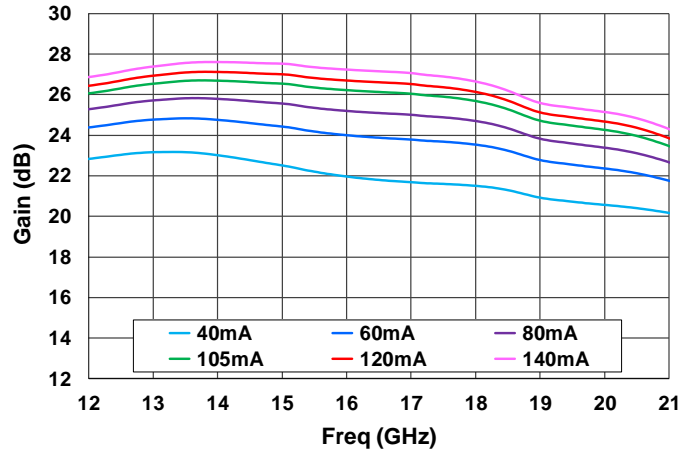
Performance Plots – Small Signal

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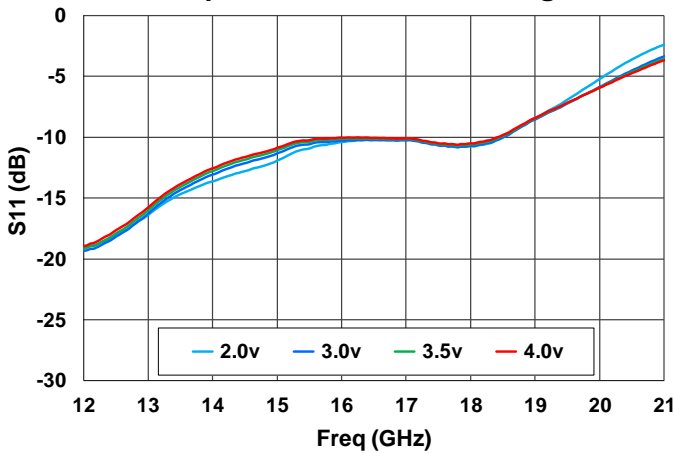
Gain vs Voltage



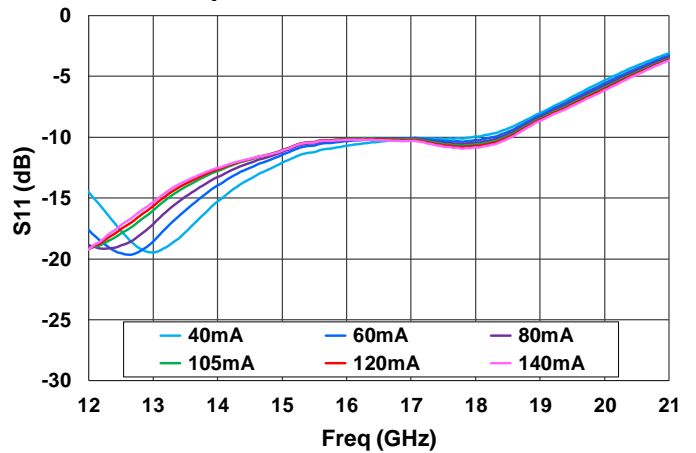
Gain vs Current



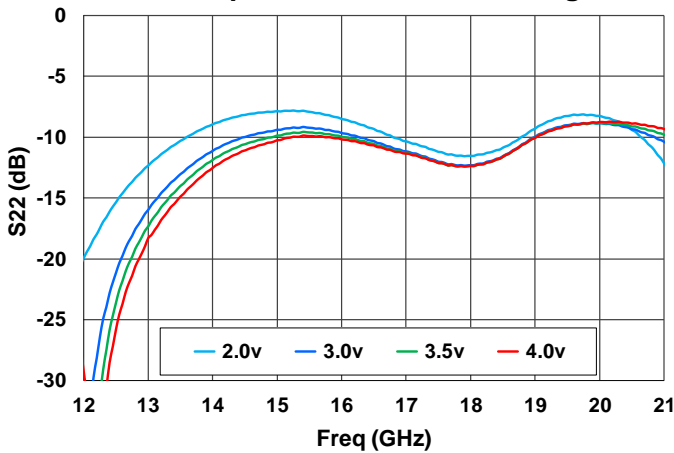
Input Return Loss vs Voltage



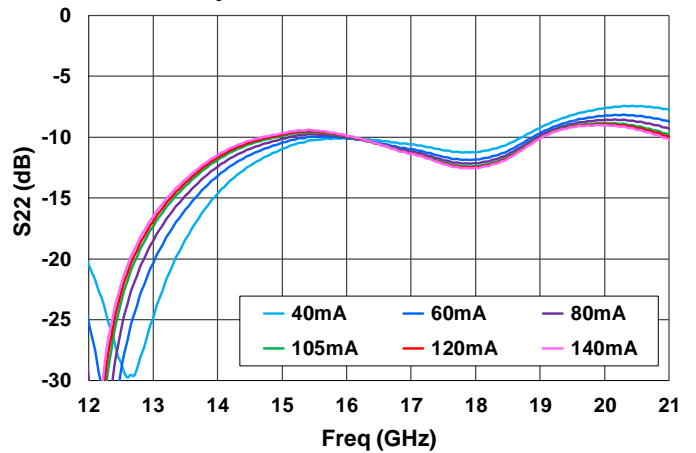
Input Return Loss vs Current



Output Return Loss vs Voltage

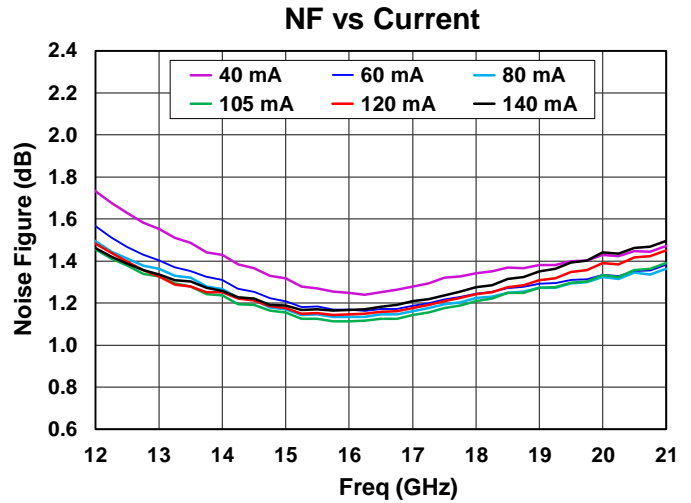
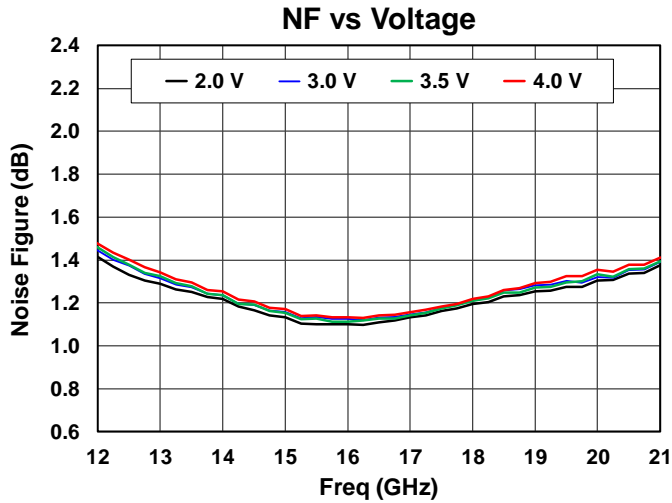
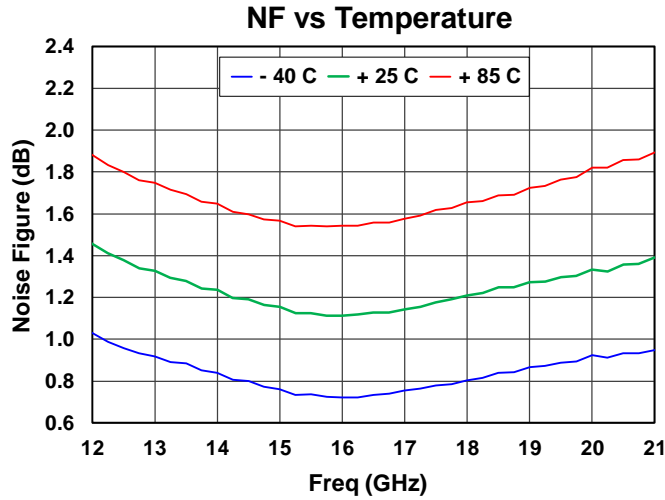


Output Return Loss vs Current



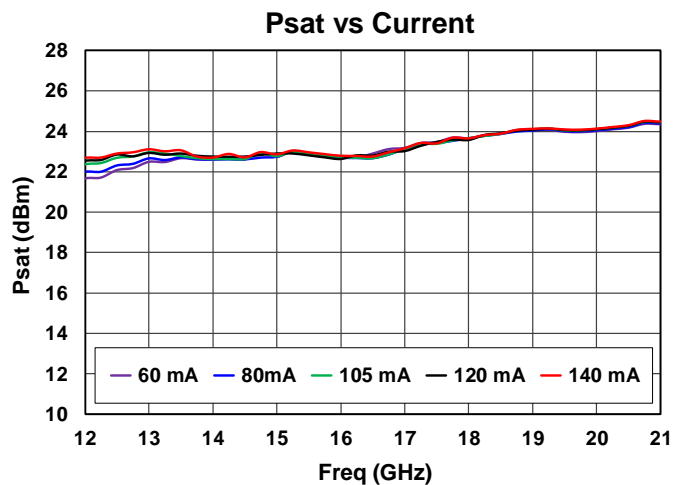
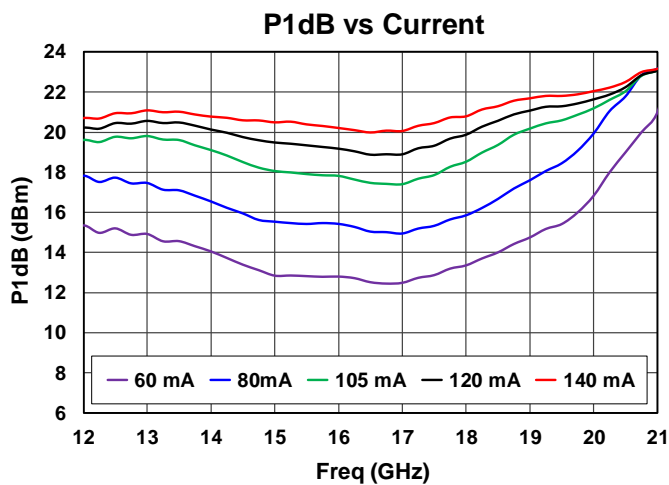
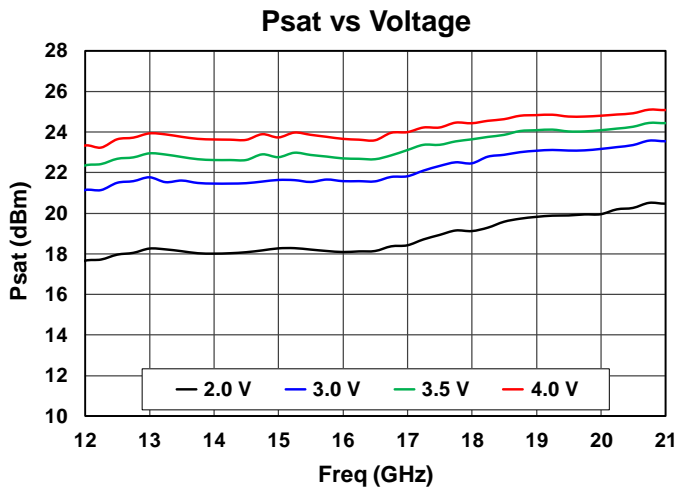
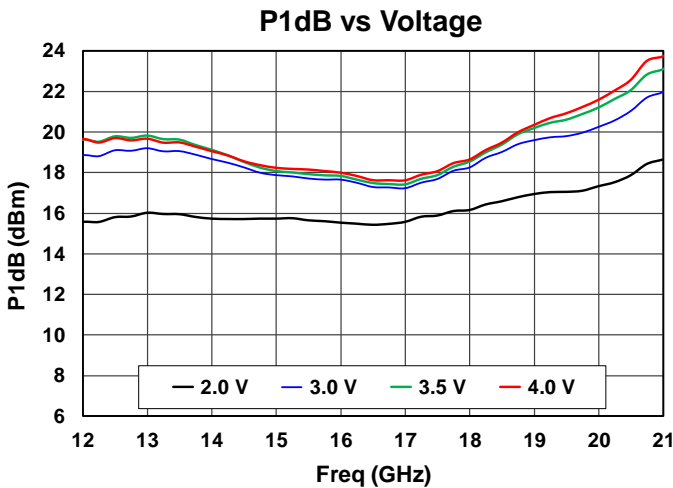
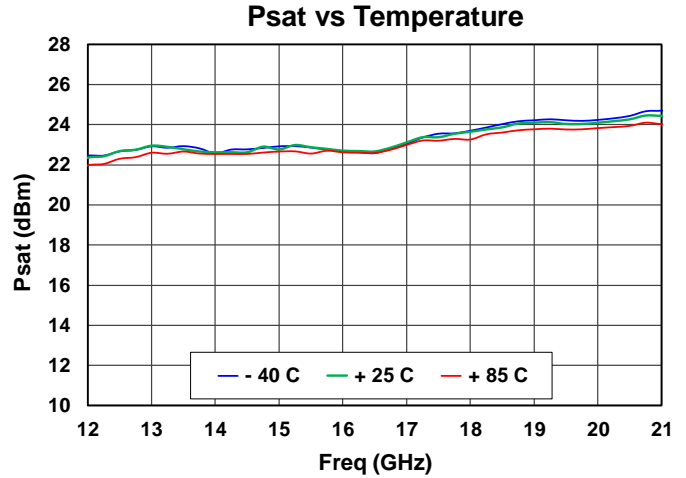
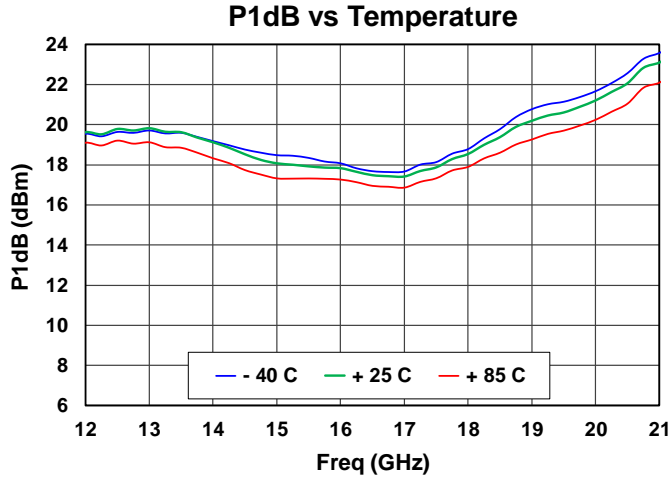
Performance Plots – Noise Figure

Test conditions unless otherwise noted:  $V_D = +3.5\text{ V}$ ,  $I_{DQ} = 105\text{ mA}$ , Temp. =  $+25\text{ °C}$



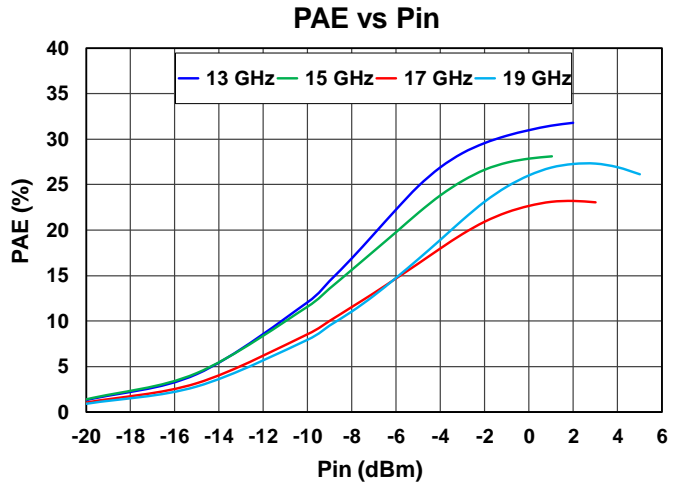
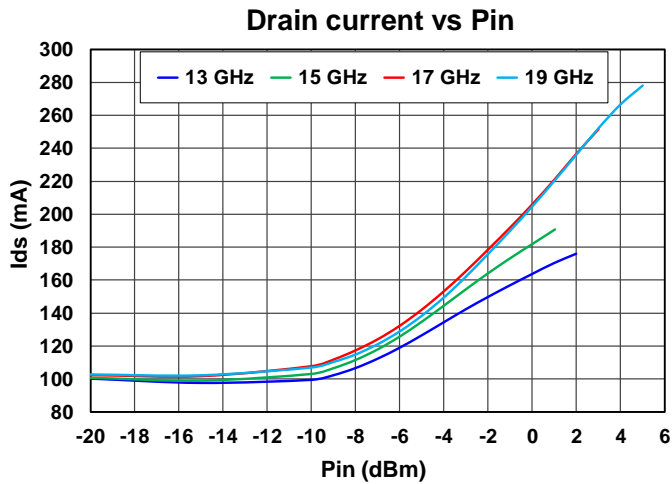
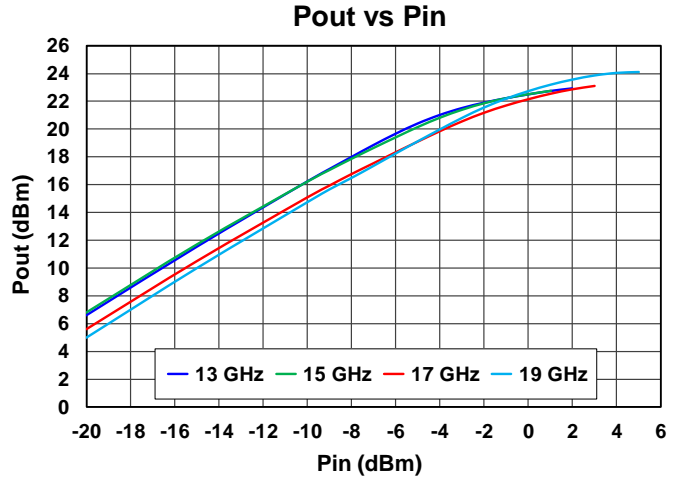
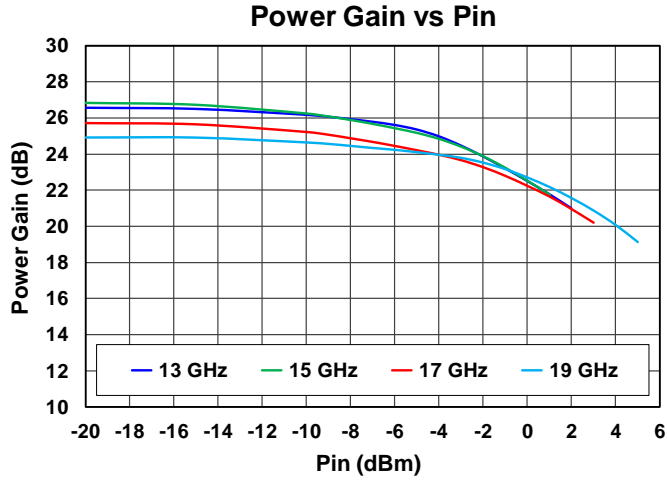
## Performance Plots – Large Signal

Test conditions unless otherwise noted:  $V_D = +3.5\text{ V}$ ,  $I_{DQ} = 105\text{ mA}$ , Temp. =  $+25\text{ }^\circ\text{C}$



## Performance Plots – Large Signal

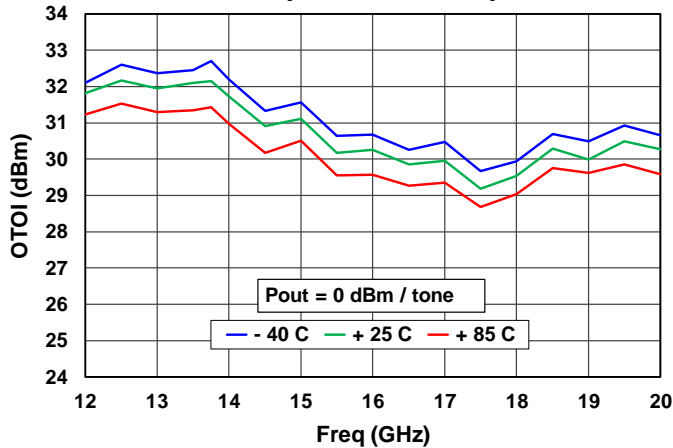
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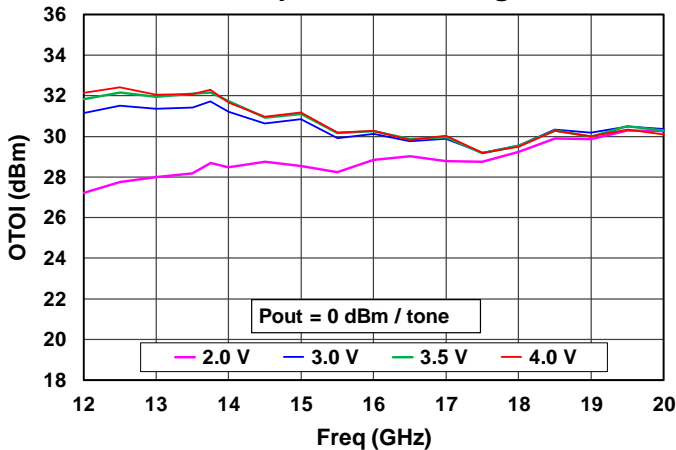
Performance Plots – Linearity

Test conditions unless otherwise noted:  $V_D = +3.5\text{ V}$ ,  $I_{DQ} = 105\text{ mA}$ ,  $\Delta f = 11\text{ MHz}$ ,  $\text{Temp.} = +25\text{ }^\circ\text{C}$

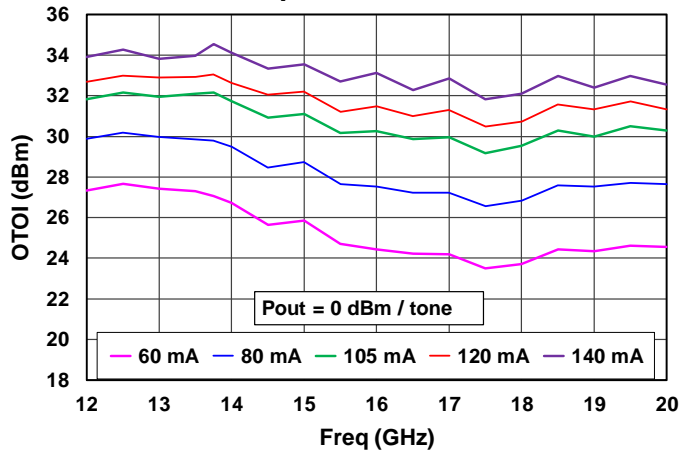
Output TOI vs Temp



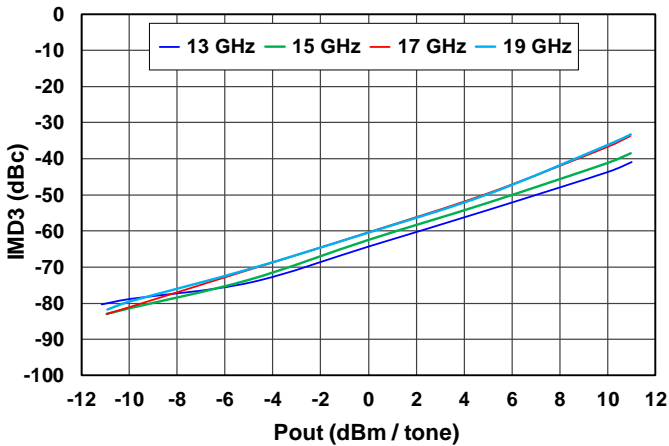
Output TOI vs Voltage



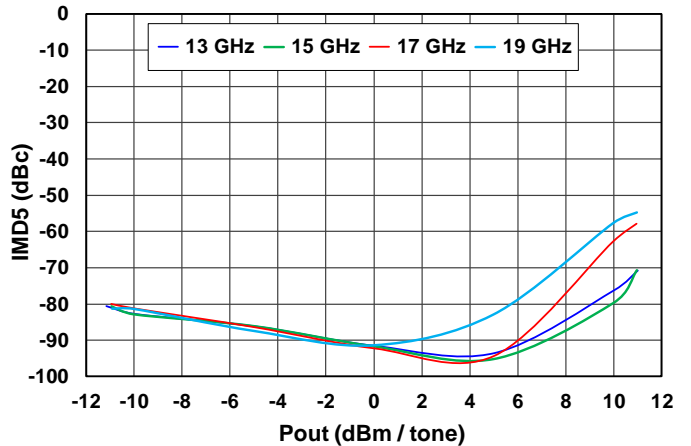
Output TOI vs Current



IMD3 vs Pout

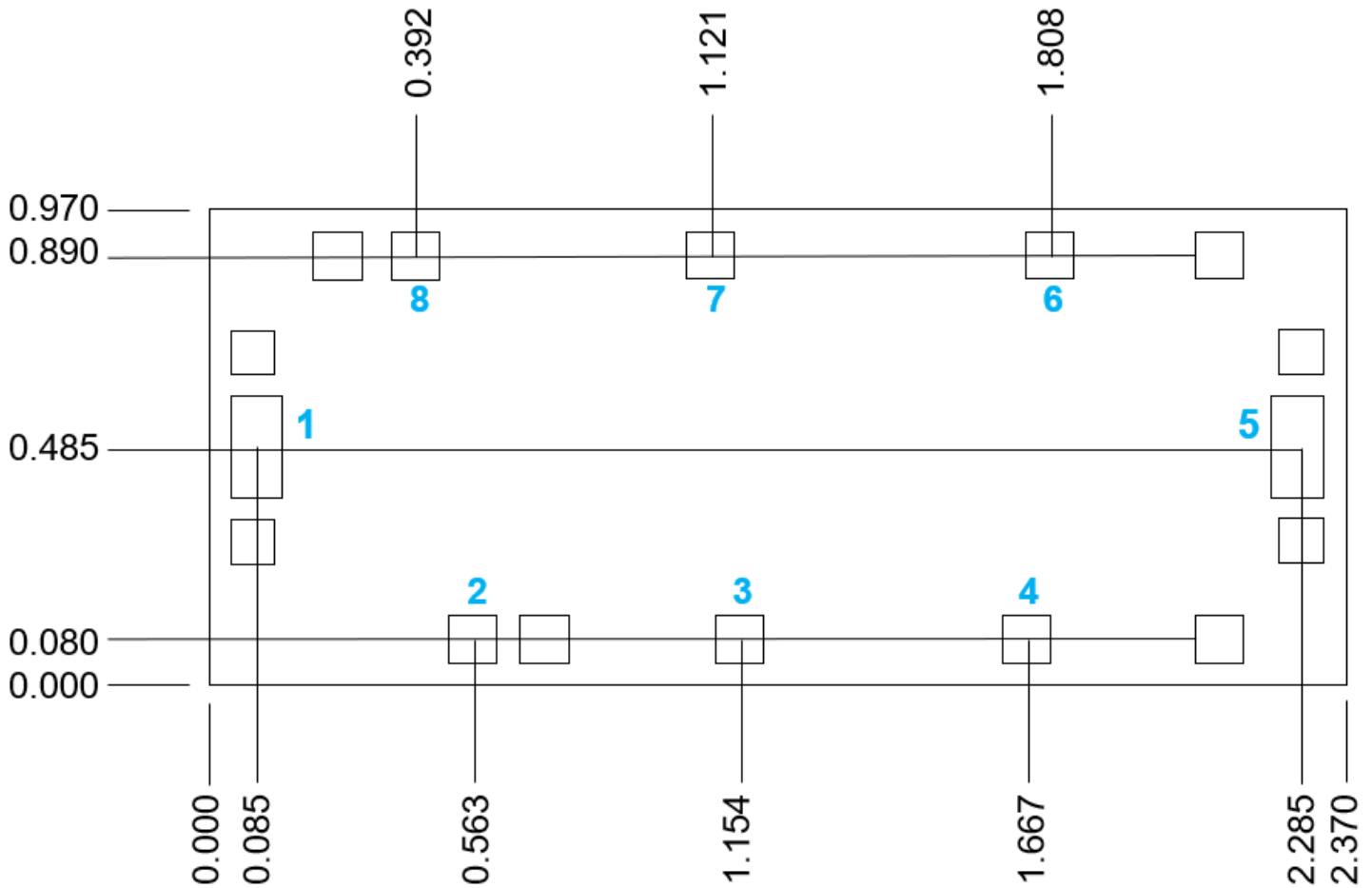


IMD5 vs Pout





Mechanical Drawing and Bond Pad Description



Unit: millimeters. Die thickness: 0.10, Die x, y size tolerance: +/- 0.010  
Chip edge to bond pad dimensions are shown to center of pad. Ground is backside of die

Pad No.	Label	Pad Size (um)	Description
1	RF Input	91 x 197	Matched to 50 ohms, DC blocked
2	VG1	82 x 82	Gate Voltage; bias network is required (VG can be tied together at PCB)
3	VG2	82 x 82	Gate Voltage; bias network is required (VG can be tied together at PCB)
4	VG3	82 x 82	Gate Voltage; bias network is required (VG can be tied together at PCB)
5	RF Output	91 x 197	Matched to 50 ohms, DC blocked
6	VD3	82 x 82	Drain Voltage; bias network is required
7	VD2	82 x 82	Drain Voltage; bias network is required (VD1 and VD2 can be tied together at PCB)
8	VD1	82 x 82	Drain Voltage; bias network is required (VD1 and VD2 can be tied together at PCB)

## Assembly Notes

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### Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment (i.e., conductive epoxy) can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.

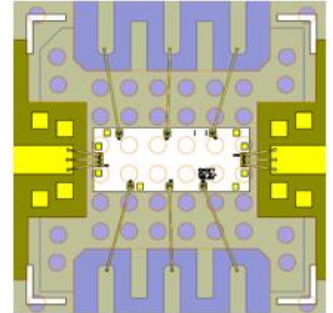
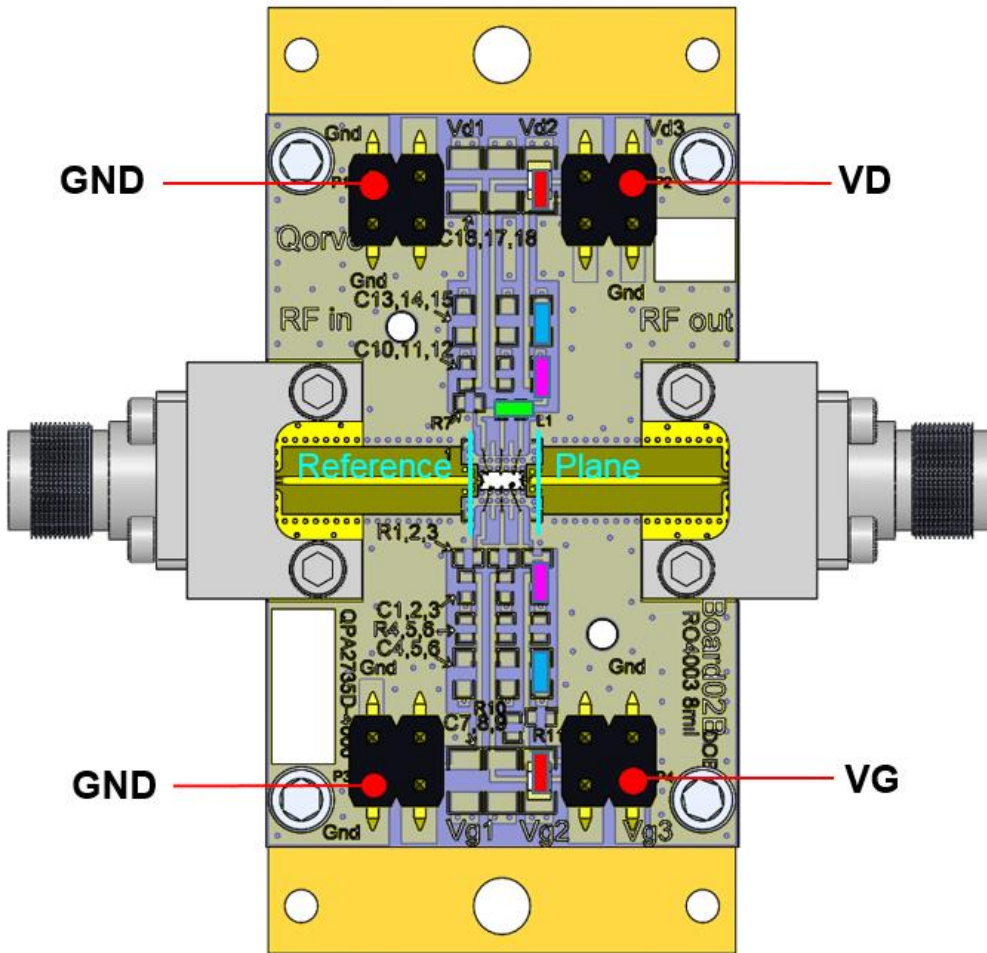
### Reflow process assembly notes:

- Use AuSn (80/20) solder and limit exposure to temperatures above 300°C to 3-4 minutes, maximum.
- Conductive epoxy die attach is recommended for PCB mounting.
- Bonding pads plating: Au.
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- Do not use any kind of flux.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

### Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonics are critical parameters.
- Aluminum wire should not be used.
- Devices with small pad sizes should be bonded with 0.0007-inch wire.

Evaluation Board and BOM



Mounting pad detail

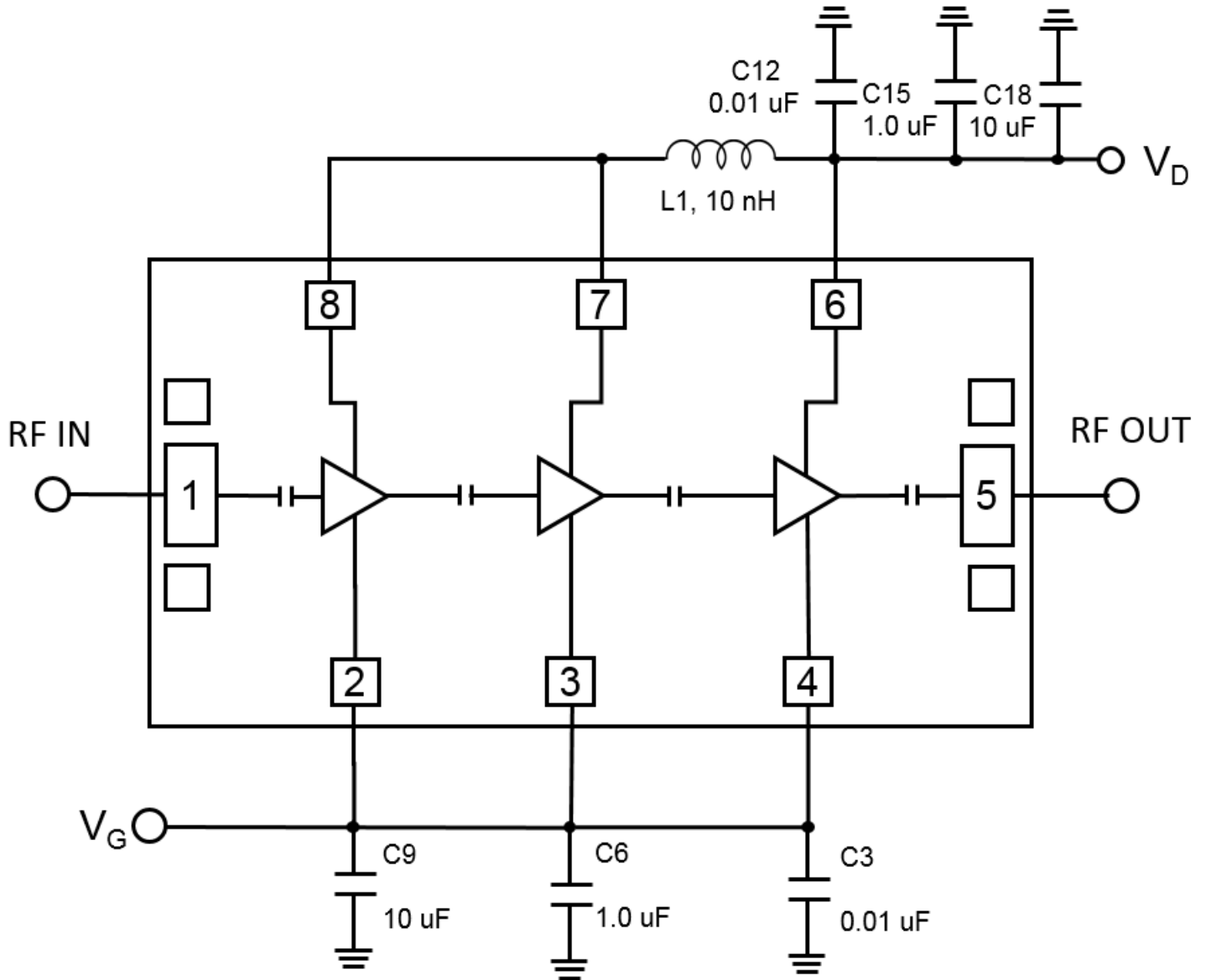
- C3, C12
- C6, C15
- C9, C18
- L1

RF Layer is 0.008" thick Rogers Corp. RO4003C ( $\epsilon_r = 3.35$ ). Metal layers are 0.5 oz. copper. The microstrip line at the connector interface is optimized for the Southwest Microwave end launch connector 1092-01A-5.

Bill of Material – Evaluation Board

Ref. Des.	Value	Description	Manuf.	Part Number
C3, C12	0.01 uF	CAP 0.01UF +/-10% 50V 0402 X7R ROHS	Various	
C6, C15	1.0 uF	CAP 1.0UF +/-10% 16V 0603 X7R ROHS	Various	
C9, C18	10 uF	CAP CER 10UF 10V X7R 10% 0805 TDK ROHS	Various	
L1	10 nH	IND 10 nH 500mA, 0402, 5.5 GHz, + / - 2%	Various	
RF IN, RF OUT	2.92 mm	2.92 MM END LAUNCH CONNECTOR	Southwest Microwave	1092-01A-5

Application Circuit and Biasing Sequence



Notes:

1. Can use separate gate and drain for individual stage controls.

**Bias-up Procedure**

1. Set  $I_D$  limit to 220 mA,  $I_G$  limit to 10 mA
2. Set  $V_G$  to  $-1.3$  V
3. Set  $V_D$  to  $+3.5$  V
4. Adjust  $V_G$  more positive until  $I_{DQ} = 105$  mA ( $V_G \approx -0.46$  V Typical)
5. Apply RF signal

**Bias-down Procedure**

1. Turn off RF signal
2. Reduce  $V_G$  to  $-1.3$  V. Ensure  $I_{DQ} \approx 0$  mA
3. Set  $V_D$  to 0V
4. Turn off  $V_D$  supply
5. Turn off  $V_G$  supply

Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Thermal Resistance ( $\theta_{JC}$ ) <sup>(1)</sup>	$T_{base} = 85^{\circ}C$ , $V_D = 3.5 V$ , $I_{DQ} = 105 mA$ Quiescent/Small Signal operation, $P_{DISS} = 0.37 W$	65.0	$^{\circ}C/W$
Channel Temperature, $T_{CH}$ (Under RF)		108.9	$^{\circ}C$
Median Lifetime ( $T_M$ )		6.7E07	Hrs

Notes:

1. Die mounted to 40 mil CuMo carrier plate with AuSn eutectic. Thermal resistance measured at back of carrier plate.

Median Lifetime

Test Conditions:  $V_D = +4 V$   
Failure Criteria is 10% reduction in  $I_{D\_MAX}$

