QPA4501

3 W, 28 V, 4.4 – 5.0 GHz GaN PA Module

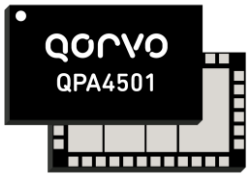
Product Overview

The QPA4501 is an integrated 2-stage Power Amplifier Module designed for massive MIMO applications up to 3 W RMS at the device output covering frequency range from 4.4 to 5.0 GHz.

The module is 50 Ω input and output and requires minimal external components. The module is also compact and offers a much smaller footprint than traditional discrete component solutions.

The QPA4501 incorporates a Doherty final stage delivering high power added efficiency for the entire module up to 3 W average power.

RoHS compliant.



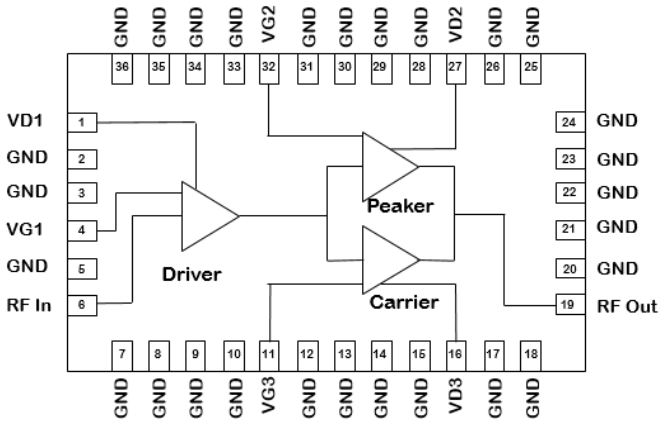
36 Pad 6 x 10 mm Plastic QFN Package

Key Features

- Operating Frequency Range: 4.4 – 5.0 GHz
- Operating Drain Voltage: +28 V
- 50 Ω Input / Output
- Integrated Doherty Final Stage
- Gain at 1.25 W Avg.: 29.9 dB
- Power Added Efficiency at 1.25 W Avg.: 25.7%
- Power Added Efficiency at 3 W Avg.: 38%
- 6 x 10 mm Plastic Surface Mount Package

Note: T = +25°C, single-carrier, 20 MHz LTE signal with 7.8 dB PAR at 0.01% CCDF.

Functional Block Diagram



Applications

- 5G Massive MIMO
- W-CDMA / LTE
- Macrocell Base Station Driver
- Microcell Base Station
- Small Cell Final Stage
- Active Antenna
- General Purpose Applications

Ordering Information

Part No.	Description
QPA4501SB	Sample Bag – 5 Pieces
QPA4501SR	Short Reel – 100 Pieces
QPA4501TR13	13” Reel – 2500 Pieces
QPA4501EVB01	Tested 4.4 – 5.0 GHz EVB

Absolute Maximum Ratings

Parameter	Value	Units
Breakdown Voltage (BV_{DG})	120	V
Gate Voltage ($V_{G1,2,3}$)	−7 to +2	V
Drain Voltage ($V_{D1,2,3}$)	+40	V
RF Input Power [1]	+12	dBm
VSWR Mismatch, P3dB Pulse (10% Duty Cycle, 100 µs Pulse Width), T = +25°C	10:1	
Power Dissipation	63	W

Notes:
1. Tested at 4.7 GHz, T = +25°C, single-carrier, 20 MHz LTE signal with 7.8 dB PAR at 0.01% CCDF.
2. Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Gate Voltage (V_{G1})		−2.6		V
Gate Voltage (V_{G2})		−4.2		V
Gate Voltage (V_{G3})		−2.6		V
Drain Voltage ($V_{D1,2,3}$)		+28		V
Quiescent Current (I_{DQ1})		50		mA
Quiescent Current (I_{DQ3})		75		mA
Power Dissipation		3.8		W

Note: Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Parameter	Conditions	Min	Typ	Max	Units
Frequency Range		4.4		5.0	GHz
Driver Quiescent Current (I_{DQ1})			50		mA
Carrier Quiescent Current (I_{DQ3})			75		mA
Gain	P_{AVG} = 31 dBm	26.0	29.9		dB
Saturated Power (P_{SAT})	Pulse (10% Duty Cycle, 500 µs Width), P_{IN} = 19 dBm	41.9	43.5		dBm
Power Added Efficiency (PAE)	P_{AVG} = 31 dBm	19.8	25.7		%
Raw ACLR	P_{AVG} = 31 dBm		−35.1		dBc

Test conditions unless otherwise noted: $V_{D1,2,3}$ = +28 V, I_{DQ1} = 50 mA, I_{DQ3} = 75 mA, V_{G2} = −4.2 V, T = +25°C, using a single-carrier, 20 MHz LTE signal with 7.8 dB PAR at 0.01% CCDF on the reference design fixture.

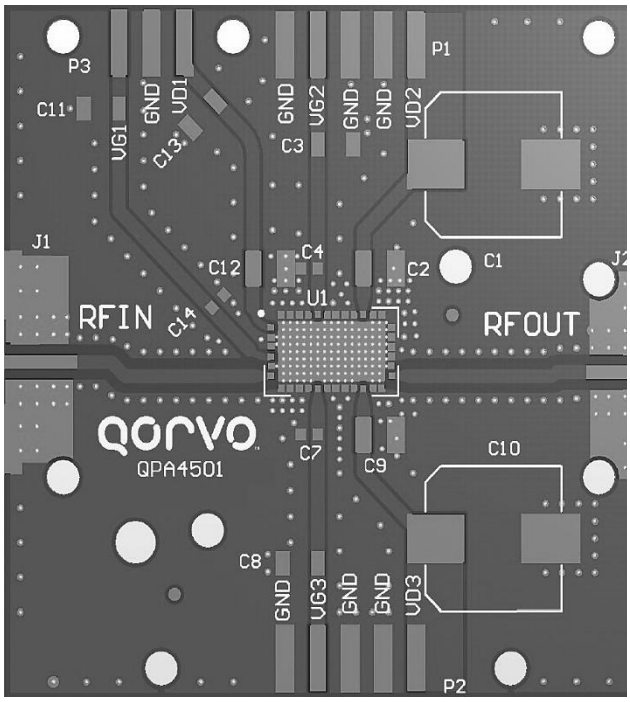
Thermal Information

Parameter	Conditions	Values	Units
Peak IR Surface Thermal Resistance at Average Power (θ_{JC})	T_{CASE} = +85°C, T_{CH} = 91°C CW: P_{DISS} = 4 W, P_{OUT} = 1.25 W	1.5	°C/W

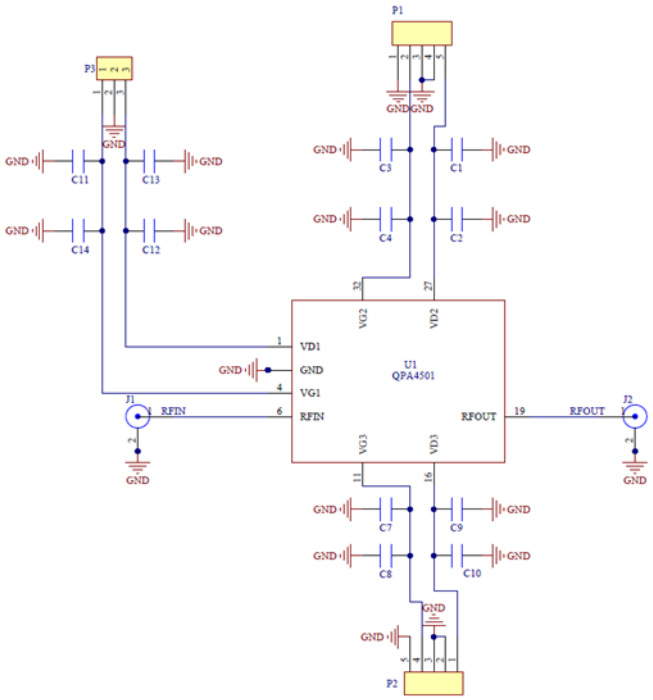
Notes:
1. Based on expected carrier amplifier efficiency of Doherty.
2. P_{OUT} assumes 10% peaking amplifier contribution of total average Doherty rated power.
3. Thermal resistance is measured to package backside.
4. Refer to the following document: GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates

QPA4501 4.4 – 5.0 GHz Reference Design

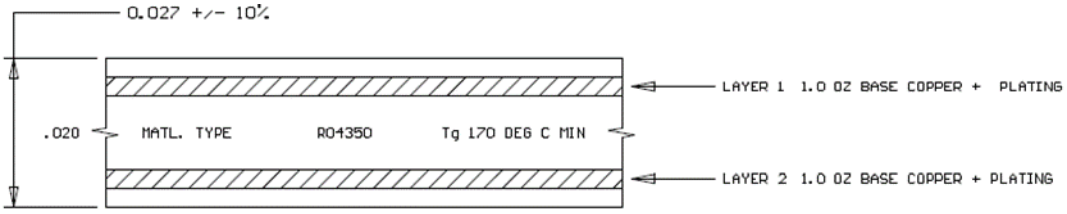
EVB Layout



EVB Schematic



PCB Stackup and Material

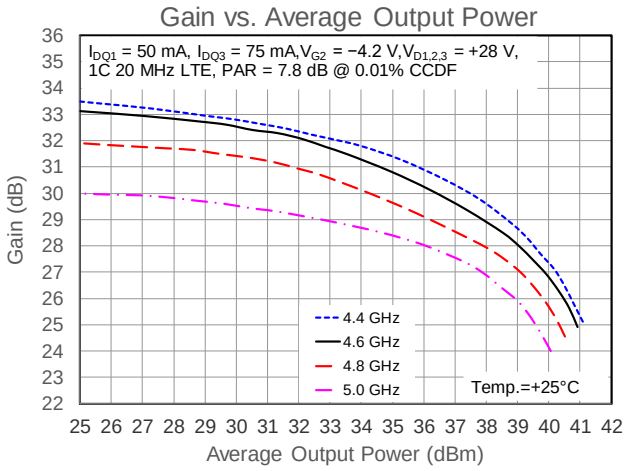


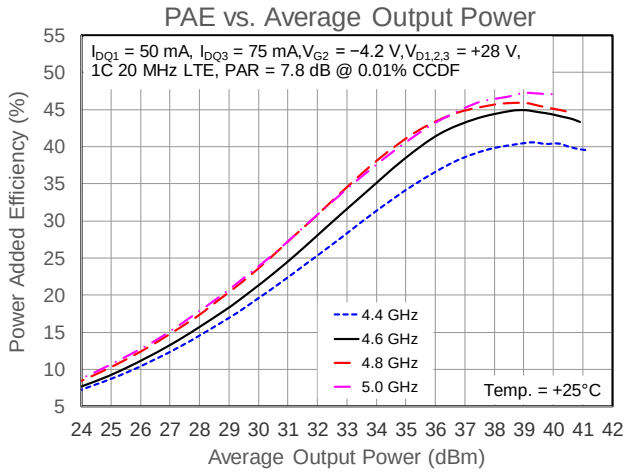
Notes:
1. All dimensions are in inches.
2. PCB is soldered on a 2 in. x 2 in. copper base plate with 0.25 in. thickness.

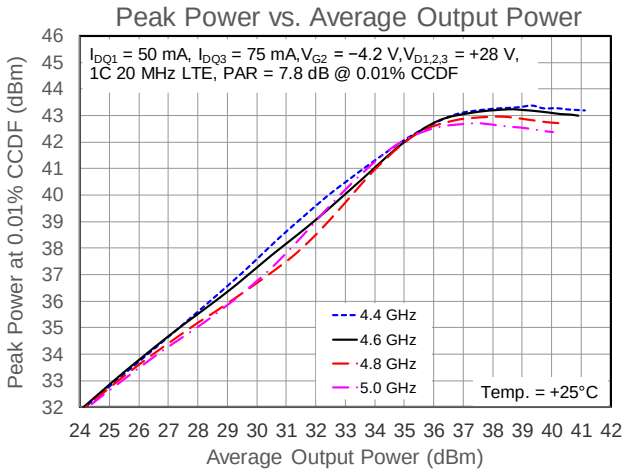
Bill of Materials – QPA4501 4.4 – 5.0 GHz Evaluation Board

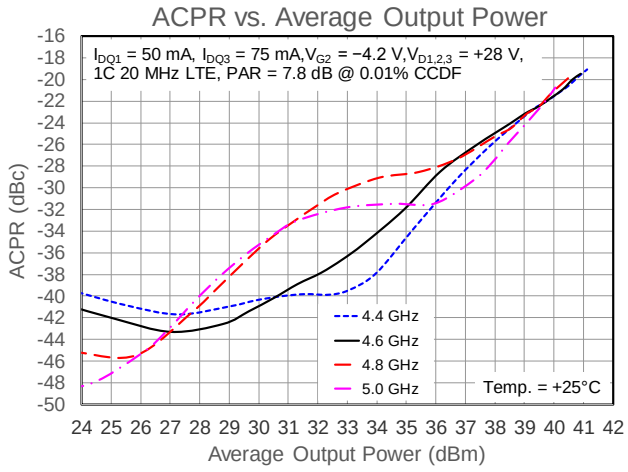
Reference Des.	Value	Description	Manufacturer	Part Number
C1, C10	220 µF	Capacitor, 220 µF, electrolytic, 50 V	Panasonic	EEEFK1H221P
C4, C7, C14	22,000 pF	Capacitor, 22,000 pF, 10%, 50 V, X7R, 0603	Murata	GRM188R71H223KA01D
C3, C8, C11, C13	4.7 µF	Capacitor, 4.7 µF, 10%, 50 V, X7R, 1206	Murata	GRM31CR71H475KA12L
C2, C9, C12	10 µF	Capacitor, 10 µF, 10%, 50 V, X7R, 1210	Murata	GRM32ER71H106KA
J1, J2		Connector, SMA, 4-Hole Panel Mount Jack	Gigalane	PAF-S00-000
P1, P2		Connector, HDR, ST, PLRZD, 5-Pin, 0.100”	ITW Pancon	MPSS100-5-C
P3		Connector, HDR, ST, 3-PIN, T/H	Molex	22-28-4033
U1		3 W 4.4 – 5.0 GHz GaN PA Module	Qorvo	QPA4501

Performance Plots



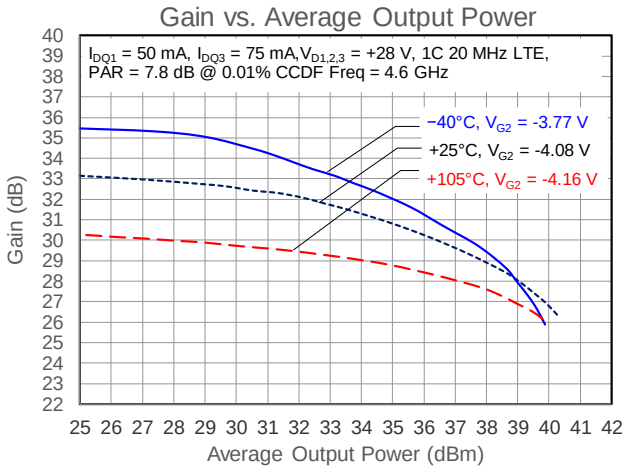


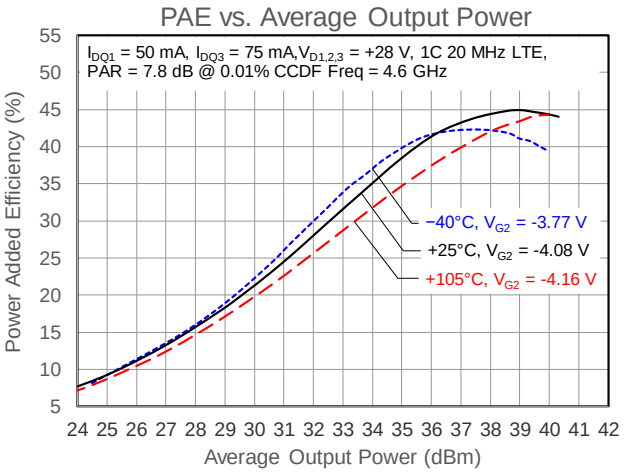


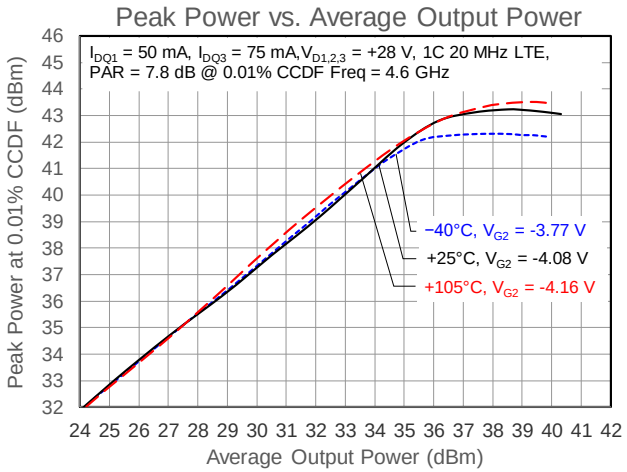


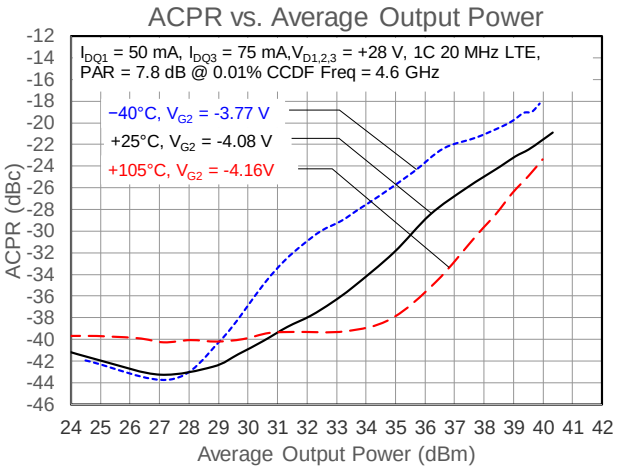
Test conditions unless otherwise noted: $V_{D1,2,3}$ = +28 V, I_{DQ1} = 50 mA, I_{DQ3} = 75 mA, V_{G2} = −4.2 V, T = +25°C, tested using a single-carrier, 20 MHz LTE signal with 7.8 dB PAR at 0.01% CCDF on a reference design fixture.

Performance Plots



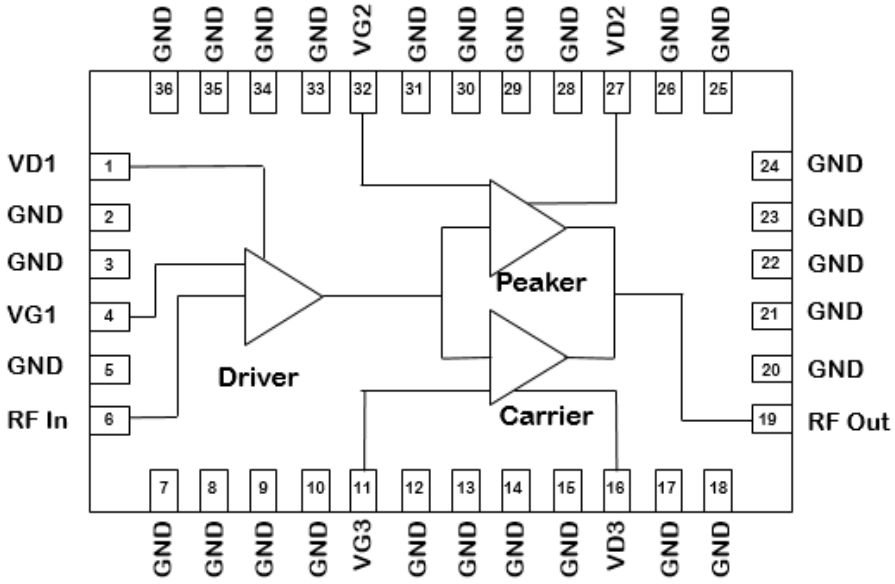






Test conditions unless otherwise noted: $V_{D1,2,3}$ = +28 V, I_{DQ1} = 50 mA, I_{DQ3} = 75 mA, V_{G2} = −4.2 V, tested at 4.6 GHz using a single-carrier, 20 MHz LTE signal with 7.8 dB PAR at 0.01% CCDF on a reference design fixture.

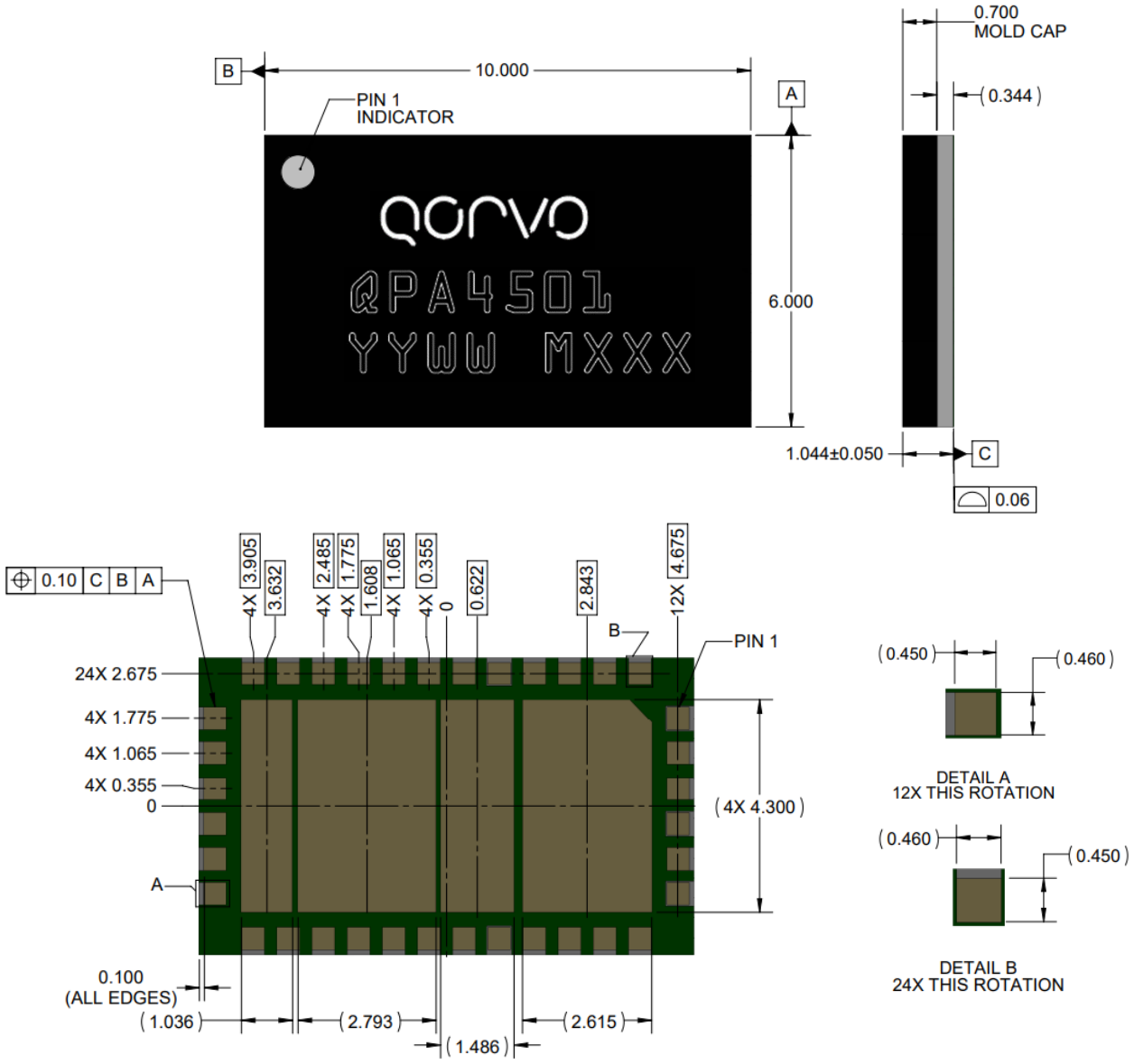
Pad Configuration and Description



Pad No.	Label	Description
1	VD1	Driver Amplifier, Drain Bias
4	VG1	Driver Amplifier, Gate Bias
6	RF IN	RF Input
11	VG3	Carrier Amplifier, Gate Bias
16	VD3	Carrier Amplifier, Drain Bias
19	RF OUT	RF Output
27	VD2	Peaking Amplifier, Drain Bias
32	VG2	Peaking Amplifier, Gate Bias
2 – 3, 5, 7, 10, 12 – 15, 17 – 18, 20 – 26, 28 – 31, 33 – 36	GND	Internal Grounding. Recommend connecting to Epad ground.
EPAD	GND	DC/RF Ground. Must be soldered to EVB ground plane over array of vias for thermal and RF performance. Solder voids under EPAD will result in excessive junction temperatures causing permanent damage.

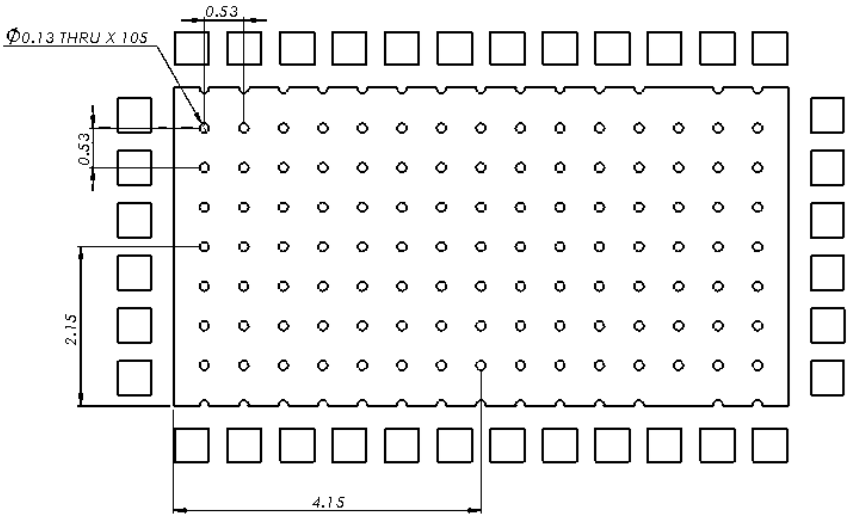
Package Marking and Dimensions

Marking: Qorvo Logo
Part Number – QPA4501
Date Code – YYWW
Batch Code – MXXXX



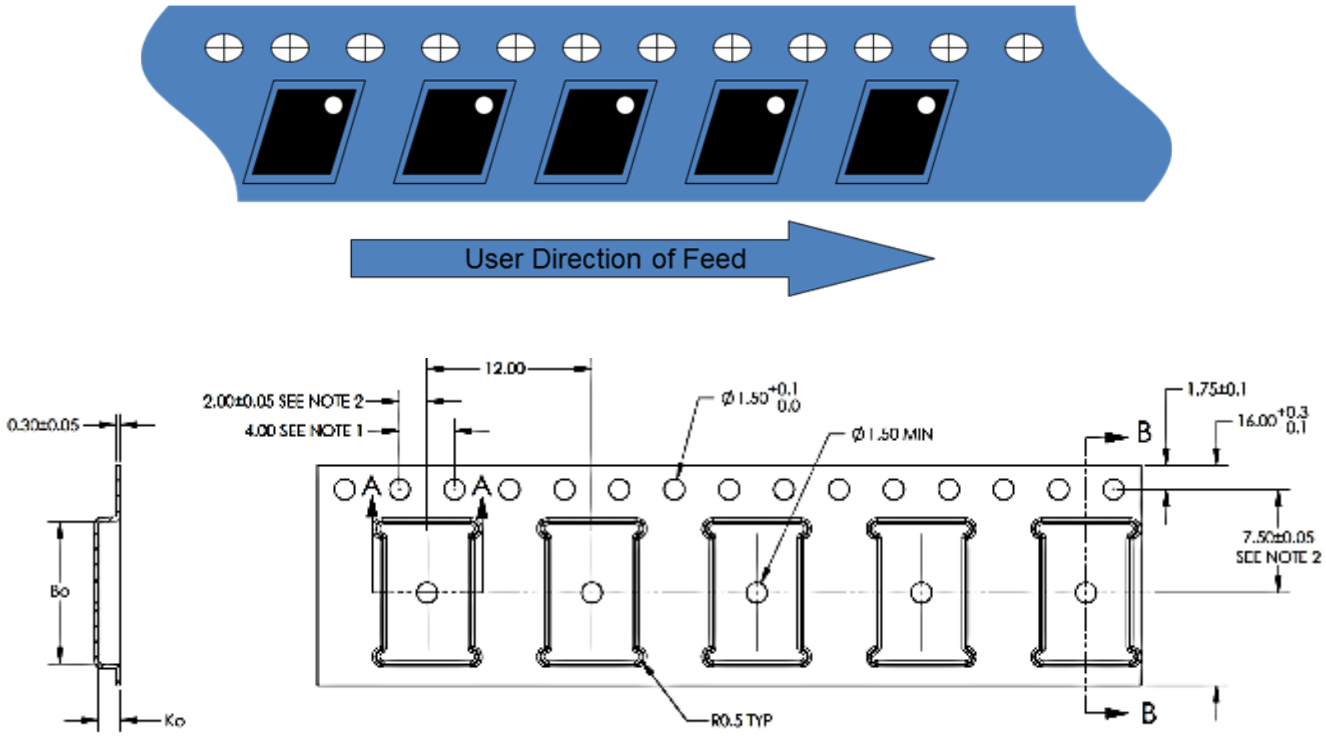
Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Exposed metallization is NiPdAu plated. Au thickness is 0.095 µm.

Mounting Footprint Pattern



Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. All vias are plated thru hole (PTH) to ground.
3. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

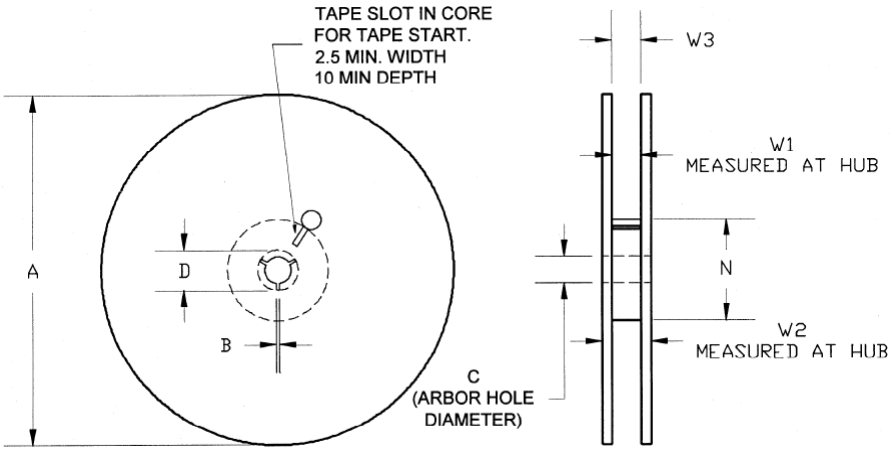
Tape and Reel Information – Carrier and Cover Tape Dimensions



Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.248	6.30
	Width	B0	0.406	10.3
	Depth	K0	0.061	1.55
	Pitch	P1	0.472	12.0
Centerline Distance	Cavity to Perforation - Length Direction	P2	0.079	2.00
	Cavity to Perforation - Width Direction	F	0.295	7.5
Cover Tape	Width	C	0.524	13.3
Carrier Tape	Width	W	0.630	16.0

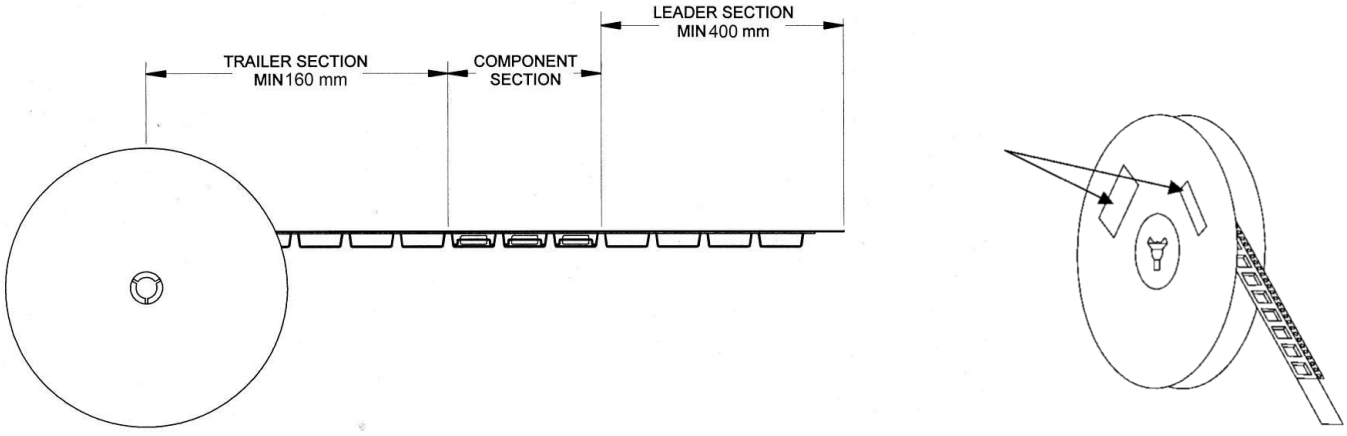
Tape and Reel Information – Reel Dimensions

Standard T/R size = 2,500 pieces on a 13” reel.



Feature	Measure	Symbol	Size (in)	Size (mm)
Flange	Diameter	A	12.992	330.0
	Thickness	W2	0.874	22.2
	Space Between Flange	W1	0.661	16.8
Hub	Outer Diameter	N	4.016	102.0
	Arbor Hole Diameter	C	0.512	13.0
	Key Slit Width	B	0.079	2.0
	Key Slit Diameter	D	0.787	20.0

Tape and Reel Information – Tape Length and Label Placement



Notes:
1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481-1-A.
2. Labels are placed on the flange opposite the sprockets in the carrier tape.

Recommended Solder Temperature Profile