QPA5263A

DC – 4500 MHz Cascadable SiGe HBT Amplifier

6 Lead SOT-363 Package

Product Overview

The QPA5263A is a high performance SiGe HBT MMIC amplifier. A Darlington configuration provides high FT and excellent thermal performance. The heterojunction increases breakdown voltage and minimizes leakage current between junctions. Cancellation of emitter junction non-linearities results in higher suppression of intermodulation products.

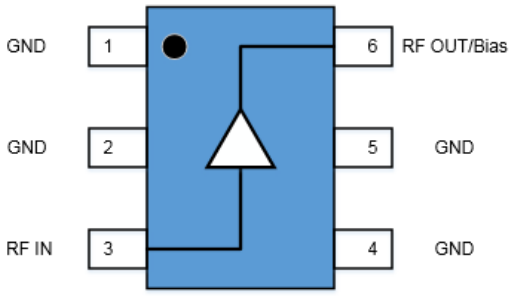
The QPA5263A may be operated from a variety of supply voltages by using a voltage dropping resistor. Two DC-blocking capacitors, bypass capacitors and an optional RF choke complete the circuit required for operation of this internally matched 50 ohm device.

The QPA5263A is assembled in an industry standard SOT-363 package that is lead-free and RoHS-compliant.

Key Features

- DC to 4500 MHz Operation
- Single Positive Voltage Supply
- Gain: 12.5 dB at 1950 MHz
- Output IP3: +30.5 dBm typical at 1950 MHz
- Noise Figure: 4.4 dB Typical at 1950 MHz
- Lead-free/RoHS-compliant SOT-363 Package

Functional Block Diagram



Top View

Applications

- Cellular, PCS, GSM, UMTS
- PA Driver Amplifier
- IF/RF Buffer Amplifier
- Wireless Data, Satellite

Ordering Information

Part No.	Description
QPA5263ASQ	25 Piece Sample Bag
QPA5263ASR	100 Pieces on 7” Reel
QPA5263ATR7	3000 pieces on a 7” reel
QPA5263APCK401	850 MHz, EVB with 5 Piece Sample Bag

Absolute Maximum Ratings

Parameter	Rating
Storage Temp	−55 to +150 °C
Device Voltage (V_D)	+6 V
Device Current (I_D)	120 mA
RF Input Power (Z_L = 50 Ω)	+16 dBm

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Bias Conditions should also satisfy the following expression:
$I_D \times V_D < (T_{JUNCTION} - T_{LEAD}) / R_{TH}$

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Operating Temperature	−40		+105	°C
Junction Temperature (T_J)			+125	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Parameter	Conditions (1)	Min	Typ	Max	Units
Small Signal Gain	850 MHz		12.8		dB
	1950 MHz		12.5		
	2400 MHz		12.4		
Output Power at 1dB Compression	850 MHz		+16.3		dBm
	1950 MHz		+15.2		
	2400 MHz		+15.1		
Output Third Intercept Point	850 MHz		+33.9		dBm
	1950 MHz (2)		+30.5		
	2400 MHz		+29.1		
Input Return Loss, |S11|	850 MHz		13.9		dB
	1950 MHz		13.8		
	2400 MHz		15.6		
Output Return Loss, |S22|	850 MHz		15.8		dB
	1950 MHz		14.5		
	2400 MHz		14.5		
Reverse Isolation, |S12|	850 MHz		17.8		dB
	1950 MHz		18.2		
	2400 MHz		18.5		
Noise Figure	850 MHz		4.3		dB
	1950 MHz		4.4		
	2400 MHz		4.5		
Device Operating Voltage		+3.05	+3.4	+3.95	V
Device Operating Current			60		mA
Thermal Resistance			97		°C/W

Notes:
1. Test conditions unless otherwise noted: V_S = +8 V, R_{BIAS} = 75 Ω, I_D =60 mA Typ., OIP3 Tone Spacing = 1 MHz, P_{OUT} per tone = −5 dBm, T_{LEAD} = +25°C, Z_S = Z_L =50 Ω
2. Pout per tone = -10 dBm

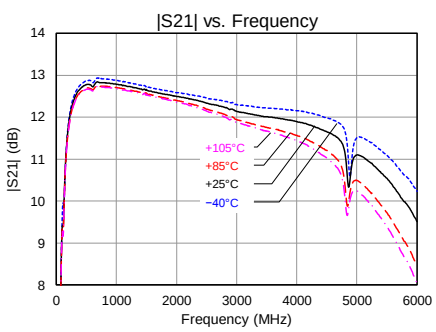
Typical Performance – 850 MHz Application Circuit

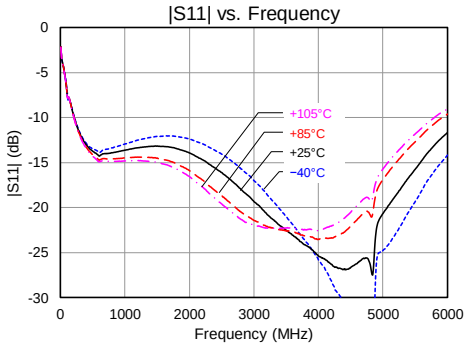
Parameter	Typical Value					Units
Frequency	500	850	1950	2400	3500	MHz
Small Signal Gain	12.8	12.8	12.5	12.4	12.0	dB
Output Third Intercept Point	+35.8	+33.9	+30.5	+29.1	+26.6	dBm
Output Power at 1dB Compression	+16.1	+16.3	+15.2	+15.1	+14.2	dBm
Input Return Loss	13.7	13.9	13.8	15.6	22.5	dB
Output Return Loss	13.3	15.8	14.5	14.5	15.7	dB
Reverse Isolation	17.8	17.8	18.2	18.5	19.4	dB
Noise Figure	4.2	4.3	4.4	4.5	5.0	dB

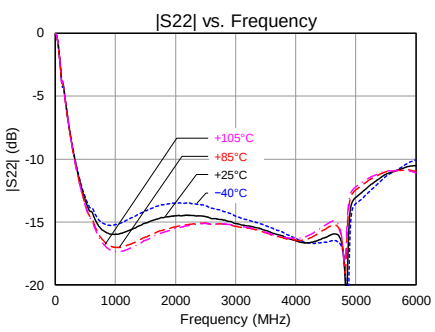
Notes:
1. Test conditions: V_S = +8 V, I_D = 60 mA Typ., OIP3 Tone Spacing=1 MHz, P_{OUT} per tone = -5 dBm, 50 Ω system, Temp = +25 °C

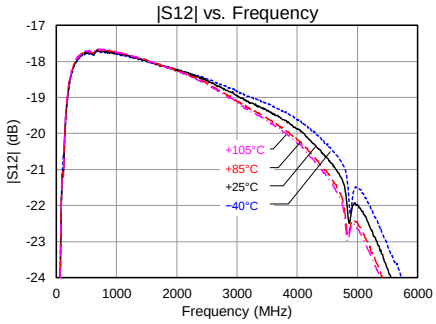
Performance Plots – 850 MHz Application Circuit

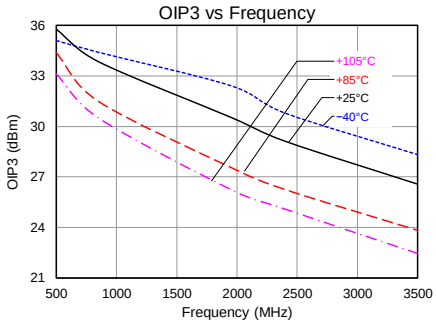
Test conditions unless otherwise noted: V_S = +8 V, R_{BIAS} = 75 Ω, I_D =60 mA Typ

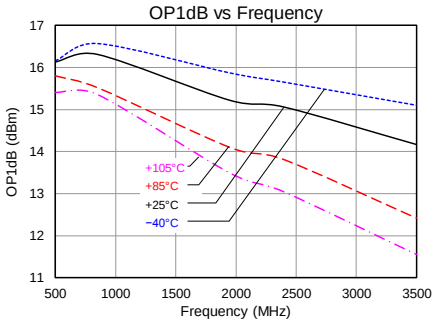


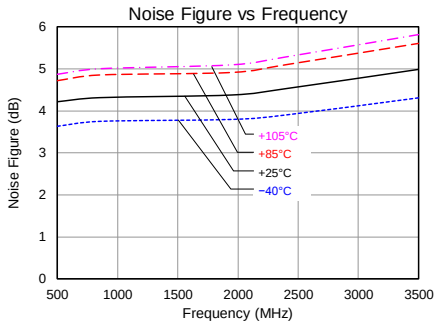


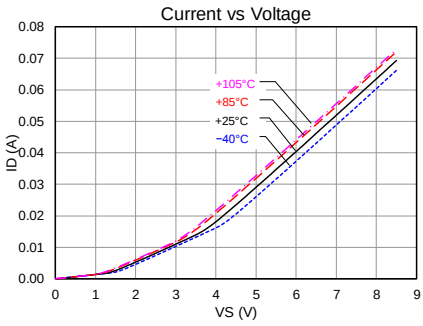




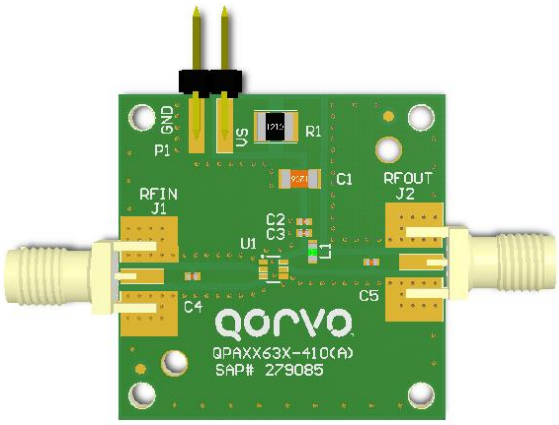


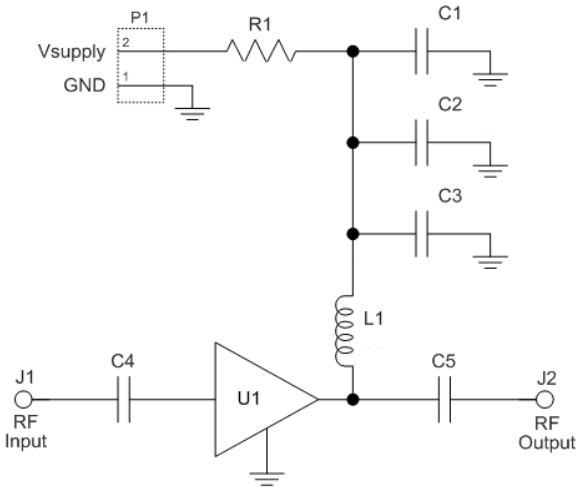






Evaluation Board and Schematic – 850 MHz Application Circuit





Bill of Material – 850 MHz Application Circuit

Reference	Value	Description	Manufacturer	Part Number
n/a	n/a	PCB	Qorvo	QPAXX63X-410(A)
U1	n/a	HBT MMIC Amplifier	Qorvo	QPA5263A
C1	1 uF	CAP, 10%, 25V, X7R, 1206	Murata Electronics	GRM31MR71E105KA01L
C2	1000 pF	CAP, 10%, 50V, X7R, 0402	Murata Electronics	GRM155R71H102KA01D
C3	68 pF	CAP, 5%, 50V, C0G, 0402	Murata Electronics	GRM1555C1H680JA01D
C4, C5	100 pF	CAP, 5%, 50V, C0G, 0402	Murata Electronics	GRM1555C1H101JA01D
R1	75 Ω	RES, 5%, 1/2W, 1210	Panasonic Industrial Devices	ERJ-14YJ750U
L1	33 nH	IND, 5%, M/L, 0603	Murata Electronics	LL1608-FSL33NJ
J1, J2	n/a	CONN, SMA, EL, FLT, 0.068" SPE-000318	Amphenol RF Asia Corp	901-10426
P1	n/a	CONN, HDR, ST, 1x2, 0.100", Hi-temp, T/H	Samtec Inc	HTSW-102-07-G-S

Component Values for Specific Frequencies

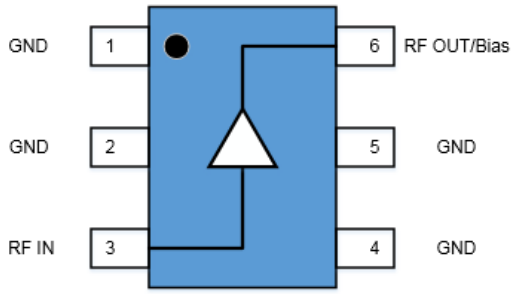
Reference Designator	500 MHz	850 MHz	1950 MHz	2400 MHz	3500 MHz
C4, C5	220 pF	100 pF	68 pF	56 pF	39 pF
C3	100 pF	68 pF	22 pF	22 pF	15 pF
L1	68 nH	33 nH	22 nH	18 nH	15 nH

Bias Resistor Values for Specific Supply Voltages

Reference Designator	V_S=+5 V	V_S=+8 V	V_S=+9 V	V_S=+12 V
R1 (Rbias) (1,2)	27 Ω	75 Ω	91 Ω	140 Ω

Notes:
1. Bias resistor improves current stability over temperature
2. Bias Resistance = $R_{BIAS} + R_{LDC} = (V_S - V_D) / I_D$

Pin Configuration and Description

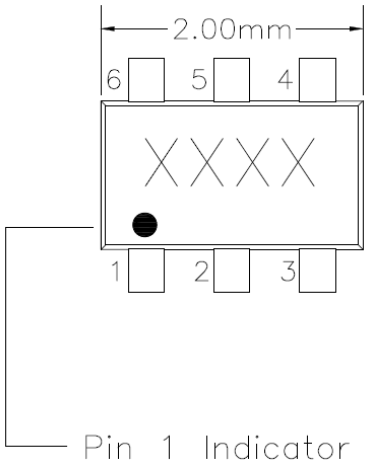


Top View

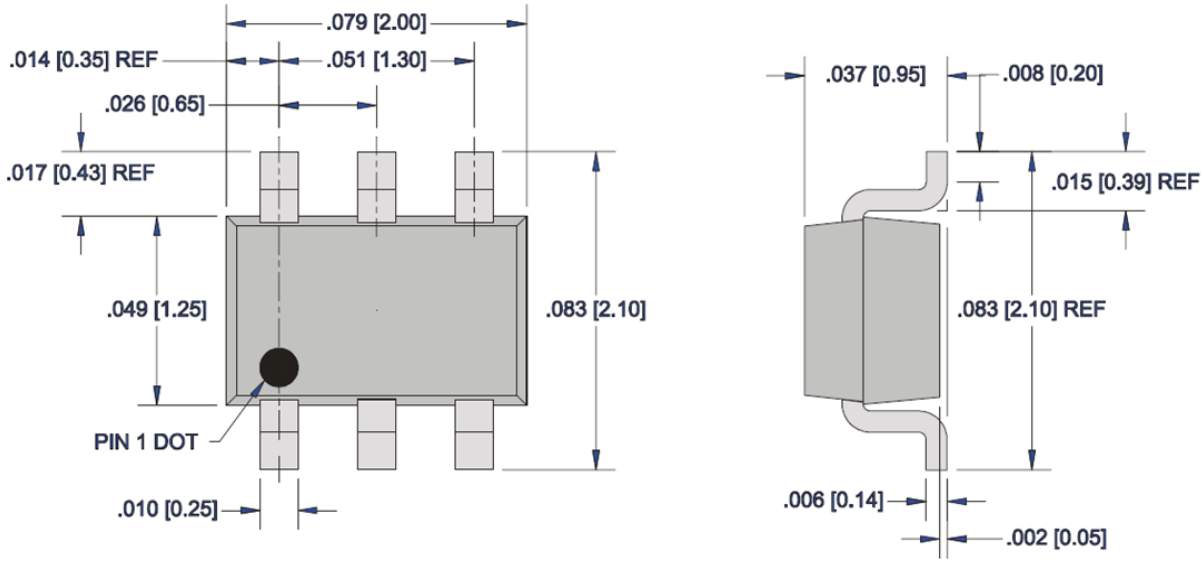
Pad No.	Label	Description
1, 2, 4, 5	GND	Connection to ground. Use via holes in PCB for best performance to reduce lead inductance as close to ground leads as possible
3	RF_{IN}	RF Input Pin. DC voltage is present on this pin therefore this pin requires the use of an external DC blocking capacitor chosen for the frequency of operation.
6	RF_{OUT}/Bias	RF Output and Bias Pin. DC voltage is present on this pin therefore this pin requires the use of an external DC blocking capacitor chosen for the frequency of operation.

Package Marking

XXXX is an Alpha-numeric trace code.

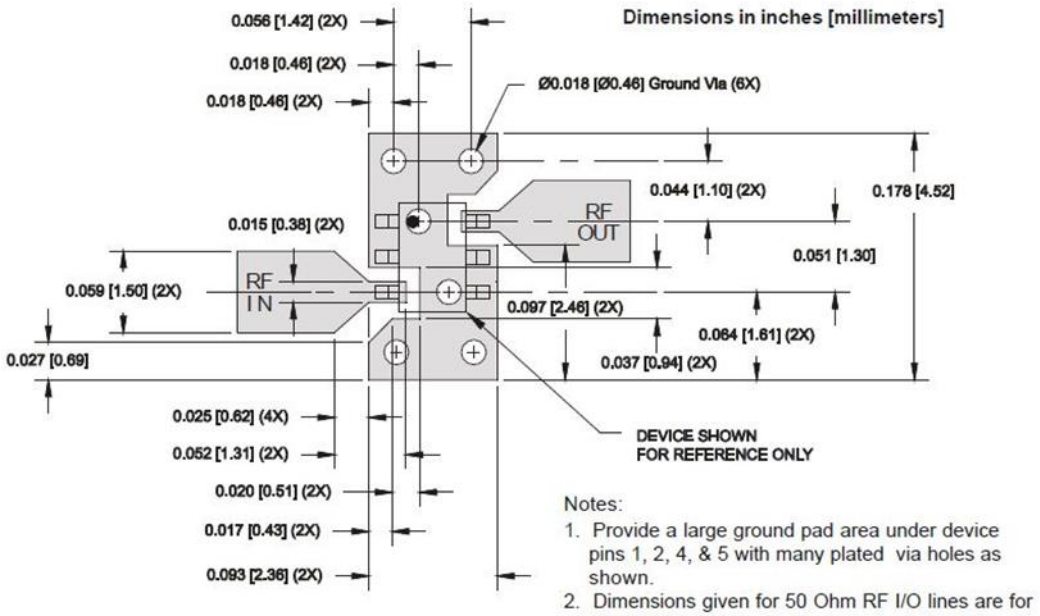


Package Dimensions



Notes:
1. All dimensions are in inches (millimeters). Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.5-2009.

PCB Mounting Pattern



Notes:
1. Provide a large ground pad area under device pins 1, 2, 4, & 5 with many plated via holes as shown.
2. Dimensions given for 50 Ohm RF I/O lines are for 31 mil thick Getek. Scale accordingly for different board thicknesses and dielectric contants.
3. We recommend 1 or 2 ounce copper. Measurements for this data sheet were made on a 31 mil thick Getek with 1 ounce copper on both sides.