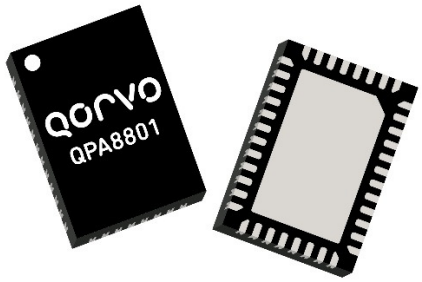
QPA8801

75Ω 11dB CATV Push Pull Amplifier (45 – 1218 MHz)

Product Overview

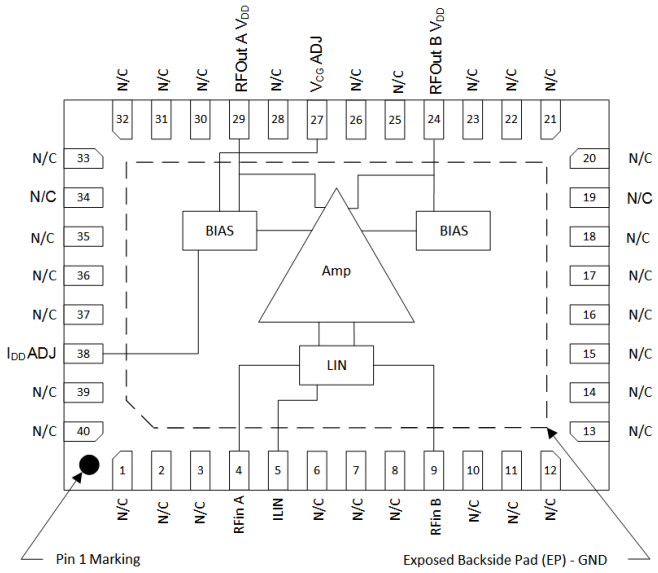
The QPA8801 is an ultra-linear, QFN GaAs amplifier MMIC intended for output stage amplification in CATV infrastructure applications. The device features a push-pull cascode design which provides flat gain along with ultra-low distortion, making it ideal for use in CATV distribution systems requiring high output power capability. The QPA8801 draws approximately 380 mA from a single +12 V supply providing approximately 11dB gain with excellent linearity. Users may adjust the bias current with external voltage enabling the QPA8801 to be used in applications such as doublers or for lower power system applications.

The QPA8801 is packaged in an industry standard 40-pin 5 x 7 mm QFN package with exposed paddle (EP) beneath the device for thermal and electrical grounding.



40P 5x7 QFN Package

Functional Block Diagram



Key Features

- Gain: 11dB at 1218 MHz
- Adjustable Bias
- 45 – 1218 MHz BW
- 49 dBmV / ch virtual 1.0 GHz, at 3 dB tilt
- Low Noise: 5.5 dB
- Excellent Composite Distortion
- pHEMT / MESFET device technologies
- Compact Size: 40P 5x7 QFN
- Power Consumption (12 V, 380 mA – 4.56 W)

Applications

- DOCSIS 3.1
- Broadband CATV hybrid modules
- Head End CMTS Equipment
- 75Ω amplifiers

Ordering Information

Part Number	Description
QPA8801SQ	Sample bag with 25 pieces
QPA8801SR	7" Reel with 100 pieces
QPA8801TR13	13" Reel with 2500 pieces
QPA8801PCK	45 – 1218 MHz PCBA with 5-piece sample bag

Absolute Maximum Ratings

Parameter	Rating
Supply Voltage (V_{DD})	+18 V
Supply Current (I_{DD})	570 mA
Maximum Input Level (single tone)	+70 dBmV
Operating Temperature Range	–40 to +85 °C
Storage Temperature Range	–40 to +100 °C
Maximum Junction Temperature	+150 °C

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

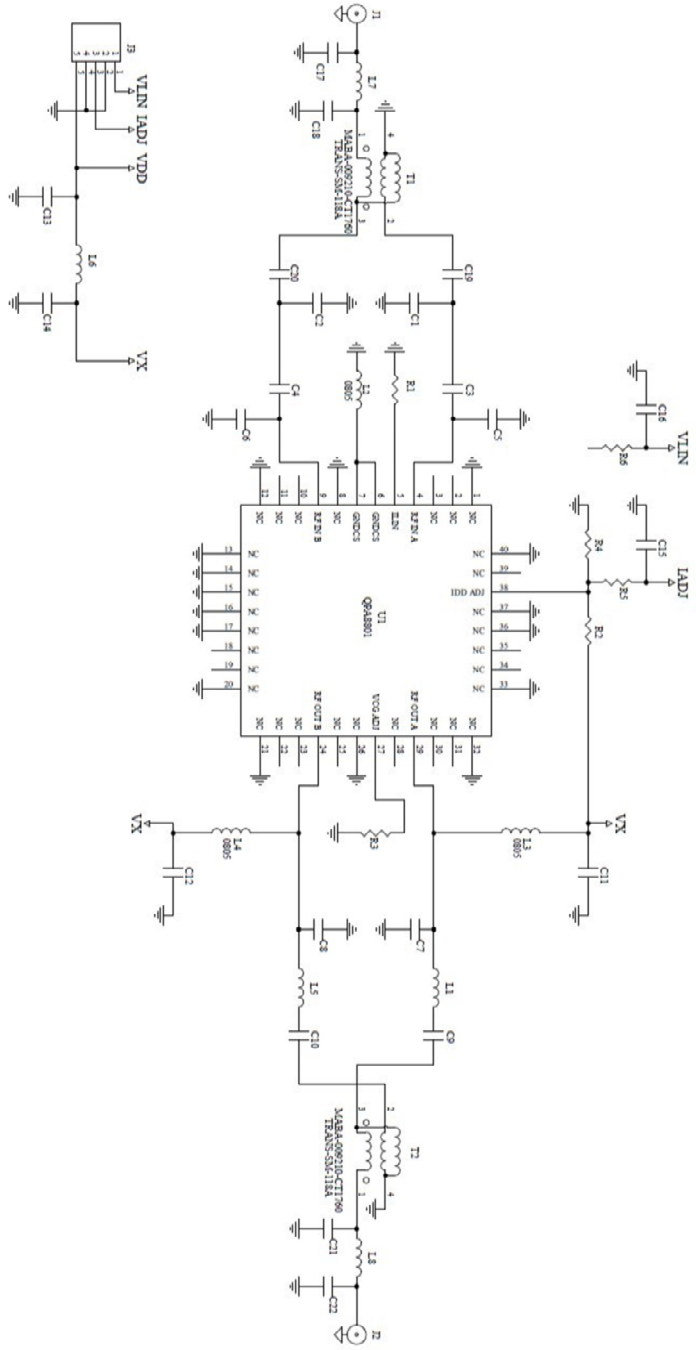
Electrical Specifications – 12V

Parameter	Condition (1)	Min	Typ	Max	Unit
Supply Voltage (V_{DD})			12		V
Supply Current (I_{DD})	V_{DD} total current		380		mA
Frequency Range		50		1218	MHz
Gain	1218 MHz		11		dB
Gain Flatness	Max. deviation from line using least squares fit from 47 to 1218 MHz		±0.5		dB
Gain Slope	Gain (1218 MHz) – Gain (50 MHz)		0.6		dB
Reverse Isolation			-18.5		dB
Input Return Loss			18		dB
Output Return Loss			18		dB
Noise Figure			5.5		dB
CSO	80 NTSC + 72 QAM (–6 dB offset), 49 dBmV / ch virtual output at 1003 MHz at 3 dB tilt		-70		dBc
CTB			-78		dBc
CIN			68		dB
OIP2	Low band: 225 MHz, 275.5 MHz, 15 dBm / tone		80		dBm
	High band: 1100 MHz, 1150.5 MHz, 15 dBm / tone		78		dBm
OIP3	Low band: 225 MHz, 275.5 MHz, 15 dBm / tone		50		dBm
	High band: 1100 MHz, 1150.5 MHz, 15 dBm / tone		47		dBm
Output P1dB	1218 MHz		27.5		dBm
Thermal Resistance	Θ_{JB} (Junction to backside of QFN)		6		˚C/W

Notes:

1. Typical performance at these conditions: Temp = +25 °C, V_{DD} = +12 V, 75 Ω system, Full band unless otherwise noted

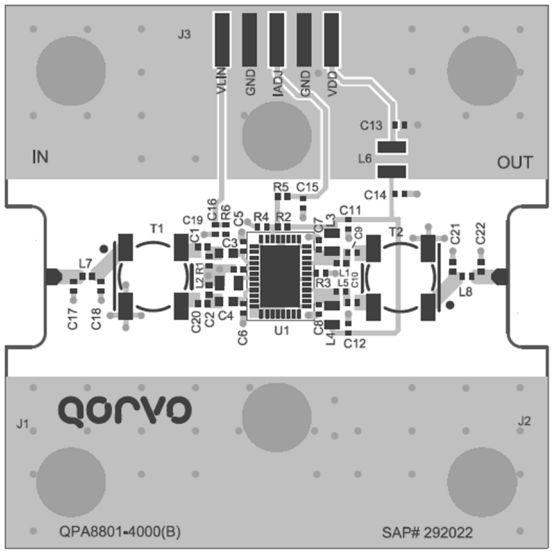
Evaluation Board Schematic (47 – 1218 MHz)

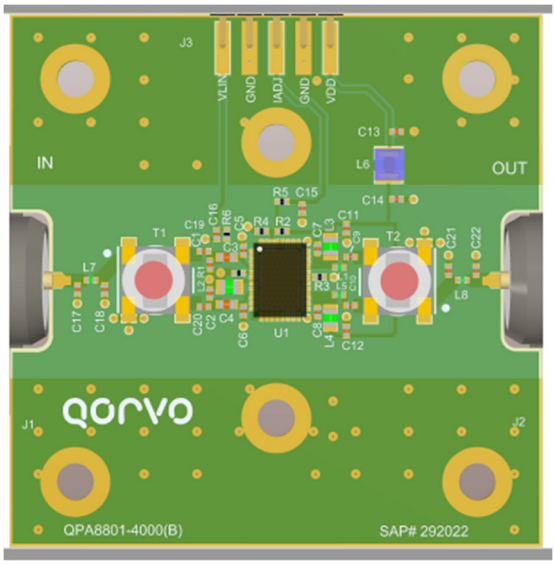


Evaluation Board Bill of Material

Ref Designator	Description	Manufacturer	Manufacturer Part #
C11, C12, C13, C14, C15, C16	CAP, 0.01 uF, 10%, 50V, X7R, 0402	Kemet	C0402C103K5RACTU
C9, C10	CAP, 390 pF, 10%, 50V, X7R, 0402	Murata Electronics	GRM155R71H391KA01D
C1, C2	CAP, 2.2 pF, 50V, C0G, 0402	Murata Electronics	GRM1555C1H2R2BA01D
C3, C4	CAP, 1000 pF, 5%, 50V, C0G, 0603	Murata Electronics	GRM1885C1H102JA01D
R2	RES, 2.7 KΩ, 5%, 1/10W, 0402	Panasonic Corp of America	ERJ-2GEJ272X
R1	RES, 560 Ω, 5%, 1/16W, 0402	KOA Speer Electronics, Inc.	RK73B1ETTP561J
C19, C20	RES, 0 Ω, 0402	KOA Speer Electronics, Inc.	RK73Z1ETTP
R5, R6	RES, 1.21 KΩ, 1%, 1/16W, 0402	KOA Speer Electronics, Inc.	RK73H1ETTP1211F
L6	IND, 0.9 uH, 10%, 1.3A, WW, 1008	Coilcraft, Inc.	1008AF-901XKL
L8	IND, 3.9 nH, 5%, W/W, 0402	Coilcraft, Inc.	0402CS-3N9XJLU
L3, L4	IND, 680 nH, 5%, 660mA, WW, 0805	Coilcraft, Inc.	0805AF-681XJR
L1, L5, L7	IND, 1.0 nH, 5%, 1.36A, 0402	Coilcraft, Inc.	0402CS-1N0XJL
T1, T2	XFMR, SMT, 75 Ω, 1:1 BALUN	Macom	MABA_009210_CT1760
J3	CONN, HDR, ST, PLRZD, 36-PIN	ITW Pancon	MPSS100-36-C
C5, C6, C7, C8, C17, C18, C21, C22, L2, R3, R4	Do Not Populate		

Evaluation Board Assembly Drawing

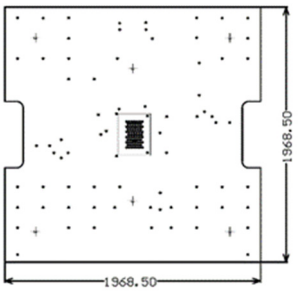


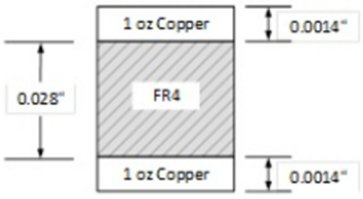


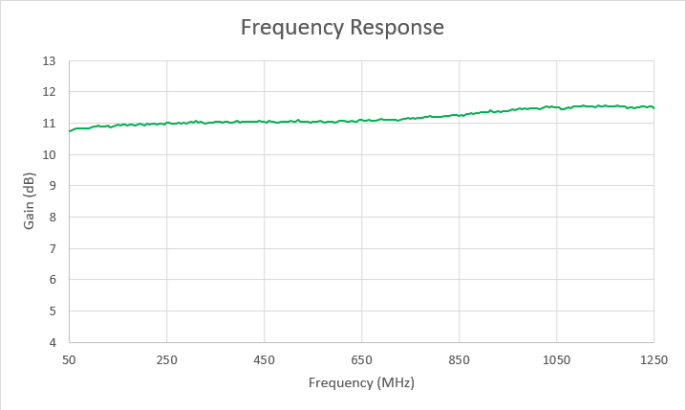
Performance Data – 12 V

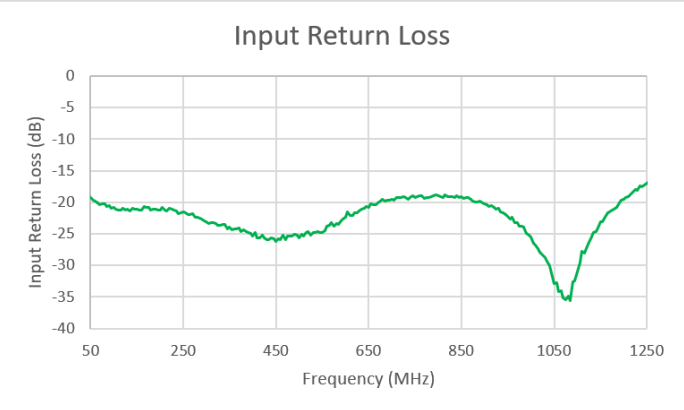
EVB PCB Material and Stack-up

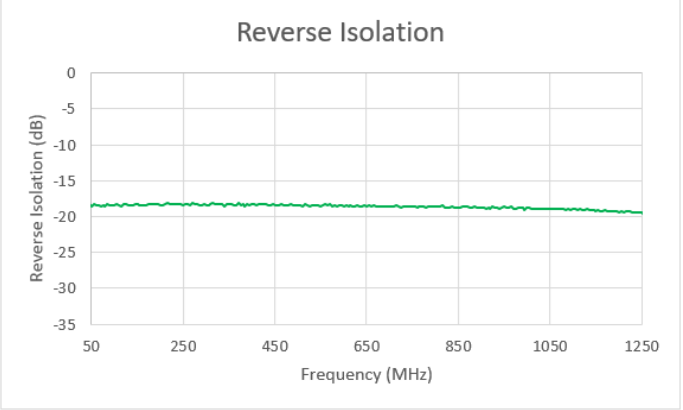
Board Material: 0.028" FR4, ε_r=4.2
Plating: 1oz Copper
Board Dimension: 1.9685" x 1.9685"

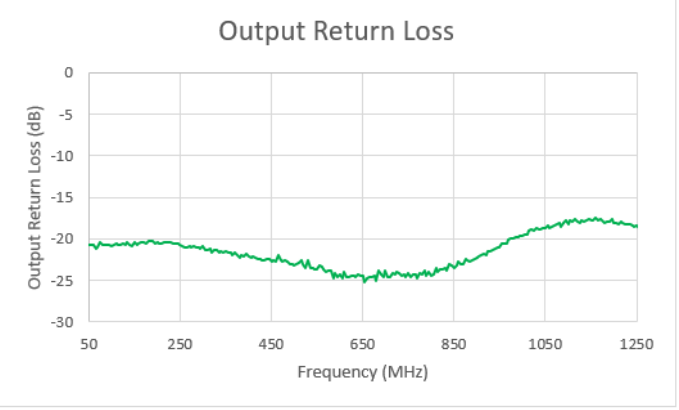


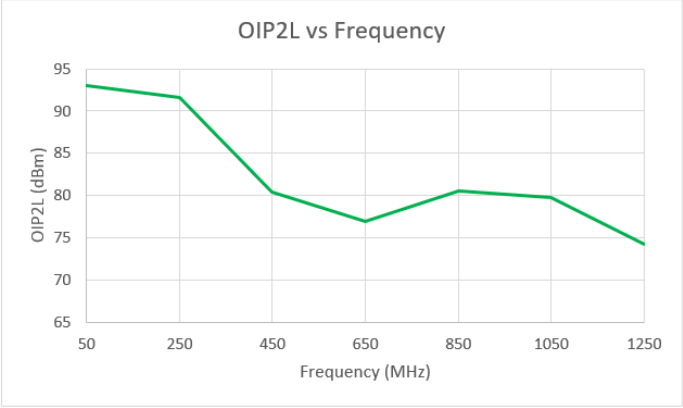


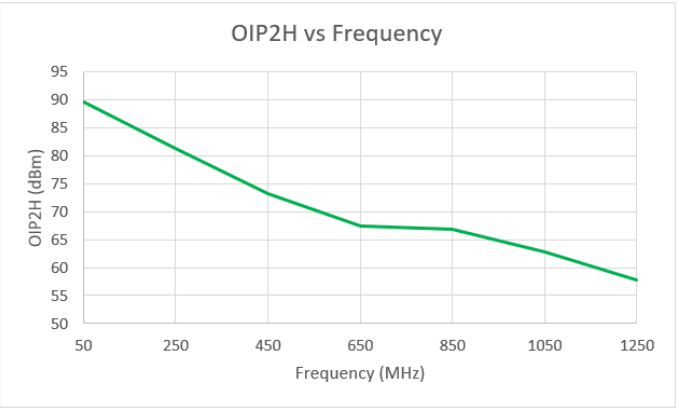

Frequency Response
Gain (dB)
13
12
11
10
9
8
7
6
5
4
50
250
450
650
850
1050
1250
Frequency (MHz)


Input Return Loss
Input Return Loss (dB)
0
-5
-10
-15
-20
-25
-30
-35
-40
50
250
450
650
850
1050
1250
Frequency (MHz)

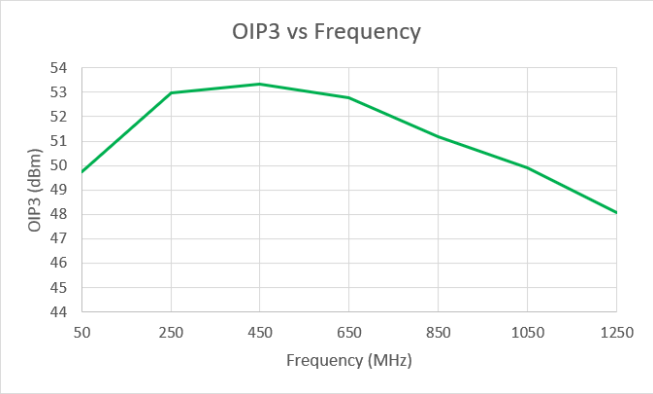

Reverse Isolation
Reverse Isolation (dB)
0
-5
-10
-15
-20
-25
-30
-35
50
250
450
650
850
1050
1250
Frequency (MHz)

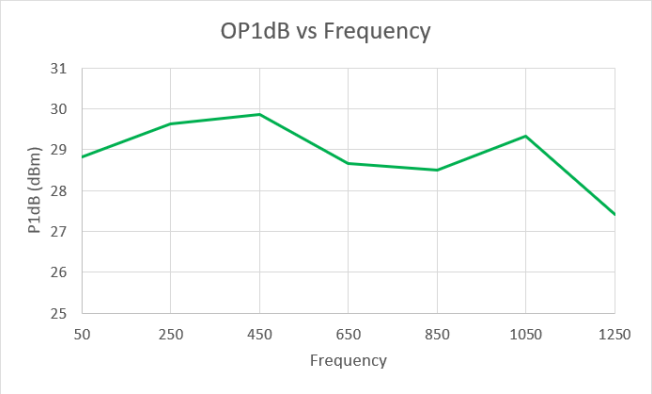

Output Return Loss
Output Return Loss (dB)
0
-5
-10
-15
-20
-25
-30
50
250
450
650
850
1050
1250
Frequency (MHz)

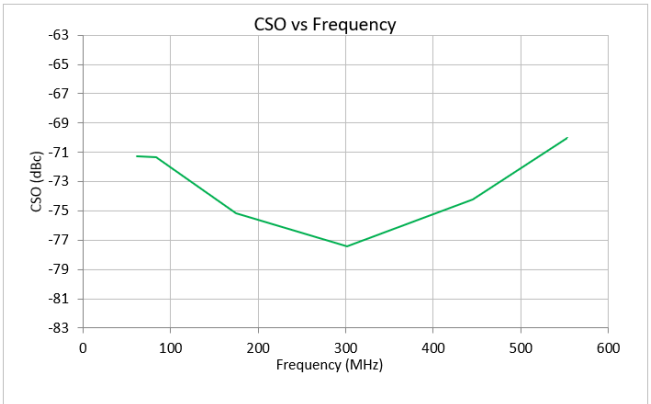

OIP2L vs Frequency
OIP2L (dBm)
95
90
85
80
75
70
65
50
250
450
650
850
1050
1250
Frequency (MHz)

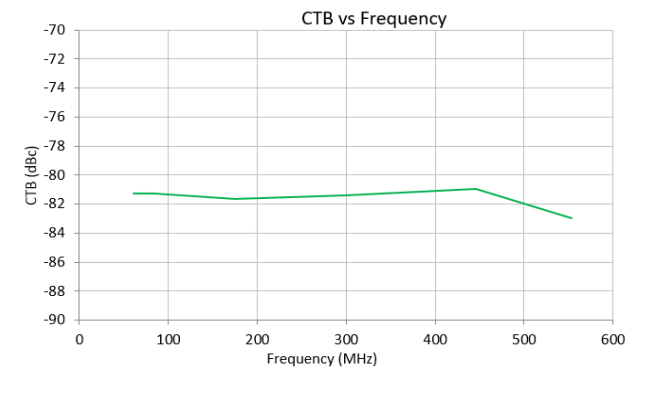

OIP2H vs Frequency
OIP2H (dBm)
95
90
85
80
75
70
65
60
55
50
50
250
450
650
850
1050
1250
Frequency (MHz)

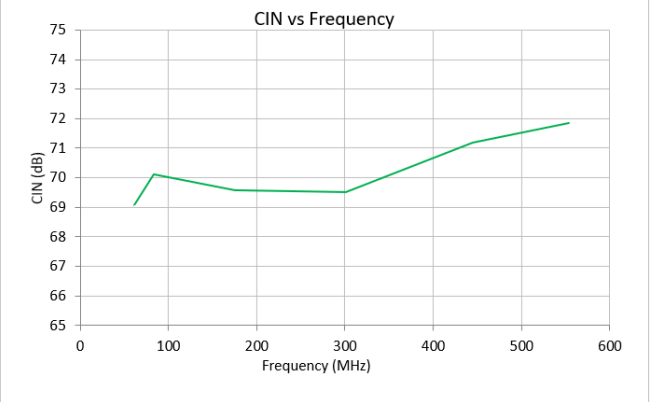
Performance Data – 12 V (cont'd)





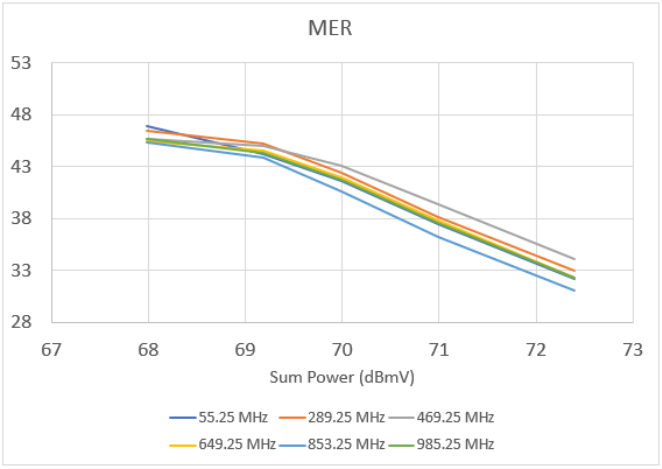


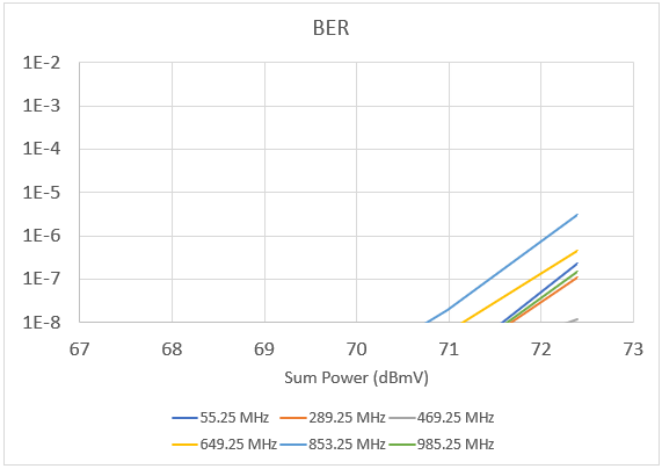


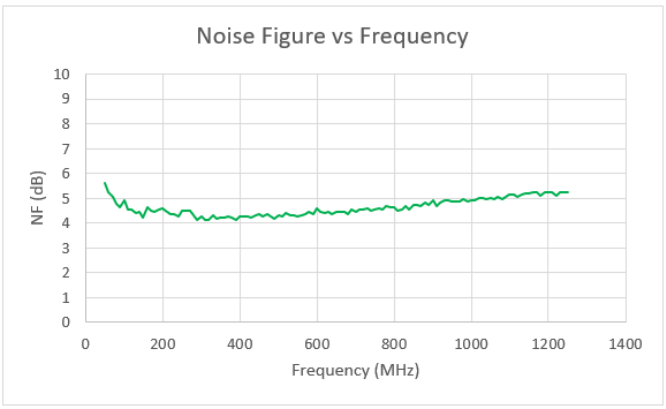


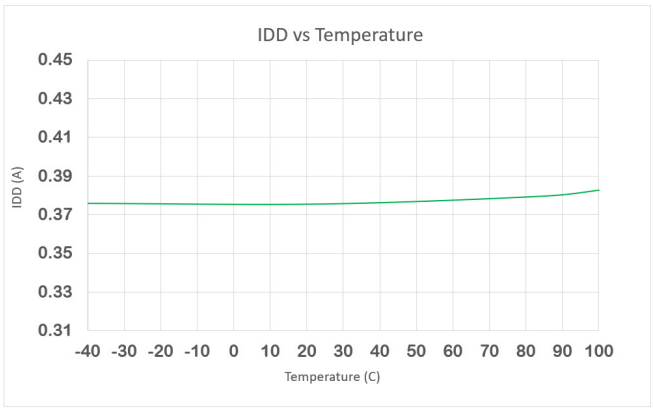
Loading for composite tests: 80 NTSC + 72 QAM (–6dB offset), 49 dBmV / ch virtual output at 1003 MHz at 3 dB tilt

Performance Data – 12 V (cont'd)

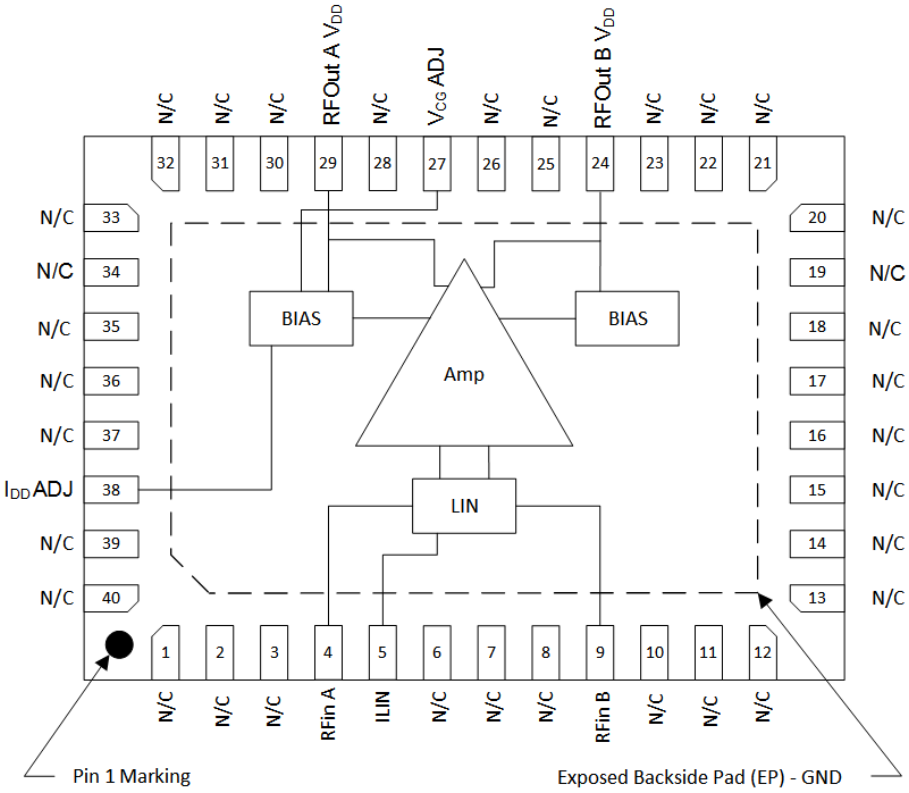








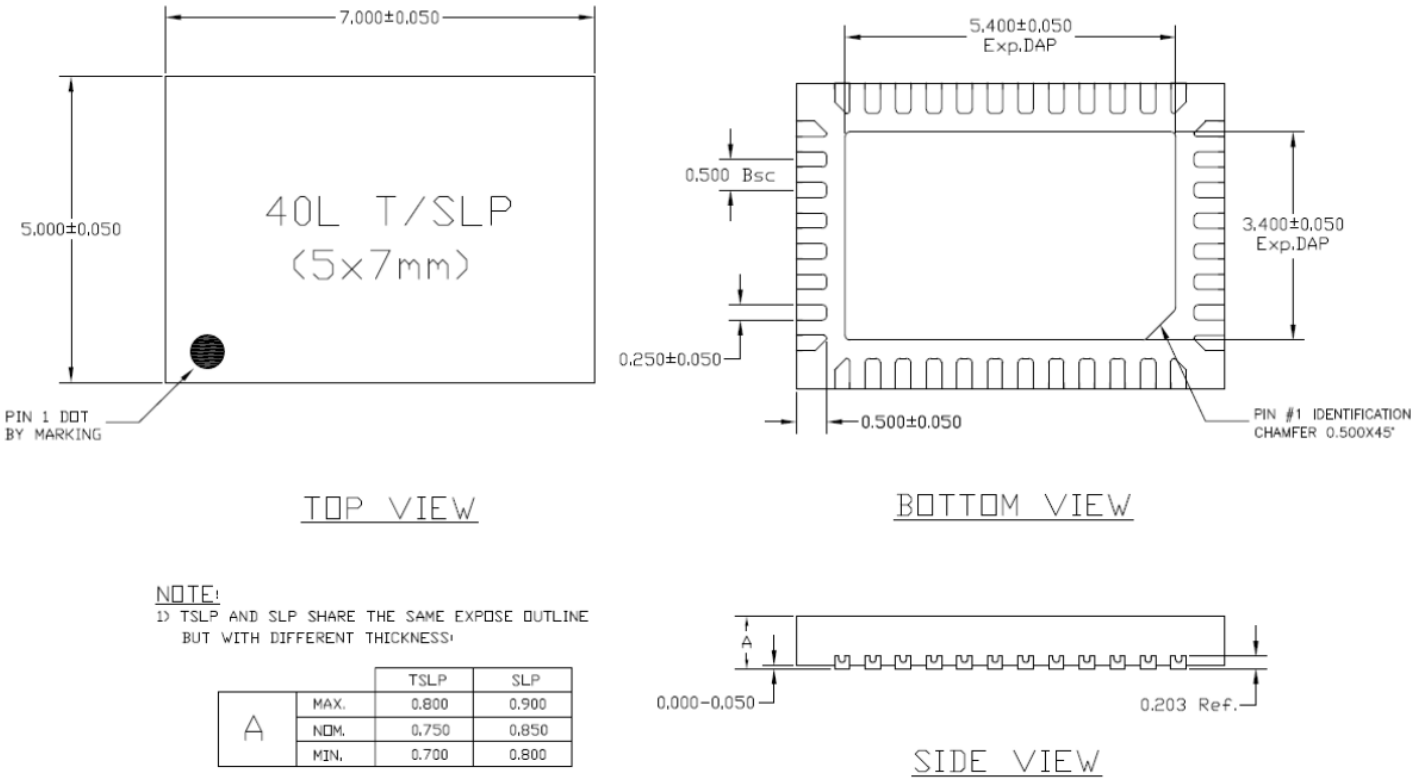
Pin Configuration and Description



Top View

Pin Number	Label	Description
4	RFin A	RF in A, requires external Balun. External DC Block required.
9	RFin B	RF in B, requires external Balun. External DC Block required.
5	ILIN	Current adjust pin to optimize Linearity
29	RFout A / V_{DD}	RF Out A and supply voltage, external DC block & Balun required.
24	RFout B / V_{DD}	RF Out B and supply voltage, external DC block & Balun required.
27	V_{CG} ADJ	Common Gate adjustment to optimize common gate amplifier bias voltage (normally open)
38	I_{DD} ADJ	I_{DD} current control (normally open), pulling to gnd lowers I_{DD} current
Backside Paddle	GND	RF / DC ground. Use recommended via pattern to minimize inductance and thermal resistance. See PCB Mounting Pattern for suggested footprint.
1,2,3,6,7,8,10 -18,19 20,21,25,26,28,32,33,34,36,37, 40,22,23,30,31,35	N / C	No connection

Package Outline



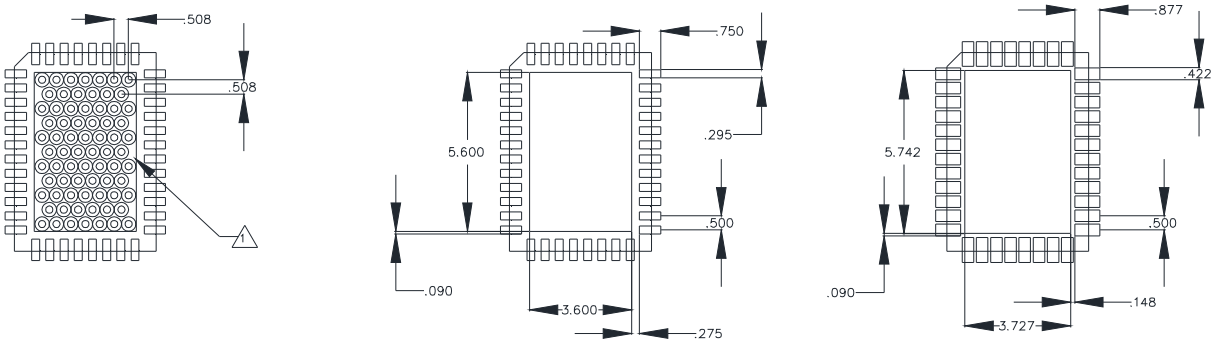
		TSLP	SLP
A	MAX.	0.800	0.900
	NOM.	0.750	0.850
	MIN.	0.700	0.800

Notes:
1. Dimensions in millimeters

Package Marking

1. Dimension and tolerance formats conform to ASME Y14.4M-1994.
2. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.
3. Co-planarity applies to the exposed ground/thermal pad as well as the contact pins.
4. Package body length/width does not include plastic flash protrusion across mold parting line.

Recommended Mounting Pattern



VIA PATTERN LAND PATTERN SOLDER MASK

NOTES:

1. GROUND/THERMAL VIAS AND MOUNTING HOLES ARE ESSENTIAL FOR THE PROPER DEVICE PERFORMANCE. DO NOT OMIT. VIAS SHOULD USE A .35mm (#80/.0135") DIAMETER DRILL AND HAVE A FINAL, PLATED THRU DIAMETER OF .25mm (.010").
2. TO ENSURE RELIABLE OPERATION, DEVICE GROUND PADDLE–TO–GROUND PAD SOLDER JOINT IS CRITICAL. NO SOLDER MASK ON BACKSIDE OF PCB IN HEAT SINK CONTACT AREA.
3. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.

- Ensure good package backside paddle solder attach for reliable operation and best electrical performance.
- Place mounting screws near the part to fasten a back-side heat sink.
- Do not apply solder mask to the back side of the PC board in the heat sink contact region.
- Ensure that the backside via region makes good physical contact with the heat sink.