QPA9120

High Gain High Linearity Driver Amplifier

Product Overview

The QPA9120 is a wideband, high gain, and high linearity driver amplifier in a low-cost, RoHS compliant 3x3 mm QFN package. With Qorvo's E-pHEMT process, this amplifier delivers exceptional performance with 36 dBm output 3rd order intercept (OIP3) power and 22 dBm output 1dB compression (OP1dB) power while consuming less than 100 mA DC current with single 5V supply.

The QPA9120 incorporates on-chip features with fast DC power shutdown, externally configurable device DC operation current, and is internally matched.

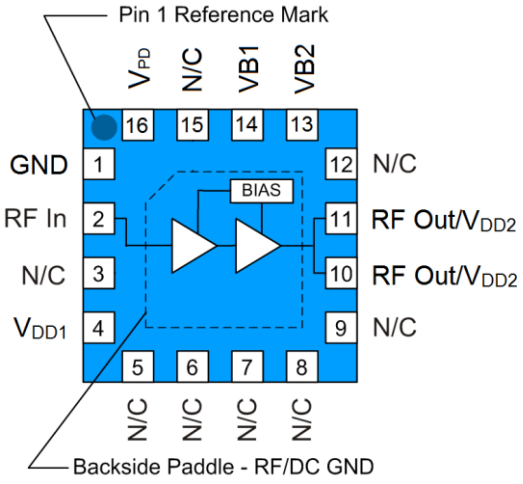
The QPA9120 is targeted for use as a pre-driver amplifier for wireless infrastructure where high linearity, medium RF power with efficient DC power operation are required. The device is an excellent choice for 5G dense-array m-MIMO radio applications.

16 Pad 3 x 3 mm QFN Package

Key Features

- 1.8 – 5.0 GHz Operational
- 50Ω Matched RF Input and Output
- 1 dB Gain Flatness over 1 GHz Bandwidth
- +22 dBm P1dB
- +35 dBm Output IP3
- 29 dB Gain
- +5 V Single Supply, I_{DD} 96 mA
- DC Power Shutdown Feature
- Small 3 x 3 mm QFN Package

Functional Block Diagram



Top View

Applications

- 5G m-MIMO
- Mobile Infrastructure
- Repeater / DAS
- General Purpose Wireless
- TDD / FDD System

Ordering Information

Part No.	Description
QPA9120TR7	2,500 pieces on a 7" reel (standard)
QPA9120EVB-01	Evaluation Board

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−65 to +150 °C
RF Input Power, CW, 50 Ω, T=25 °C	22 dBm
Device Voltage (V_{DD1}, V_{DD2})	+6 V

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Device Voltage (V_{DD1}, V_{DD2})	+3.3	+5.0	+5.25	V
T_{CASE}	−40		+105	°C
Tj for >10^6 hours MTTF			+190	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

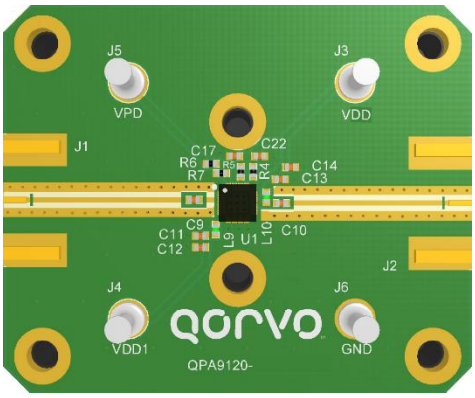
Parameter	Conditions (1)	Min	Typ	Max	Units
Operational Frequency Range		1800		5000	MHz
Gain	At 3.5 GHz	27	29	33	dB
	At 4.8 GHz	26	28	32.5	dB
Input Return Loss			10		dB
Output Return Loss			12		dB
Output P1dB	At 3.5 GHz	20	22		dBm
	At 4.8 GHz	19	21		dBm
Output IP3	Pout = +2 dBm/tone, Δf = 1 MHz, 3.5 GHz	32	35		dBm
	Pout = +2 dBm/tone, Δf = 1 MHz, 4.8 GHz	30	34		dBm
Noise Figure	At 3.5 GHz or 4.8 GHz		1.5		dB
Device Current, ON	V_{DD1} and V_{DD2}	70	96	130	mA
Device Current, OFF	V_{PD} = 0 V		2		mA
V_{PD}, Logic Low		0		0.63	V
V_{PD}, Logic High		1.17		V_{DD}	V
Device ON or OFF Timing	10%-90% Rising or 90%-10% Falling		0.2		µS
Thermal Resistance, θ_{jc}	Junction to case			50.1	°C/W

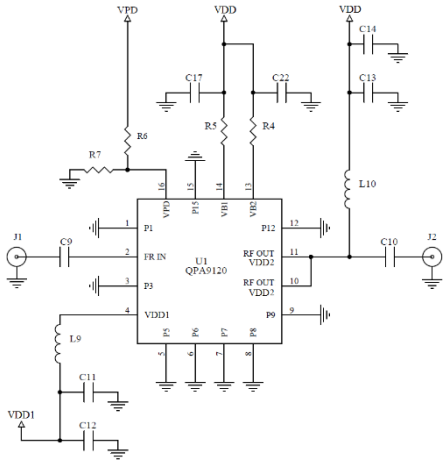
Notes:
1. Test conditions unless otherwise noted: V_{DD1} and V_{DD} on EVB = +5.0 V, V_{PD} = +1.8 V, Temp = +25 °C, 50 Ω system.

Logic Table

Parameter, V_{PD}	High	Low
Device State	ON	OFF

3300 to 5000MHz Evaluation Board - QPA9120EVB01





Notes:
1. See Evaluation Board PCB Information for material and stack up
2. Total operation current can be adjusted by changing the values of R4 and/or R5

Bill of Material

Ref. Des.	Value	Description	Manuf.	Part Number
n/a	-	Printed Circuit Board	Qorvo	
U1	-	High Gain High Linearity Amplifier	Qorvo	QPA9120
R4	1.6 KΩ	Res, 1.6 KΩ, 0402, 1%, 1/16W	various	
R5	5.62 KΩ	Res, 5.62 KΩ, 0603, 1%, 1/16W	various	
R6	0 Ω	Res, 0 Ω, 0402, 1/10W	various	
R7	100 KΩ	Res, 100 KΩ, 0402, 5%, 1/16W	various	
C9, C10	18 pF	Cap, 18 pF, 0402, 5%, 50V NPO/C0G	various	
C11, C13, C17, C22	100 pF	Cap, 100 pF, 0402, 5%, 50V NPO/C0G	various	
C12, C14	1.0 µF	Cap, 1.0 µF, 0402, 10%, 10V, X5R	various	
L9, L10 (1)	2.2 nH	Inductor, 2.2 nH, 0402, ±0.1nH	muRata	LQP15MN2N2B02D
J1, J2	-	Conn, SMA F STRT .062”	Cinch Connectivity	142-0701-851

Notes:
1. L10 value needs to be 18 nH for operation frequency < 3 GHz

Typical Performance on EVB

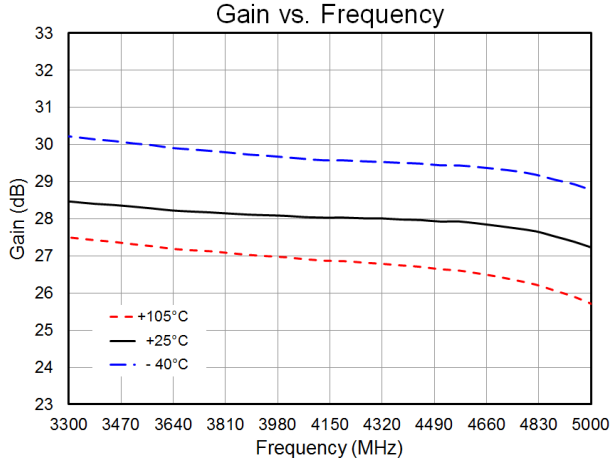
Parameter	Conditions	Typical Value				Units
Frequency		1800	2600	3500	4800	MHz
Gain		32.2	30.5	28.3	27.6	dB
Input Return Loss		6	10	13	11	dB
Output Return Loss		24	14	15	12	dB
Output P1dB		21.5	22.0	21.9	21.3	dBm
Output IP3	Pout = +2 dBm/tone, Δf = 1 MHz	31.9	33.1	35.4	34.4	dBm
Device Current	V_{DD} and V_{DD1}	96				mA

Notes:
1. Test Conditions unless otherwise noted: V_{DD1} and V_{DD} on EVB = +5.0 V, V_{PD} = +1.8 V, Temp.=+25 °C, L10 = 18 nH on EVB for Freq. < 3 GHz

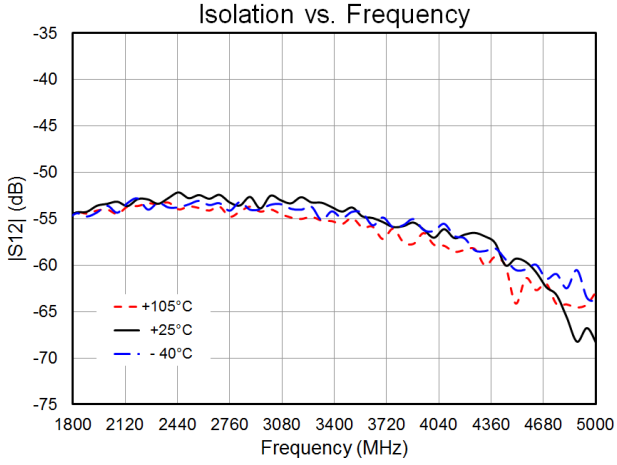
Performance Plots – QPA9120EVB01

Test conditions unless otherwise noted: V_{DD1} and V_{DD} on EVB = +5.0 V, I_{DD} = 96 mA, V_{PD} = +1.8 V, Temp.=+25 °C

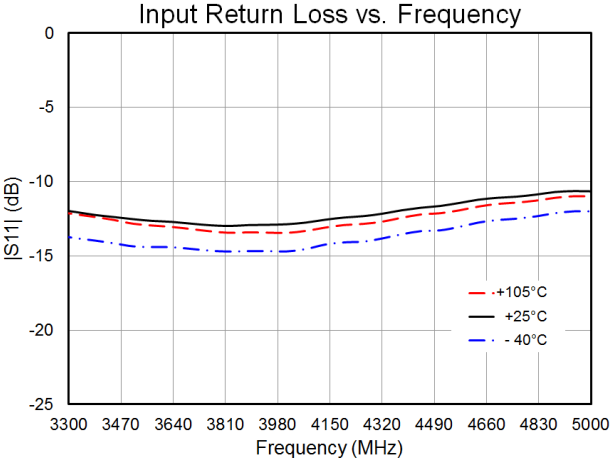
Gain vs. Frequency



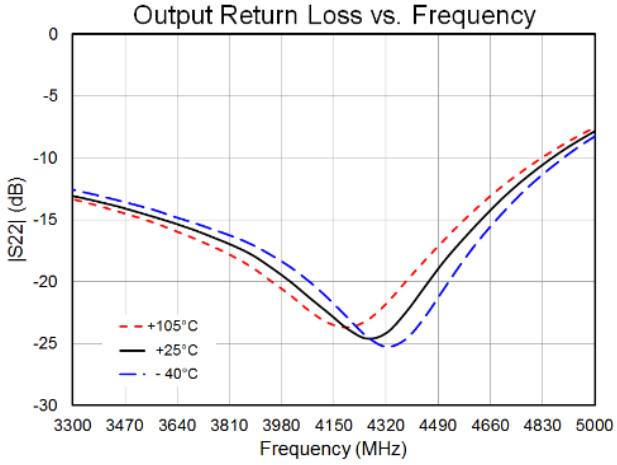
Isolation vs. Frequency



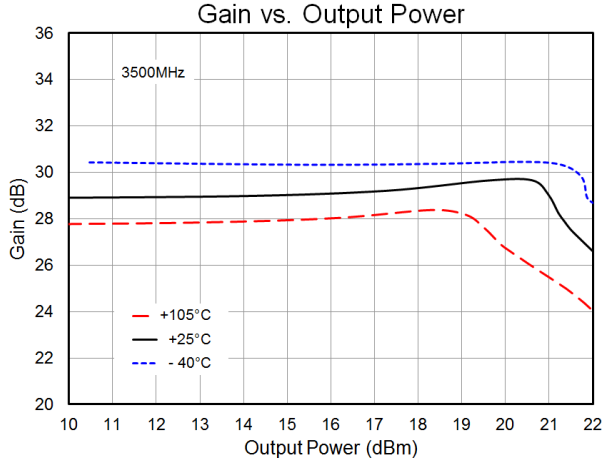
Input Return Loss vs. Frequency



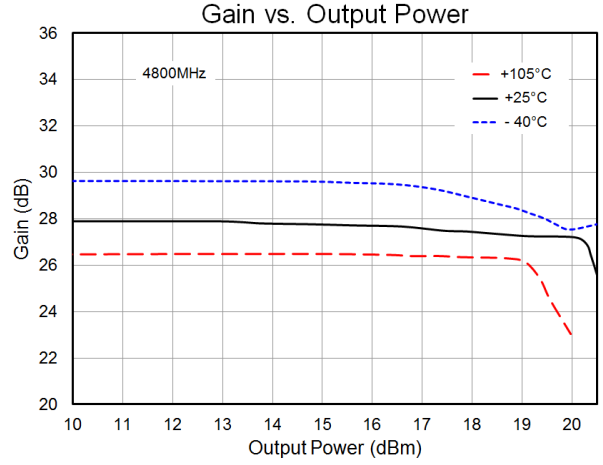
Output Return Loss vs. Frequency



Gain vs. Output Power

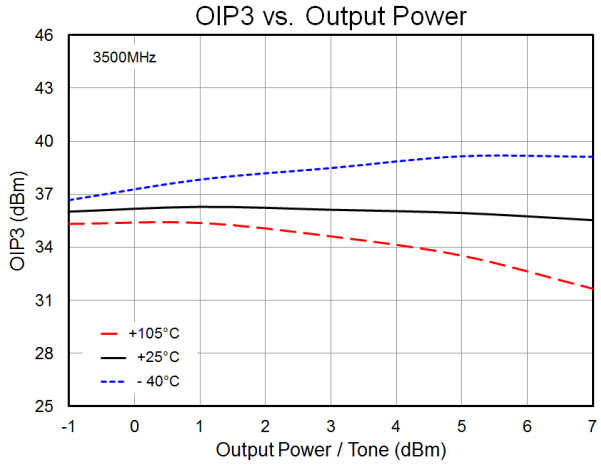


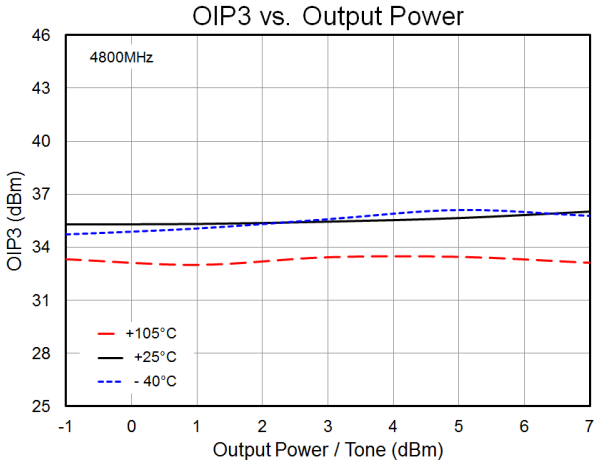
Gain vs. Output Power

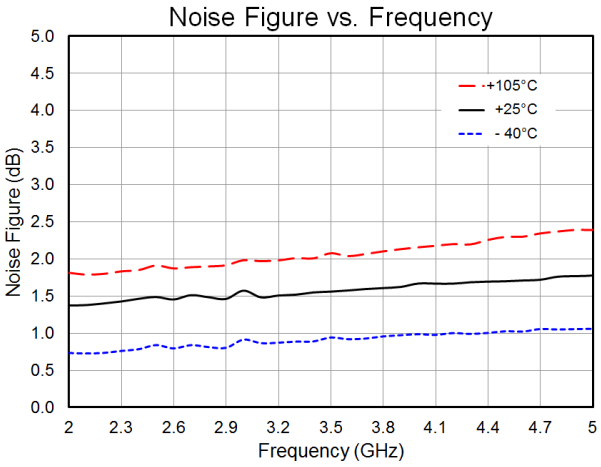


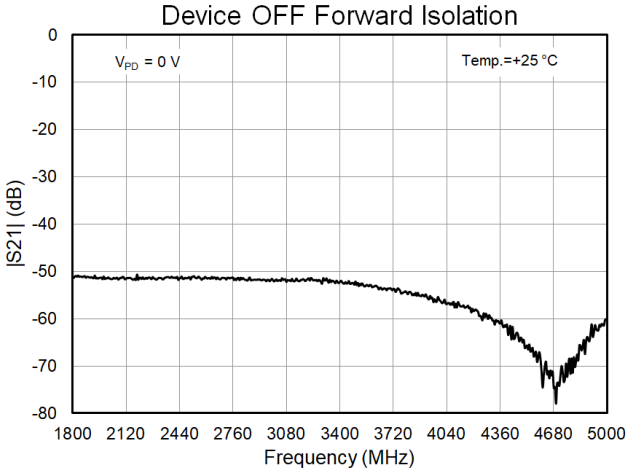
Performance Plots – QPA9120EVB01 (Continue)

Test conditions unless otherwise noted: V_{DD1} and V_{DD} = +5.0 V, I_{DD} = 96 mA, V_{PD} = +1.8 V, Temp.=+25 °C



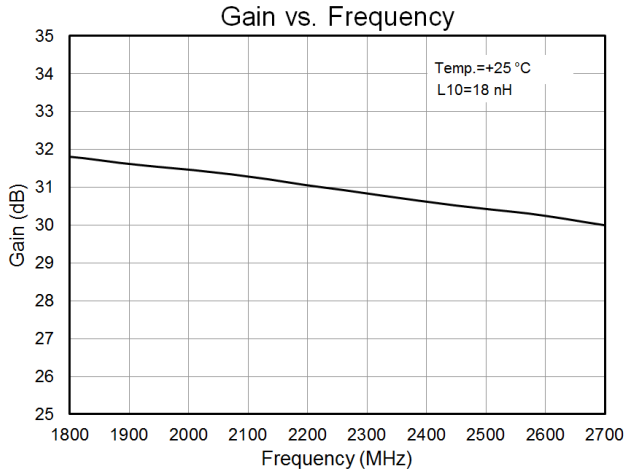


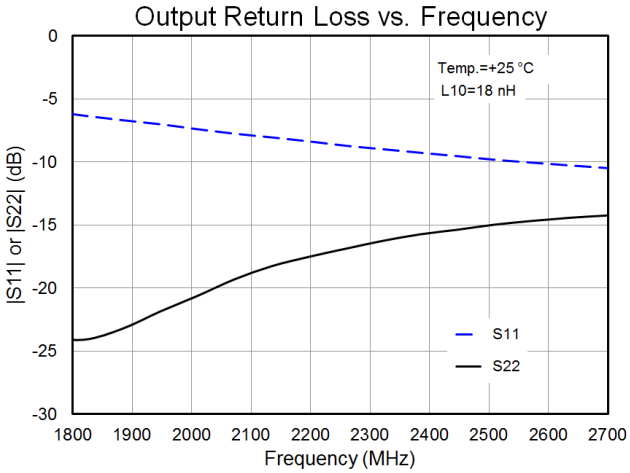


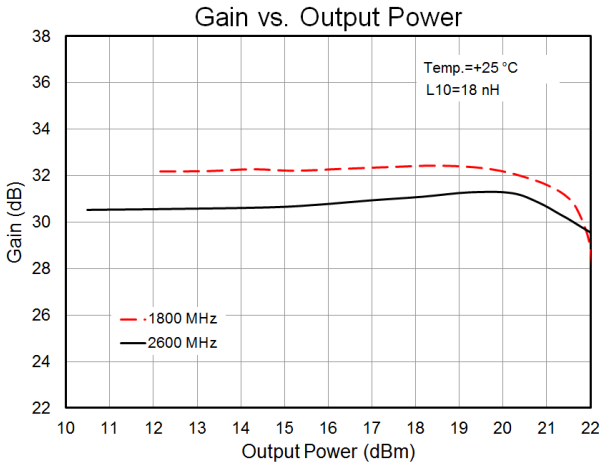


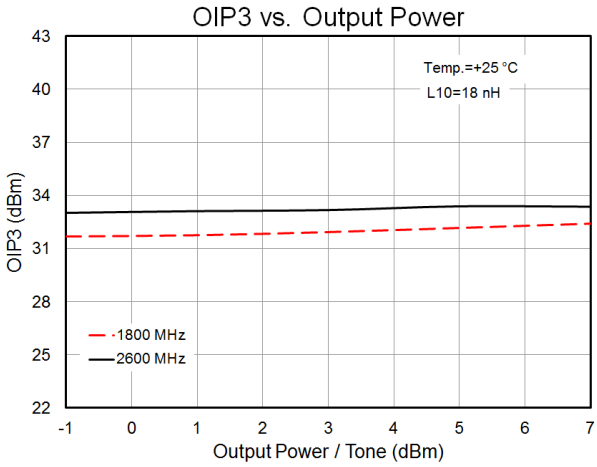
Performance Plots – 1800 MHz to 2700MHz

Test conditions unless otherwise noted: V_{DD1} and V_{DD} on EVB = +5 V, I_{DD} = 96 mA, V_{PD} = +1.8 V, Temp.=+25 °C, L10 = 18 nH on QPA9120EVB01





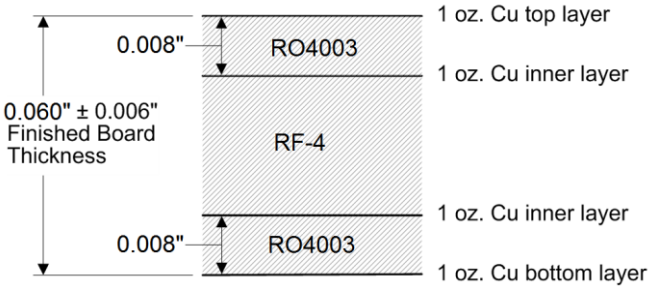




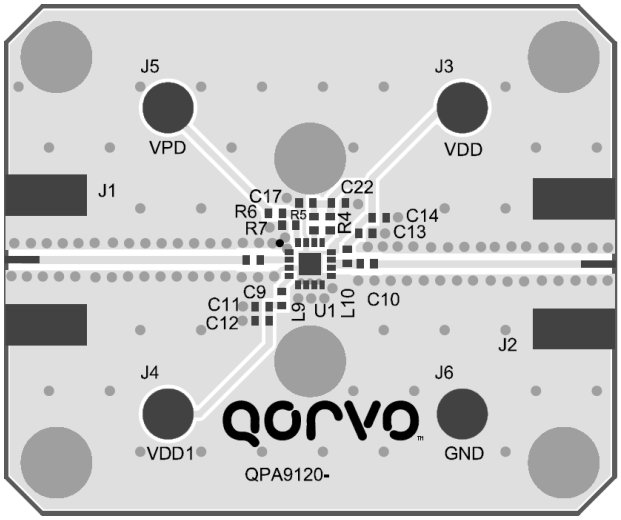
Evaluation Board PCB Information

PC Board Layout

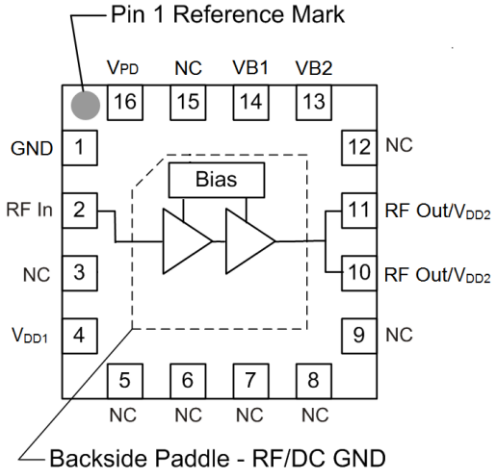
PCB Material Stackup



50 ohm line dimensions: width = 0.017”, spacing = 0.017”



Pad Configuration and Description

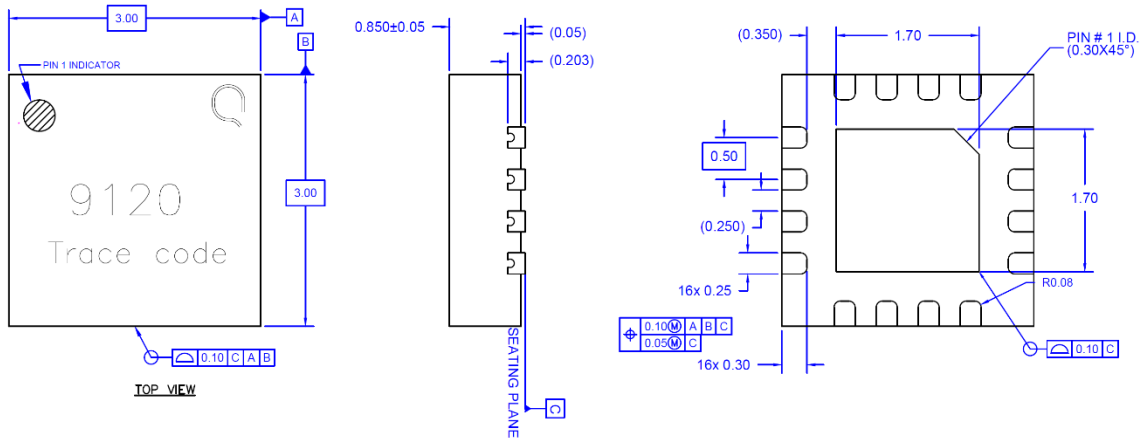


Top View

Pad No.	Label	Description
1	GND	Ground connection
2	RF IN	RF input. External DC Block required
3, 5, 6, 7, 8, 9, 12, 15	NC	No electrical connection internally. It may be left floating or connected to ground. Land pads should be provided for PCB mounting integrity.
4	V_{DD1}	The first stage DC supply. External choke required
10, 11	RF OUT / V_{DD2}	RF output and the second stage DC supply. External chock and DC Block capacitor required.
13	VB2	Sets the bias current for the second stage of the amplifier
14	VB1	Sets the bias current for the first stage of the amplifier
16	V_{PD}	Amplifier ON/OFF logic control
Backside Paddle	GND	RF/DC ground. Use recommended via pattern to minimize inductance and thermal resistance. See PCB Mounting Pattern for suggested footprint.

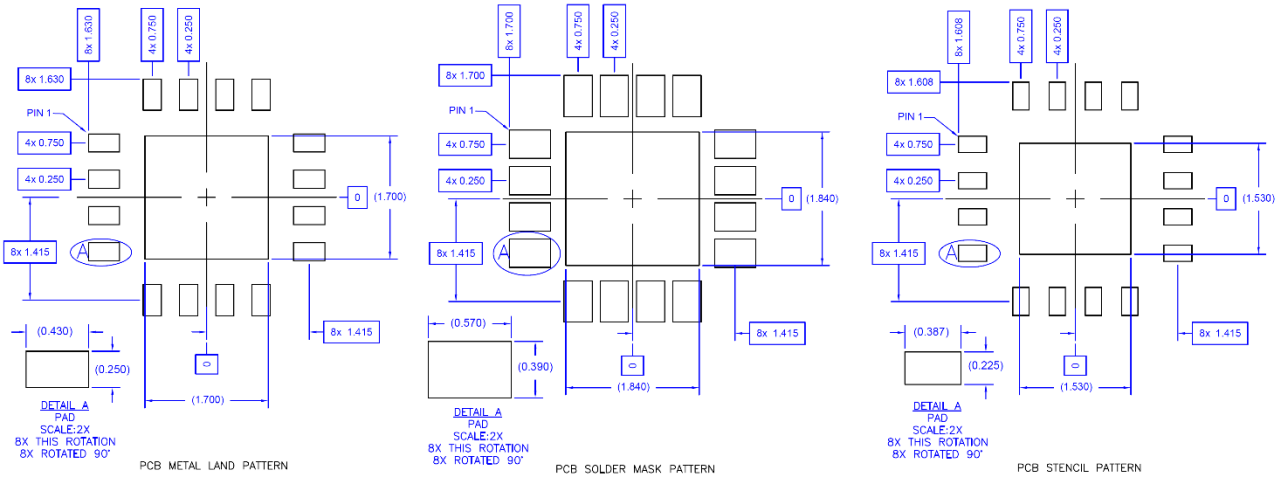
Package Marking and Dimensions

Marking: Pin 1 marker – Dot and Logo – Q
Part Number – 9120
Trace Code – XXXX up to 4 Characters assigned by sub-contractor



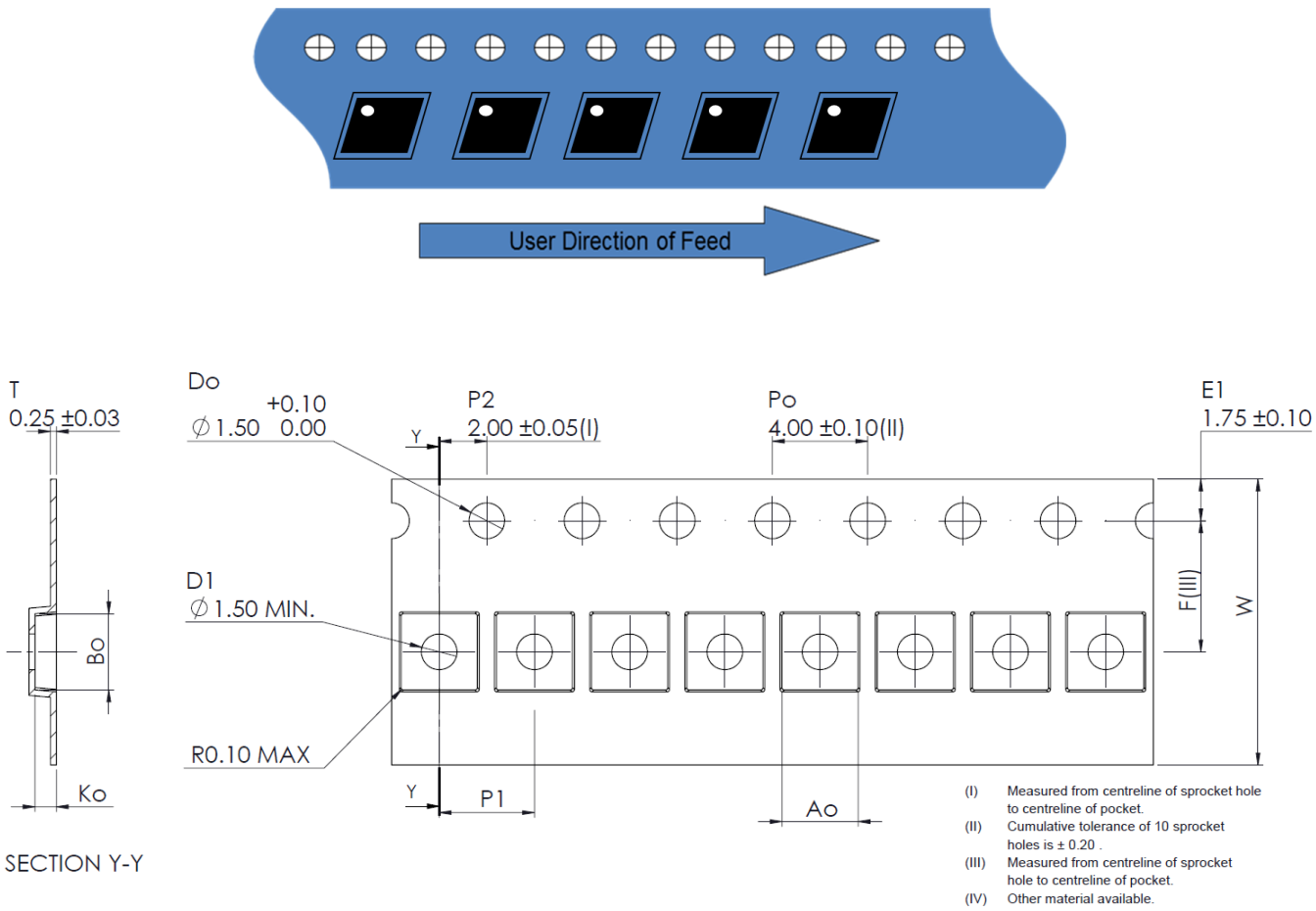
Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.
3. Contact plating: NiPdAu

Recommended PCB Layout Pattern



Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Via holes are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.01").
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

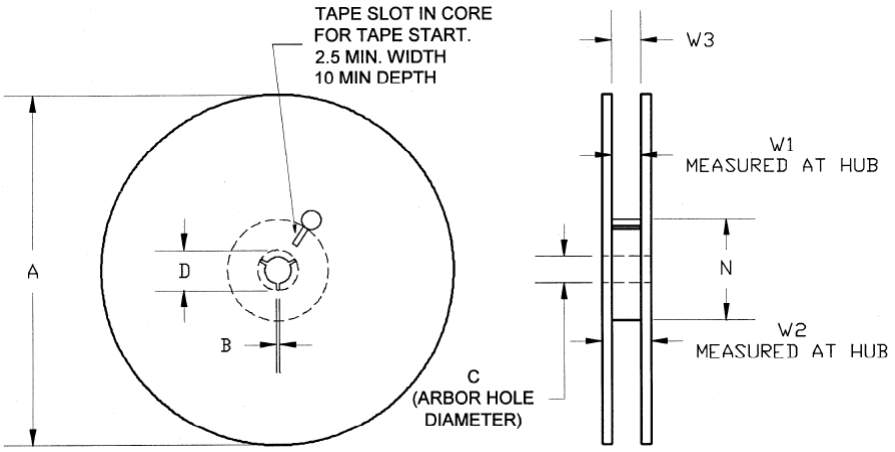
Tape and Reel Information – Carrier and Cover Tape Dimensions



Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.126	3.20
	Width	B0	0.126	3.20
	Depth	K0	0.039	1.00
	Pitch	P1	0.157	4.00
Centerline Distance	Cavity to Perforation - Length Direction	P2	0.079	2.00
	Cavity to Perforation - Width Direction	F	0.217	5.50
Cover Tape	Width	C	0.362	9.20
Carrier Tape	Width	W	0.472	12.00

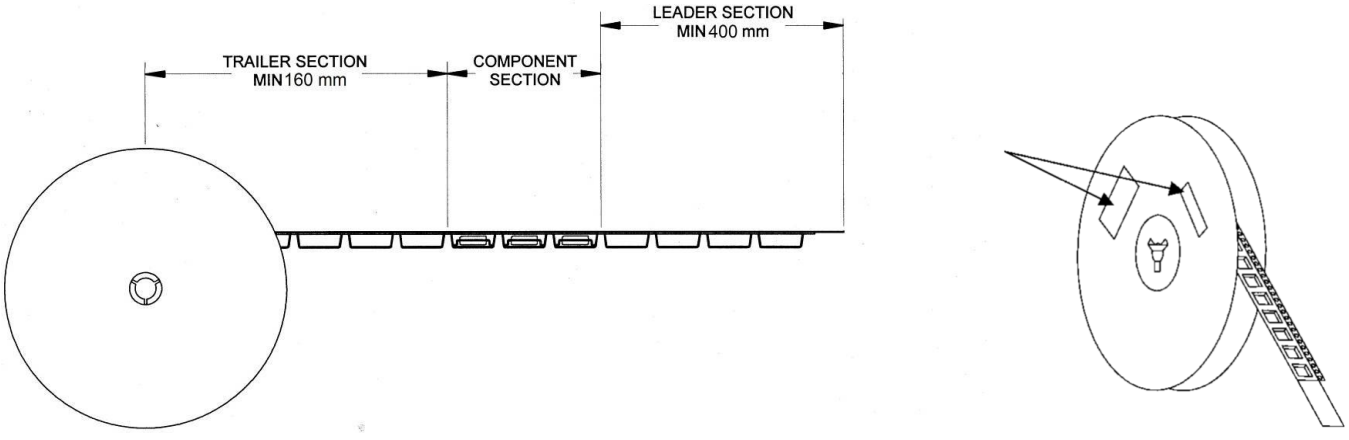
Tape and Reel Information – Reel Dimensions

Standard T/R size = 2,500 pieces on a 7” reel.



Feature	Measure	Symbol	Size (in)	Size (mm)
Flange	Diameter	A	6.969	177.0
	Thickness	W2	0.717	18.2
	Space Between Flange	W1	0.504	12.8
Hub	Outer Diameter	N	2.283	58.0
	Arbor Hole Diameter	C	0.512	13.0
	Key Slit Width	B	0.079	2.0
	Key Slit Diameter	D	0.787	20.0

Tape and Reel Information – Tape Length and Label Placement



Notes:
1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481-1-A.
2. Labels are placed on the flange opposite the sprockets in the carrier tape.