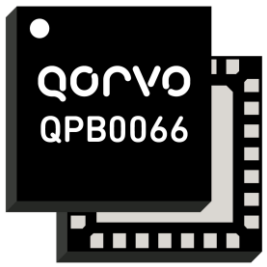
QPB0066

Digital Controlled Variable Gain Amplifier (5 – 500 MHz)

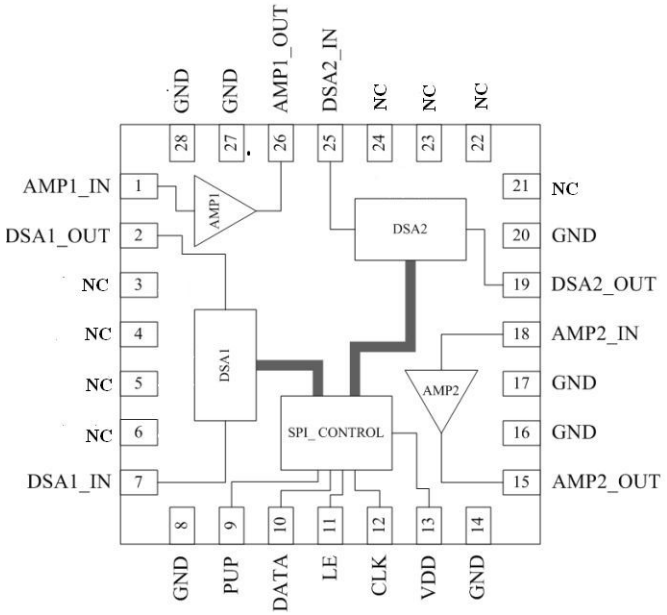
Product Overview

The QPB0066 is a digital controlled variable gain amplifier featuring high linearity over the entire gain control range with noise figure less of 4.3 dB in its maximum gain state. The gain of the dual 6-bit digital step attenuators programmed with a 12-bit Serial Peripheral Interface (SPI). The QPB0066 is packaged in a small 6.0 mm x 6.0 mm leadless laminate MCM, which contains plated through thermal vias for ultra-low thermal resistance. The module is easy to use with a few external DC blocks and RF chokes.



28-Pin, 6.0 mm x 6.0 mm MCM

Functional Block Diagram



Top View

Key Features

- 5 MHz to 500 MHz Operation
- Dual 6-Bit Digital Step Attenuator
- SPI Serial Control Programming
- Max Gain = 44 dB at 100 MHz
- Gain Control Range = 63 dB (0.5 dB Steps)
- High OIP3 / P1dB = +38 dBm / 22.6 dBm
- +5 V Supply for DSA and +8 V Supply for Amplifier with a Drop Resistor
- Small 28-Pin, 6.0 mm x 6.0 mm MCM
- Power-up Programming

Applications

- High Linearity Power Control
- CATV Drivers
- Transceiver IF DVA
- Cellular, PCS, GSM, UMTS
- Wireless Data, Satellite Terminals

Ordering Information

Part Number	Description
QPB0066SQ	Sample bag with 25 pieces
QPB0066SR	7" Reel with 100 pieces
QPB0066TR13	13" Reel with 2500 pieces
QPB0066PCK	5 – 500 MHz PCBA with 5 pc sample bag

Absolute Maximum Ratings

Parameter	Rating
Supply Voltage (V_{DD}) for DSA	-0.5 to +5.75 V
VD_{MAX} (device voltage at RFOUT pins)	+7 V
Supply Current (I_{CC}) for amplifiers	340 mA
Power Dissipation for each amplifier	1980 mW
Maximum RF Input Power	+16 dBm
Operating Temperature Range	−40 to +85 °C
Storage Temperature Range	−65 to +150 °C
Maximum Junction Temperature	+125 °C

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

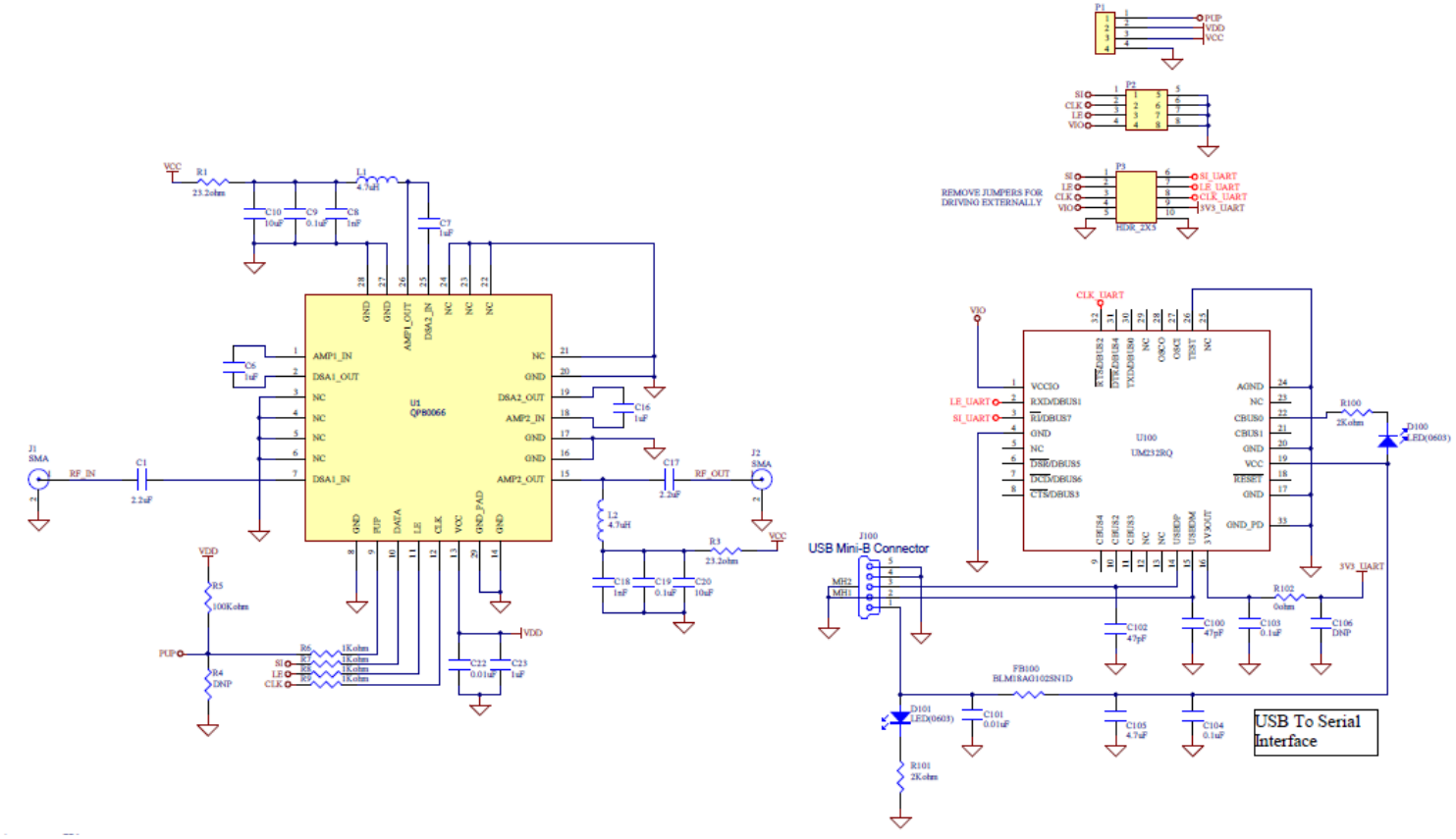
Electrical Specifications

Parameter	Condition (1)	Min	Typ	Max	Unit
Attenuator Supply Voltage		3.0	5.0	5.5	V
Attenuator Supply Current			500		µA
Amplifier Supply Voltage (2)			5.0		V
Amplifier Supply Current			250		mA
Frequency Range		5		500	MHz
Max Gain	Attenuation = 0 dB		42		dB
Gain Control Range			63.0		dB
Step Accuracy	Major state error up to 250 MHz	+/- 0.2 +4% attenuation setting			dB
P1dB	Attenuation = 0 dB		22.5		dBm
Output IP3	P_{OUT} = 0 dBm / tone, 1 MHz spacing		36		dBm
Control Interface	SPI Interface		12		bit
Switching Speed	50% Control to 10%/90% RF		120		ns
Noise Figure	Attenuation = 0 dB		4.3		dB
Impedance			50		Ω
Input Return Loss	At Maximum Gain		24		dB
Output Return Loss	At Maximum Gain		12		dB
Thermal Resistance	Θ_{JC}		70		˚C / W

Notes:

1. Typical performance at these conditions: Temp = +25 °C, V_{DD} = +5 V, 50 Ω system, Full band unless otherwise noted
2. V_D at the RF output pins

Evaluation Board Schematic (5 – 500 MHz)



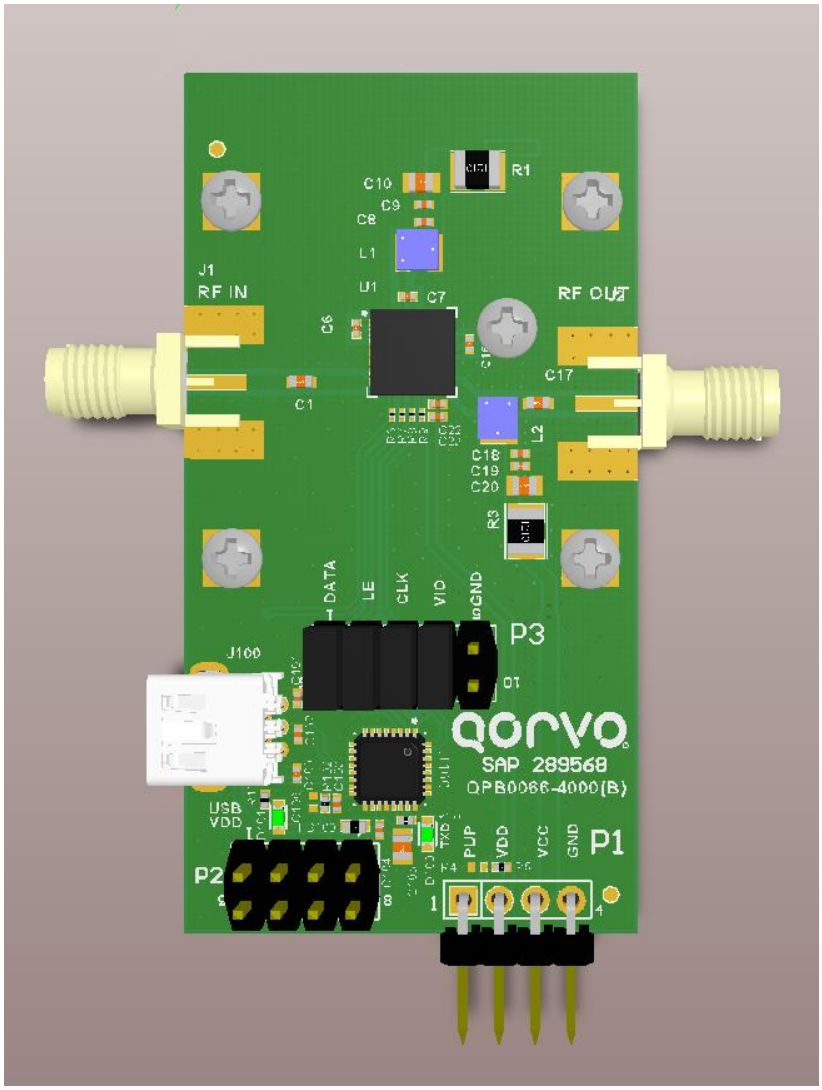
Notes:

1. QPB0066-4000(B) removes unused capacitor pads and test path from QPB0066-4000(A). All other connections and programming remain the same.

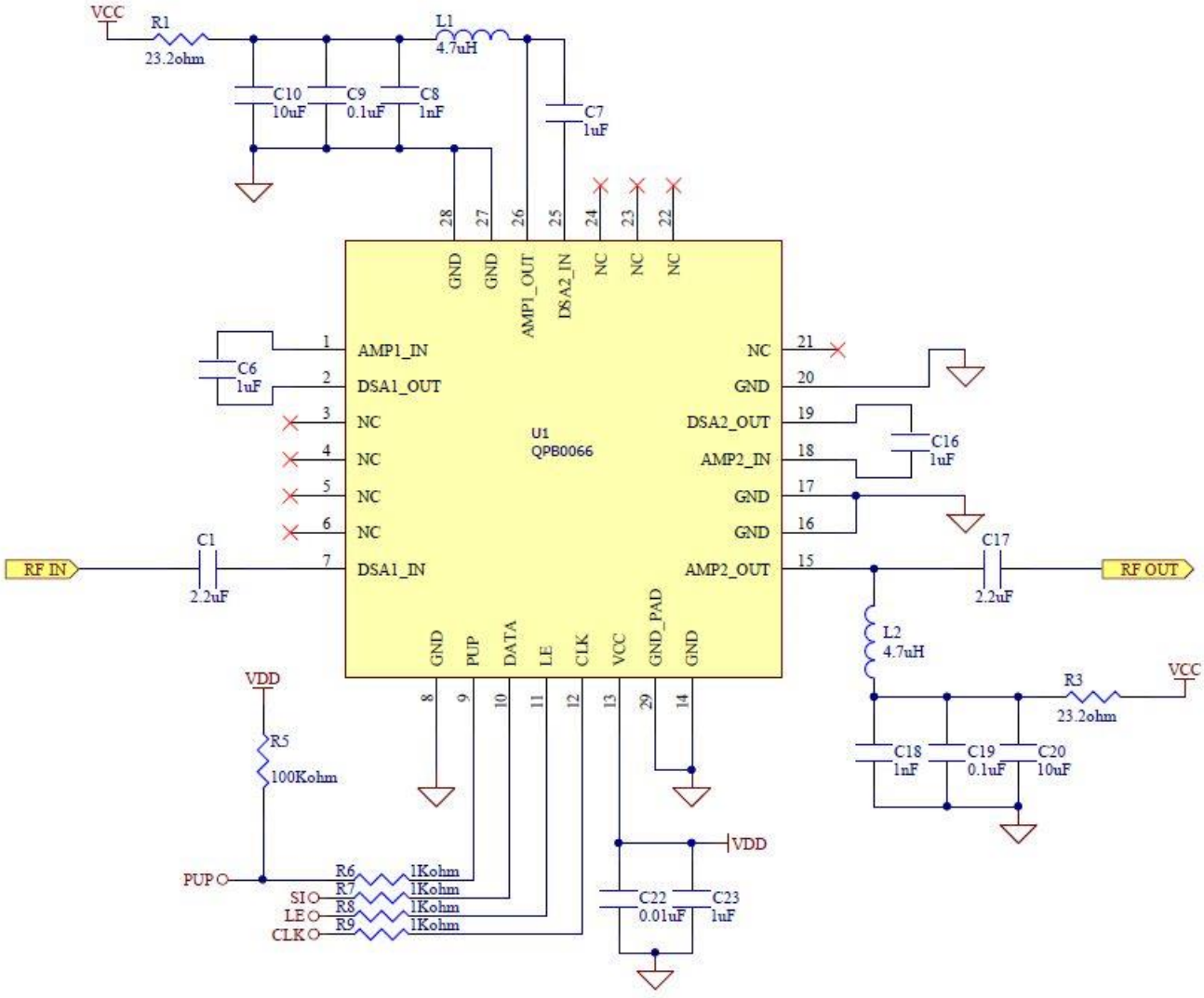
Evaluation Board Bill of Materials

Designator	Description	Manufacturer	Part Number
PCB	QPB0066 PCB Board	Qorvo	QPB0066-4000(B)
U1	Digital Controlled Variable Gain Amplifier	Qorvo	QPB0066SB
C1, C17	CAP, 2.2uF, 10%, 10V, X5R, 0603	Murata Electronics	GRM188R61A225KE34D
C22, C101	CAP, 0.01uF, ±10%, 50V, X7R, 0402	Murata Electronics	GRM155R71H103KA88D
C100, C102	CAP, 47pF, 5%, 50V, C0G, 0402	Murata Electronics	GRM1555C1H470JA01D
C8, C18	CAP, 1000pF, 10%, 50V, X7R, 0402	Taiyo Yuden (USA), Inc.	RM UMK105BJ102KV-F
C10, C20	CAP, 10uF, 10%, 16V, TANT-B	AVX Corporation	TAJB106K016R
C9, C19, C103, C104	CAP, 0.1uF, 10%, 16V, X7R, 0402	Murata Electronics	GRM155R71C104KA88D
C105	CAP, 4.7uF, 10%, 16V, X7R, 0805	AVX Asia Limited	0805YC475KAT2A
C6, C7, C16, C23	CAP, 1uF, 10%, 10V, X7S, 0402	Murata Electronics	GRM155C71A105KE11D
R6, R7, R8, R9	RES, 1K, 5%, 1/20W, 0201	Kamaya, Inc	RMC1/20-102JPA15
R102	RES, 0 OHM, 5%, 1/10W, 0402	Kamaya, Inc	RMC1/16SJPTH
R5	RES, 100K, 5%, 1/16W, 0402	Kamaya, Inc	RMC1/16S-104JTH
R100, R101	RES, 2K, 5%, 1/16W, 0402	Kamaya, Inc	RMC1/16S-202JTH
R1, R3	RES, 23.2 OHM, 1%, 1/2 W, 1210	Panasonic Industrial Devices	ERJ-14NF23R2U
D100, D101	LED, GRN, CLR, 3.2V, 30mA, 0603	Wurth Elektronik	150060GS75000
L1, L2	IND, 4.7uH, 5%, 260mA, W/W, 1008	Coilcraft, Inc.	1008CS-472XJRC
FB100	FER, BEAD, 1K, 100mA, 0603	Murata Electronics	BLM18AG102SN1D
U100	IC, USB-UART, 3.3-5.25V,QFN-32	Future Technology Devices Int'l	FT232RQ
P2	CONN, HDR, ST, 2x4, 0.100"	Samtec, Inc.	TSW-104-14-G-D
J1, J2	CONN, SMA, EL, FLT, 0.068" SPE-000318	Amphenol RF Asia Corp	901-10426
P1	CONN, HDR, RT-ANG, 4 POS, 0.100", T/H	3M Interconnect Solutions	961104-5604-AR
J100	CONN, USB, MINI-B, RT ANG, 5-PIN, T/H	Molex	054819-0519
P3	CONN, HDR, ST, 2x5, 0.100"	Samtec, Inc.	TSW-105-08-L-D
R4, C106	Not Populated	N/A	N/A

Evaluation Board Assembly Drawing



Typical Application Schematic (5-500MHz)

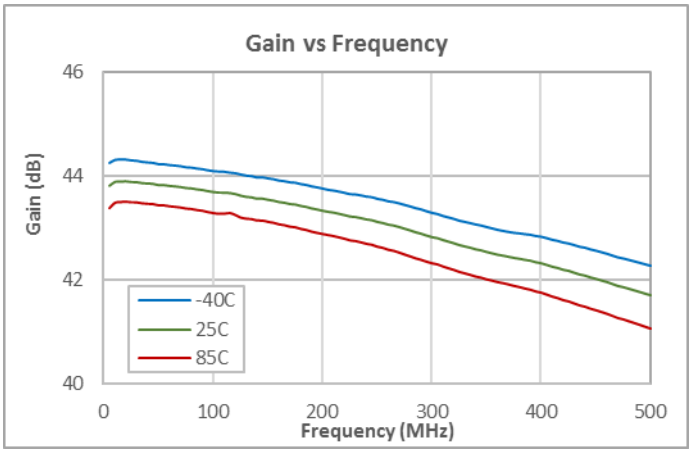


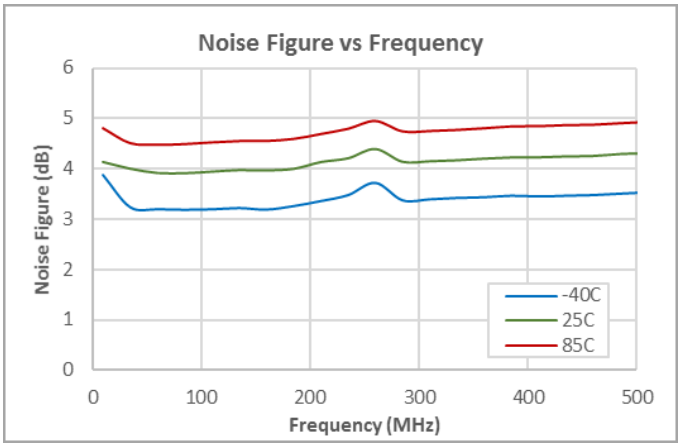
Required Bias Resistance for I_{CC} = 125 mA (one amplifier):
Bias Resistance = R_{BIAS}+ R_{CHOKE} = (V_{CC} – V_{DD}) / I_{CC}
(V_{CC}: Amplifier supply voltage; V_D: Amplifier device voltage at the RF output ~4.75 to 5.0 V; R_{BIAS}: Bias Resistor; R_{CHOKE}: DCR of Bias Choke

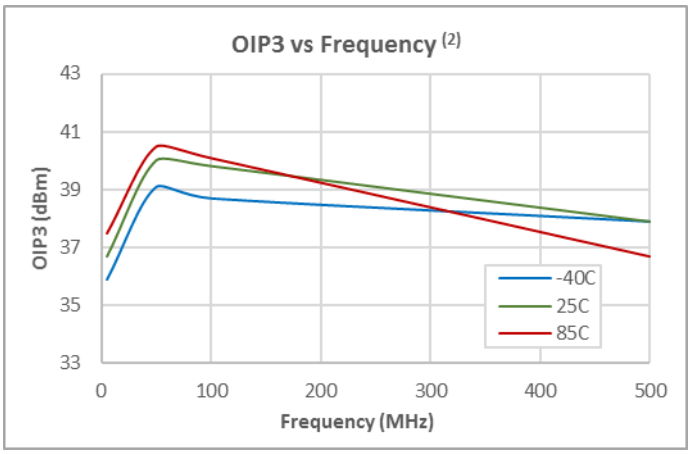
Total Bias Resistance (R_{BIAS} + R_{CHOKE})

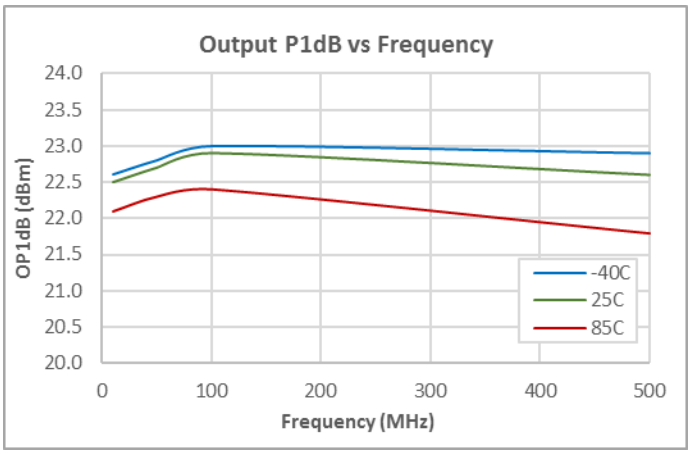
Supply Voltage	7V	8V	9V	10V
Bias Resistance	18.0	26.0	34.0	58.0

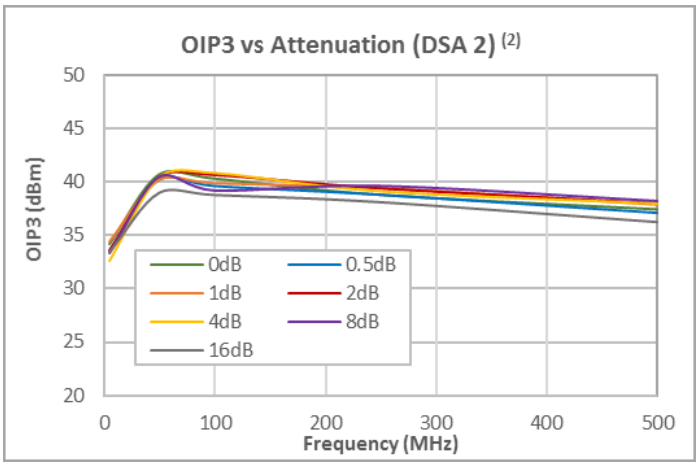
Performance Data: 5 – 500 MHz Broadband Application Circuit (1)

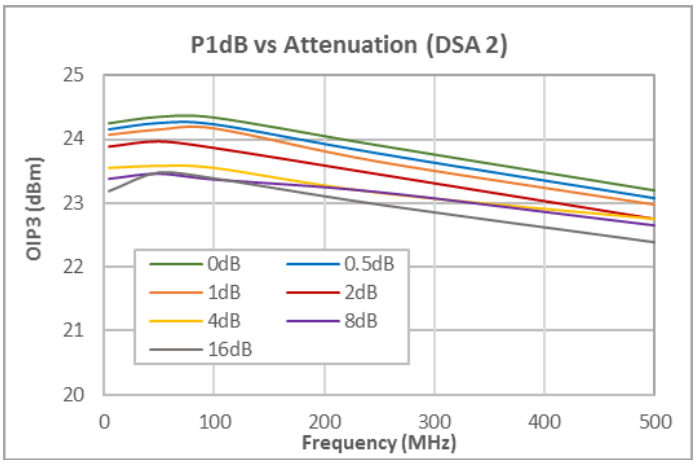








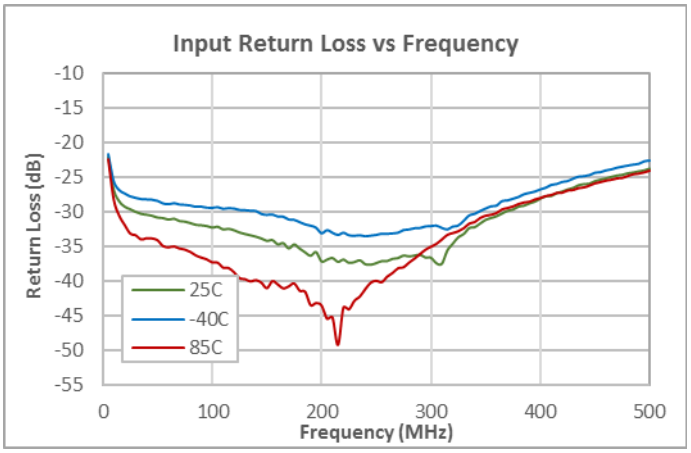


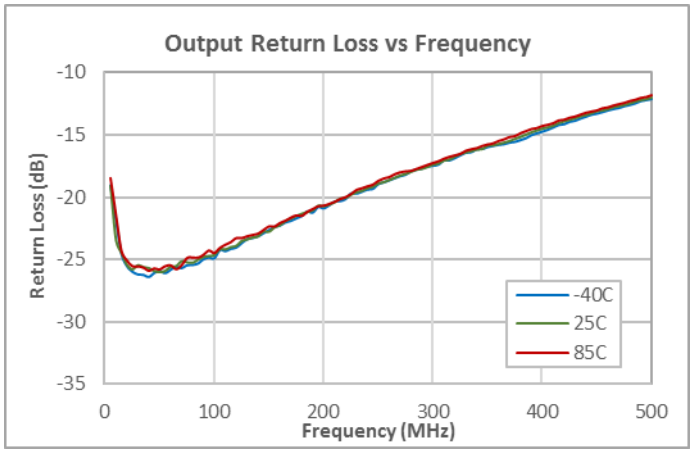


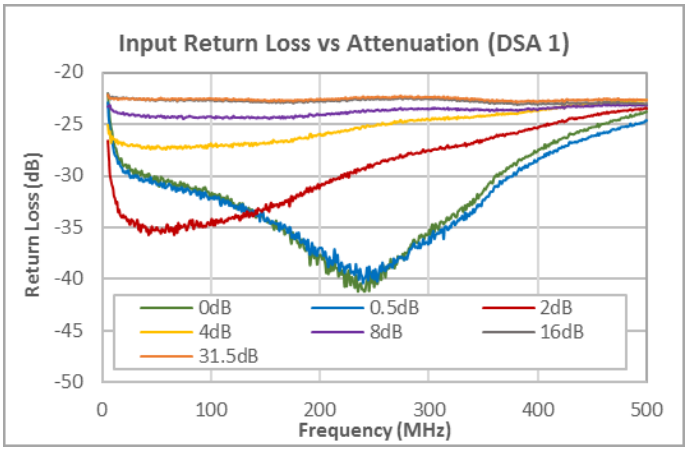
Notes:

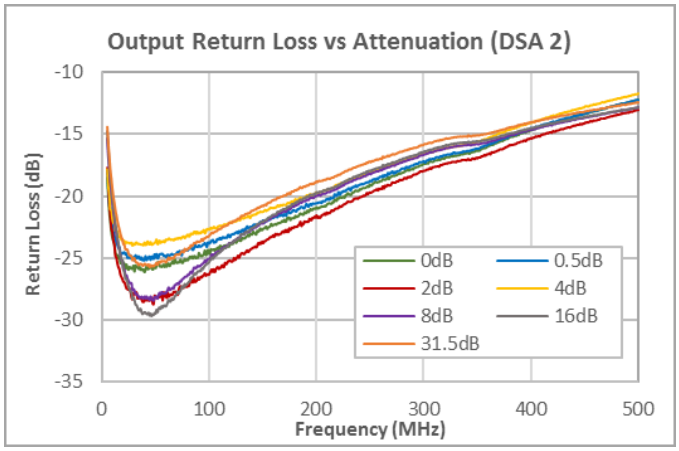
1. Typical performance at these conditions: Temp = +25 °C, V_{DD} = +5 V, V_{CC} = +8 V, Maximum Gain, 50 Ω system, Full band unless otherwise noted.
2. 0 dBm / tone.

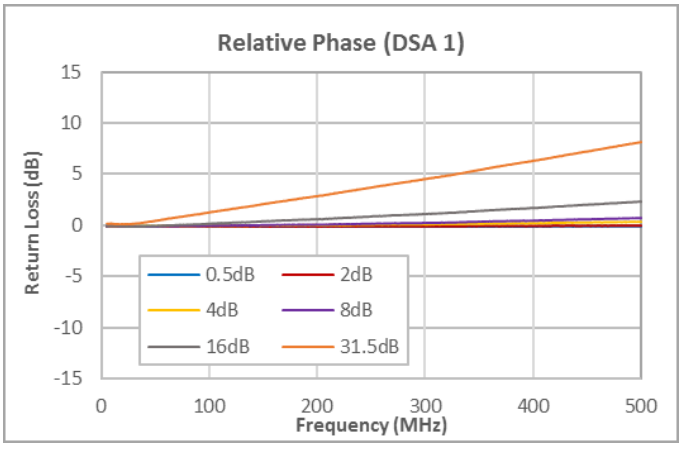
Performance Data: 5 – 500 MHz Broadband Application Circuit (1)

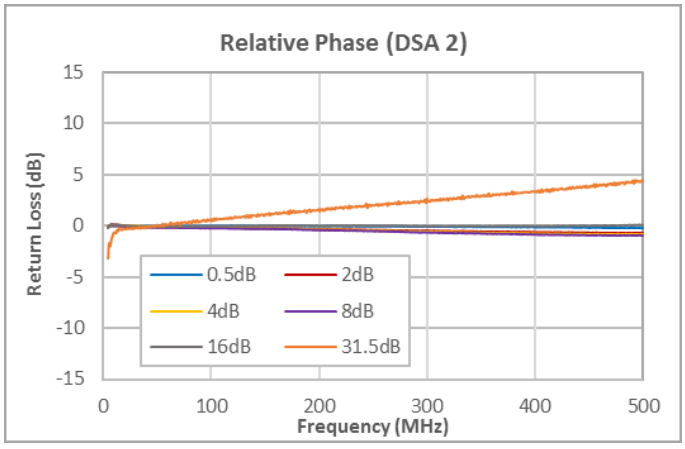








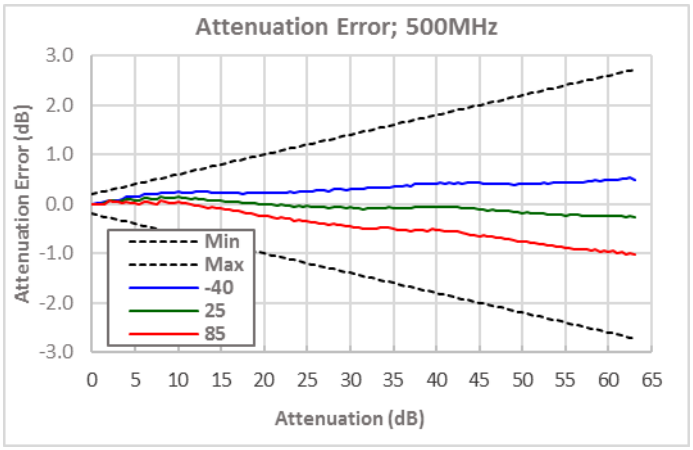


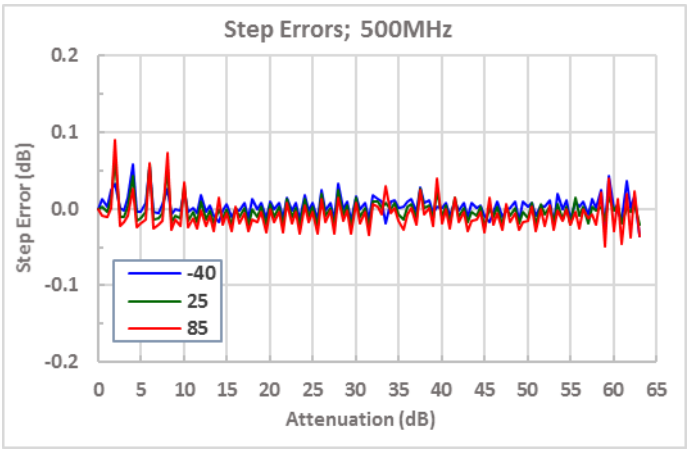


Notes:

(1) Typical performance at these conditions: Temp = +25 °C, V_{DD} = +5 V, V_{CC} = +8 V, Maximum Gain, 50 Ω system, Full band unless otherwise noted.

Performance Data: 5 – 500 MHz Broadband Application Circuit (1)





Notes:

(1) Typical performance at these conditions: Temp = +25 °C, V_{DD} = +5 V, V_{CC} = +8 V, Maximum Gain, 50 Ω system, Full band unless otherwise noted.

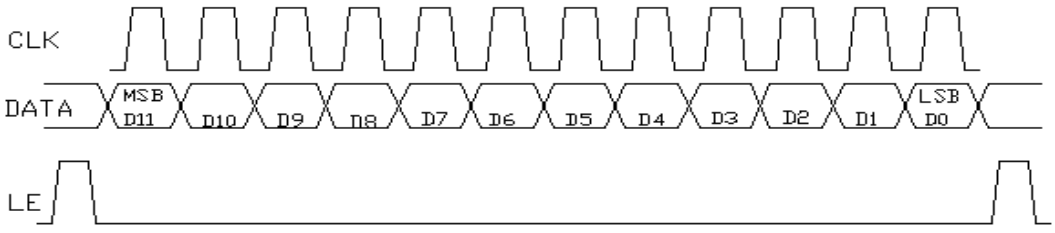
Truth Table: DSA1 Control Bit

D5	D4	D3	D2	D1	D0	Gain Relative to Maximum Gain
1	1	1	1	1	1	0 dBm
1	1	1	1	1	0	-0.5 dBm
1	1	1	1	0	1	-1 dBm
1	1	1	0	1	1	-2 dBm
1	1	0	1	1	1	-4 dBm
1	0	1	1	1	1	-8 dBm
0	1	1	1	1	1	-16 dBm
0	0	0	0	0	0	-31.5 dBm

Truth Table: DSA2 Control Bit

D11	D10	D9	D8	D7	D6	Gain Relative to Maximum Gain
1	1	1	1	1	1	0 dBm
1	1	1	1	1	0	-0.5 dBm
1	1	1	1	0	1	-1 dBm
1	1	1	0	1	1	-2 dBm
1	1	0	1	1	1	-4 dBm
1	0	1	1	1	1	-8 dBm
0	1	1	1	1	1	-16 dBm
0	0	0	0	0	0	-31.5 dBm

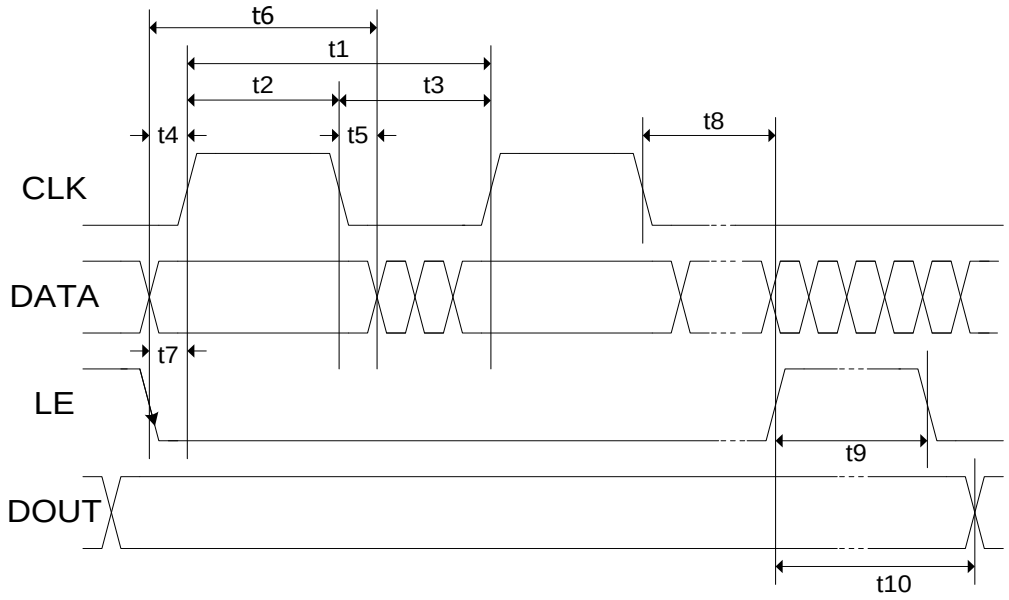
Programming Example - 12 Bit



Power-up Programming Truth Table	
PUP	Attenuator Setting
Low	Maximum = 63 dB
High	Minimum = 0 dB

Logic Voltage Levels	
State	Logic
Low	0 to 0.8 V
High	2.0 to 5.0 V

SPI Timing Diagram



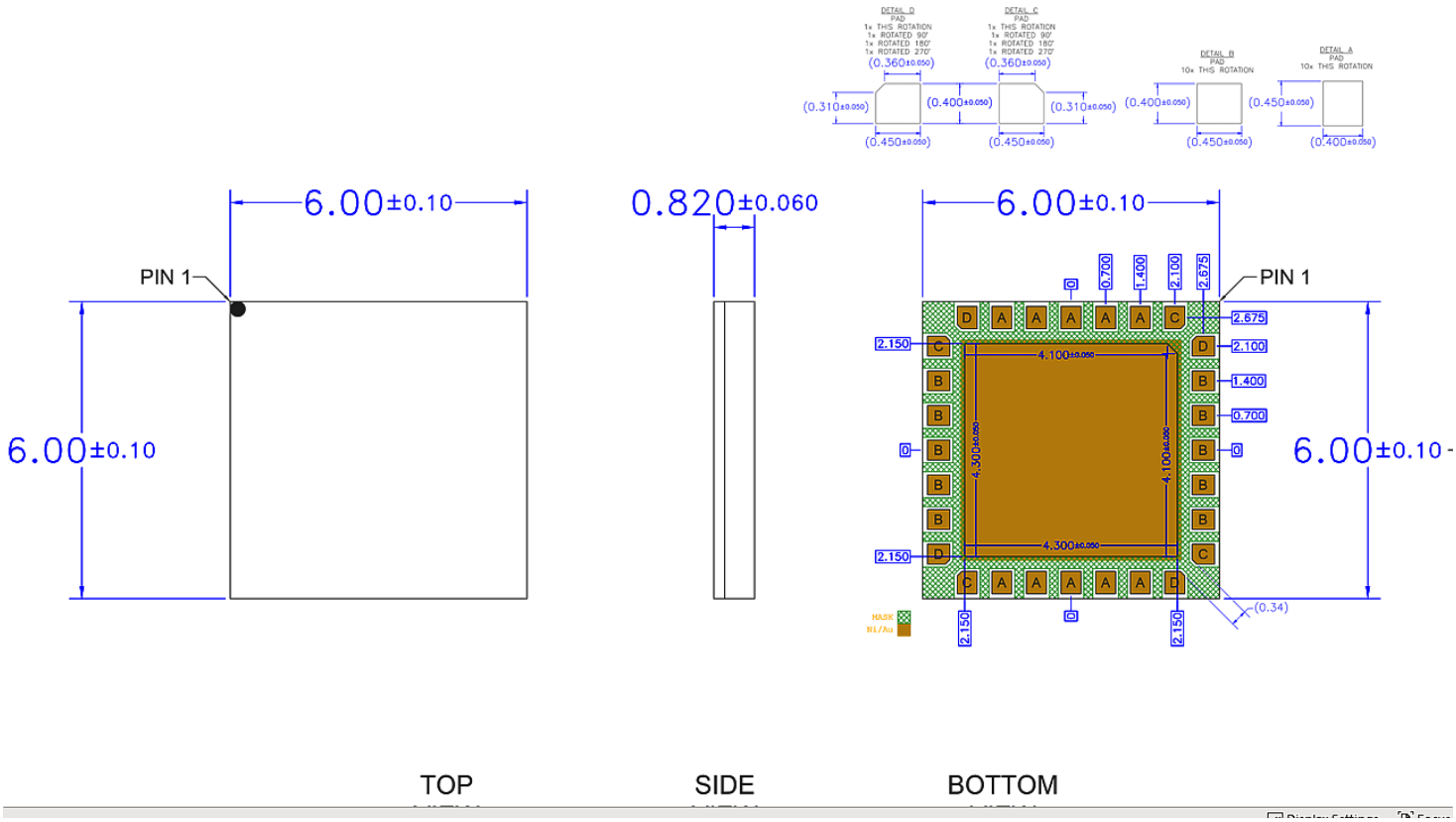
SPI Timing Diagram Specifications

Parameter	Limit	Unit	Comment
t1	25	MHz max	CLK Frequency
t2	20	ns min	CLK High
t3	20	ns min	CLK Low
t4	5	ns min	DATA to CLK Setup Time
t5	5	ns min	DATA to CLK Hold Time
t6	30	ns min	DATA Valid
t7	5	ns min	LE to CLK Setup Time
t8	5	ns min	CLK to LE Setup Time
t9	10	ns min	LE Pulse Width
t10	20	ns max	Output Set

Pin Configuration and Description

Pin Number	Label	Description
1	AMP1_IN	AMP1 Input
2	DSA1_OUT	DSA1 Output
3	NC	Not Connected Internally
4	NC	Not Connected Internally
5	NC	Not Connected Internally
6	NC	Not Connected Internally
7	DSA1_IN	DSA1 Input
8	GND	RF/DC Ground Connection
9	PUP	Power Up Programming Pin
10	DATA	Serial Data Input
11	LE	Serial Latch Enable
12	CLK	Serial Clock Input
13	VDD	Supply Voltage for DSA and SPI Control
14	GND	RF/DC Ground Connection
15	AMP2_OUT	AMP2 OUT and Bias Pin
16	GND	RF/DC Ground Connection
17	GND	RF/DC Ground Connection
18	AMP2_IN	AMP2 Input
19	DSA2_OUT	DSA2 Output
20	GND	RF/DC Ground Connection
21	NC	Not Connected Internally
22	NC	Not Connected Internally
23	NC	Not Connected Internally
24	NC	Not Connected Internally
25	DSA2_IN	DSA2 Input
26	AMP1_OUT	AMP1 Output and Bias Pin
27	GND	RF/DC Ground Connection
28	GND	RF/DC Ground Connection

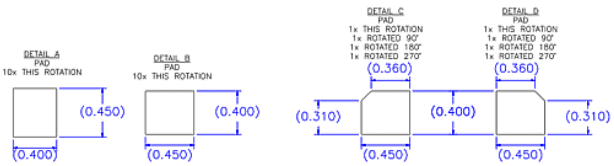
Package Outline

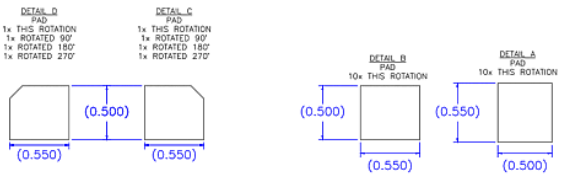


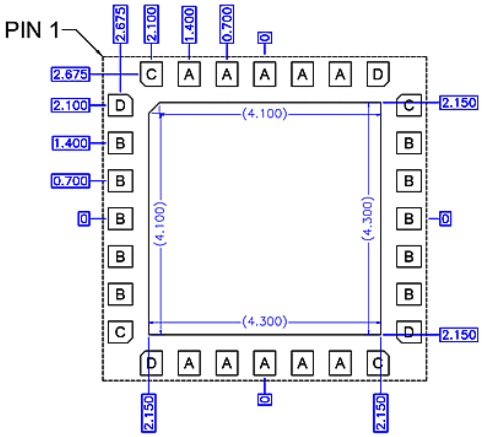
Notes:

1. Dimensions in millimeters.

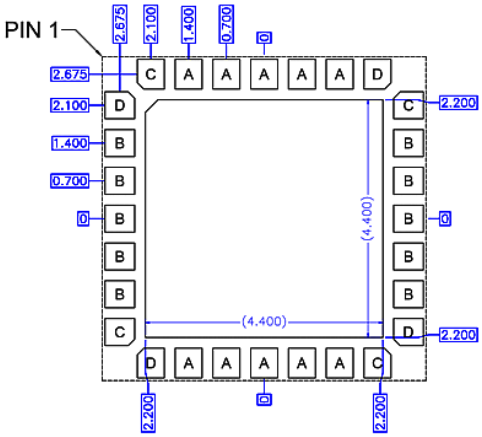
Package Dimensions







RECOMMENDED
LAND PATTERN



RECOMMENDED
LAND PATTERN MASK

Notes:
1. Dimensions in millimeters