QPB9325

High Power Switch LNA Module

Product Overview

The Qorvo® QPB9325 is a highly integrated front-end module targeted for TDD macro or picocell base stations. The LNA switch module integrates RF functional blocks such as a pin-diode based high power switch capable of handling up to 52 W with an LTE signal (8 dB PAR) along with two LNA stages. Further integration is also implemented where the pin diode driver and DC-DC converter circuits are implemented inside the module to enable only the need for an external 5 V power supply. The control voltage for the switch and Gain control. mode is with 3.3 V logic.

The QPB9325 can be utilized across the 3.3-4.2 GHz range to provide 1.2 dB noise figure for operation in the receive mode and 0.5 dB insertion loss in the transmit mode. The LNAs utilize Qorvo's high performance E-pHEMT process while the switch allows for power levels up to 360 W peak power to be routed to an external load termination.

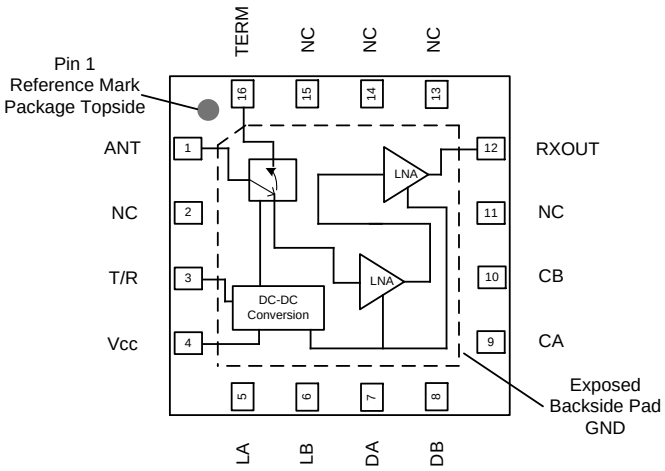
The QPB9325 is packaged in a RoHS-compliant, compact 8x8 mm surface-mount leadless package. The switch LNA module is targeted for wireless infrastructure applications configured for TDD-based architectures.

16 Pin 8 mm x 8 mm Leadless SMT Package

Key Features

- 3.3-4.2 GHz frequency range
- Integrates a high-power switch, two LNA stages, pin diode driver circuits, and dc converter
- Ideal for TDD systems with an isolator
- Only requires a 5 V supply with 3.3 V logic Ctrl.
- Max RF Input power: 52 W Pavg (8 dB PAR)
- 34.1 dB gain
- 1.2 dB noise figure
- -2.2 dBm IIP3 (Rx mode)
- 0.5 dB Insertion Loss (Tx mode)
- Compact package size, 8x8 mm

Functional Block Diagram



Top View

Applications

- Wireless Infrastructure
- Macro or picocell base stations
- TDD-based architectures

Ordering Information

Part No.	Description
QPB9325TR13	2500 pcs on a 13" reel
QPB9325EVB	Evaluation board

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-50 to +150 °C
Max Operating Temperature	+115 °C
V_{CC}	+6 V
RF at ANT (Tx Mode) (1)	+47.2 dBm
RF at ANT (Tx Mode) (2)	+44.2 dBm
RF at ANT (Rx Mode) (2)	+20 dBm

Notes:
1. 10s, 8 dB PAR, 88% duty cycle, +100 °C, 1CH LTE
2. Indefinitely, 8 dB PAR, 88% duty cycle, +100 °C, 1CH LTE

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V_{CC}	+4.75	+5	+5.25	V
T/R Mode Low Voltage	0		0.8	V
T/R Mode High Voltage	2.0		3.6	V
T_{CASE}	−40		+105	°C
Tj for >10^6 hours MTTF (3)			+190	°C

Notes:
3. For RX Mode operation

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

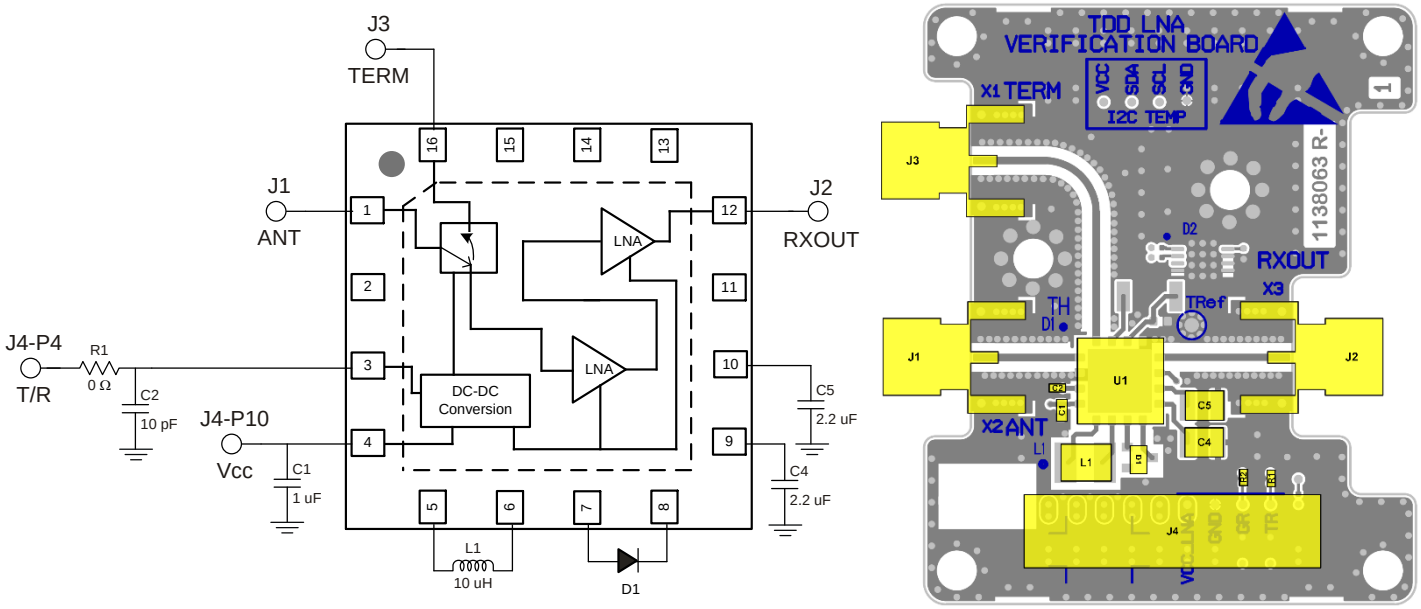
Electrical Specifications

Test conditions unless otherwise noted: V_{CC} = +5.0 V, Temp. = +25 °C, 50 Ω system

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		3300 (4)		4200	MHz
Test Frequency			3700		MHz
Gain	Rx mode	31	34.1		dB
Gain Flatness	Rx mode		1.0		dB
Noise Figure	Rx mode		1.2	1.65	dB
Input IP3	Rx mode, Pin/tone = -33 dBm, Δf = 1 MHz	-10	-2.2		dBm
Input P1dB	Rx mode	-20	-15		dBm
Input Return Loss (ANT)	Rx mode		30		dB
Output Return Loss (Rx Out)	Rx mode		26		dB
Reverse Isolation	Rx mode		58		dB
Insertion Loss	Tx mode		0.5	1.0	dB
Input P0.1dB	Tx mode		>+46.6		dBm
Return Loss (ANT, TERM)	Tx mode		25		dB
Operating Current	Rx mode		240		mA
Operating Current	Tx mode		140	150	mA
Switching Time (ANT to Rx Out)	RF<0.1dB after T/R command		2		µs
Switching Time (ANT to Term)	RF<0.1dB after T/R command		1		µs
Switching Time (ANT to Rx Out/Term)	ANT to RXOUT/TERM with RF<0.5dB after DC turn on		1		s
In Band Spurious Emission (5)	Rx Mode at Rx out with Pin = -49 dBm (6)		-85		dBc
Out of Band Emissions (7)	Rx Mode at Rx out from DC to 12275 MHz		-73		dBm
Thermal Resistance	Rx mode			22	°C/W
Thermal Resistance	Tx mode			22	°C/W

Notes:
4. External matchings applied
5. Pin is a CW signal swept from 3.6 to 3.8 GHz. Spec refers to any spurious mixing product that occurs from 3.6 to 3.8 GHz.
6. Recommend to follow Qorvo EVB layout for lowest spur level; any deviation can increase spur level.
7. Measure Pout with IBW = 4.5 MHz over frequency range with no input power applied.

Application Circuit Schematic and Layout – QPB9325EVB



Note: L1 is placed 5mm from bottom edge of U1 to top edge of L1 for in band spur suppression.

Bill of Material – QPB9325EVB

Ref Des	Value	Description	Manuf.	Part Number
-	-	Printed Circuit Board		
U1	-	High Power Switch LNA Module	Qorvo	QPB9325
R1, R2	0 Ω	Resistor, Chip, 0402, 5%	Various	
C1	1 µF	Capacitor, Chip, 0603, 20%, X7R	Various	
C2	10 pF	Capacitor, Chip, 0402, NPO/COG, 5%	Various	
C4, C5	2.2 µF	Capacitor, Chip, 1210, 100 V, 10%, X7R	Various	
D1	-	Diode, 200 V 200 mA SOT23	Various	
L1	10 µH	Inductor, Power, 10 µH, 20%, 0.84 A	Coilcraft	LPS4018-103ML

Logic Table

Parameter	High	Low
T/R	Rx Mode	Tx Mode

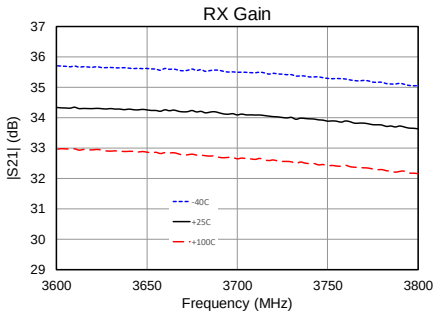
Typical Performance, Rx Mode – QPB9325EVB

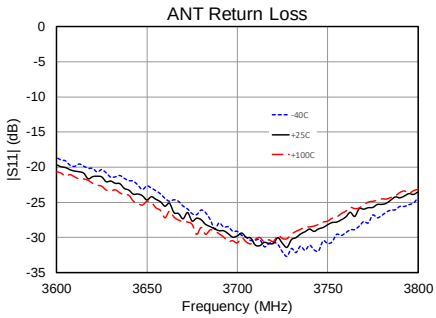
Parameter	Conditions (1)	Typical Value			Units
Frequency		3600	3700	3800	MHz
Gain		34.3	34.1	33.6	dB
Input IP3	Pin = -33 dBm/tone, Δf=1 MHz	-1.1	-2.2	-1.4	dBm
Input P1dB		-15.4	-15.3	-15.0	dBm
Noise Figure	De-embedded from Evaluation board PCB	1.2	1.2	1.2	dB
Return Loss	ANT port	20	30	24	dB
Return Loss	Rx Out port	30	26	24	dB
Reverse Isolation	Rx Out to ANT port	58	58	58	dB

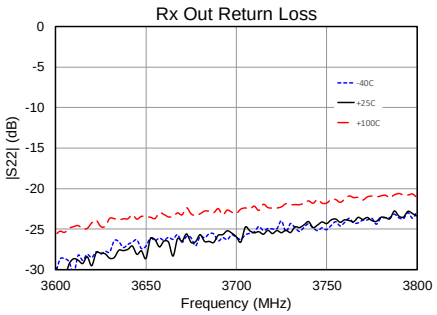
Notes:
1. Test conditions unless otherwise noted: V_{CC} = +5.0 V, T/R = 3 V, Temp. = +25 °C

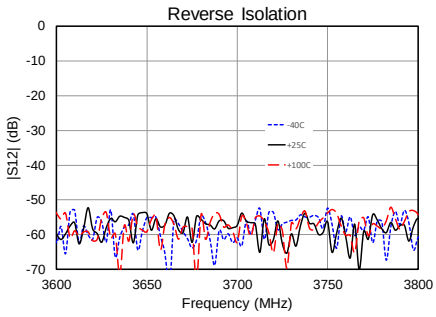
Performance Plots, Rx Mode – QPB9325EVB

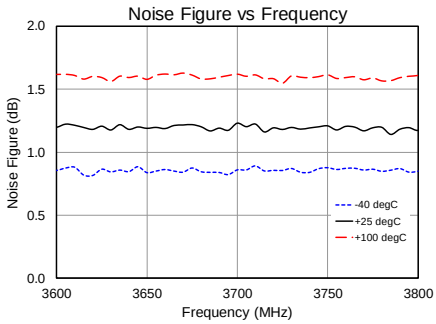
Test conditions unless otherwise noted: V_{CC} = +5.0 V, T/R = 3 V; Temp.= +25 °C

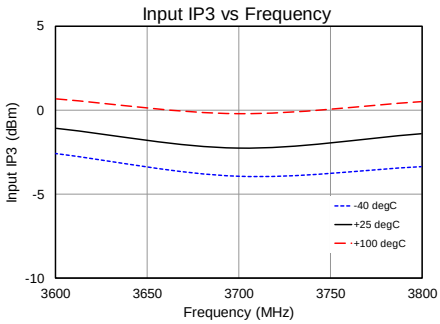


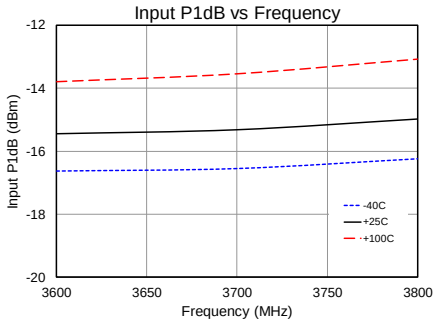












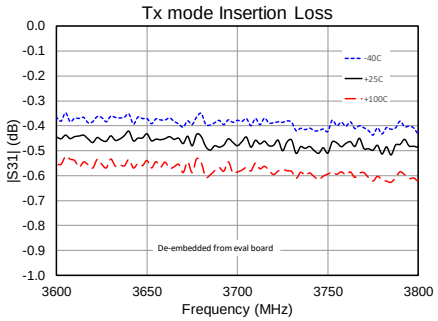
Typical Performance, Tx Mode – QPB9325EVB

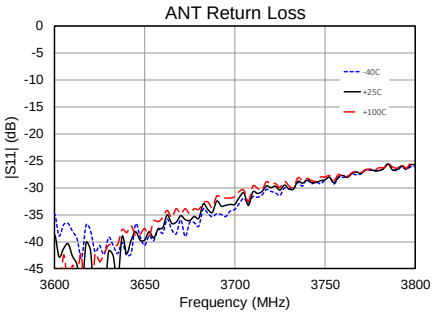
Parameter	Conditions (1)	Typical Value			Units
Frequency		3600	3700	3800	MHz
Insertion Loss	De-embedded from Evaluation board PCB	0.5	0.5	0.5	dB
Input Compression	Pin = +46.6dBm	< 0.1	< 0.1	< 0.1	dB
Return Loss	ANT port	40	33	26	dB
Return Loss	TERM port	26	25	23	dB

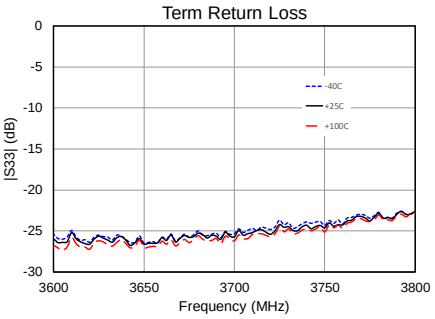
Notes:
1. Test conditions unless otherwise noted: V_{CC} = +5.0 V, T/R = 0 V, Temp. = +25 °C

Performance Plots, Tx Mode – QPB9325EVB

Test conditions unless otherwise noted: V_{CC} = +5.0 V, T/R = 0 V; Temp.= +25 °C







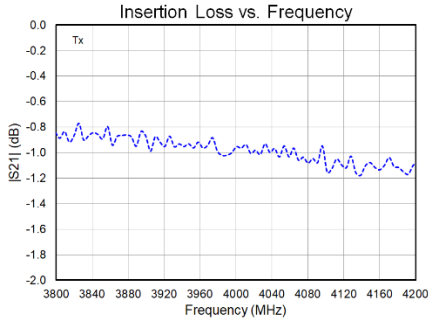
3.9 GHz to 4.2 GHz Performance, Tx Mode – QPB9325EVB

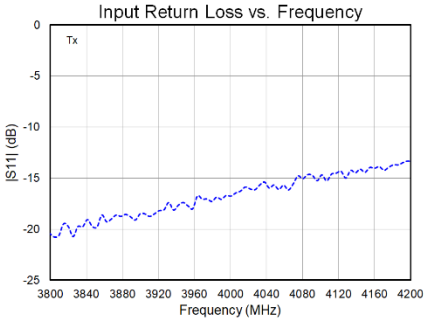
Parameter	Conditions (1)	Typical Value			Units
Frequency		3900	4000	4200	MHz
Insertion Loss	Evaluation board	0.87	0.95	1.07	dB
Return Loss	ANT port	18	16.7	13.4	dB
Return Loss	TERM port	19	17.9	14.4	dB

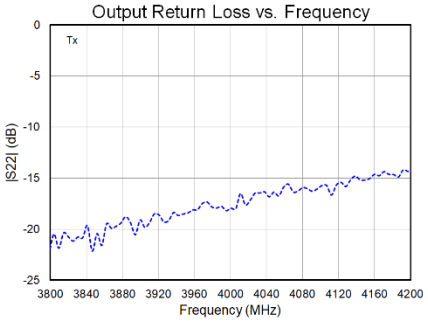
Notes:
1. Test conditions unless otherwise noted: V_{CC} = +5.0 V, T/R = 0 V, Temp. = +25 °C

3.9 GHz to 4.2 GHz Performance Plots, Tx Mode – QPB9325EVB

Test conditions unless otherwise noted: V_{CC} = +5.0 V, T/R = 0 V, Temp.= +25 °C, Input ANT port, Output TERM port, On EVB







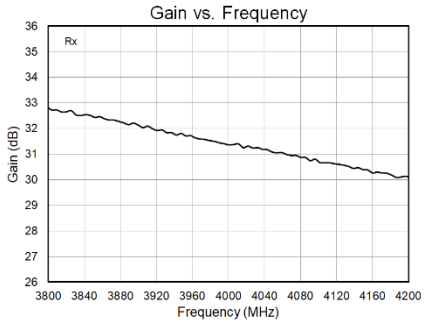
3.9 GHz to 4.2 GHz Performance, Rx Mode – QPB9325EVB

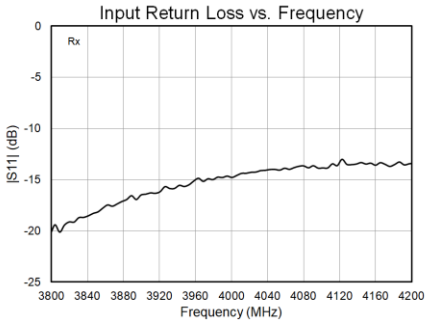
Parameter	Conditions (1)	Typical Value			Units
Frequency		3900	4000	4200	MHz
Gain		32.1	31.4	30.1	dB
Input IP3	Pin = -33 dBm/tone, Δf=1 MHz	-1.31	-0.56	0.47	dBm
Input P1dB		-15.3	-14.7	-13.0	dBm
Noise Figure	Trace Loss de-embedded	1.30	1.34	1.45	dB
Return Loss	ANT port	16	15	13	dB
Return Loss	Rx Out port	20	19	18	dB
Reverse Isolation	Rx Out to ANT port	50	51	52	dB

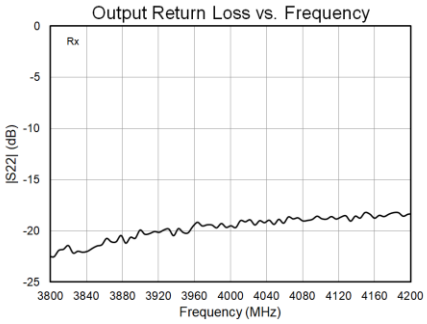
Notes:
1. Test conditions unless otherwise noted: V_{CC} = +5.0 V, T/R = 3 V, Temp. = +25 °C

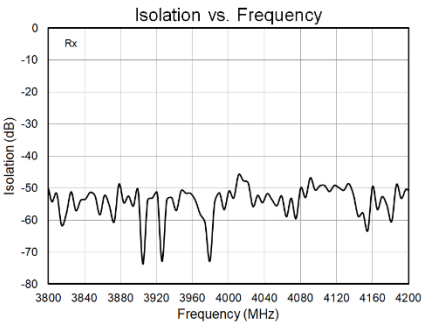
3.9 GHz to 4.2 GHz Performance Plots, Rx Mode – QPB9325EVB

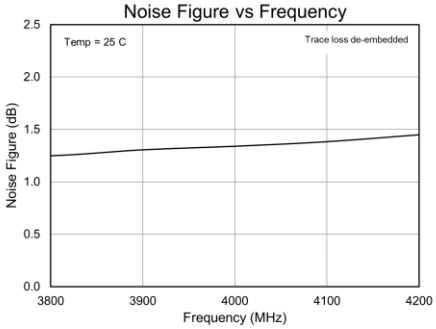
Test conditions unless otherwise noted: V_{CC} = +5.0 V, T/R = 3 V; Temp.= +25 °C

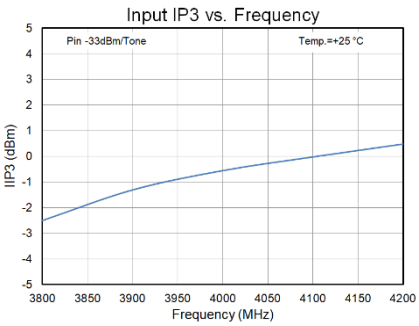


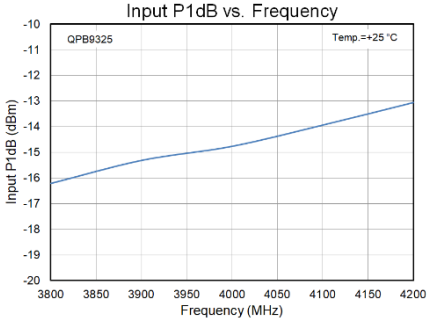




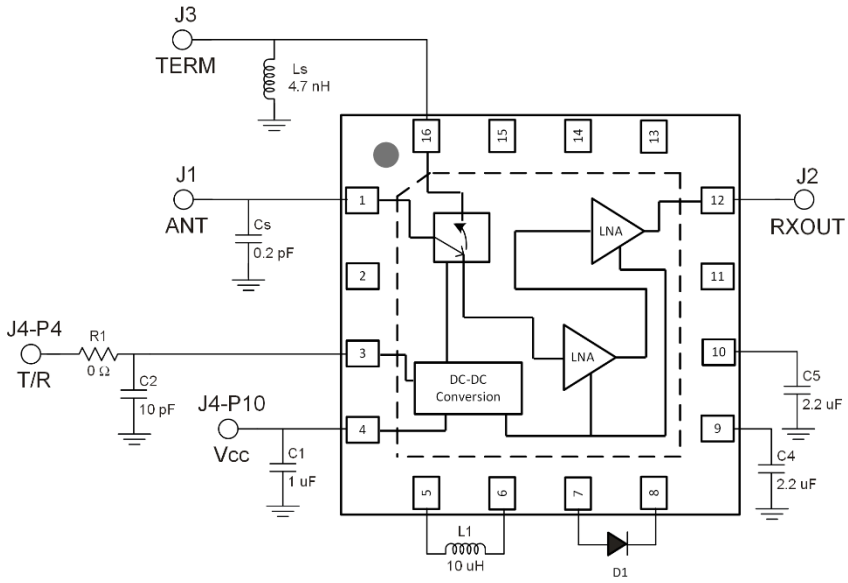


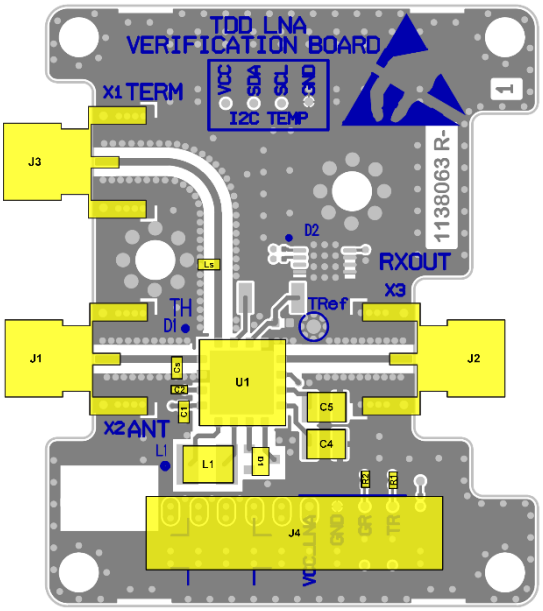






Application Reference – 3.3GHz to 3.8GHz with on EVB Matchings





Note: L1 is placed 5mm from bottom edge of U1 to top edge of L1 for in band spur suppression.

Bill of Material – 3.3GHz to 3.8GHz with on EVB Matchings

Ref Des	Value	Description	Manuf.	Part Number
-	-	Printed Circuit Board		
U1	-	High Power Switch LNA Module	Qorvo	QPB9325
R1, R2	0 Ω	Resistor, Chip, 0402, 5%	Various	
C1	1 µF	Capacitor, Chip, 0603, 20%, X7R	Various	
C2	10 pF	Capacitor, Chip, 0402, NPO/COG, 5%	Various	
C4, C5	2.2 µF	Capacitor, Chip, 1210, 100 V, 10%, X7R	Various	
D1	-	Diode, 200 V 200 mA SOT23	Various	
L1	10 µH	Inductor, Power, 10 µH, 20%, 0.84 A	Coilcraft	LPS4018-103ML
Cs	0.2 pF	Capacitor, Chip, 0603	AVX	
Ls	4.7 nH	Inductor, Chip, 0603	Toko	

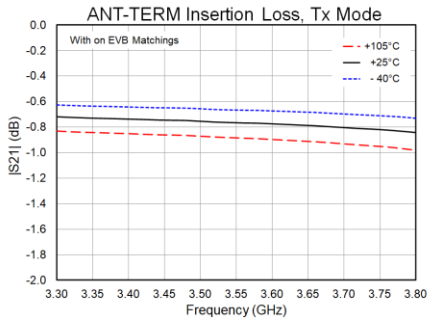
3.3 GHz to 3.8 GHz Performance, Tx Mode – with on EVB Matchings

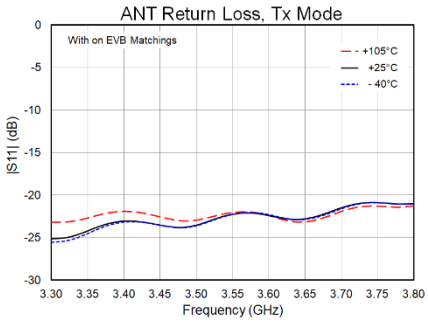
Parameter	Conditions (1)	Typical Value					Units
Frequency		3300	3400	3600	3700	3800	MHz
Insertion Loss	Evaluation board	0.72	0.74	0.78	0.81	0.84	dB
Return Loss	ANT port	25.1	23.0	22.3	21.5	20.9	dB
	TERM port	26.4	24.4	25.8	24.1	23.6	dB

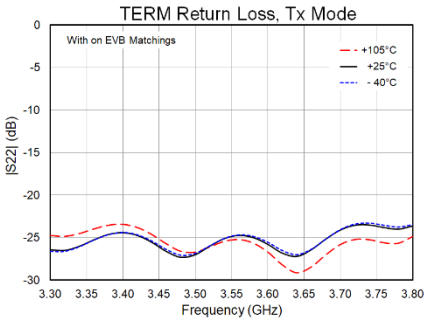
Notes:
1. Test conditions unless otherwise noted: V_{CC} = +5.0 V, T/R = 0 V, Temp. = +25 °C, with on EVB matchings

3.3 GHz to 3.8 GHz Performance Plots, Tx Mode – with on EVB Matchings

Test conditions unless otherwise noted: V_{CC} = +5.0 V, T/R = 0 V, ANT-input port, TERM-output port, with on EVB matchings







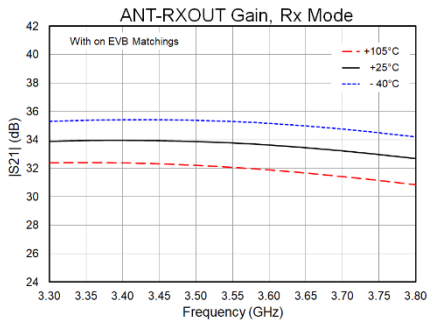
3.3 GHz to 3.8 GHz Performance, Rx Mode – with on EVB Matchings

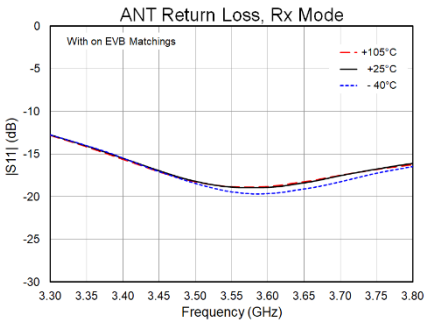
Parameter	Conditions (1)	Typical Value					Units
Frequency		3300	3400	3600	3700	3800	MHz
Gain		33.9	33.9	33.6	33.2	34.2	dB
Input IP3	Pin = -33 dBm/tone, Δf=1 MHz	-2.24	-3.73	-3.16	-3.25	-2.53	dBm
Input P1dB		-16.9	-17.9	-16.9	-17.0	-16.0	dBm
Noise Figure	PCB trace loss deducted	1.31	1.27	1.26	1.30	1.35	dB
Return Loss	ANT port	12.8	15.5	18.9	17.2	16.1	dB
	RXOUT port	22.1	26.2	31.5	24.2	20.7	dB
Reverse Isolation	RXOUT to ANT port	54.9	56.0	57.6	57.6	57.0	dB

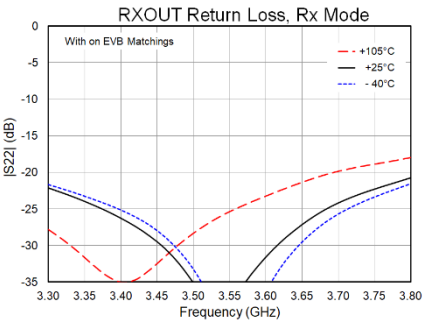
Notes:
1. Test conditions unless otherwise noted: V_{CC} = +5.0 V, T/R = 3 V, Temp. = +25 °C, with on EVB matchings

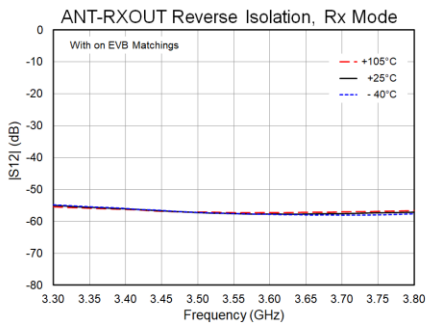
3.3 GHz to 3.8 GHz Performance Plots, Rx Mode – with on EVB Matchings

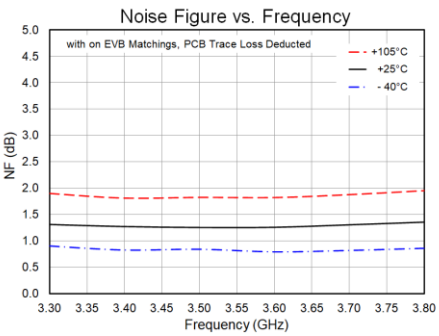
Test conditions unless otherwise noted: V_{CC} = +5.0 V, T/R = 3 V; Temp.= +25 °C

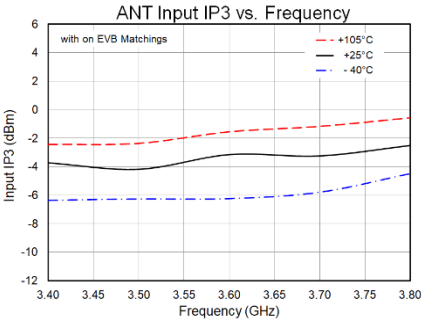


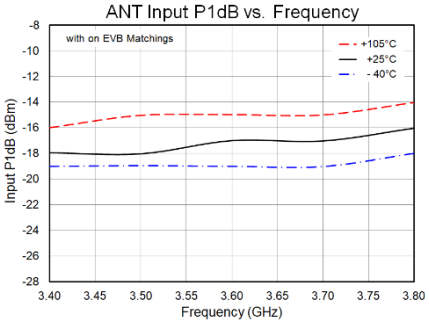










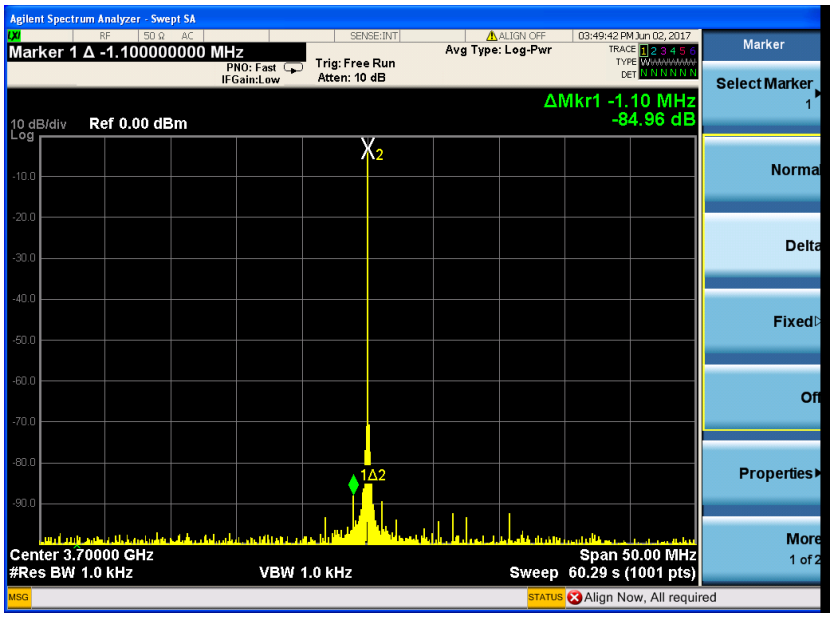


Application Circuit for Reduced Spurious

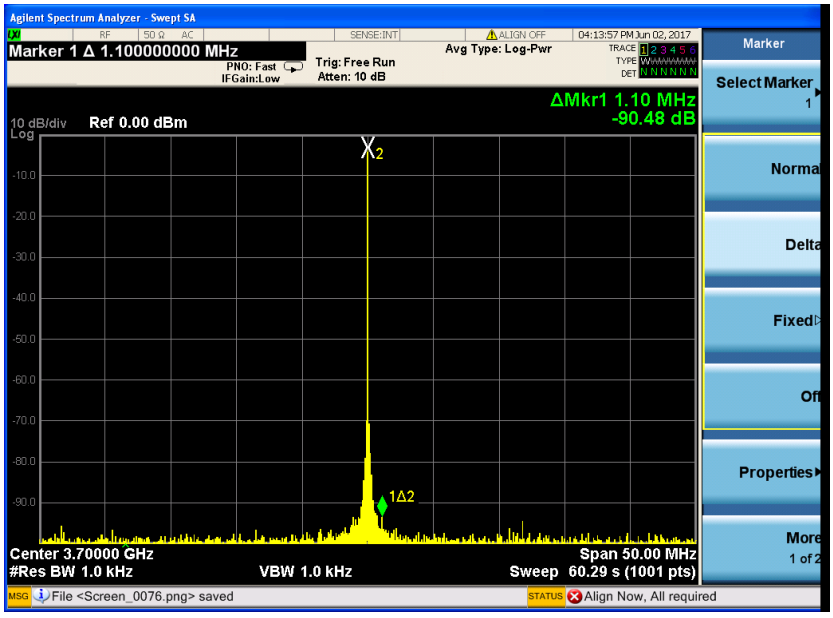
This section describes an alternative way to route the DC-DC converter signals for further improvement of in-band spurious emissions.

Spurious Performance – Modified PCB

Test conditions unless otherwise noted: V_{CC} = +5.0 V, T/R = +3.0 V, RFin = -35dBm CW; Temp.= +25 °C

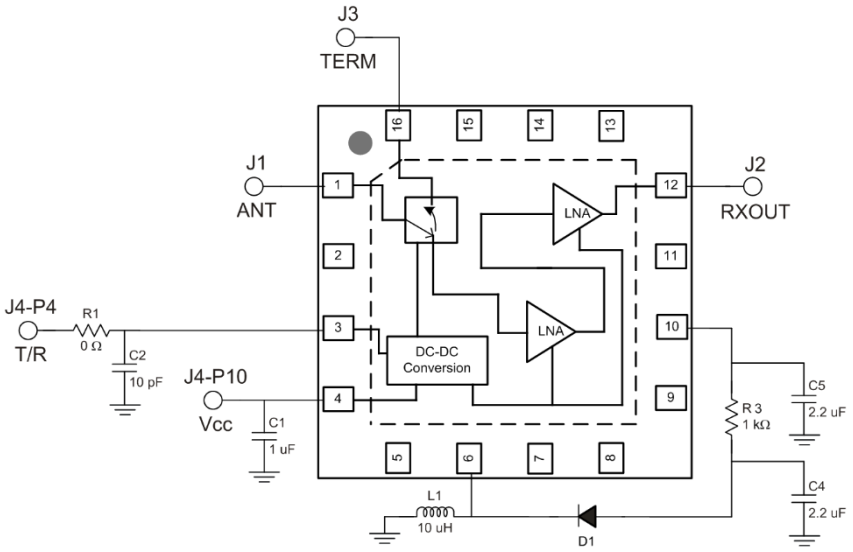


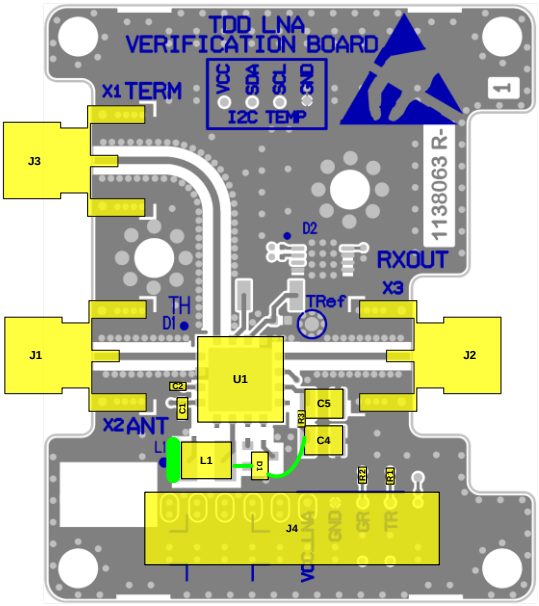
Original PCB Configuration



Modified PCB Configuration

Application Circuit Schematic and Layout – Modified PCB



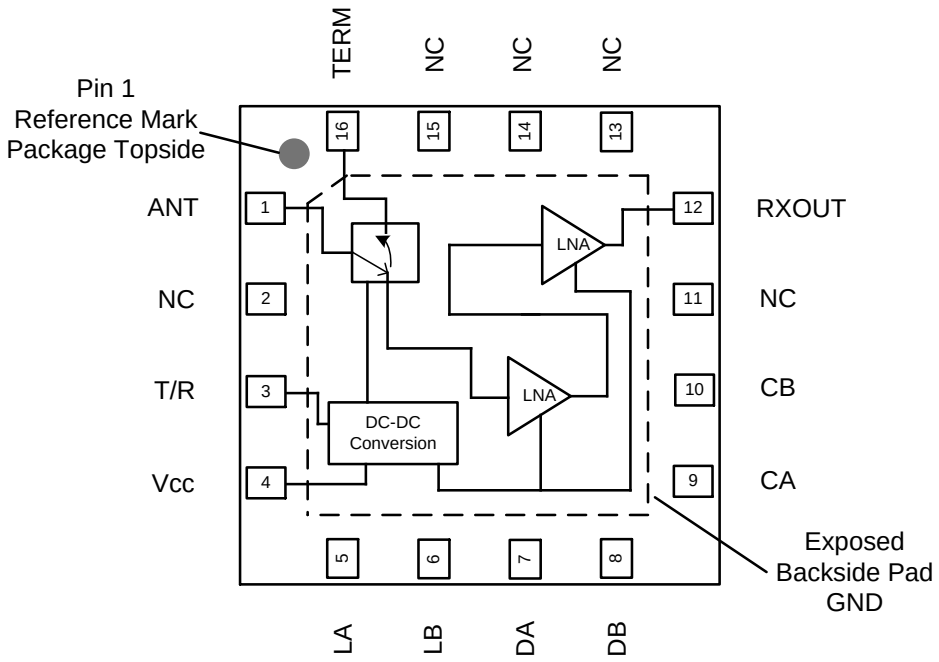


Note: R3 is the only additional component. All other parts are same as unmodified Evaluation Board

Bill of Material – Modified PCB

Ref Des	Value	Description	Manuf.	Part Number
-	-	Printed Circuit Board		
U1	-	High Power Switch LNA Module	Qorvo	QPB9325
R1, R2	0 Ω	Resistor, Chip, 0402, 5%	Various	
C1	1 µF	Capacitor, Chip, 0603, 20%, X7R	Various	
C2	10 pF	Capacitor, Chip, 0402, NPO/COG, 5%	Various	
C4, C5	2.2 µF	Capacitor, Chip, 1210, 100 V, 10%, X7R	Various	
D1	-	Diode, 200 V, 200 mA, SOT23	Various	
L1	10 µH	Inductor, Power, 10 µH, 20%, 0.84 A	Coilcraft	LPS4018-103ML
R3	1 kΩ	Resistor, Chip, 0402, 5%	Various	

Pin Configuration and Description

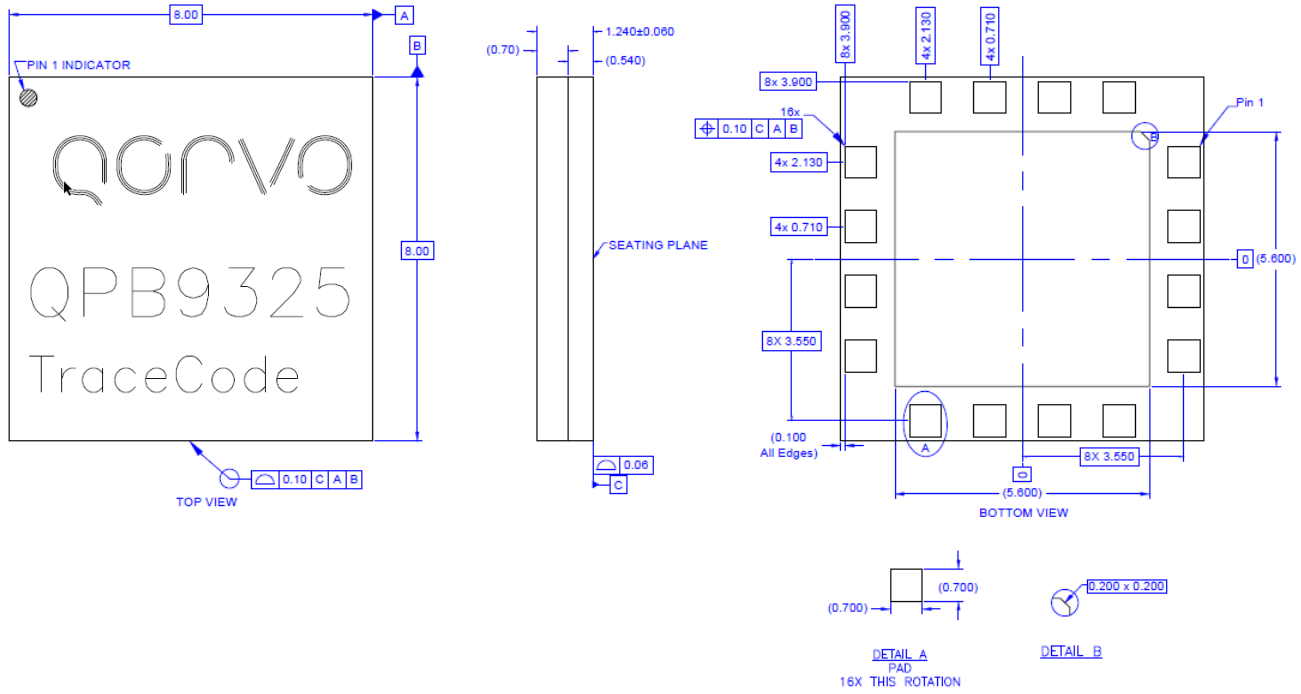


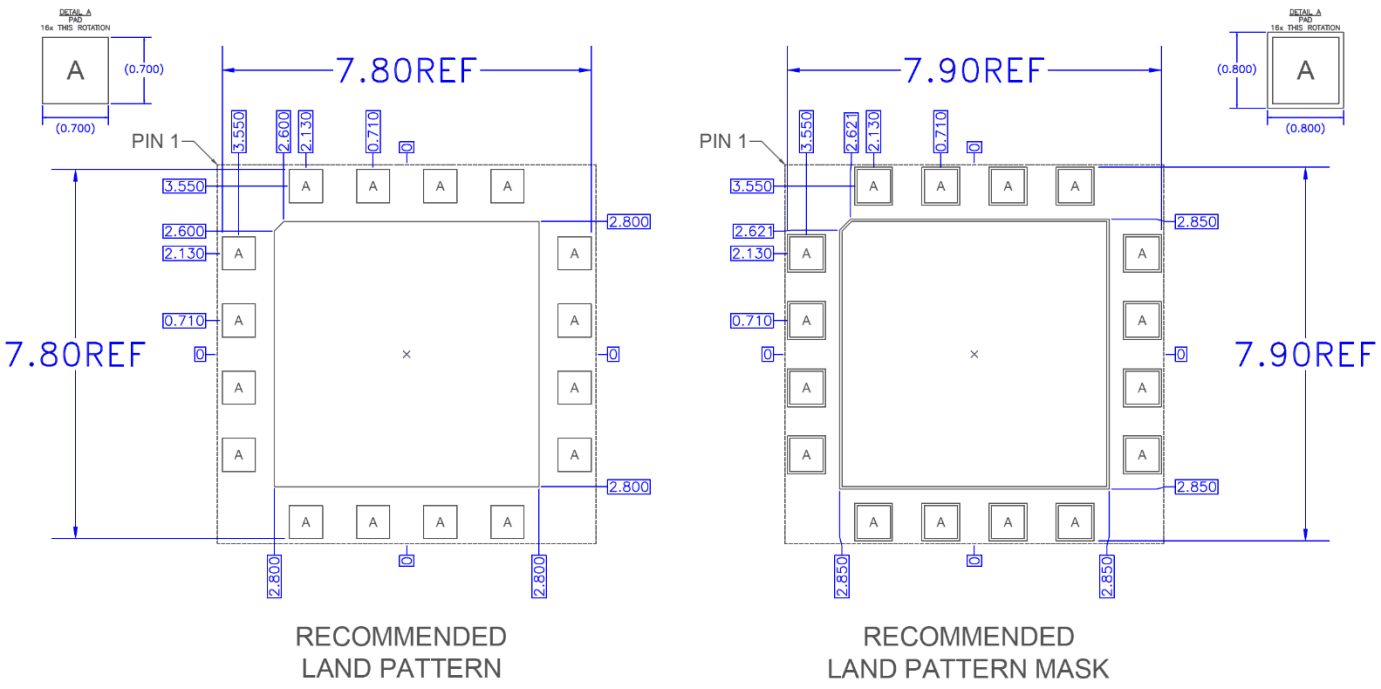
Top View

Pin No.	Label	Description
1	ANT	RF antenna input/output port 50 ohms. Internally DC blocked.
2, 11, 13, 14, 15	NC	No Internal Connection.
3	T/R	Switch Control, Tx mode Low state, Rx mode High state.
4	V_{CC}	DC Power Supply Voltage.
5	LA	External inductor connection for internal power supply.
6	LB	External inductor connection for internal power supply.
7	DA	External diode anode connection for internal power supply.
8	DB	External diode cathode connection for internal power supply.
9	CA	External bypass capacitor connection.
10	CB	External bypass capacitor connection.
12	RXOUT	RF LNA output port 50 ohms. Internally DC blocked.
16	TERM	RF termination port 50 ohms. Internally DC blocked.
Backside Pad	GND	Ground connection. The back side of the package should be connected to the ground plan though as short of a connection as possible. PCB vias under the device are required.

Package Marking and Dimensions

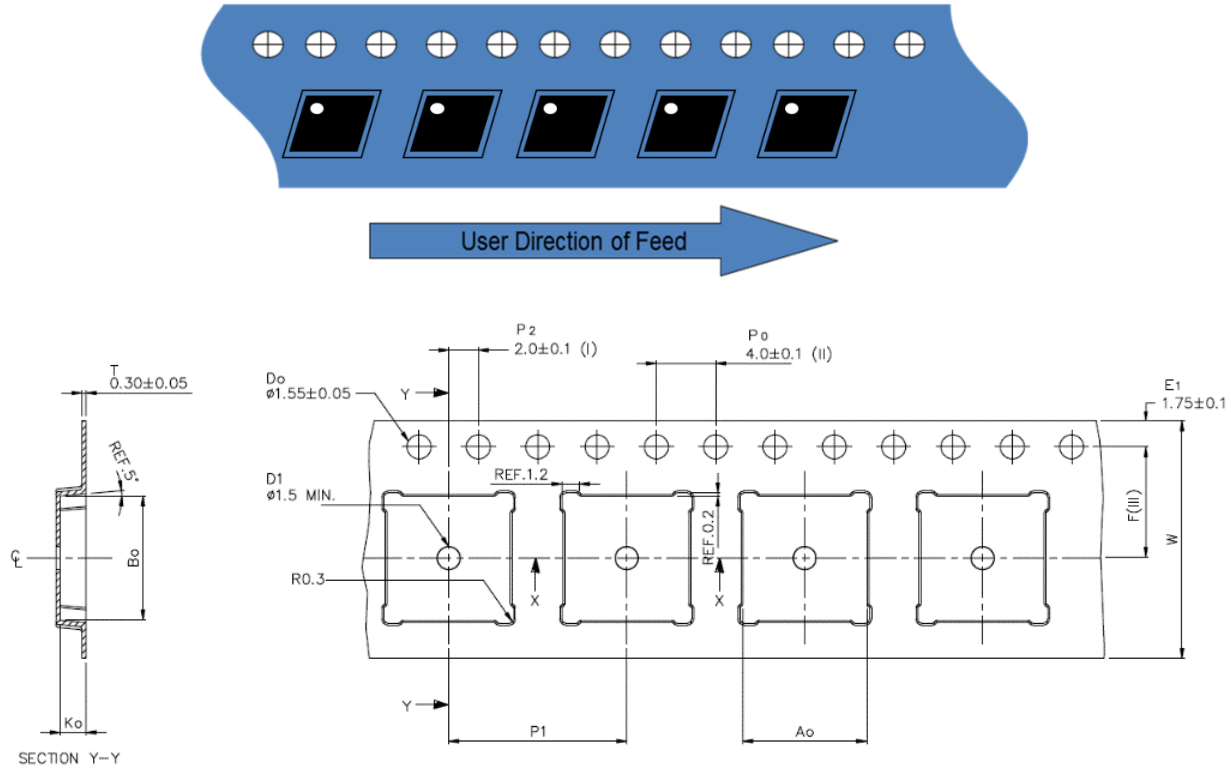
Marking: Part number – QPB9325
Trace Code





Notes:
1. All dimensions are in microns. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

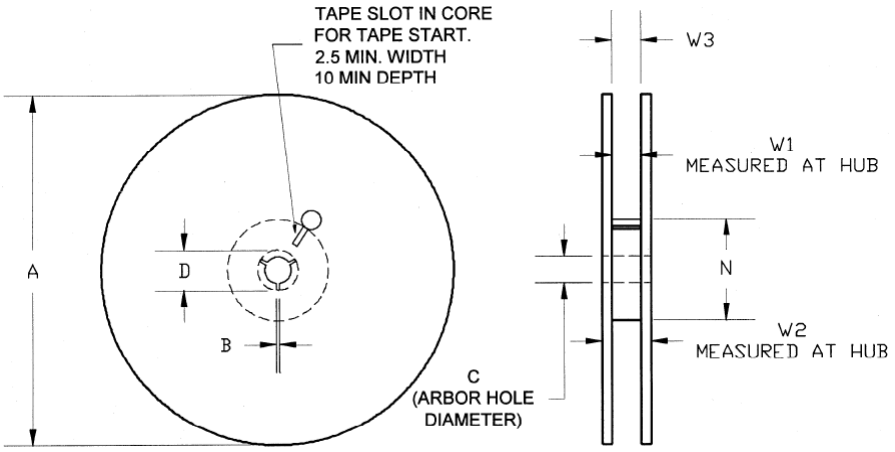
Tape and Reel Information – Carrier and Cover Tape Dimensions



Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.329	8.35
	Width	B0	0.329	8.35
	Depth	K0	0.069	1.76
	Pitch	P1	0.472	12.00
Centerline Distance	Cavity to Perforation - Length Direction	P2	0.079	2.00
	Cavity to Perforation - Width Direction	F	0.295	7.50
Cover Tape	Width (Reference Only)	C	0.524	13.30
Carrier Tape	Width	W	0.630	16.0

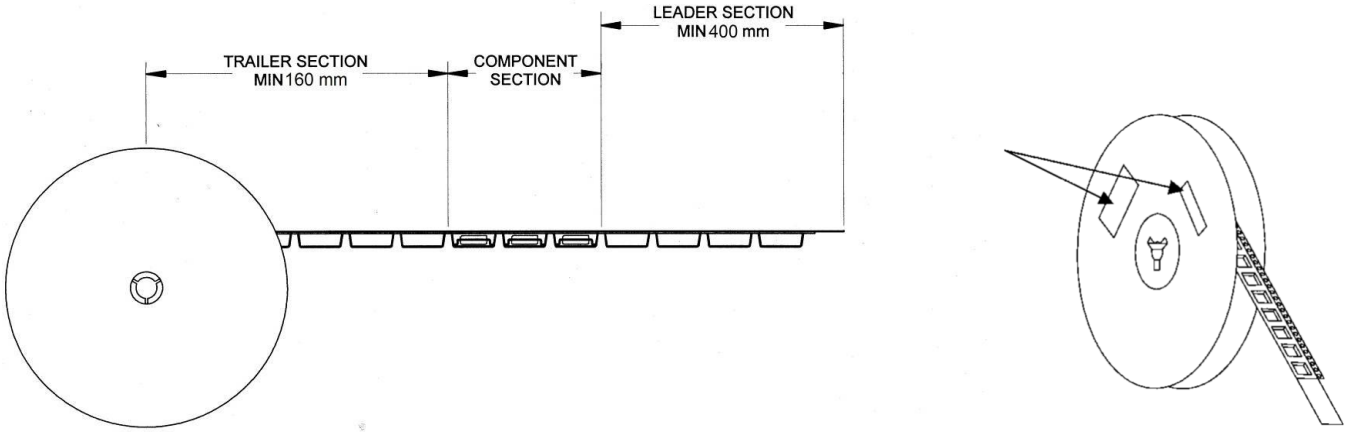
Tape and Reel Information – Reel Dimensions (13”)

Standard T/R size = 2,500 pieces on a 13” reel.



Feature	Measure	Symbol	Size (in)	Size (mm)
Flange	Diameter	A	12.992	330.0
	Thickness	W2	0.874	22.2
	Space Between Flange	W1	0.661	16.8
Hub	Outer Diameter	N	4.016	102.0
	Arbor Hole Diameter	C	0.512	13.0
	Key Slit Width	B	0.079	2.0
	Key Slit Diameter	D	0.787	20.0

Tape and Reel Information – Tape Length and Label Placement



Notes:
1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481-1-A.
2. Labels are placed on the flange opposite the sprockets in the carrier tape.