QPC2040

X-Band 10 W GaN SPDT Switch

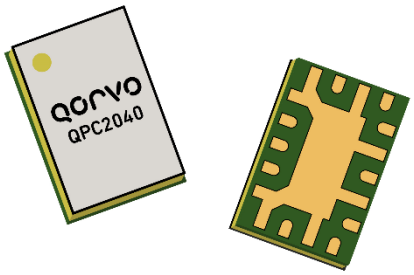
Product Overview

Qorvo's QPC2040 is a Single-Pole, Double–Throw (SPDT) switch fabricated on Qorvo's QGaN15 0.15um GaN on SiC production process.

Operating from 8 to 12 GHz, the QPC2040 typically supports 10 W input power handling at control voltages of 0/−28 V for pulsed RF operations. This switch maintains low insertion loss less than 1.2 dB and greater than 30 dB isolation, making it ideal for high power switching applications across both defense and commercial platforms.

QPC2040 is offered in a 3 x 4.5 mm plastic over-molded QFN package.

Lead-free and RoHS compliant



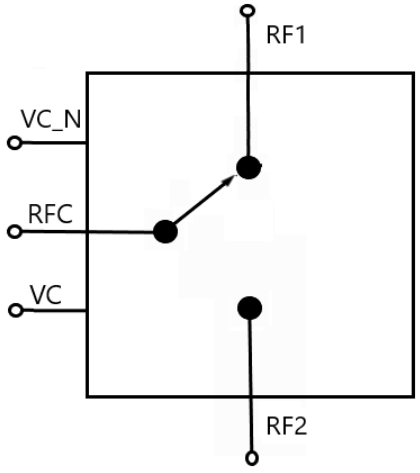
3 x 4.5 mm 18 Lead OVM QFN

Key Features

- SPDT
- Frequency Range: 8 to 12 GHz
- Input Power: 10 W
- Insertion Loss: < 1.2 dB
- Isolation: >30 dB Typical
- Switching Speed: 35 ns
- Control Voltages: 0 V/−28 V
- Redundant Control Lines
- Package Dimensions: 3 x 4.5 x 1.05 mm

Performance is typical across frequency. Please reference electrical specification table and data plots for more details.

Functional Block Diagram



Applications

- Radar
- Communications
- Electronic Warfare

Ordering Information

Part No.	Description
QPC2040SR	X-Band GHz 10W SPDT Switch 100 Piece 7" Reel
QPC2040EVB01	QPC2040 Evaluation Board

Absolute Maximum Ratings

Parameter	Rating
Control Voltage ($V_{C,}$ V_{C_N})	−30 V to 0V
Control Current ($I_{C,}$ I_{C_N})	See Plot
Power Dissipation, 85 °C	7.5 W
RF Input Power, PW = 100µ, DC = 25%, 50 Ω, T_{BASE} = 85 °C	44.5 dBm
RF Input Power, PW = 100µ, DC = 25%, 3:1 VSWR, T_{BASE} = 85 °C	43 dBm
Mounting Temperature (30 sec)	260 °C
Storage Temperature	−55 to 150 °C

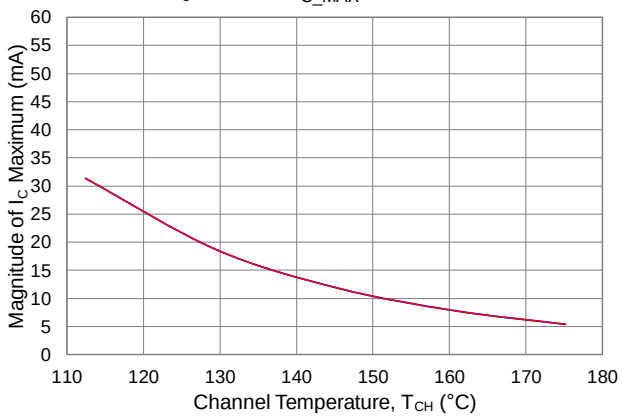
Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ.	Max	Units
V_C		0/-28		V
V_{C_N}		-28/0		V
Temperature Range	-40	+25	+85	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

QPC2040 I_{C_MAX} vs. T_{CH}



Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1,2)	T_{BASE} = 85 °C, V_C = 0 V, V_{C_N} = -28 V, Pulsed RF: PW = 100µ, DC = 25% Freq. = 10.0 GHz, P_{IN} = 44 dBm, P_{OUT} = 42.5 dBm, P_{DISS} = 1.83 W	14.75	ºC/W
Channel Temperature (T_{CH}) (1,2)		112	°C

Notes:
1. Measured to the back of the package.
2. Refer to the following document: GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates
3. This is a total P_{DISS} in the FETs.

Electrical Specifications

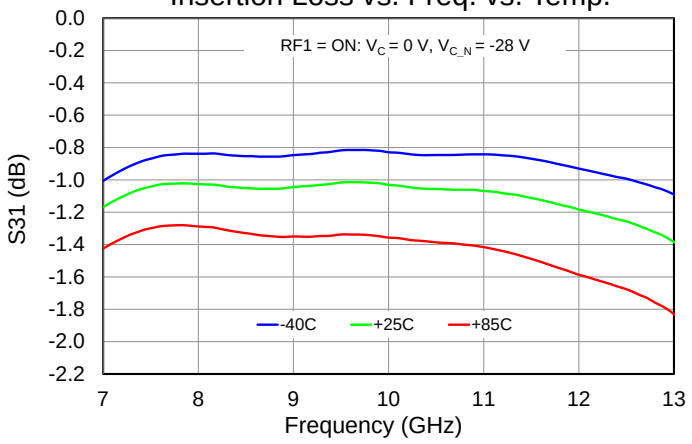
Test conditions unless otherwise noted: 25 °C, V_C = 0 V/-28V, V_{C_N} = -28 V/0V, see function table on page 15.

Parameter		Min	Typ.	Max	Units
Operational Frequency Range		8	–	12	GHz
Insertion Loss (On-State)	Frequency = 8 GHz	–	1.0	–	dB
	Frequency = 10 GHz	–	1.05	–	
	Frequency = 12 GHz	–	1.18	–	
Input Return Loss (On-State) Common Port RL	Frequency = 8 GHz	–	14	–	dB
	Frequency = 10 GHz	–	22	–	
	Frequency = 12 GHz	–	19	–	
Output Return Loss (On-State) Switched Port RL	Frequency = 8 GHz	–	14	–	dB
	Frequency = 10 GHz	–	17	–	
	Frequency = 12 GHz	–	25	–	
Isolation (Off-State)	Frequency = 8 GHz	–	35	–	dB
	Frequency = 10 GHz	–	36	–	
	Frequency = 12 GHz	–	34	–	
Output Return Loss Isolated Port	Frequency = 8 GHz	–	4.0	–	dB
	Frequency = 10 GHz	–	4.5	–	
	Frequency = 12 GHz	–	4.5	–	
Input Power ($P_{0.1dB}$)		–	41.7	–	dBm
Control Voltage		-30	-28	–	V
Total Supply Current		–	<3	–	mA
Switching Speed		–	35	–	ns
Insertion Loss Temperature Coefficient		–	-0.004	–	dB/°C

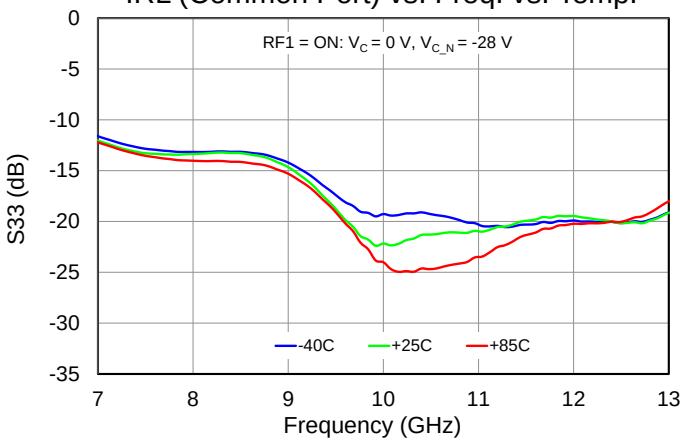
Performance Plots – Small Signal (RF1 Port)

Notes: RFC = Port 3; RF1 = Port 1; RF2 = Port 2

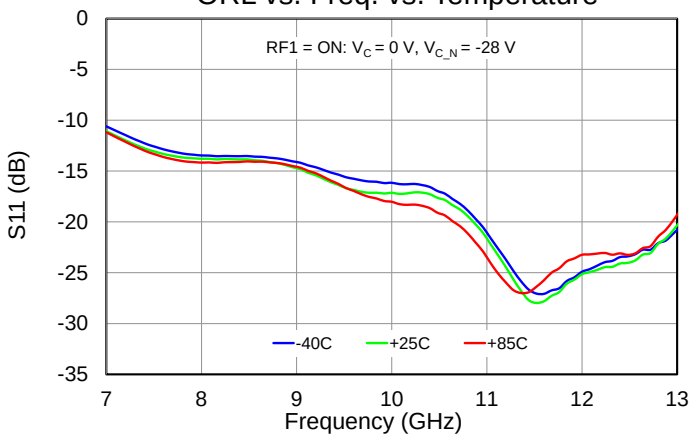
Insertion Loss vs. Freq. vs. Temp.



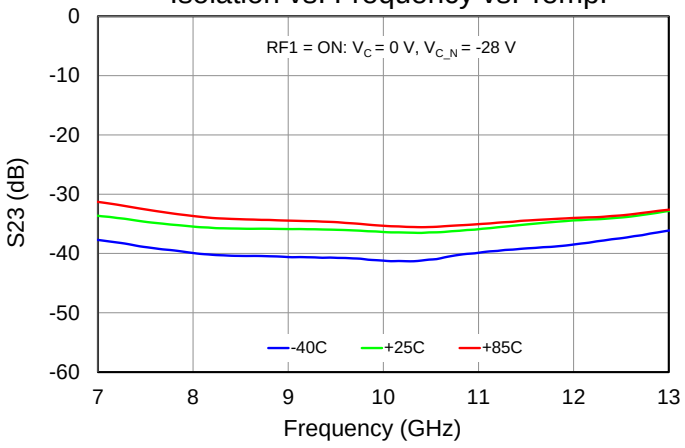
IRL (Common Port) vs. Freq. vs. Temp.



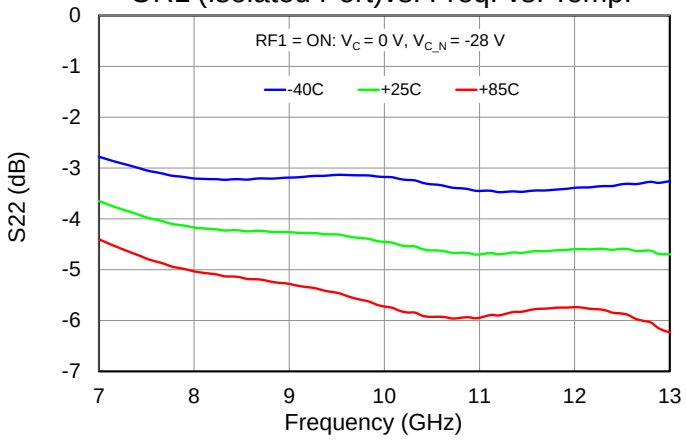
ORL vs. Freq. vs. Temperature



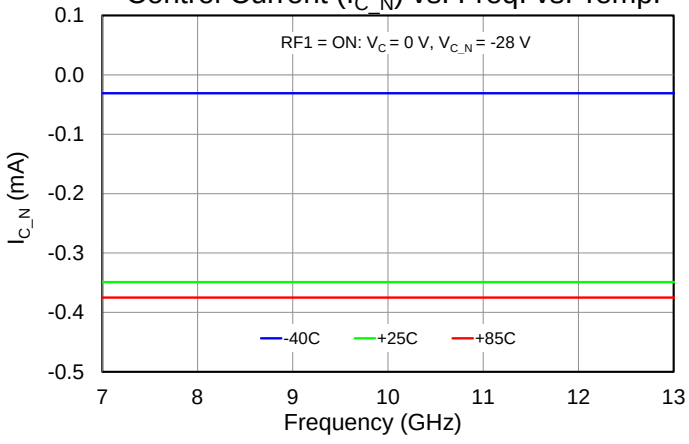
Isolation vs. Frequency vs. Temp.



ORL (Isolated Port)vs. Freq. vs. Temp.



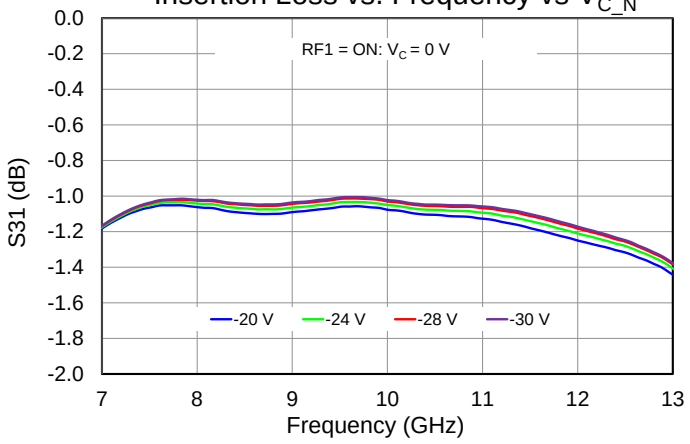
Control Current (I_{C_N}) vs. Freq. vs. Temp.



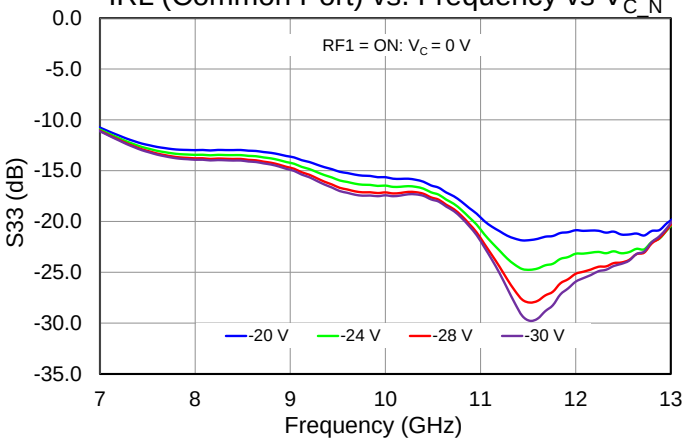
Performance Plots – Small Signal (RF1 Port)

Notes: RFC = Port 3; RF1 = Port 1; RF2 = Port 2

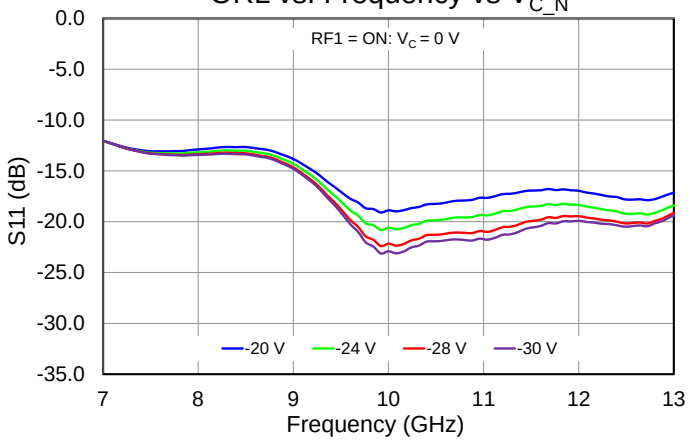
Insertion Loss vs. Frequency vs V_{C_N}



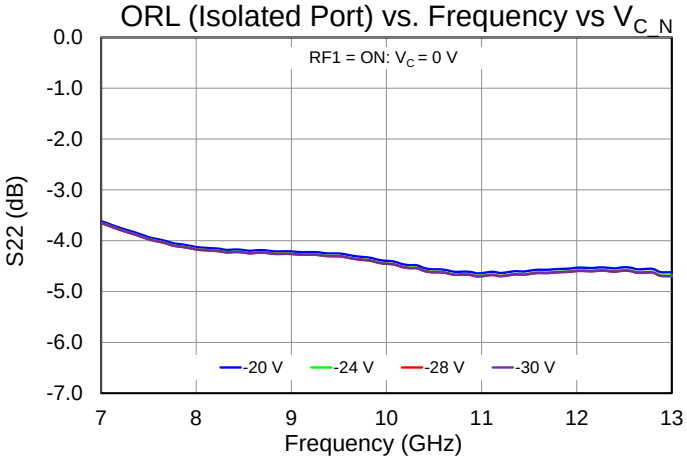
IRL (Common Port) vs. Frequency vs V_{C_N}



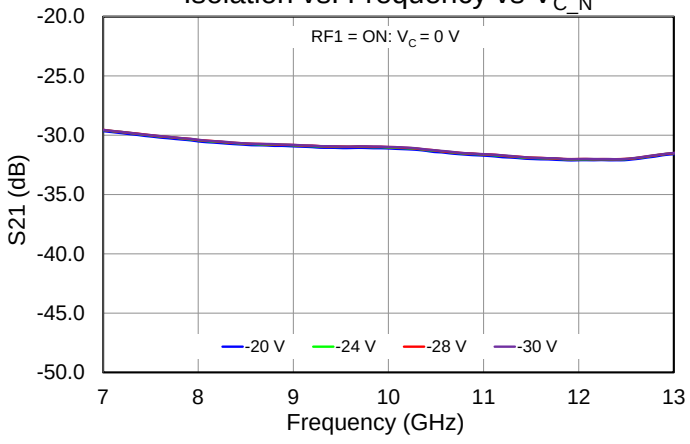
ORL vs. Frequency vs V_{C_N}



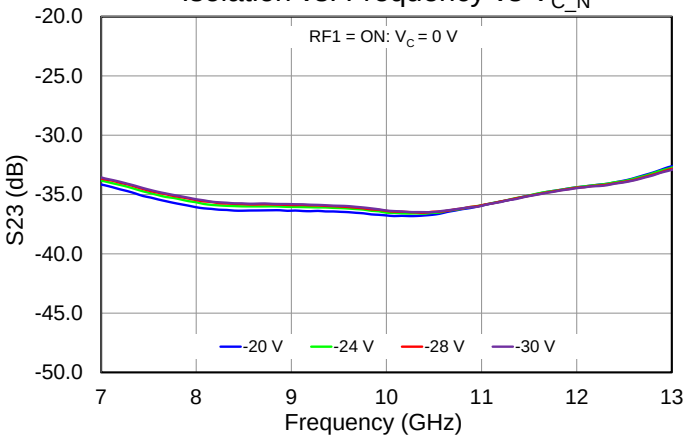
ORL (Isolated Port) vs. Frequency vs V_{C_N}



Isolation vs. Frequency vs V_{C_N}



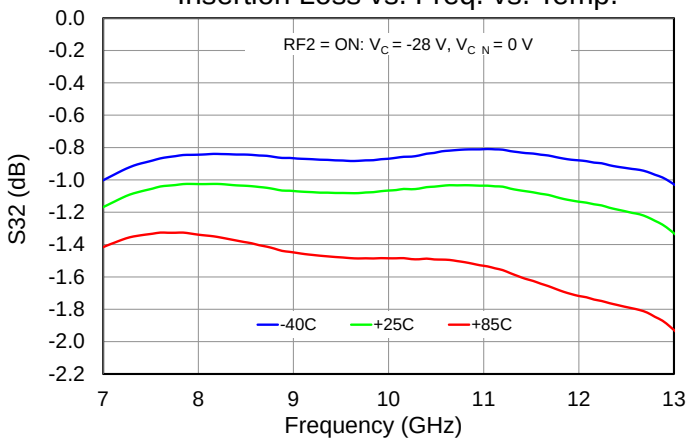
Isolation vs. Frequency vs V_{C_N}



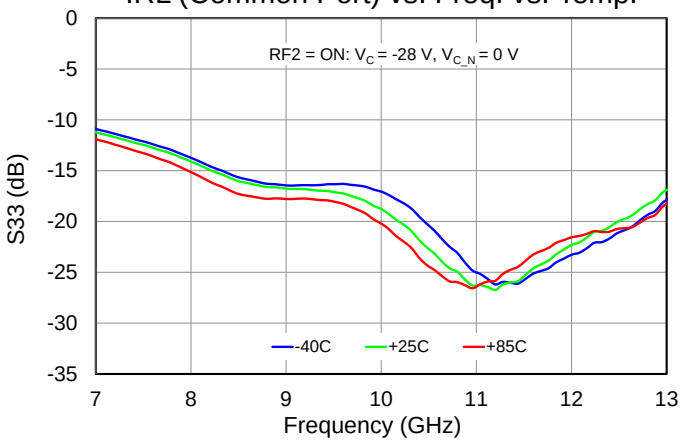
Performance Plots – Small Signal (RF2 Port)

Notes: RFC = Port 3; RF1 = Port 1; RF2 = Port 2

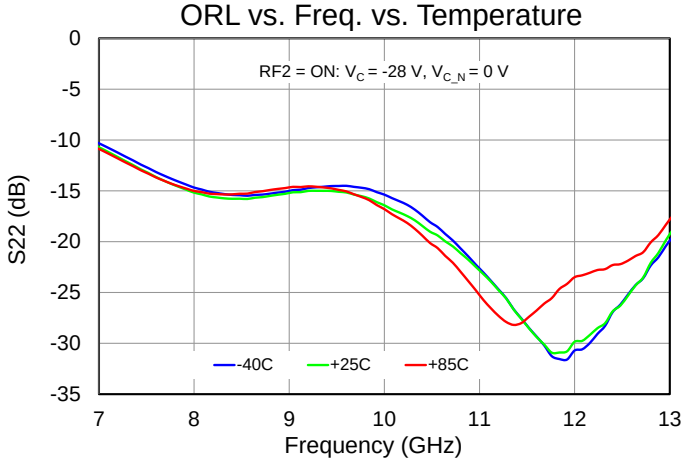
Insertion Loss vs. Freq. vs. Temp.



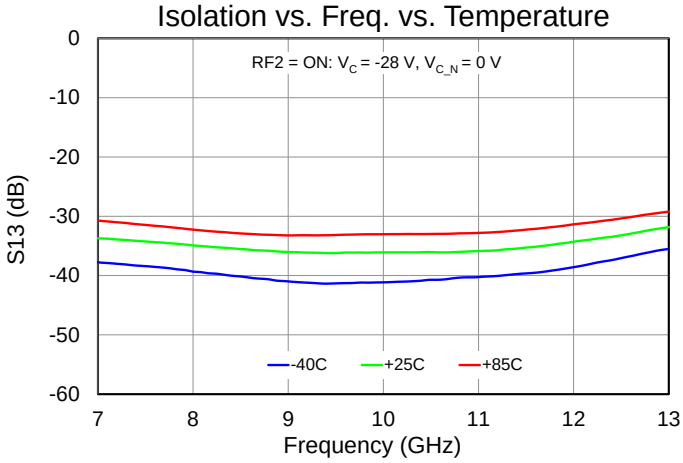
IRL (Common Port) vs. Freq. vs. Temp.



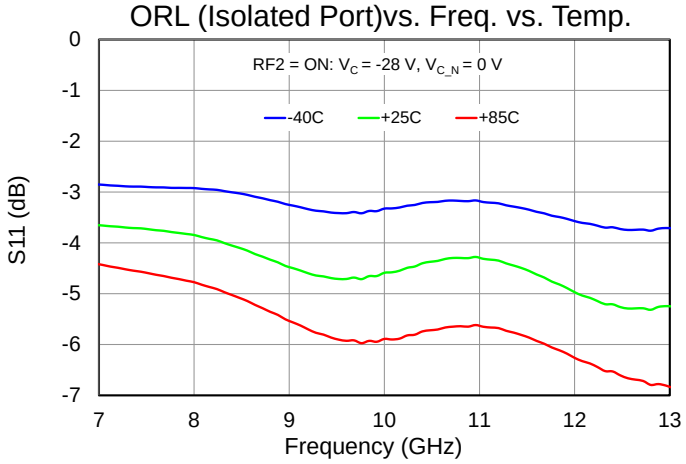
ORL vs. Freq. vs. Temperature



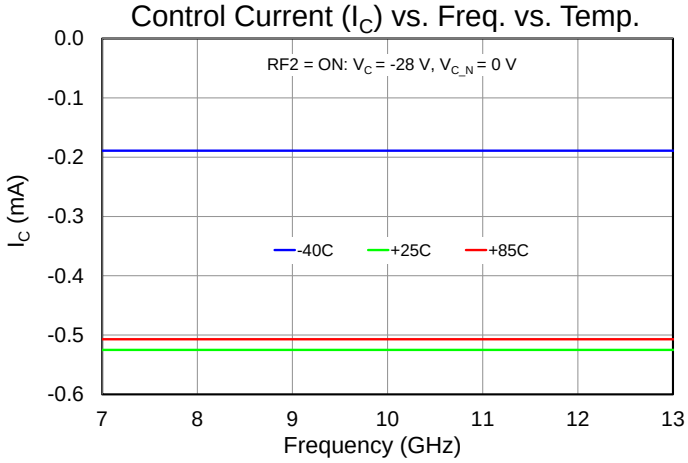
Isolation vs. Freq. vs. Temperature



ORL (Isolated Port)vs. Freq. vs. Temp.



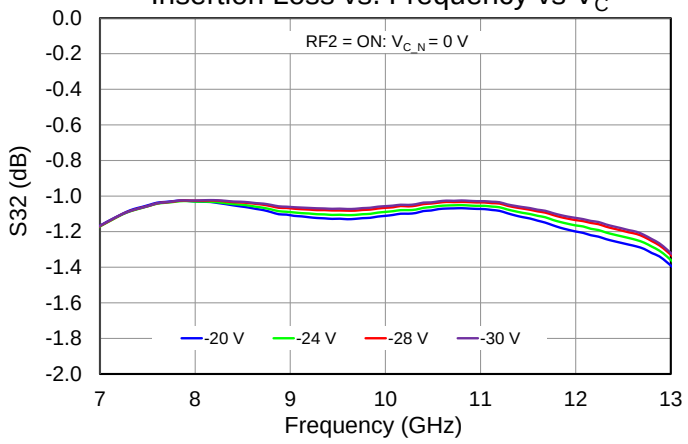
Control Current (I_C) vs. Freq. vs. Temp.



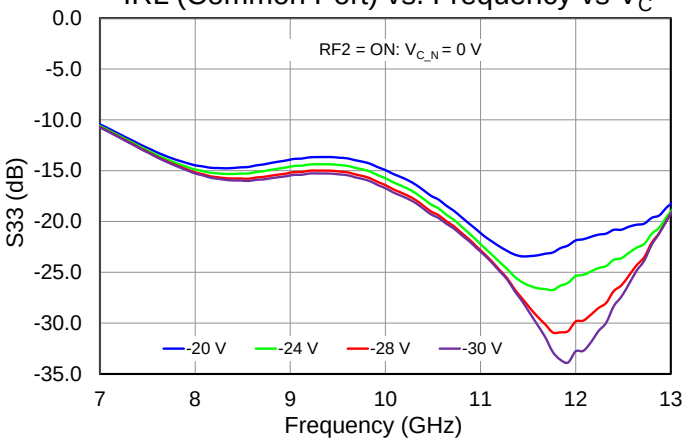
Performance Plots – Small Signal (RF2 Port)

Notes: RFC = Port 3; RF1 = Port 1; RF2 = Port 2

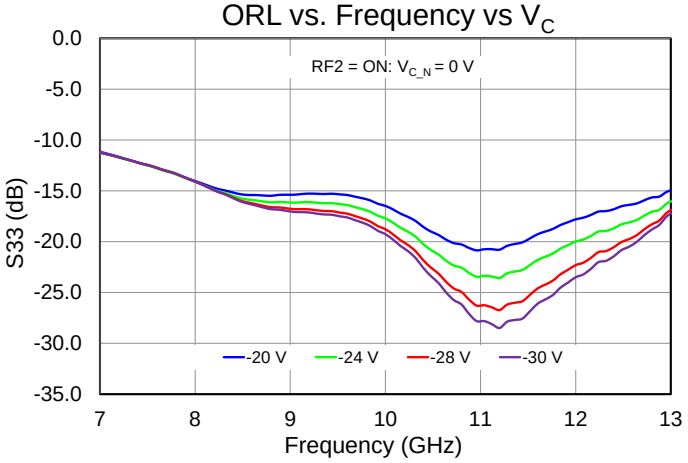
Insertion Loss vs. Frequency vs V_C



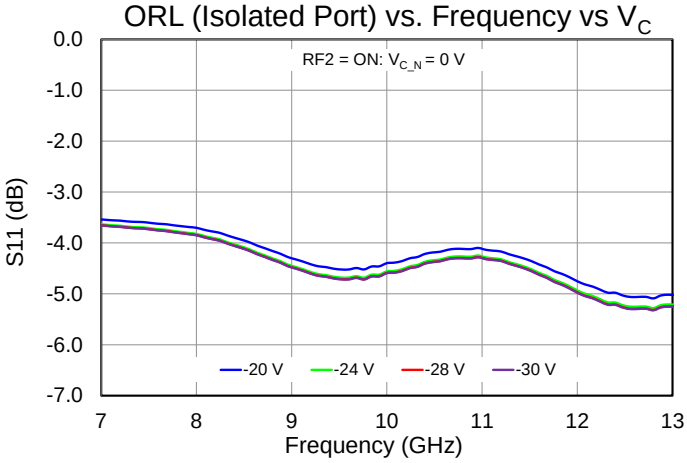
IRL (Common Port) vs. Frequency vs V_C



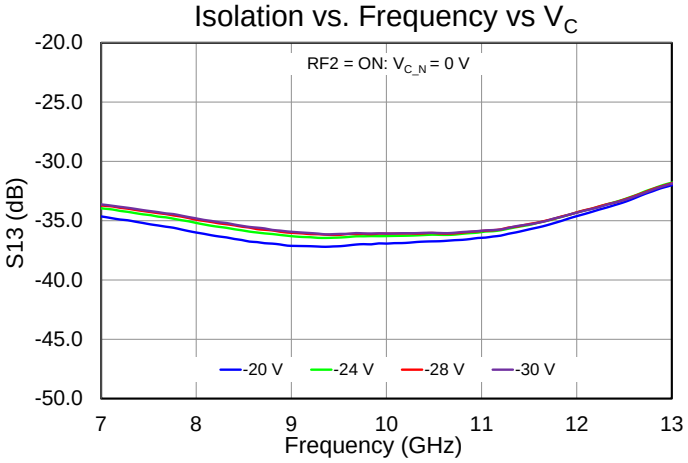
ORL vs. Frequency vs V_C



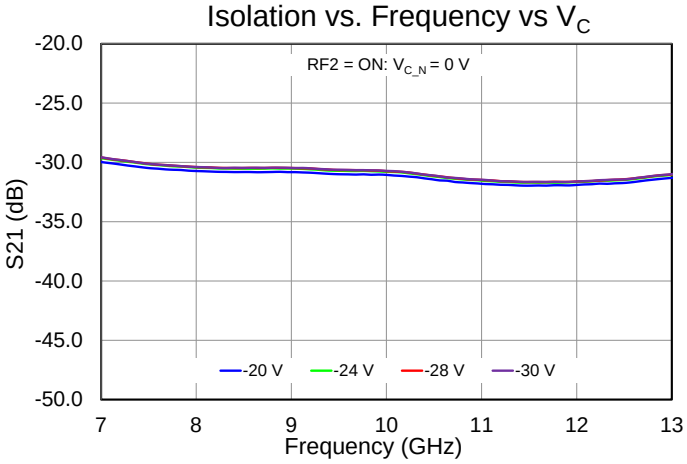
ORL (Isolated Port) vs. Frequency vs V_C



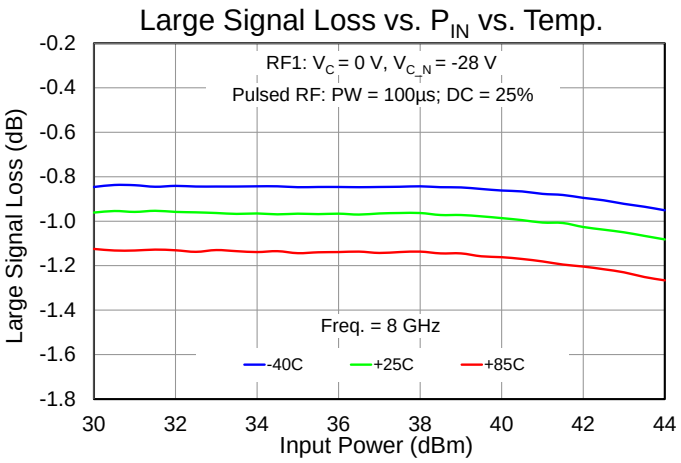
Isolation vs. Frequency vs V_C

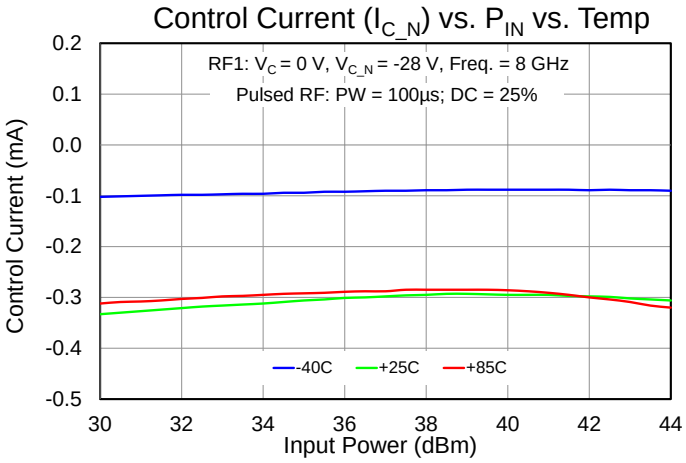


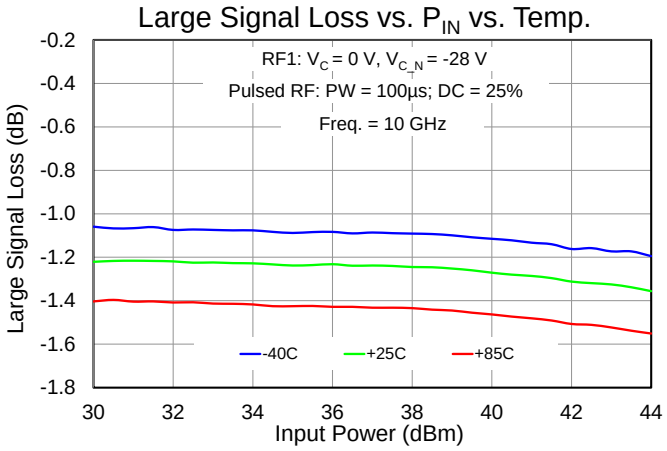
Isolation vs. Frequency vs V_C

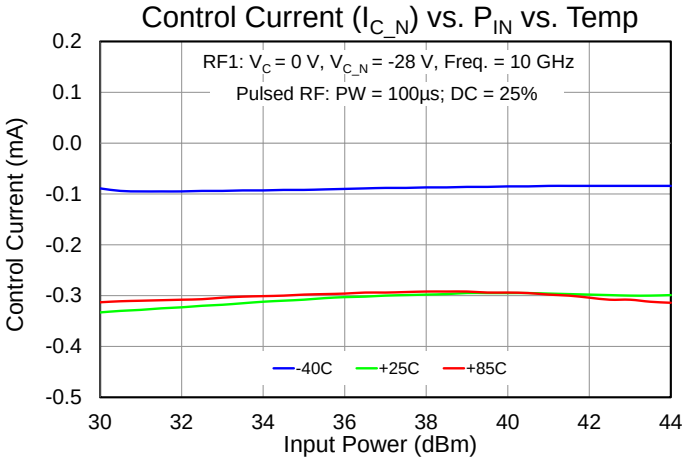


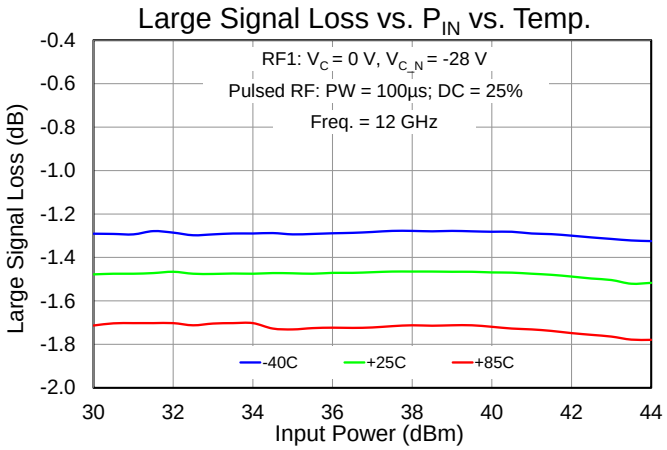
Performance Plots – Compression (Pulsed) RF1 Port

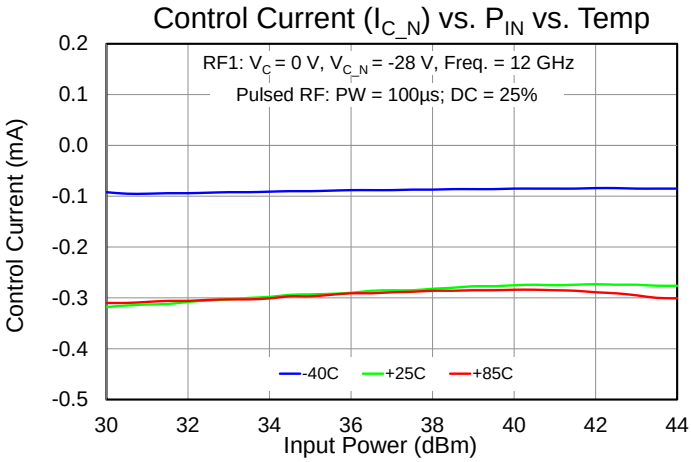




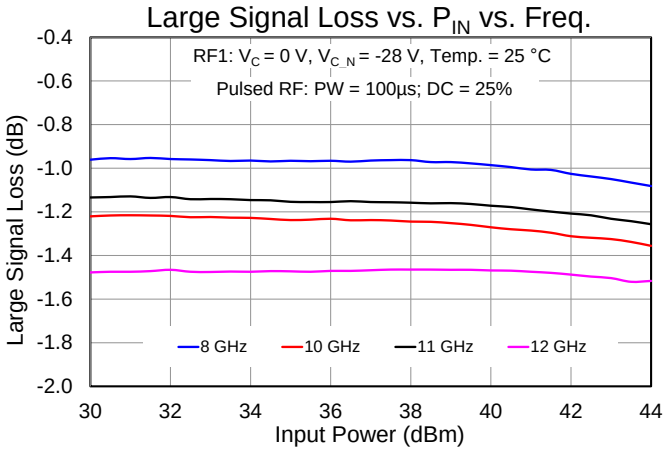


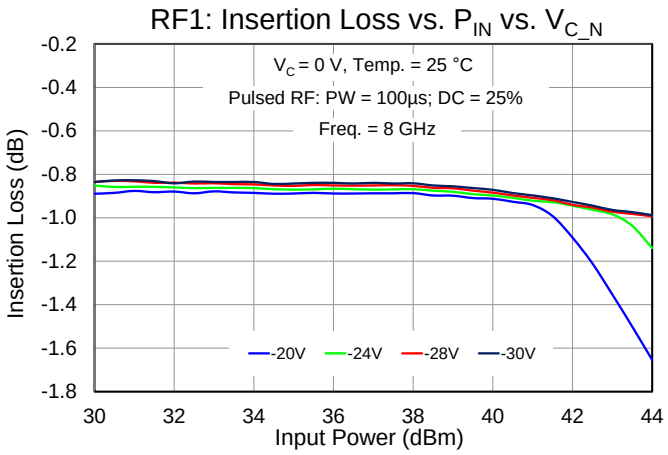


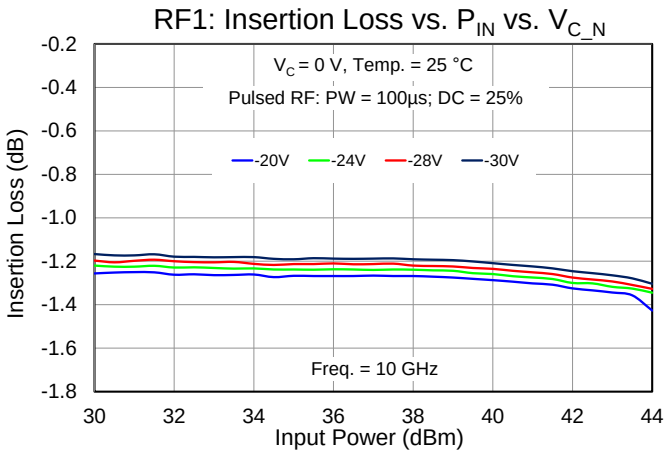


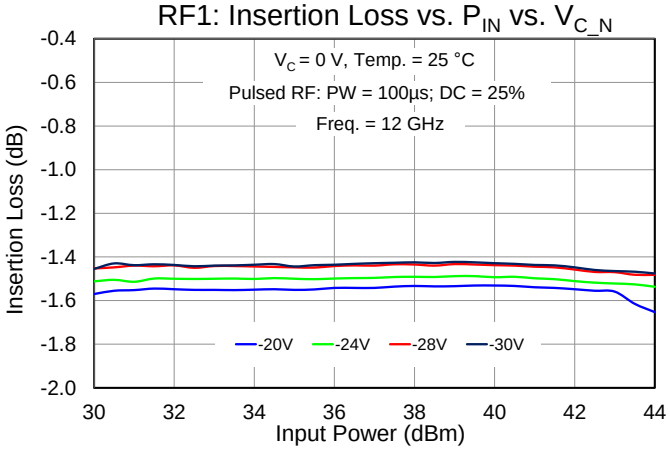


Performance Plots – Compression (Pulsed) RF1 Port

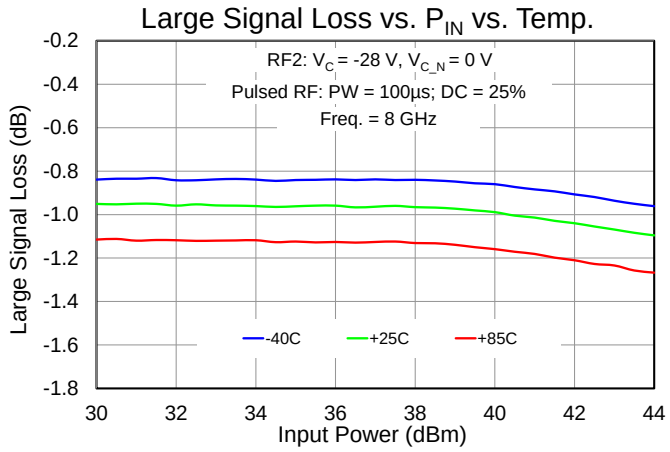


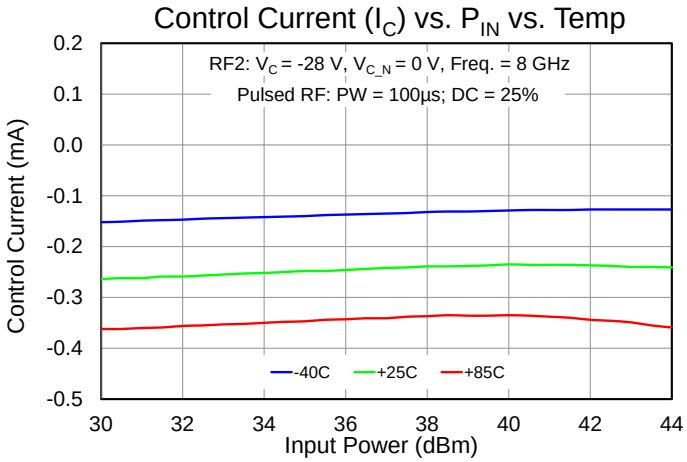


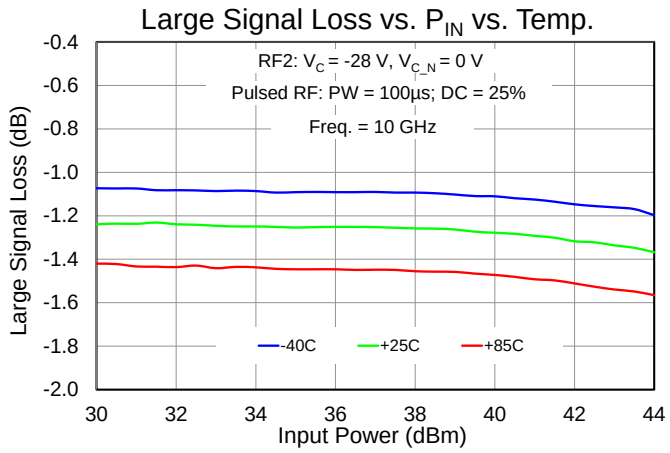


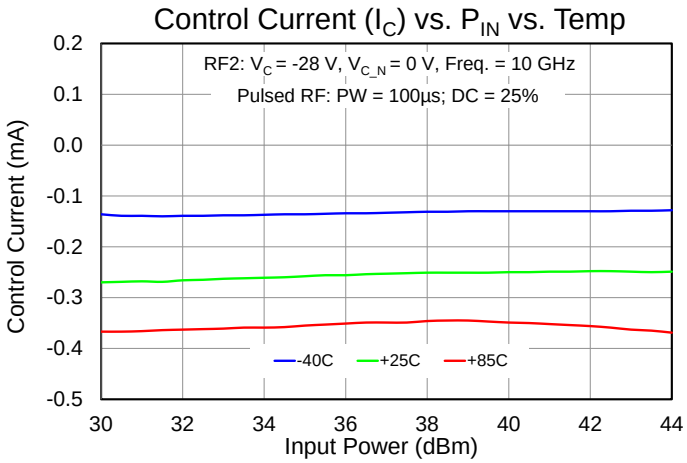


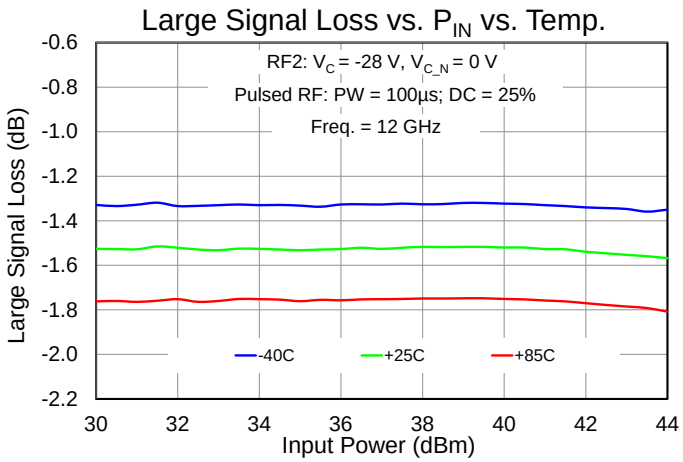
Performance Plots – Compression (Pulsed) RF2 Port

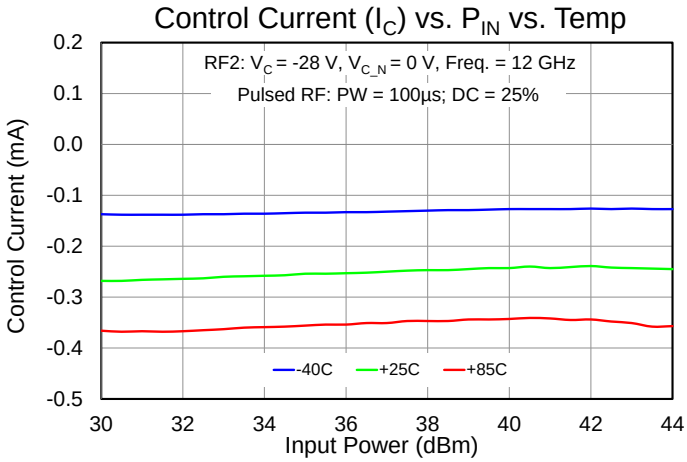




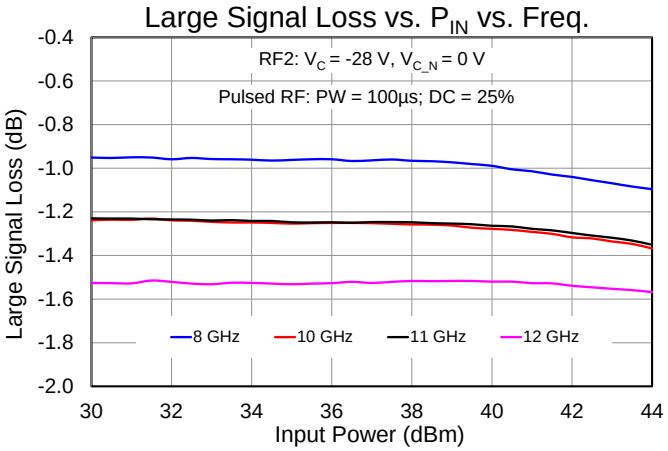


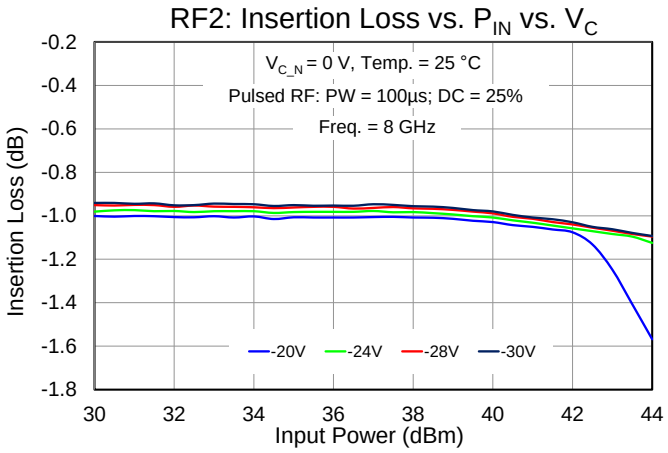


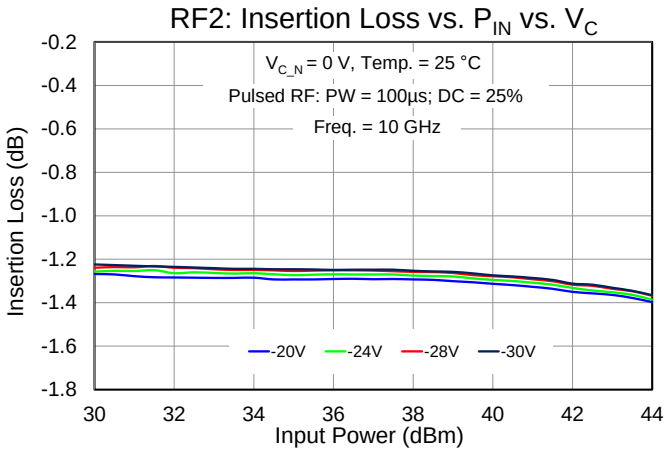


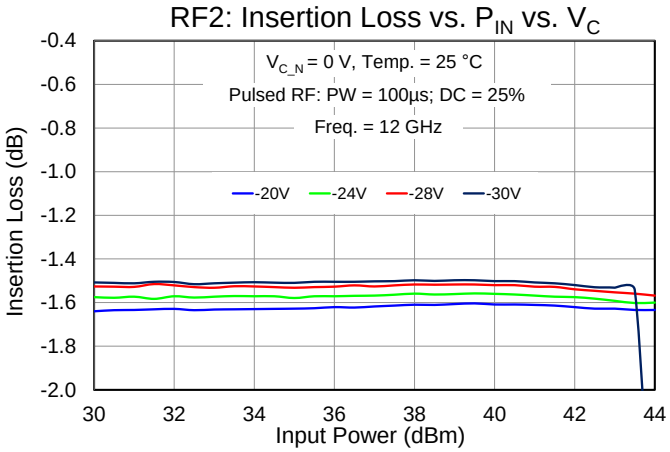


Performance Plots – Compression (Pulsed) RF2 Port

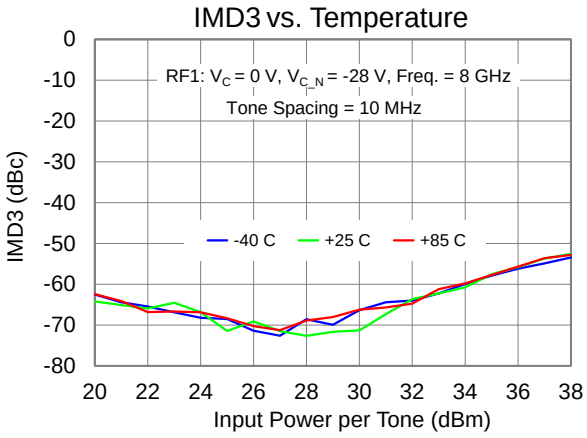


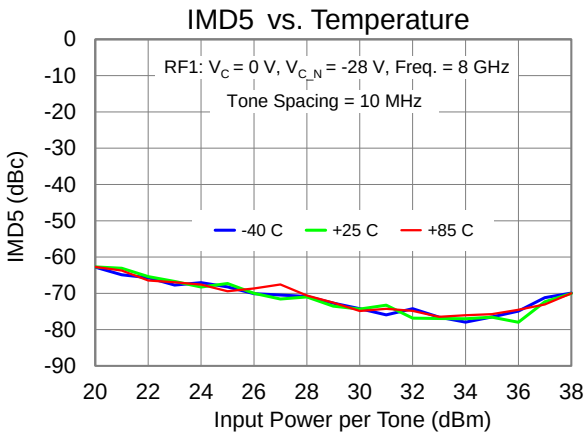


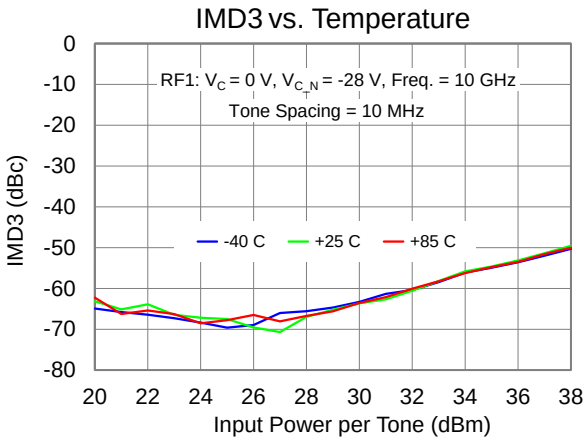


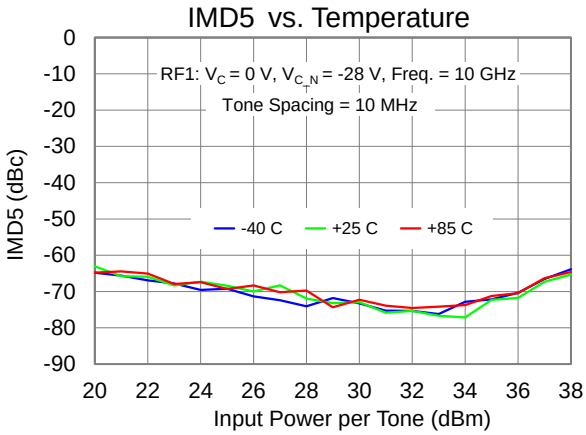


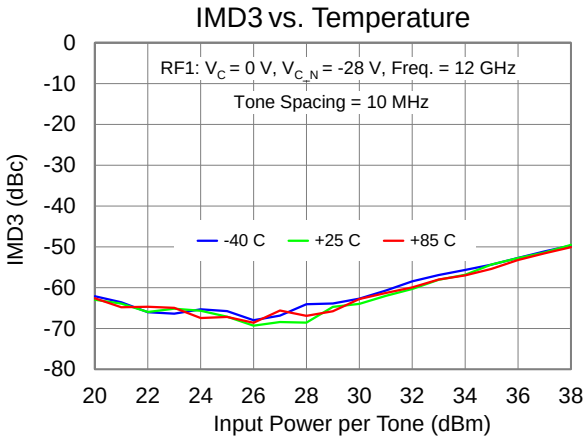
Performance Plots – Linearity

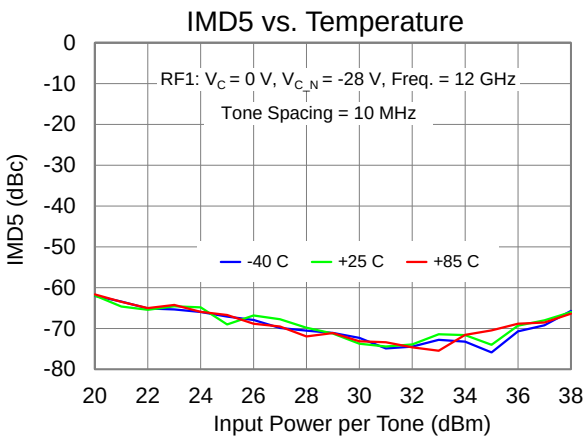




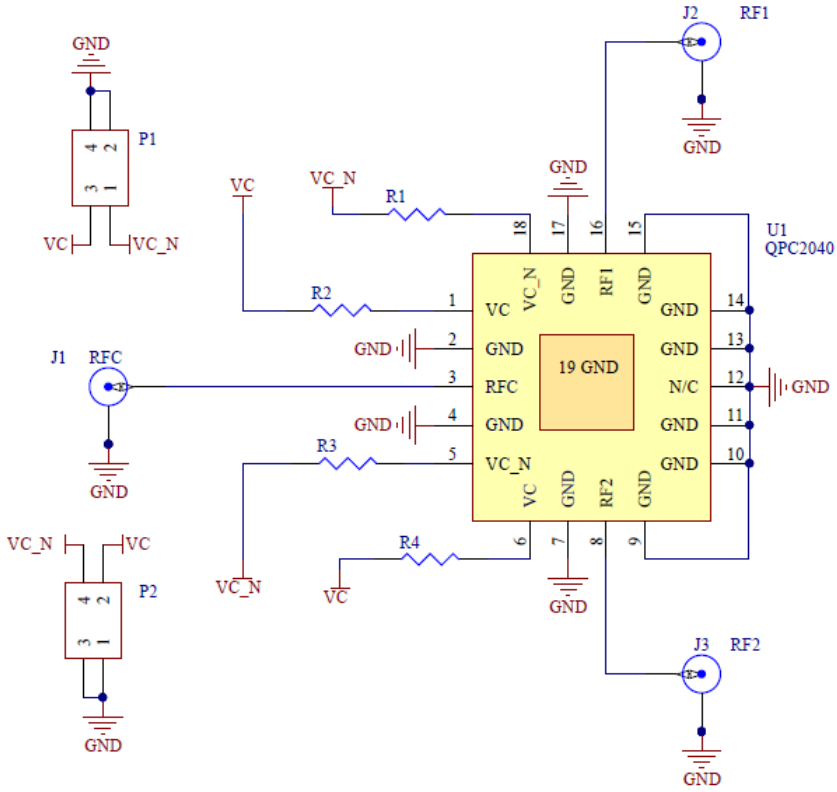








Application Circuit



Notes:

1. This switch can be configured as a Single Pole, Single Throw (SPST) by terminating one unused RF switched port with a 50 Ohm load.
2. V_C can be biased from either pin 1 or 6 and the non-biased pin can be left open.
3. V_{C_N} can be biased from either pin 5 or 18 and the non-biased pin can be left open.
4. External components are not required

Bias Up Procedure

1. V_C or V_{C_N} set to 0 V (see Function Table for RF Path)
2. V_{C_N} or V_C set to -28 V (see Function Table for RF Path)
3. Apply RF signal to RF Input

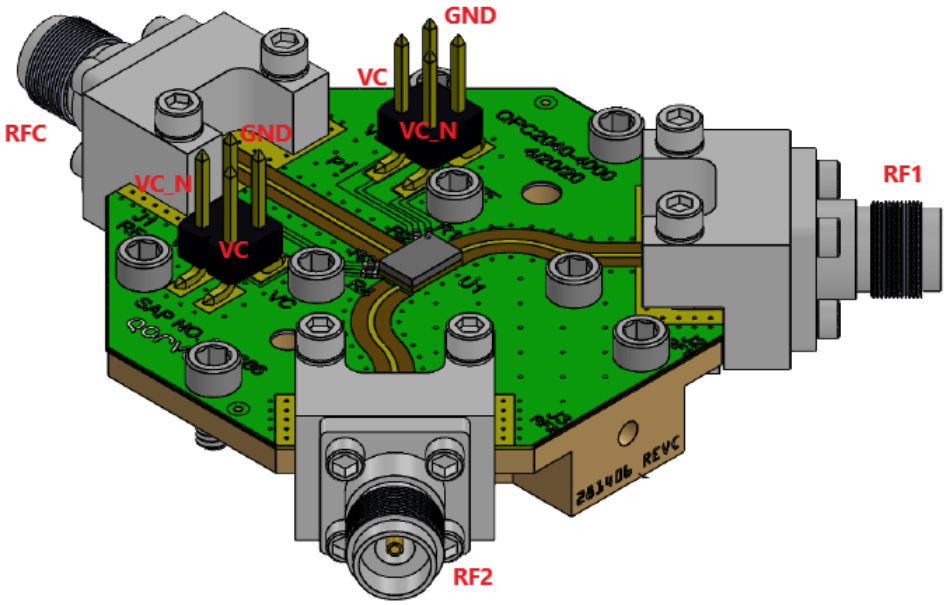
Bias Up Down

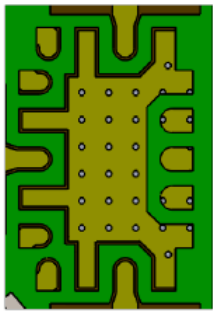
1. Turn off RF supply
2. Turn V_{C_N} or V_C to 0 V
3. Turn V_C or V_{C_N} to 0 V

Function Table

RF Path	State	V_C	V_{C_N}
RFC to RF1 ON	On-State (Insertion Loss)	0 V	−28 V
	Off-State (Isolation)	−28 V	0 V
RFC to RF2 ON	On-State (Insertion Loss)	−28 V	0 V
	Off-State (Isolation)	0 V	−28 V

Evaluation Board (EVB) Assembly Layout.





MOUNTING DETAIL

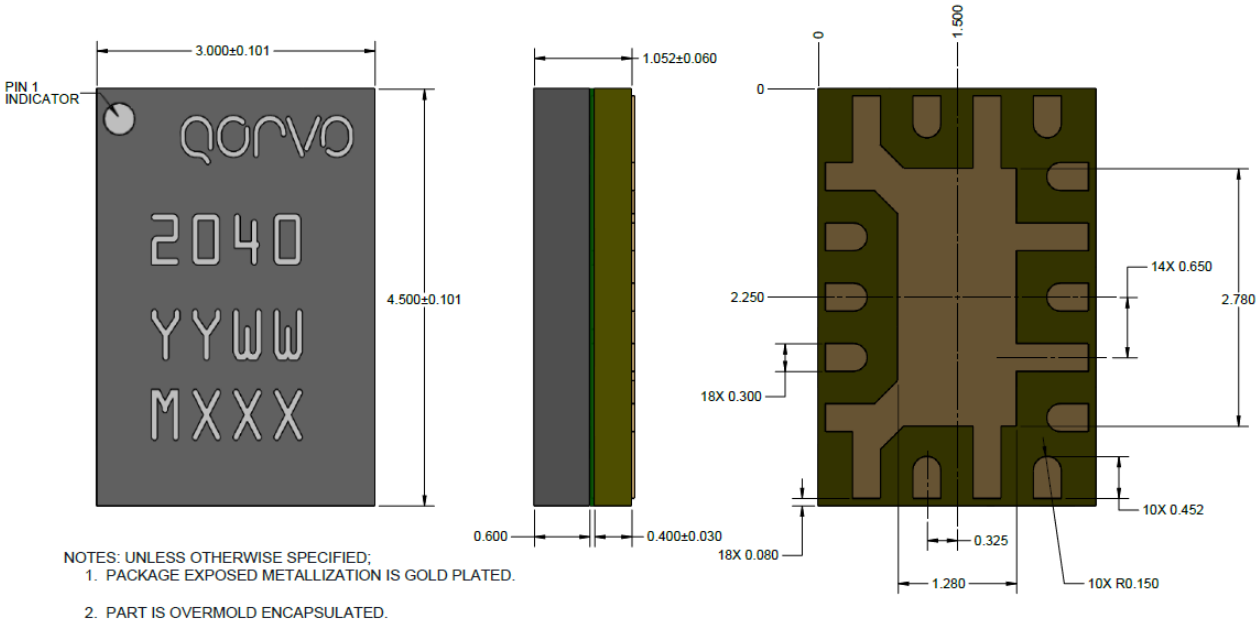
Notes:

1. This switch can be configured as a Single Pole, Single Throw (SPST) by terminating one unused RF switched port with a 50 Ohm load.
2. V_C can be biased from either top or bottom pin and the non-biased pin can be left open.
3. V_{C_N} can be biased from either top or bottom pin and the non-biased pin can be left open.
4. External components are required

Bill of Materials for EVB – QPC2040

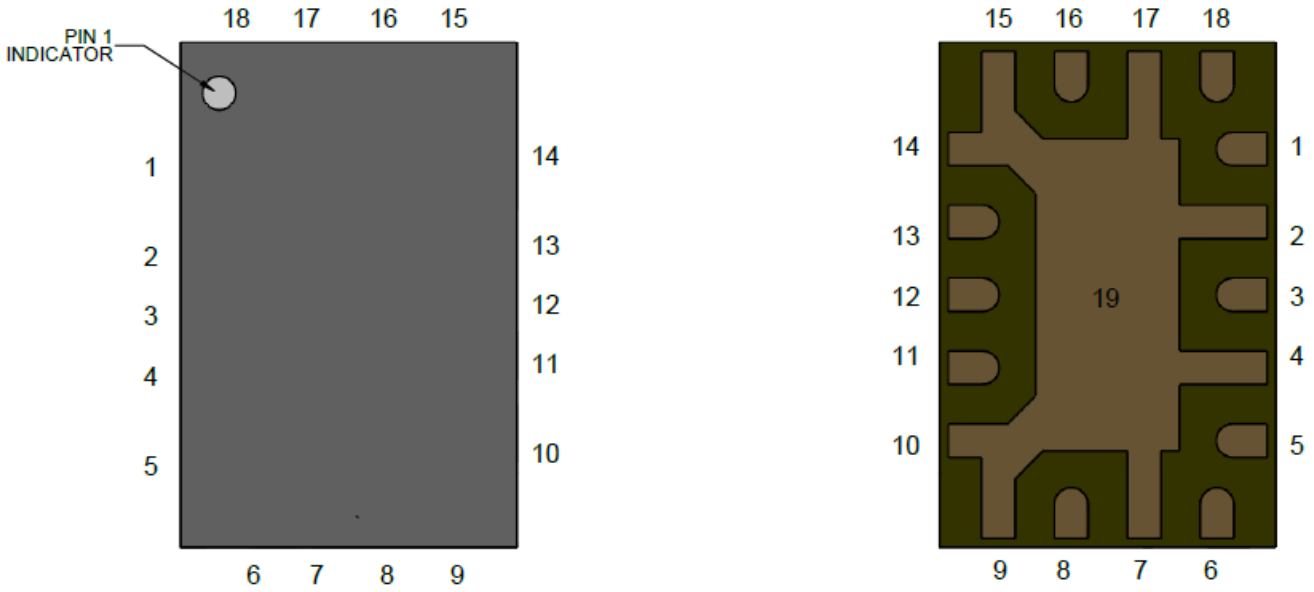
Reference Des.	Value	Description	Manuf.	Part Number
R1, R2, R3, R4	1.1 KΩ	RES, 0402, 1%, 1/10 W	Various	–

Mechanical Information



Units: millimeters
Tolerances: unless specified
x.xx = ± 0.25
x.xxx = ± 0.100
Materials:
Base: Laminate
Packaged Exposed Metallization is gold plated
Marking:
QPC2040: Part Number
YY: Part Assembly Year
WW: Part Assembly Week
MXXX: Batch ID

Package Layout



Pin Description

Pad No.	Symbol	Description
1, 6	V_C	Control voltage #1; External components are required
2, 4, 7, 9-11, 13-15, 17	GND	Ground. Connected to GND paddle (pin 19); should be grounded on PCB to improve isolation
3	RFC	RF common port (port 3); matched to 50 Ω; DC coupled
5, 18	V_{C_N}	Control voltage #2; External components are required
8	RF2	RF switched port 2; matched to 50 Ω; DC coupled
12	N/C	Not connected internally. Recommended to be grounded at EVB level
16	RF1	RF switched port 1; matched to 50 Ω; DC coupled
19	GND	Backside Paddle. Multiple vias should be employed to minimize inductance and thermal resistance.

Assembly Notes

1. Compatible with the latest version of J-STD-020, lead-free solder, 260° C, and tin/lead (245°C max. reflow temp.) soldering processes.
2. Contact plating: Thin Ni ENEPIG

Recommended Soldering Profile