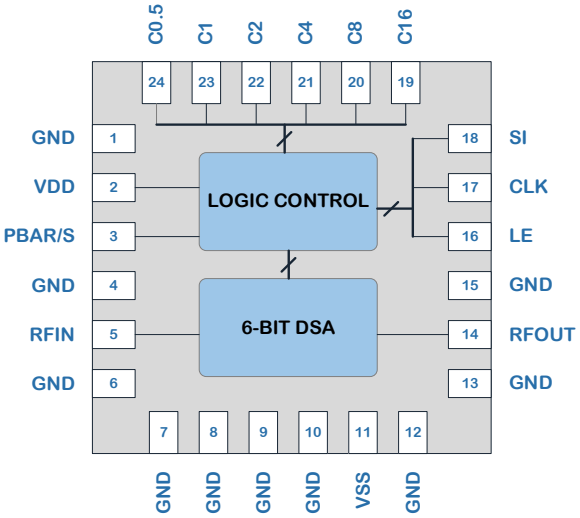
QPC3624

75Ω 47–2000 MHz Digital Step Attenuator

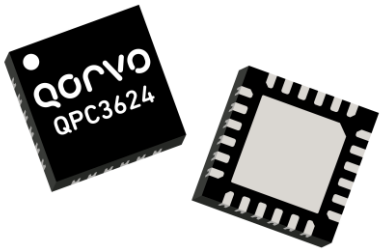
Product Overview

The QPC3624 is a 75Ω 6-bit digital step attenuator (DSA) that features high linearity over the entire 31.5 dB gain control range in 0.5 dB steps and has a low insertion loss of 1.2 dB at 1 GHz. The QPC3624 features three modes of control: serial, latched parallel, and direct parallel programming. Patented circuit architecture provides overshoot-free transient switching performance. The QPC3624 is available in a 24-pad 4mm x 4mm x 0.90 mm QFN package.

Functional Block Diagram



Top View



24 Pad 4 x 4 mm QFN Package

Key Features

- 6-Bit, 31.5 dB Range, 0.5 dB Step
- Patented Circuit Architecture
- Overshoot-free Transient Switching Performance
- Frequency Range 47 MHz to 2000 MHz
- High Linearity, IIP3 55dBm Typical
- Serial and Parallel Control Interface
- Fast Switching Speed, <250 nsec Typical
- RF Pads Have No DC Voltage, Can be DC Grounded Externally
- Option to Turn Off Negative Voltage Generator and Supply V_{SS} Externally
- Power-up Default Setting Is Maximum Attenuation

Applications

- Optical Nodes
- Point-to-Point
- MDU Amplifiers
- Pre-amplifier Attenuation
- Inter-stage Attenuation
- Return Attenuation
- AGC

Ordering Information

Part No.	Description
QPC3624SQ	Sample bag with 25 pieces
QPC3624SR	7" Reel with 100 pieces
QPC3624TR13	13" Reel with 2500 pieces
QPC3624PCK	47 – 2000 MHz PCBA with 5 pc. sample bag

Absolute Maximum Ratings

Parameter	Rating
Supply Voltage (V_{DD})	-0.5 to + 6.0 V
Supply Voltage (V_{SS})	-6.0 to + 0.5 V
All Other DC and Logic Pads (Supply Voltage Must Be Applied Prior to Any Other Pin Voltage)	-0.5 to VDD
Maximum Input Power at RFIN Pad at 85 °C Case Temperature	+30 dBm
Maximum Input Power at RFOUT Pad at 85 °C Case Temperature	+27 dBm
Storage Temperature Range	−65 to +150 °C

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Supply Voltage, V_{DD}	+2.7	+5.0	+5.5	V
Supply Voltage, V_{SS}	−5.5	−5.0	−4.5	V
Temperature Range	−40		+85	°C
Junction Temperature			+125	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

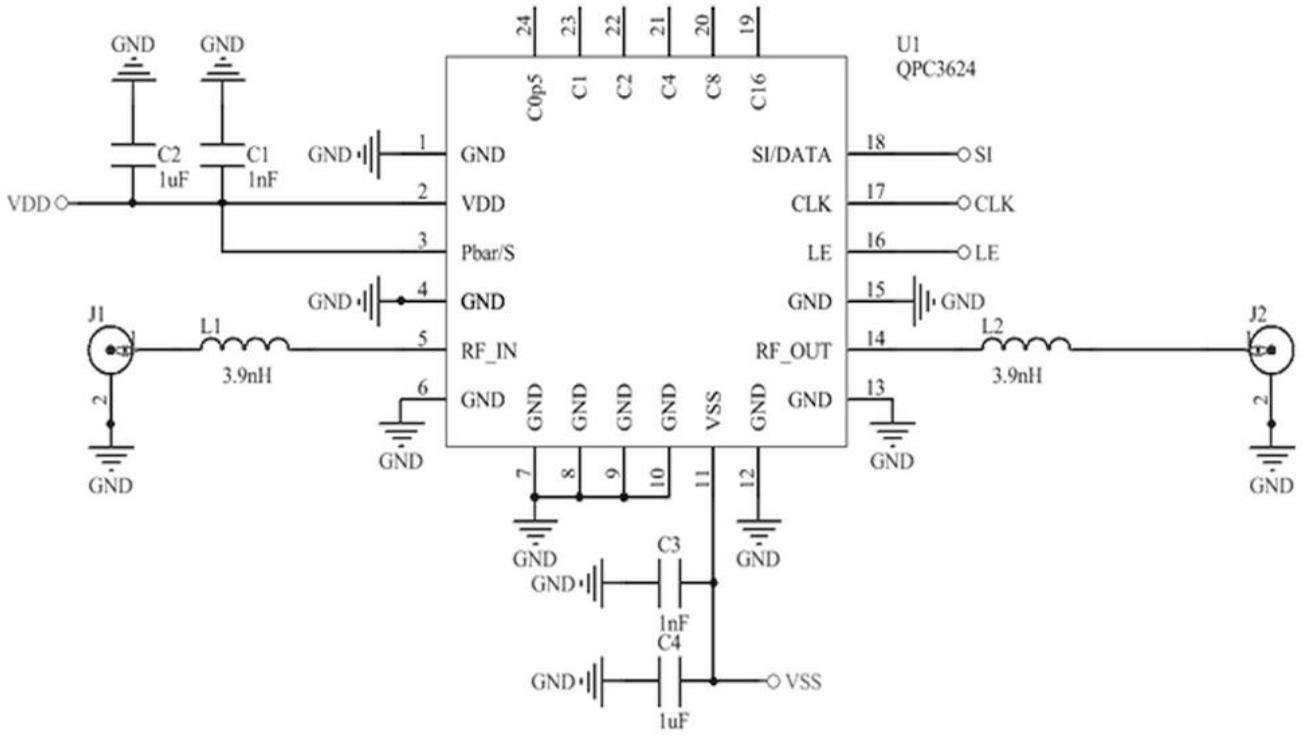
Electrical Specifications

Parameter	Condition [1]	Min	Typ	Max	Unit
Supply Current (I_{DD})	Steady state operation, current draw during attenuation state transitions is higher.		190		µA
Supply Current (I_{SS})	Steady state operation, current draw during attenuation state transitions is higher.		105		µA
Frequency Range		47		2000	MHz
Insertion Loss	1GHz		1.2		
Maximum Attenuation			31.5		dB
Absolute Attenuation Error			±(0.2 + 4%)		dB
Input IP3	47MHz, Two tones, 13dBm/tone		55		dBm
Input P0.1dB[2]			>30		dBm
CSO	130 Channel, Flat Tilt, +42 dBmV/ch, 0dB Atten		-80		dBc
CTB	130 Channel, Flat Tilt, +42 dBmV/ch, 0dB Atten		<-90		dBc
Return Loss	1GHz		20		dB
Input and Output Impedance			75		Ω
Switching Speed	50% control to 10% / 90% RF		230		nsec
Digital Logic Low				0.63	V
Digital Logic High		1.17			V
Thermal Resistance, θjc	Junction to case		56		°C/W

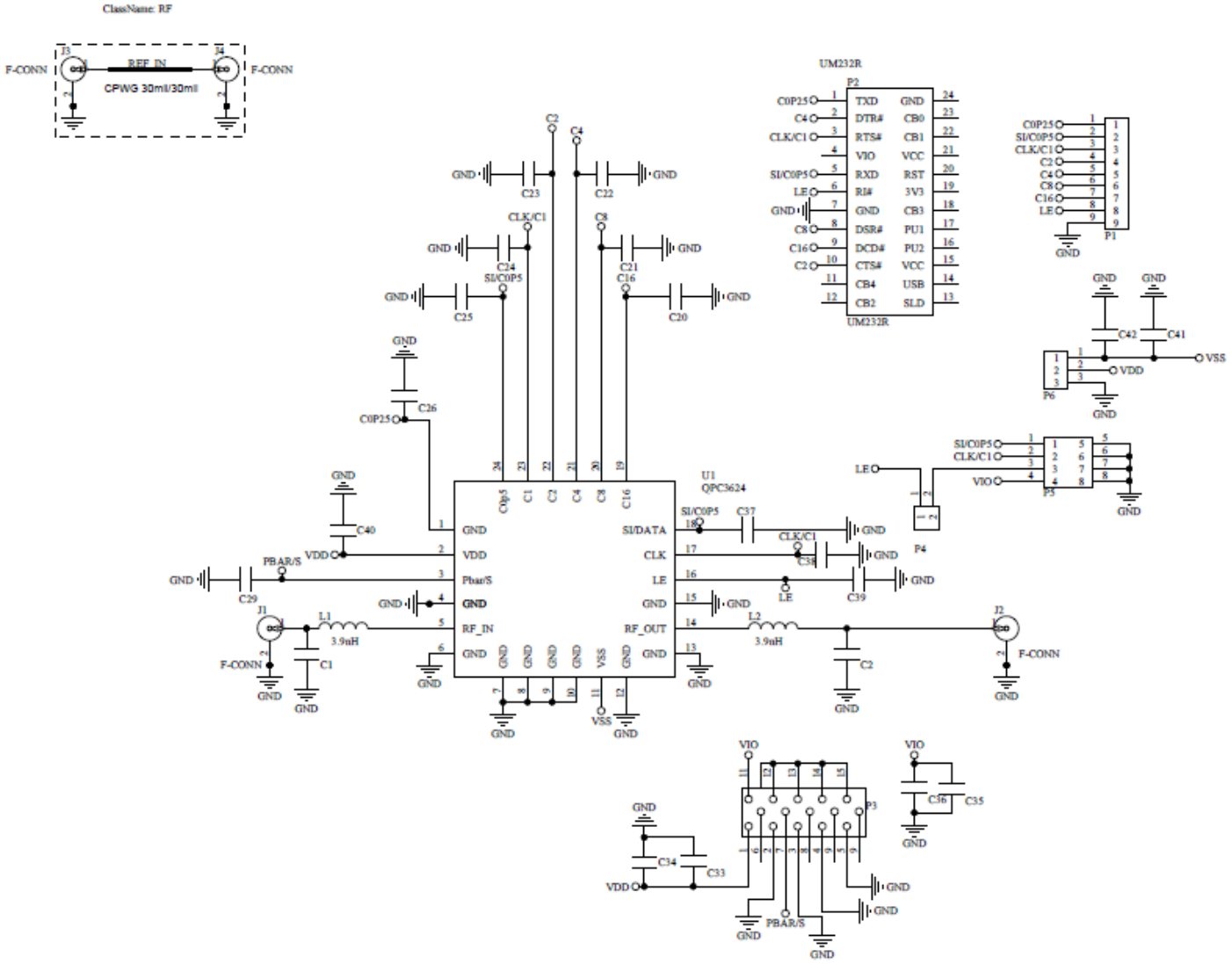
Notes:

1. Typical performance at these conditions: Temp = +25°C, 1000MHz, V_{DD} = +5V, V_{SS} = -5V, 75Ω system.
2. Figure of merit – exceeds maximum input power of device.

Typical Application Schematic – Serial Mode 47–1200 MHz



Evaluation Board Schematic 47–2000 MHz

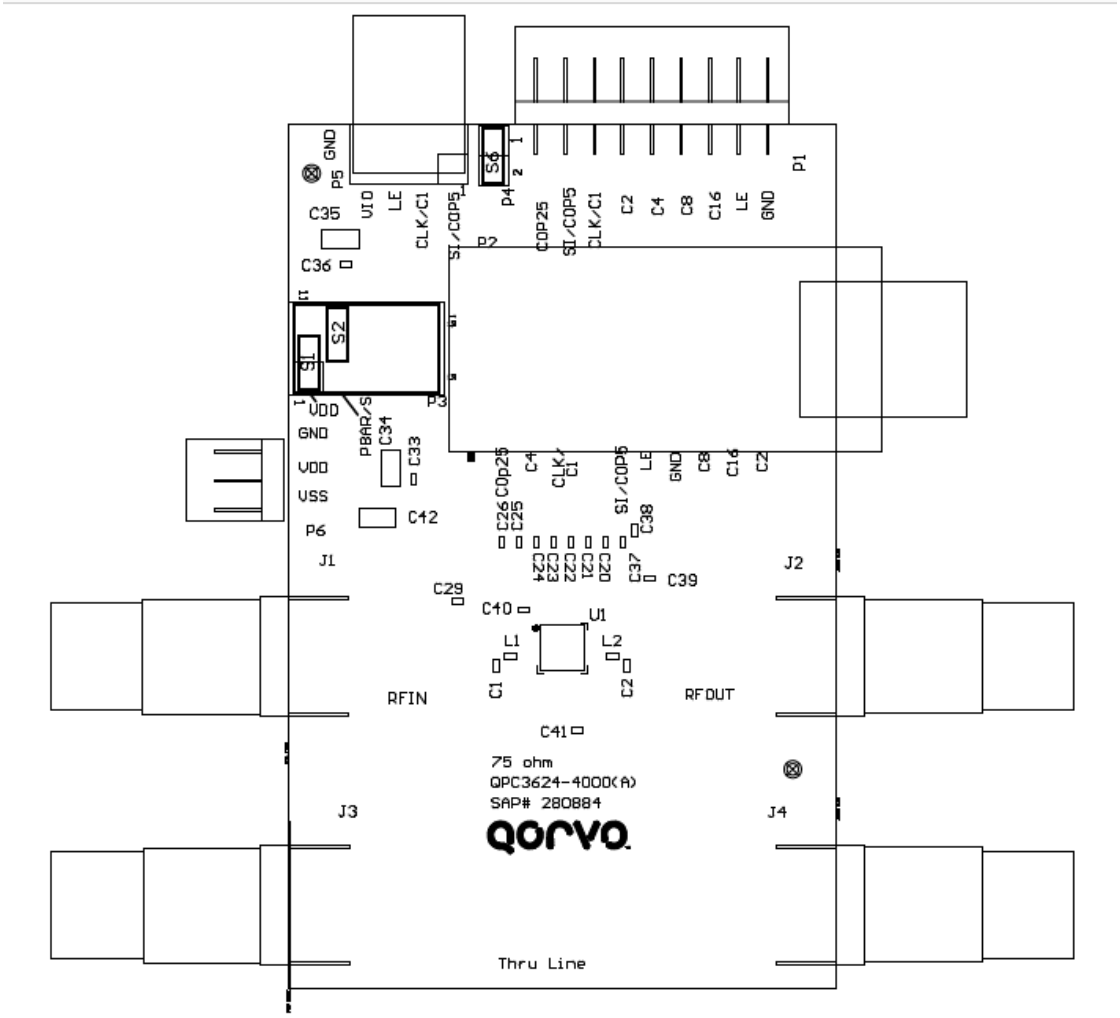


Ref. Designator	Description	Manufacturer	Part Number
PCB	QPC3624–4000	Viasystems	QPC3624-4000(A)
U1	Digital Step Attenuator, 47 MHz to 2000 MHz	Qorvo	QPC3624SB
C34, C42	CAP, 1 µF, 10%, 25 V, X7R, 1206	Taiyo Yuden (USA), Inc.	CE TMK316BJ105KL-T
J1-J4	CONN, F FEM, EDGE MOUNT, 75 Ω, 0.065”	Genesis Technology USA	GT20-300204
P1	CONN, HDR, ST, 9-PIN, 0.100”	Samtec Inc.	TSW-109-07-G-S
P3	CONN, HDR, ST, 3 x 5, 0.100”, T/H	Samtec Inc.	TSW-105-07-L-T
P4	CONN, HDR, ST, 2-PIN, 0.100”	Samtec Inc.	TSW-102-07-G-S
P5	CONN, HDR, 2 x 4, RA, 0.100”, T/H	Samtec Inc.	TSW-104-08-G-D-RA
P2	CONN, SKT, 24-PIN DIP, 0.600”, T/H	Aries Electronics Inc.	24-6518-10
P6	CONN. HDR, SRT, PLRZD, 3-PIN, 0.100”	ITW Pancon	MPSS100-3-C
M1 (See Note 1)	MOD, USB TO SERIAL UART, SSOP-28	Future Technology Devices Int’l	UM232R
S1, S2	JMPR, 2-PIN	3M Interconnect Solutions	929950-00
C40, C41	CAP, 1 nF, 5%, 50 V, C0G, 0402	Murata Electronics	GRM1555C1H102JA01D
L1, L2	IND, 3.9 nH, FILM, 0402, +/- 0.1 nH	Murata Electronics	LQP15MN3N9B02
C1, C2, C5-C13, S6	DNP	N/A	N/A

Notes:

1. M1 should be mounted into P2 with respect to the Pin 1 alignment of M1 and P2.
2. Jumpers S1 and S2 should be installed on P3. Jumper S6 is DNP.

Evaluation Board Assembly Drawing

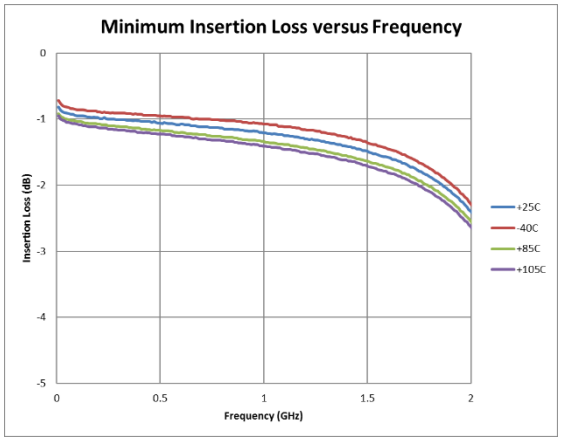


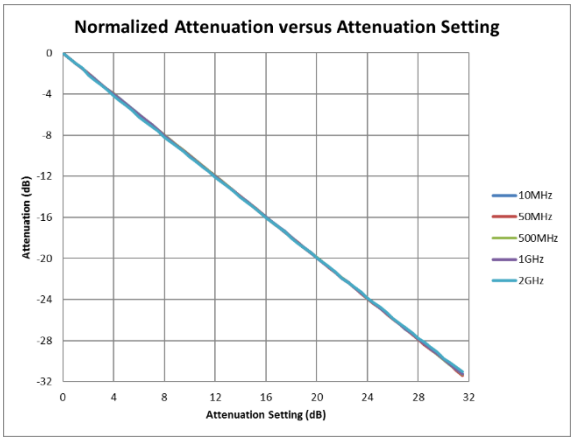
On Board Jumpers

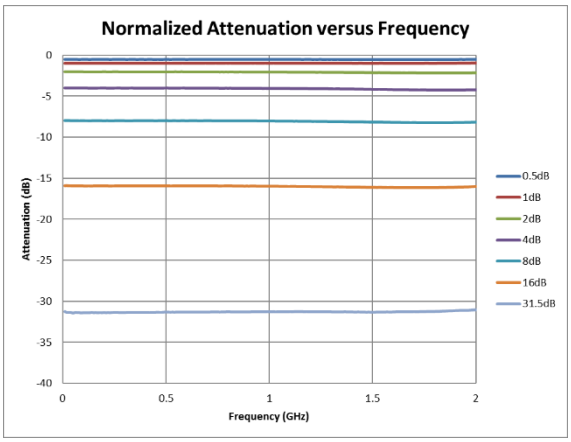
Jumpers	Connector	Signal	Position	U1 Connection	Comment
S1	P3	Logic Voltage	0	VDD (From P6)	
			1	VIO (From P5)	
S2		PBar/S	0	GND	Parallel Mode
			1	U1_VDD	Serial Mode
S6	P4	LE	OPEN	LE (from UM232R)	Only install for external SPI control through P5
			INSTALLED	LE (from P5.3)	

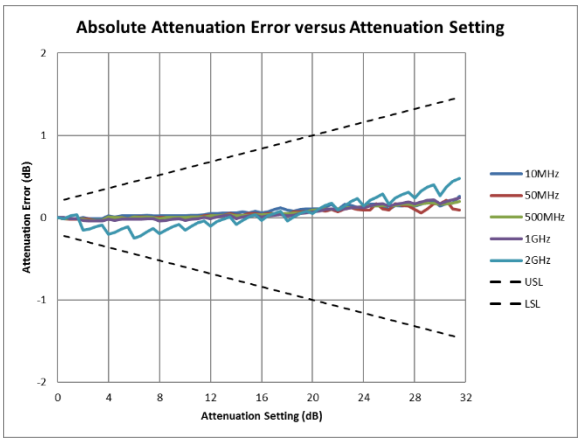
Performance Plots

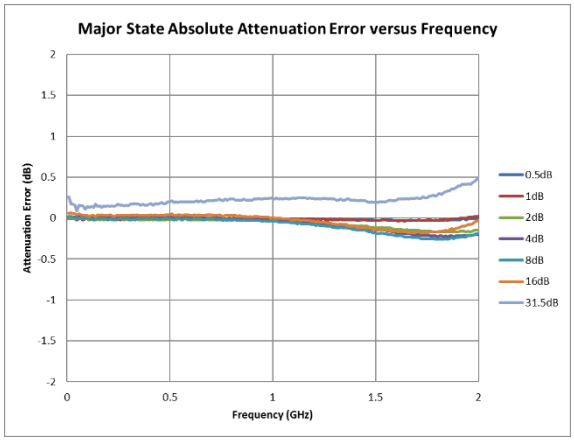
Test conditions unless otherwise noted: V_{DD} =+5 V, V_{SS} = -5V, Temp= +25 °C, Z_o = 75Ω

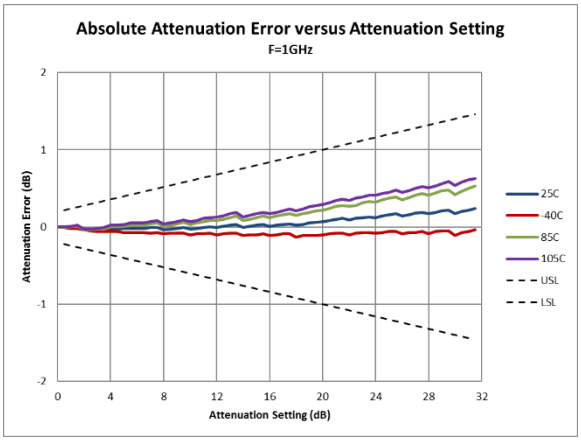






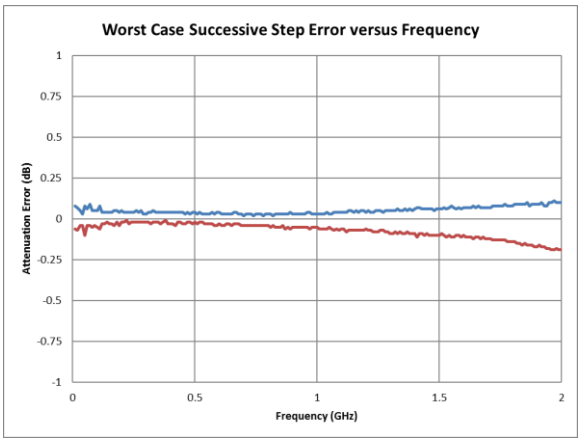


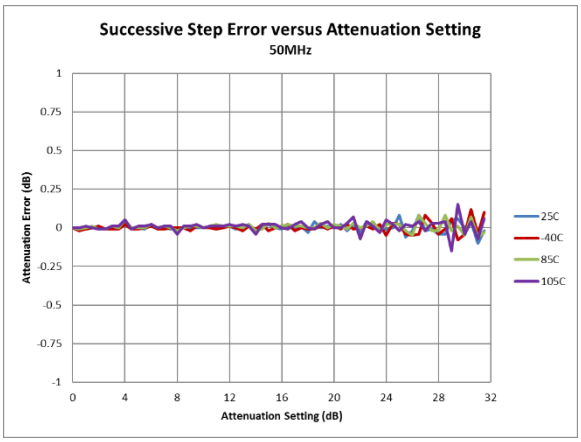


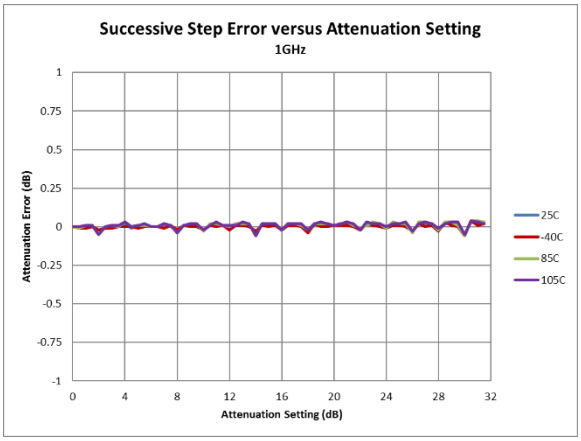


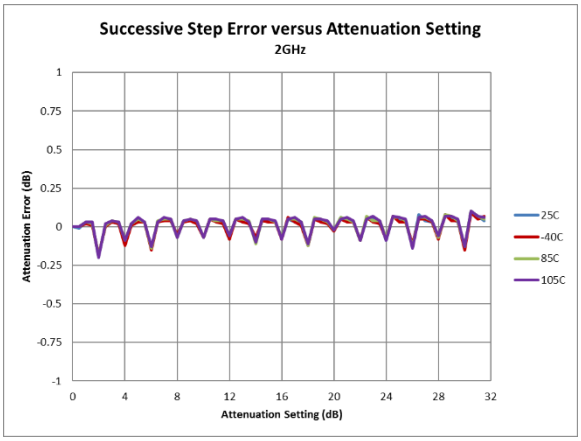
Performance Plots (cont'd.)

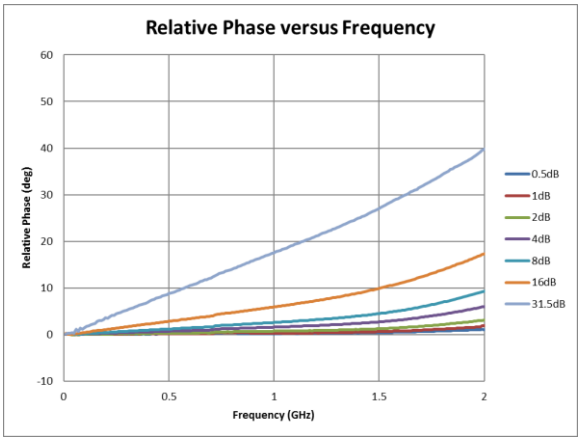
Test conditions unless otherwise noted: V_{DD} =+5 V, V_{SS}= -5V Temp= +25 °C, Z_o = 75Ω

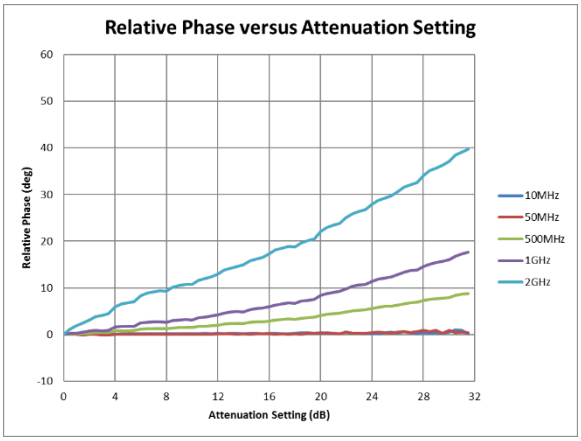






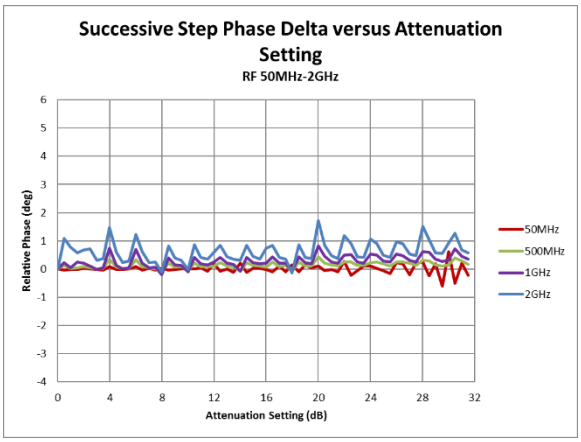


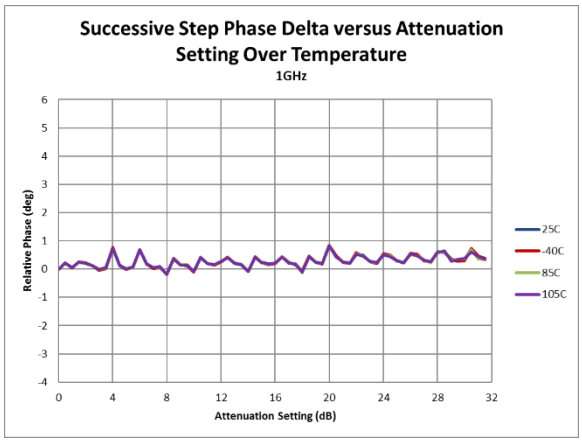


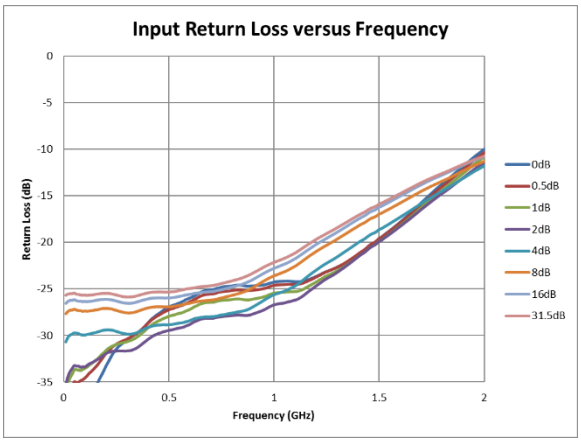


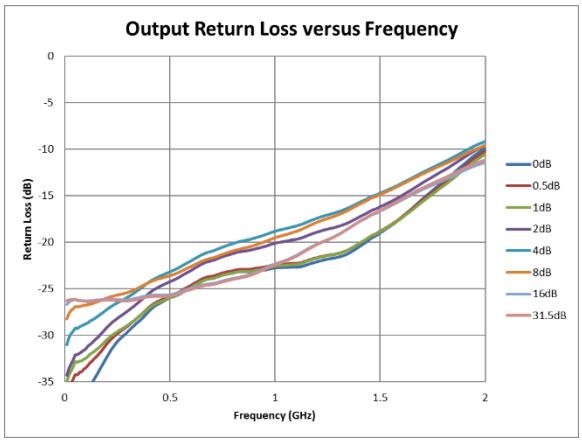
Performance Plots (cont'd.)

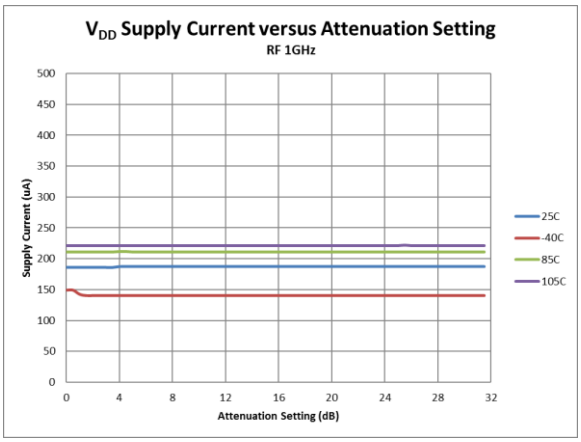
Test conditions unless otherwise noted: V_{DD} =+5 V, V_{SS}= -5V Temp= +25 °C, Z_o = 75Ω

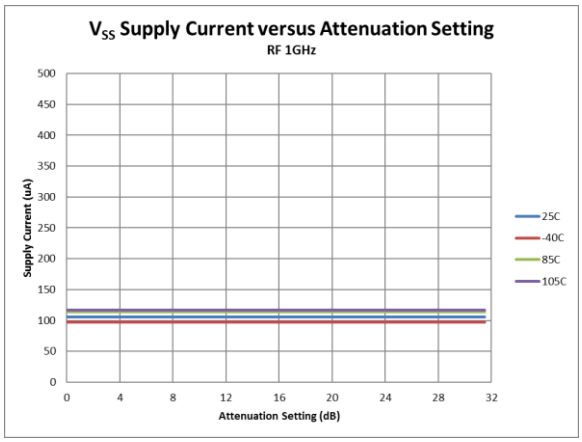






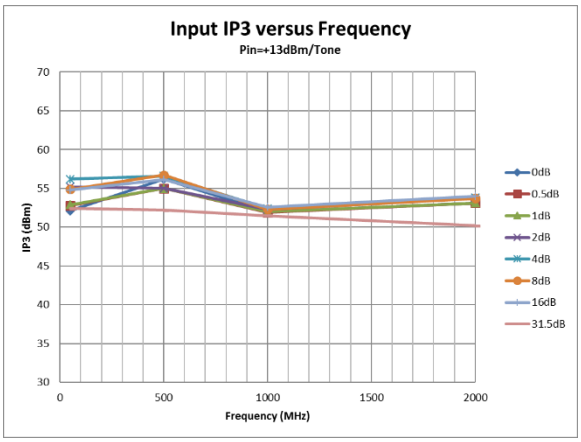


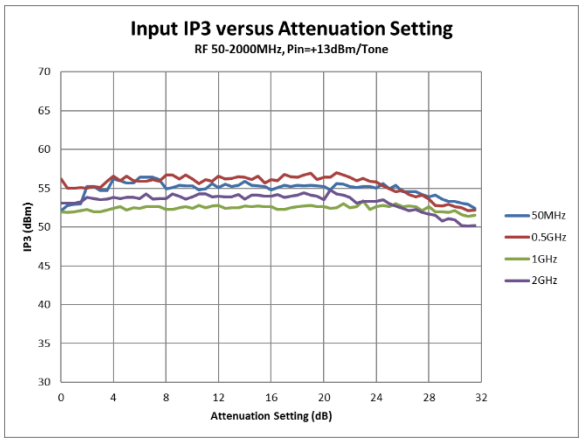


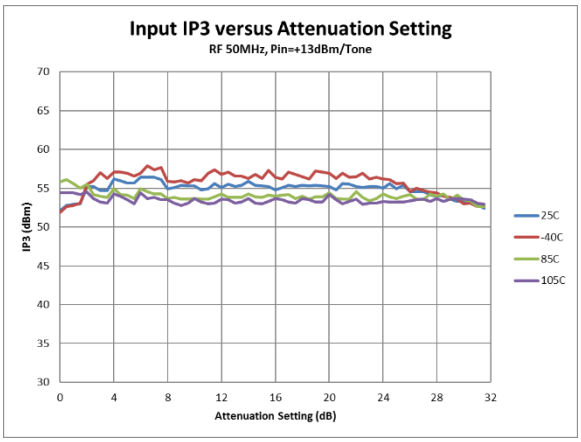


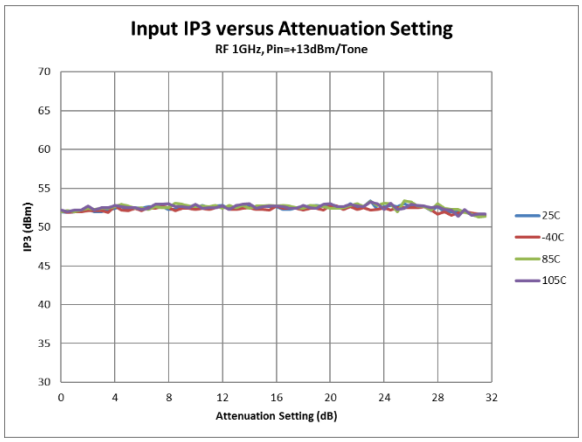
Performance Plots (cont'd.)

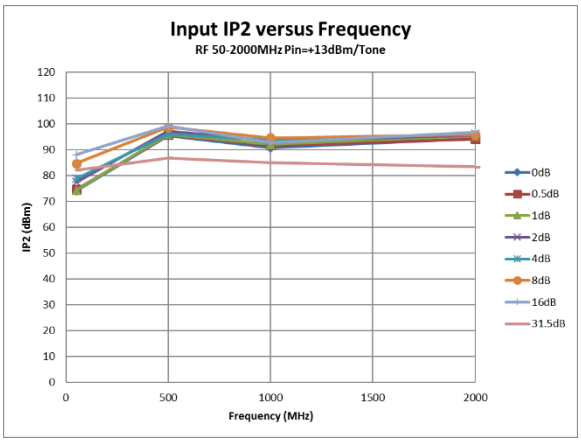
Test conditions unless otherwise noted: V_{DD} =+5 V, V_{SS}= -5V Temp= +25 °C, Z_o = 75Ω

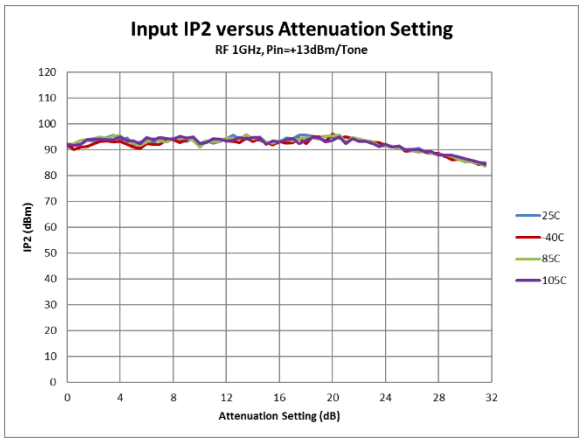






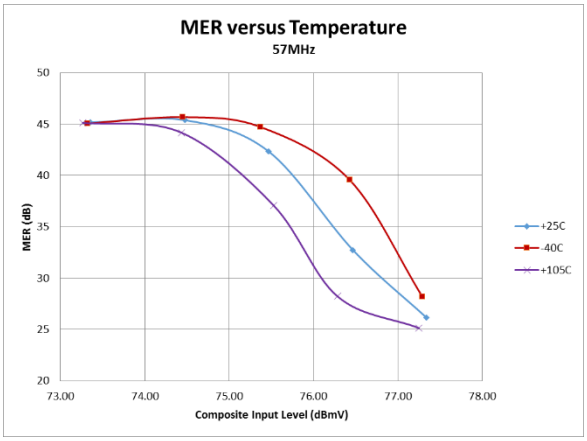


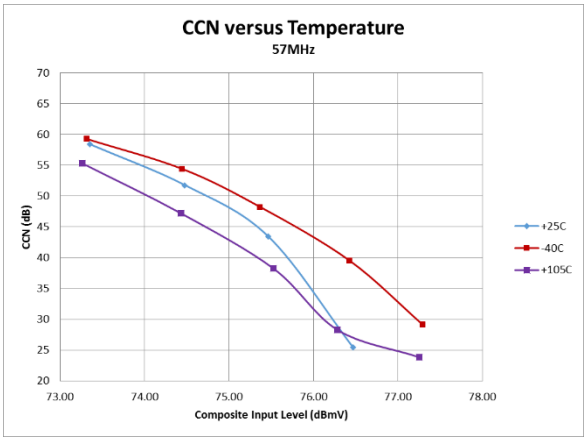


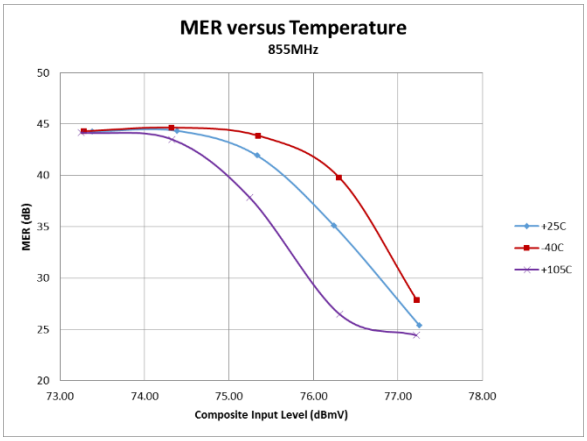


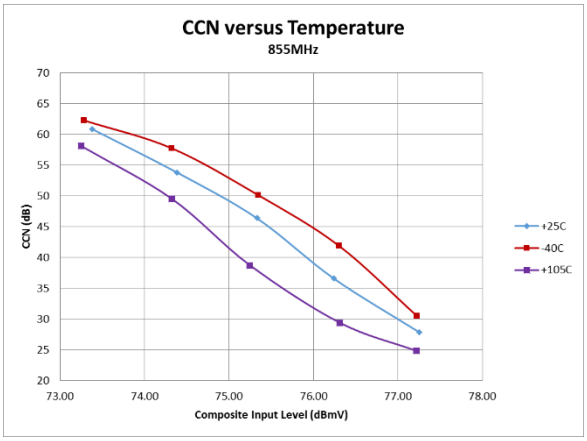
Performance Plots (cont'd.)

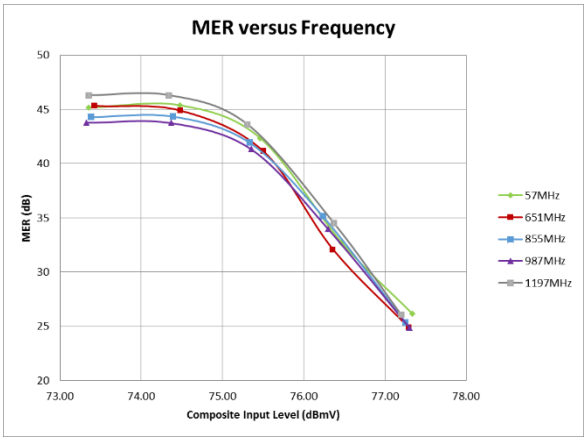
Test conditions unless otherwise noted: V_{DD} =+5 V, V_{SS}= -5V Temp= +25 °C, Z_o = 75Ω

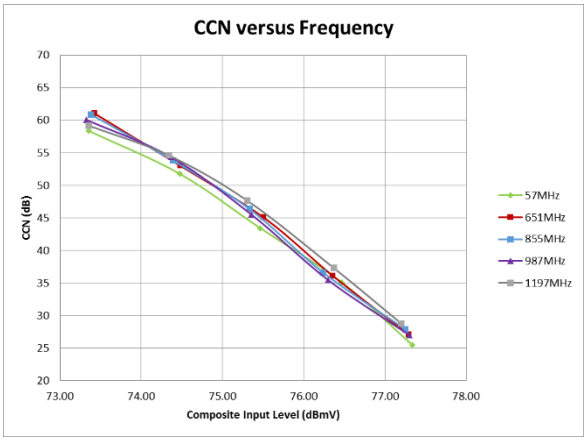












MER/CCN Test Conditions:

1. 190 QAM256 Channels, 57-1215MHz, ITU-T J.83, Annex B
2. CCN test procedure according to ANSI/SCTE 17. System BW 5.36MHz.
3. 0dB Attenuation Setting

Evaluation Board Programming Using USB Interface

Serial Mode
All programming jumpers on the evaluation board are set to the default values indicated in the table. Refer to the Control Bit Generator (CBG) Software Reference Manual for instructions on how to setup the software for use. Apply supply voltage to P6. Select ‘QPC3624’ for serial operation from the parts list of the CBG user interface. Set the attenuation value using the CBG user interface.

Direct Parallel Mode
Evaluation board programming jumper S2 is set to ‘0’. Refer to the Control Bit Generator (CBG) Software Reference Manual for instructions on how to setup the software for use. Apply the supply voltage to P6. Select ‘QPC3624-P’ from the parts list of the CBG user interface. Set the attenuation value using the CBG user interface.

Evaluation Board Programming Using External Bus

Serial Mode
This configuration allows the user to control the attenuator through the P5 connector using an external harness. Remove the USB interface board if it is currently installed on the evaluation board. Connect a user-supplied harness to the P5 connector. Note that the top row of P5 contains the serial bus signals and the bottom row is ground. Programming jumper S2 is set to ‘1’ to select serial mode. Jumper S6 is installed and allows the LE signal to be routed from the P5 connector to the attenuator. Apply the supply voltage to P6. Send the appropriate signals onto the serial bus lines in accordance with the Serial Addressable Mode Timing Diagram.

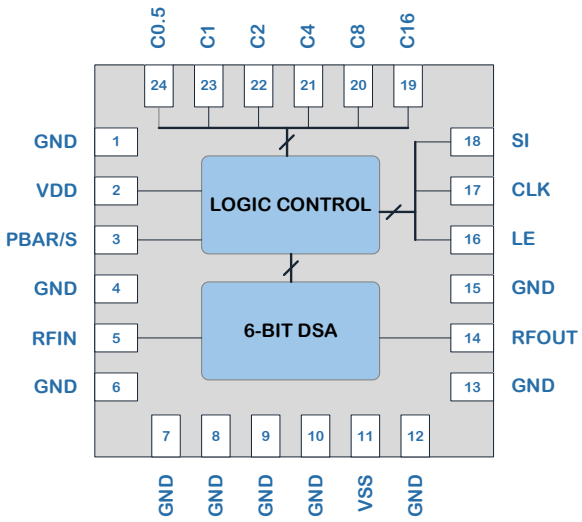
Latched Parallel Mode
This configuration allows the user to control the attenuator through the P1 connector using an external harness. Remove the USB interface if it is currently installed on the evaluation board. Connect a user-supplied harness to the P1 connector. The parallel bus signal names for P1 are indicated on the evaluation board. Programming jumper S2 is set to ‘0’ to select parallel mode. Apply the supply voltage to P6. Send the appropriate signals onto the parallel bus lines in accordance with the Latched Parallel Mode Timing Diagram.

Direct Parallel Mode
This configuration allows the user to control the attenuator through the P1 connector using an external harness. When using this mode the LE signal is held at logic high so that the attenuation will change immediately when there is a change in logic state for any of the parallel bus signals. Remove the USB interface if it is currently installed on the evaluation board. Connect a user-supplied harness to the P1 connector. The parallel bus signal names for P1 are indicated on the evaluation board. Programming jumper S2 is set to ‘0’ to select parallel mode. Apply the supply voltage to P6. Send the appropriate signals onto the parallel bus lines.

Default Power-up State

This default attenuation state is maximum (31.5 dB) when supply voltage is applied to the attenuator in both serial and parallel modes. If a different attenuation state is desired during power-up, this can be accomplished by applying signals according to the Parallel Mode Truth Table. The attenuator will power-up to the state applied to the parallel bus during turn on. The LE signal must be held to logic ‘0’ during power-up. Note that the FDTI controller can interfere with the default power-up state – removing the plug in module will allow normal expected power default operation.

Pad Configuration and Description



Top View

Pad No.	Label	Description
1, 4, 6, 7, 8, 9, 10, 12, 13, 15	GND	Ground Pad
2	VDD	Positive Supply Voltage
3	PBAR/S	Mode Select Pad, Logic Low = Parallel, Logic High = Serial
5	RF_{IN}	RF Input Pad. Incident RF power must enter this pad for rated thermal performance and reliability Do not apply DC power to this pad. Pad may be DC grounded externally and is grounded thru resistors internal to the part.
11	VSS	External Negative Supply Voltage. Grounding pin enables on-chip negative voltage generator. Apply negative voltage to disable on-chip generator.
14	RF_{OUT}	RF Output Pad; Do not apply DC power to this pad. Pad may be DC grounded externally and is grounded thru resistors internal to the part.
16	LE	Latch Enable. The leading edge of signal on LE causes the attenuator to change states for serial and latched parallel modes. For direct parallel mode, keep LE at a logic high level.
17	CLK	Serial Clock Input
18	SI	Serial Data Input
19	C16	16 dB Parallel Control Bit
20	C8	8 dB Parallel Control Bit
21	C4	4 dB Parallel Control Bit
22	C2	2 dB Parallel Control Bit
23	C1	1 dB Parallel Control Bit
24	C0.5	0.5 dB Parallel Control Bit
Backside Paddle	RF/DC GND	RF/DC ground. Use recommended via pattern to minimize inductance and thermal resistance. See PCB Mounting Pattern for suggested footprint.

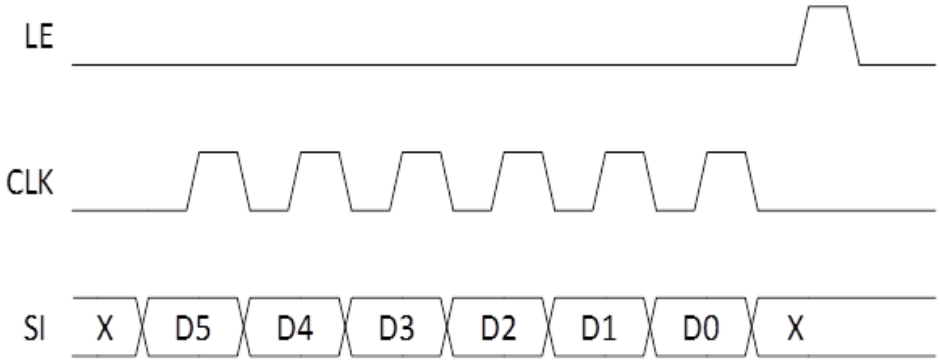
Serial Mode Attenuation Word Truth Table

Attenuation Word							Attenuation State
D5	D4	D3	D2	D1	D0 (LSB)		
L	L	L	L	L	L		0 dB / Reference Insertion Loss
L	L	L	L	L	H		0.5 dB
L	L	L	L	H	L		1 dB
L	L	L	H	L	L		2 dB
L	L	H	L	L	L		4 dB
L	H	L	L	L	L		8 dB
H	L	L	L	L	L		16 dB
H	H	H	H	H	H		31.5 dB

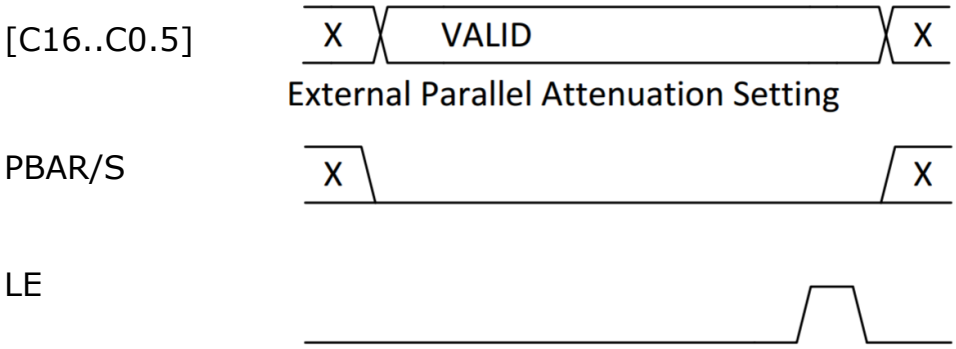
Parallel Mode Attenuation Word Truth

Attenuation Word							Attenuation State
C16	C8	C4	C2	C1	C0.5 (LSB)		
L	L	L	L	L	L		0 dB / Reference Insertion Loss
L	L	L	L	L	H		0.5 dB
L	L	L	L	H	L		1 dB
L	L	L	H	L	L		2 dB
L	L	H	L	L	L		4 dB
L	H	L	L	L	L		8 dB
H	L	L	L	L	L		16 dB
H	H	H	H	H	H		31.5dB

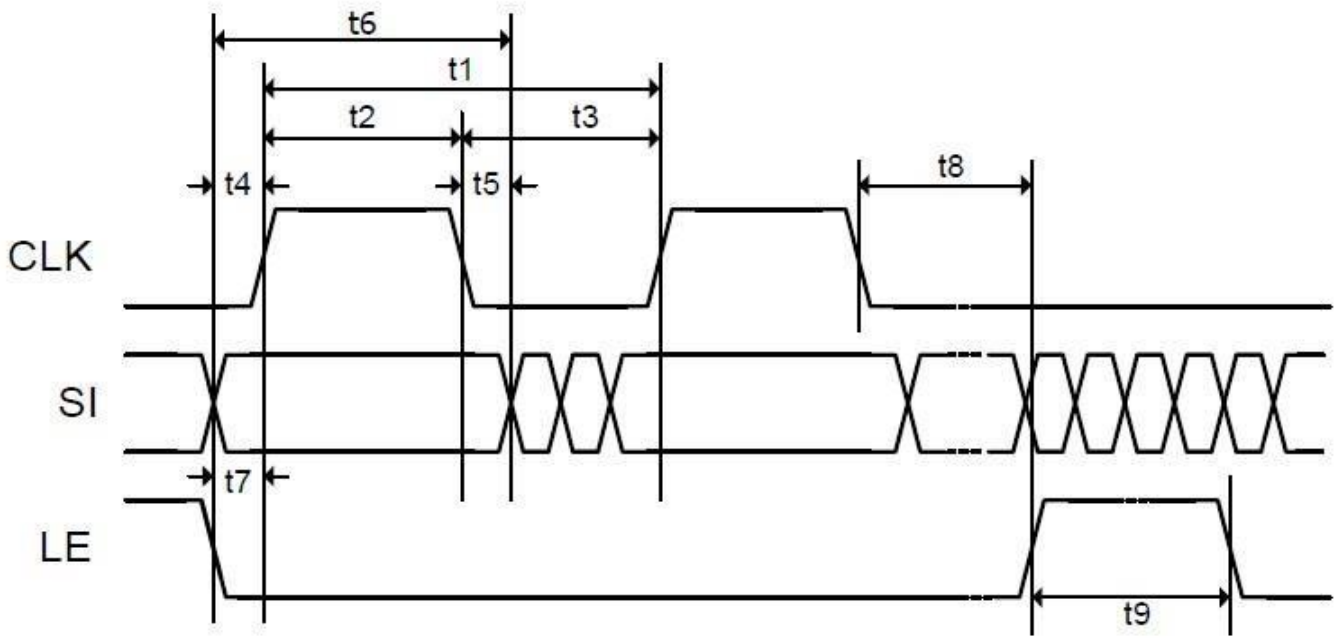
Serial Mode Timing Diagram



Latched Parallel Mode Timing Diagram

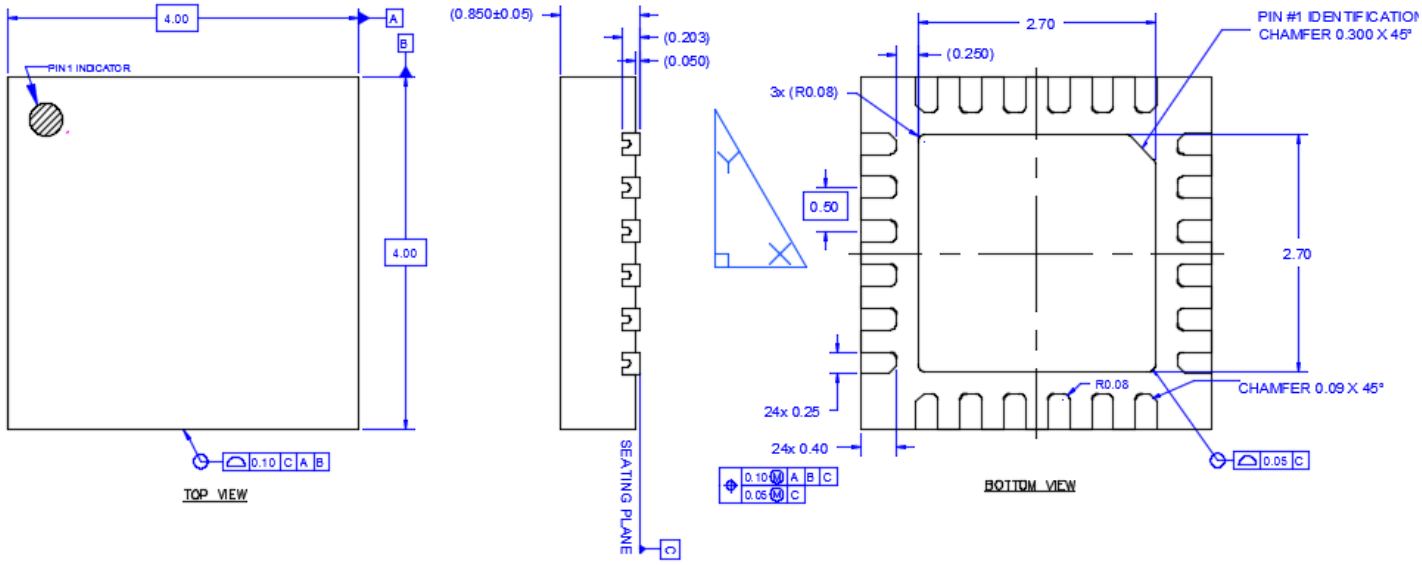


Serial BUS Timing Specifications



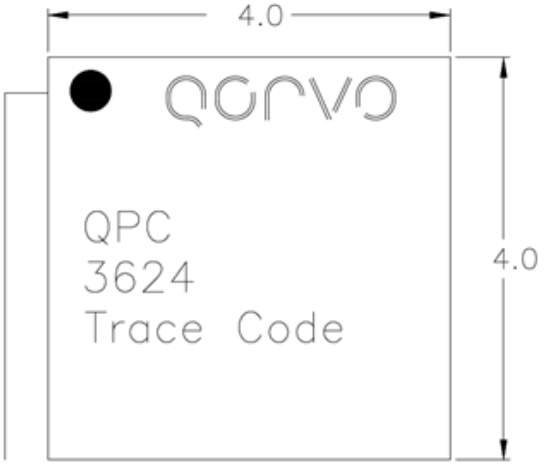
Parameter	Limit	Unit	Comment
t1	25	MHz max	CLK Frequency
t2	20	ns min	CLK High
t3	20	ns min	CLK Low
t4	5	ns min	SI to CLK Setup Time
t5	5	ns min	SI to CLK Hold Time
t6	30	ns min	SI Valid
t7	5	ns min	LE to CLK Setup Time
t8	5	ns min	CLK to LE Setup Time
t9	10	ns min	LE Pulse Width

Package Dimensions



Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.
4. Contact plating: NiPdAu

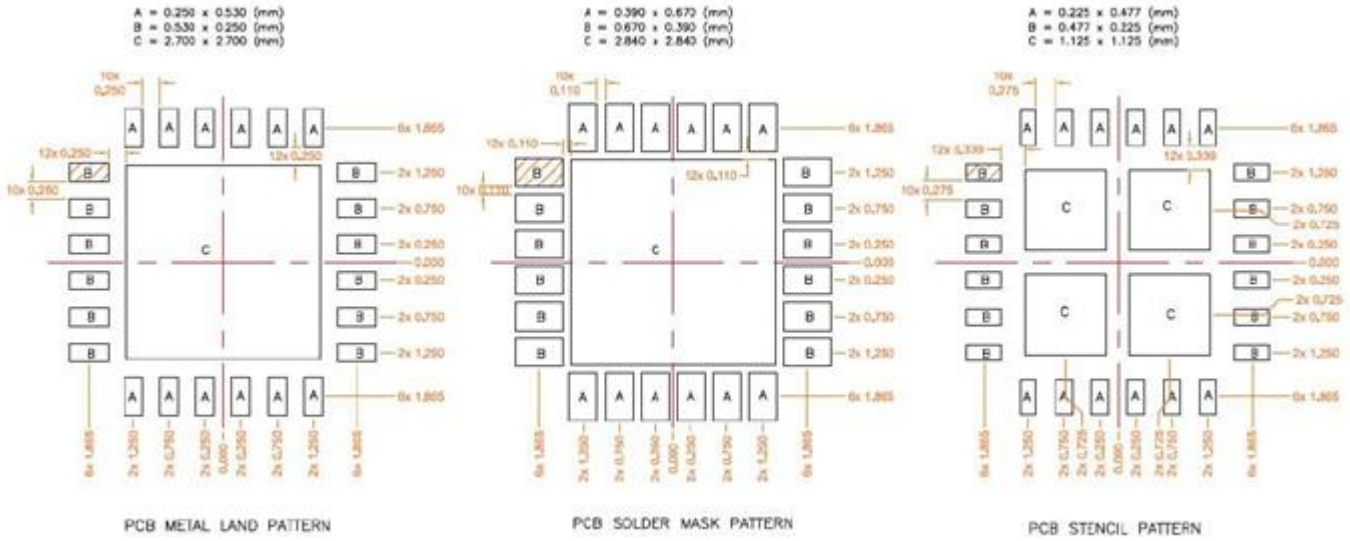
Package Marking



Pin 1 Indicator

Trace Code to be assigned by SubCon

Recommended Mounting Pattern



Thermal vias for center slug "C" should be incorporated into the PCB design. The number and size of thermal vias will depend on the application, the power dissipation, and the electrical requirements. Example of the number and size of vias can be found on the Qorvo evaluation board layout.