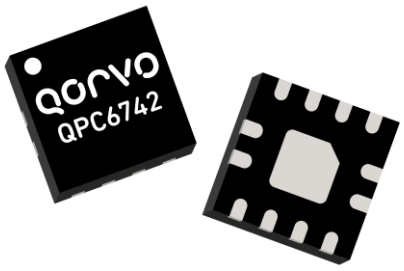
QPC6742

75Ω SP4T Switch 5MHz to 2000MHz

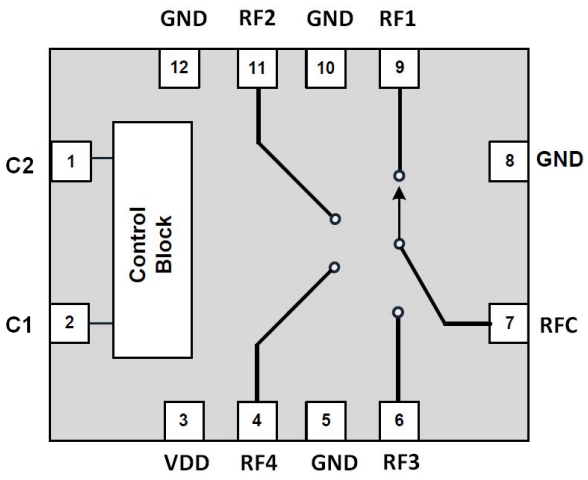
Product Overview

The QPC6742 is a 75Ω Silicon on Insulator (SOI) single-pole, four throw (SP4T) switch designed for use in CATV, satellite set top, and other high-performance communications systems. It offers a high isolation symmetric topology with excellent linearity and power handling capability. No blocking caps are necessary on the RF ports. QPC6742 is packaged in a convenient 1.8mm x 1.8mm QFN package



12 Pin 1.8 x 1.8mm QFN Package

Functional Block Diagram



Top View

Key Features

- 5 MHz to 2000 MHz Operation
- 5 MHz to 3300 MHz Operation with Additional Matching
- Low Insertion Loss: 0.35 dB at 800 MHz
- No Blocking Caps Required Unless Voltage on RF Line
- High Isolation: 42 dB at 800 MHz
- High Input IP3: 82 dBm at 850 MHz
- 2kV ESD
- +1.8V Logic Compatible
- 3V to 5V Operation

Applications

- MDU Amplifiers
- Point To Point
- Optical Nodes
- Set Top Box
- PCTV
- Multi-tuner DVR

Ordering Information

Part No.	Description
QPC6742SQ	Sample bag with 25 pieces
QPC6742SR	7" Reel with 100 pieces
QPC6742TR7	7" Reel with 2500 pieces
QPC6742PCK	5 – 2000MHz PCBA with 5 pc. sample bag

Absolute Maximum Ratings

Parameter	Rating
Control Voltage ($V_{C1, C2}$)	+3.0V
Supply Voltage (V_{DD})	+6.0V
Maximum CW Input Power at 25°C	+35dBm
Max Input Power During Active Switching	+27dBm
Storage Temperature Range	−40 to +150°C

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Supply Voltage, V_{DD}	+2.7	+3	+5.5	V
Temperature Range	−40		+85	°C

Electrical specifications are measured at specified test conditions.
Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications; QPC6742-4000B EVB

Parameter	Conditions [1]	Min	Typ	Max	Units
Frequency Range		5		2000	MHz
Insertion Loss (RFC to RF1/RF2/RF3/RF4)	5MHz		0.20		dB
	50MHz		0.30		
	800MHz		0.35		
	1.2GHz		0.40		
	2GHz		0.45		
Return Loss [2] (RFC, RFx)	5MHz		40		dB
	50MHz		45		
	800MHz		30		
	1.2GHz		30		
	2GHz		30		
Isolation [3] (RFC to RF1/RF2/RF3/RF4)	5MHz		75		dB
	50MHz		62		
	800MHz		42		
	1.2GHz		38		
	2GHz		31		
Isolation [3] (RF1/RF2/RF3/RF4)	5MHz		80		dB
	50MHz		65		
	800MHz		43		
	1.2GHz		39		
	2GHz		34		

Notes:

1. Test Conditions Unless Otherwise Specified: T_A = +25°C, V_{DD} = +3.0V, $V_{C1,C2}$ = 0/+2.5V, 75Ω system.
2. Includes series matching. Refer to EVB Schematic on page 5.
3. Average Isolation. Refer to Performance Plots on pg.8 for more detail.

Electrical Specifications (cont'd.)

Parameter	Conditions [1]	Min	Typ	Max	Units
Input IP3	850MHz +12dBm input power per tone, 30MHz tone spacing		82		dBm
Input IP2	850MHz +12dBm input power per tone, 30MHz tone spacing		130.6		
Input 1dB Compression Point	850MHz		40.2		
Input 0.1dB Compression Point	850MHz		34.0		
MER [2]	75dBmV composite at 885MHz		41.7		dB
CCN [2]	75dBmV composite at 885MHz		55.8		
Switching Speed	10/90% RF		0.6		µs
Switching Speed	50% control to 10/90% RF		1.3		
Turn On Time	Time for VDD = 0V to part ON and RF = 90%		20		
NVG Spurs	F<30MHz		-118		dBm
Harmonics-2nd	5 MHz		-76		dBc
	50MHz		-88		
	850MHz		-129		
	1800MHz		-114		
Harmonics-3rd	5MHz		-97		dBc
	50MHz		-110		
	850MHz		-129		
	1800MHz		-110		

Notes:

1. Test Conditions Unless Otherwise Specified: T_A = +25°C, V_{DD} = +3.0V, V_{CTL} = 0/+2.5V, 75Ω system. Drive RFC, RFx output.
2. V_{DD} = +3.0V, V_{CTL} = 0/+2.5V, 75Ω system.

Electrical Specifications - Power Supply

Parameter	Conditions [1]	Min	Typ	Max	Units
Supply Current (I_{DD})	V_{DD} = +3.0V		65	130	µA
Control Current				5	µA
Control Voltage High		1.3		2.7	V
Control Voltage Low		0		0.45	V

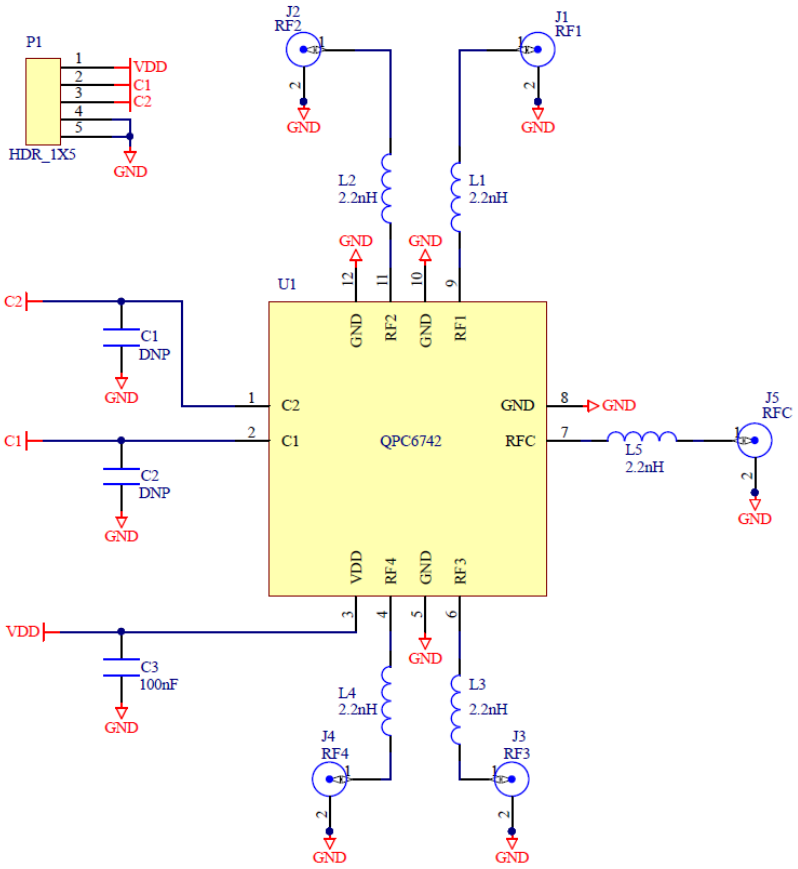
Power Supply Sequencing Requirements

Condition	Sequence
Power Up	Turn on VDD, then C1 and C2, then (20µs or greater), apply RF signal
Power Down	Turn off RF signal, then C1 and C2, turn off VDD

Truth Table

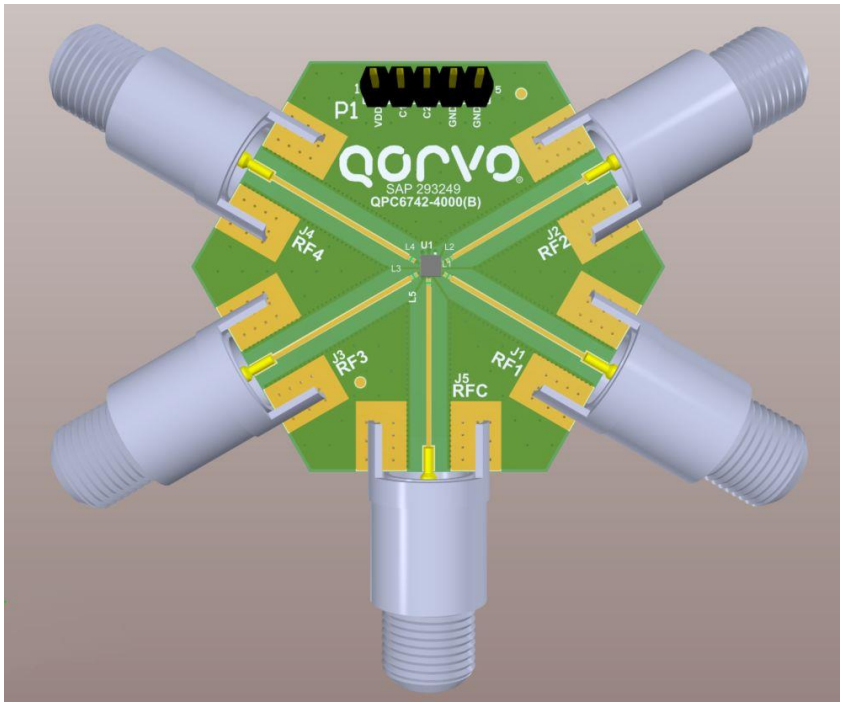
Mode	Control Signals	
	C1	C2
RFC to RF1	High	Low
RFC to RF2	Low	High
RFC to RF3	High	High
RFC to RF4	Low	Low

5-2000 MHz Evaluation Board Schematic (QPC6742PCK)



Ref. Designator	Description	Manufacturer	Part Number
PCB	Evaluation Board PCB	Viasystems	QPC6742-4000B
U1	75ohm SP4T Switch	Qorvo	QPC6742
J1, J2, J3, J4, J5	F Connector, Edge Mount, 75 Ω, 0.065"	Genesis Technology	GT20-300204
P1	CONN, HDR, ST, PLRZD, 5-PIN, 0.100"	ITW Pancon	MPSS100-5-C
C3	CAP, 0.1uF, 10%, 16V, X7R, 0402	Kemet	C0402C104K4RACTU
L1, L2, L3, L4, L5	IND,2.2nH,+/-0.2nH, M/L, MID-Q, 0201	TDK	MLG0603PPA2N2CT000
C1, C2	DNP	N/A	N/A

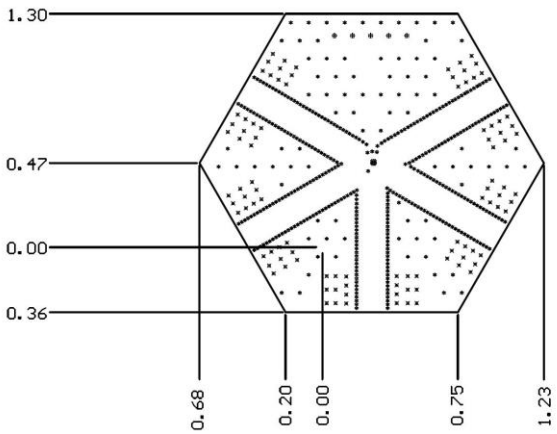
Evaluation Board Assembly (QPC6742PCK)



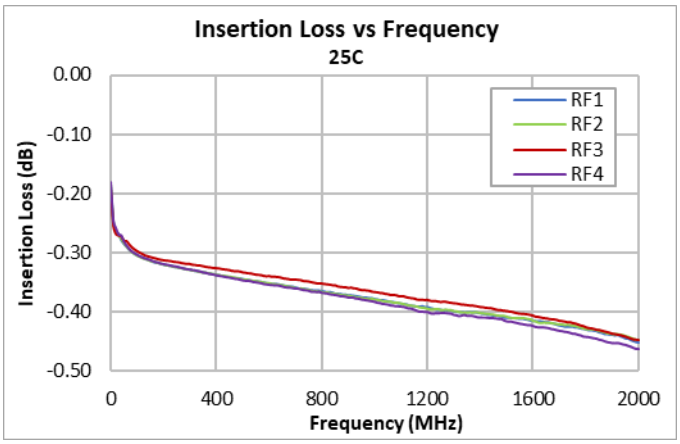
EVB PCB Material and Stack-up

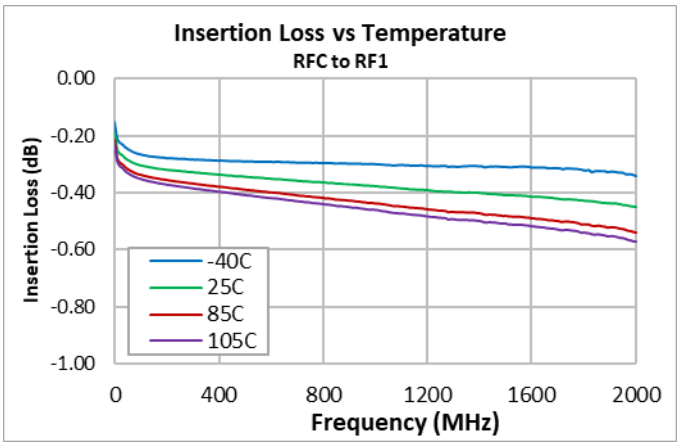
Board Material: 0.020" RO4003C, ε_r=3.38
Final Plating: 0.5oz Copper
Board Dimension: 1.1" x 2.55"
Total Thickness: 50.2 mils

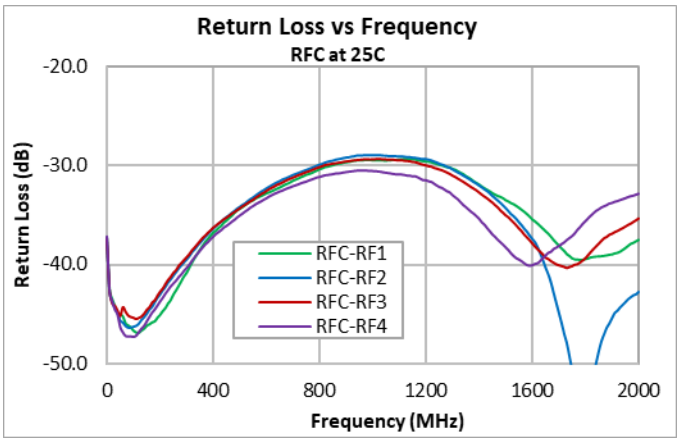
Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	0.70mil		
4	Dielectric1	RO4003C	20.00mil	3.38	
5	MidLayer1	Copper	1.40mil		
6	Dielectric2	370HR	4.22mil	3.7	
7	MidLayer2	Copper	1.40mil		
8	Dielectric3	370HR	21.00mil	4.34	
9	Bottom Layer	Copper	0.70mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				

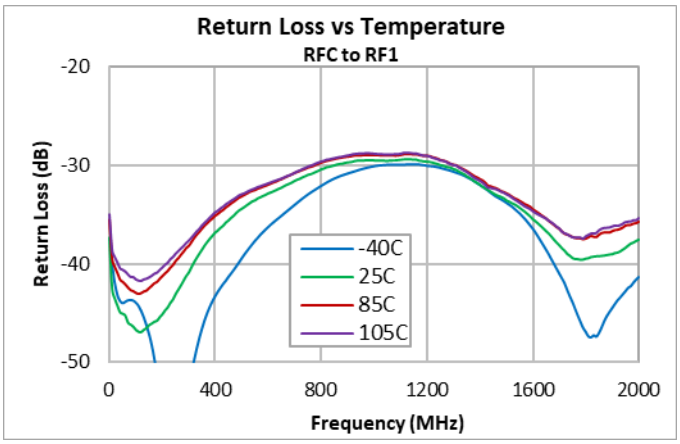


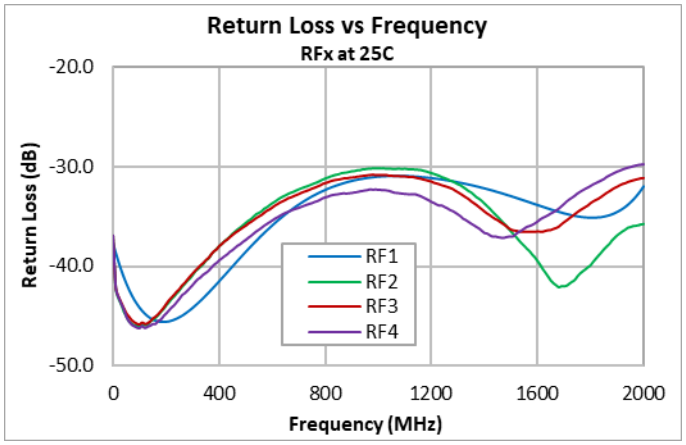
Performance Plots, QPC6742PCK

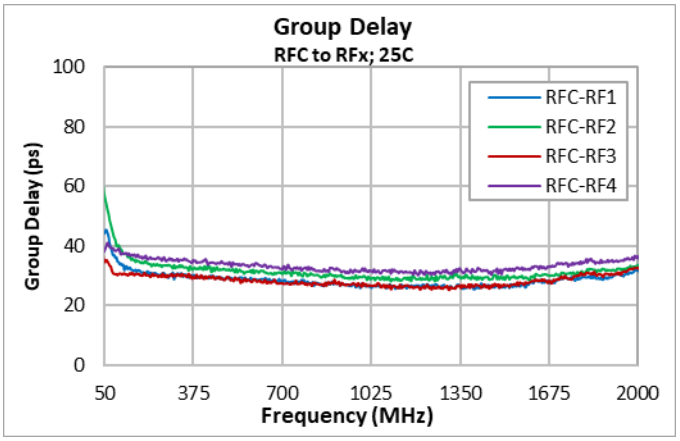








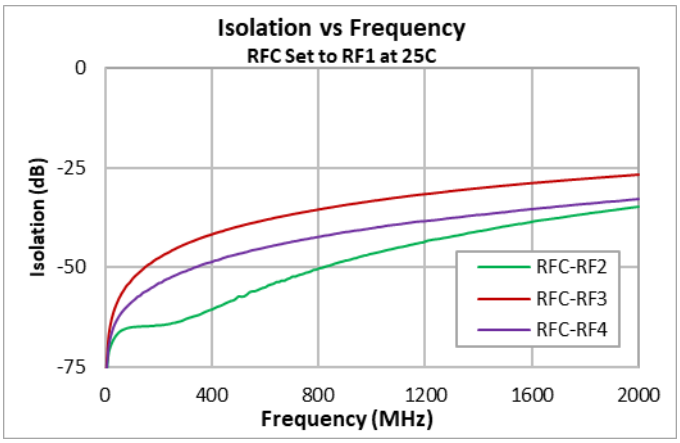


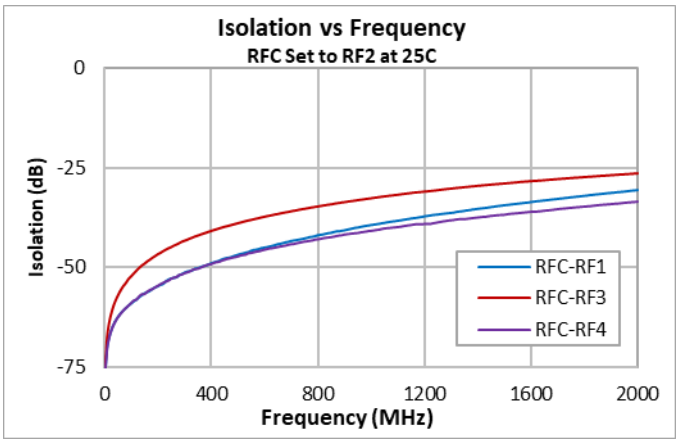


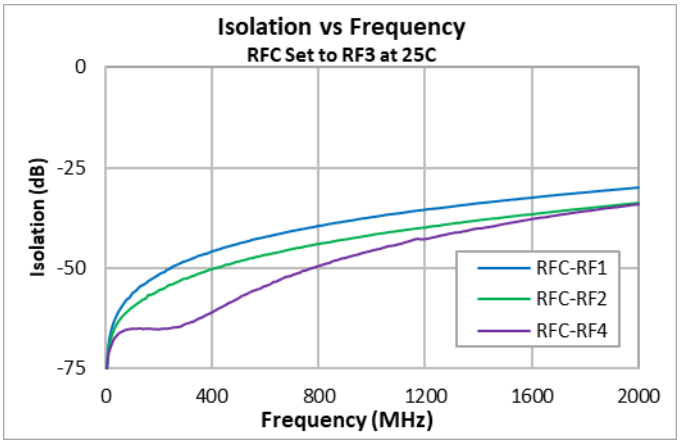
Notes:

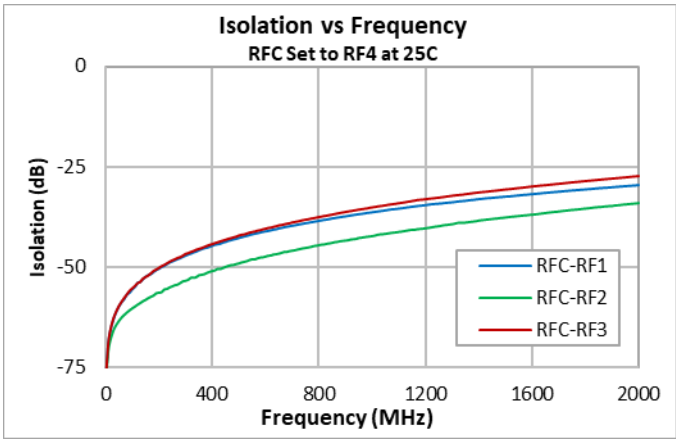
1. VDD =+3.0V, VC2, C1= 0 / 2.5V, Temp= +25°C, Zo = 75Ω
2. Insertion Loss plots are loss compensated to remove effects of EVB.
3. Group Delay is deembedded to remove effects of EVB and matching elements.

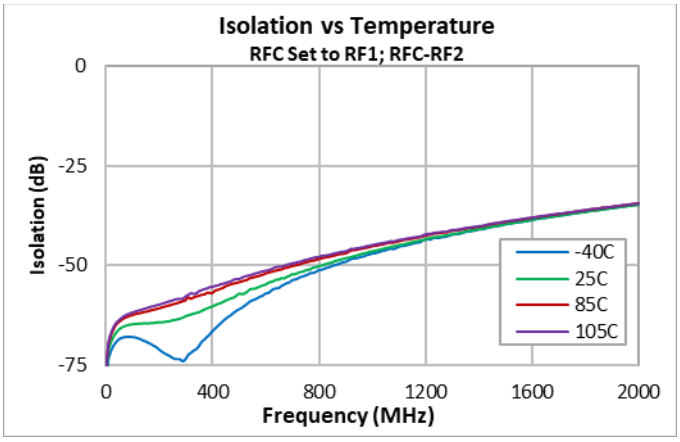
Performance Plots (cont'd.)

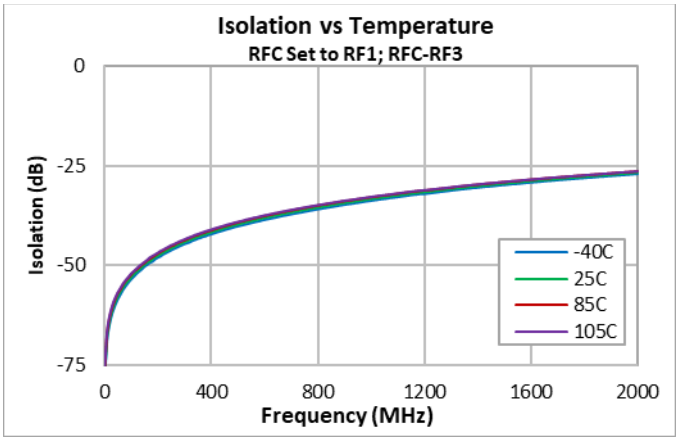












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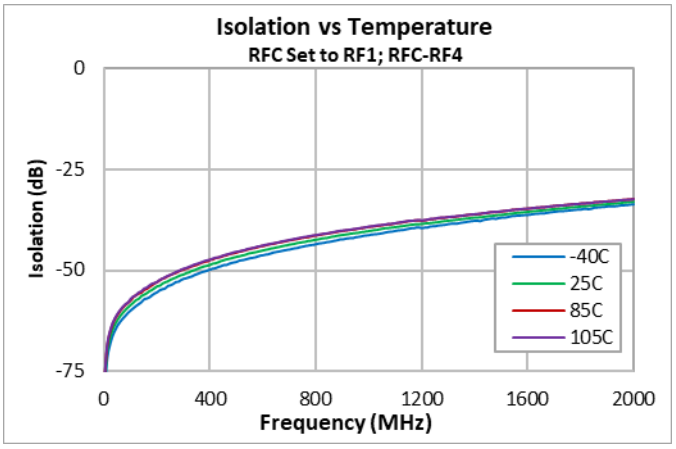
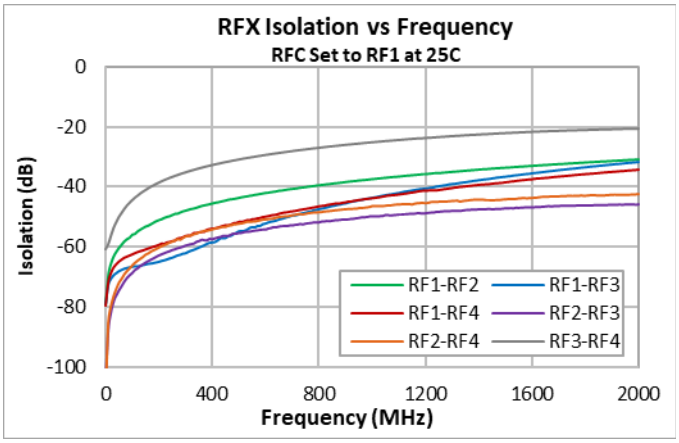
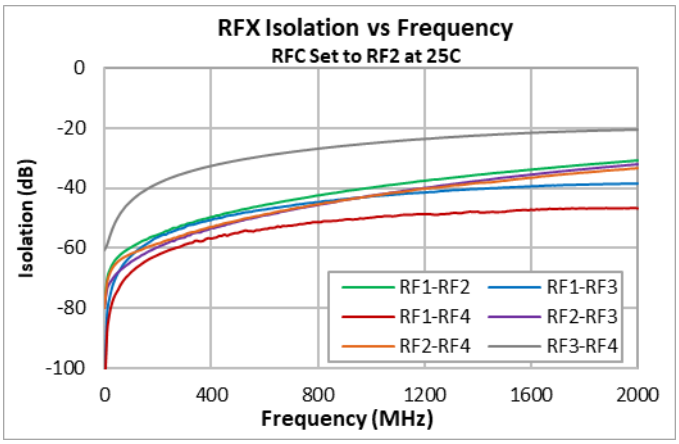
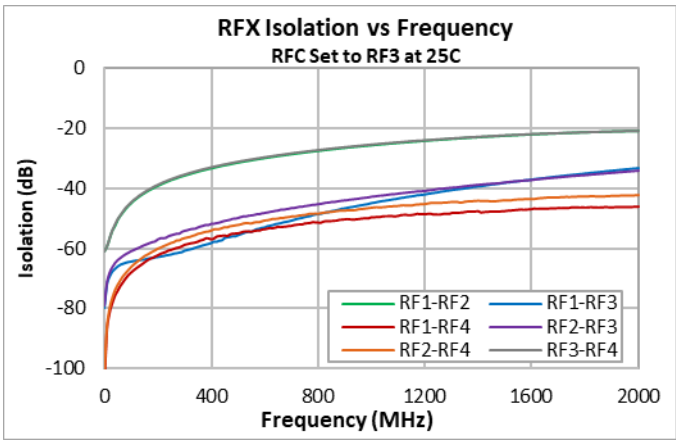
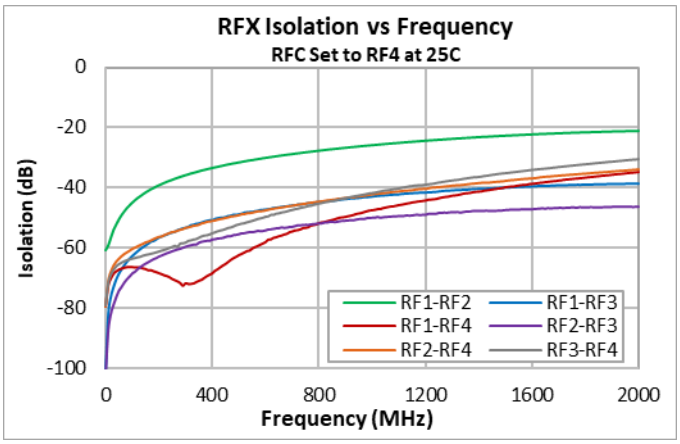
Performance Plots (cont'd.)

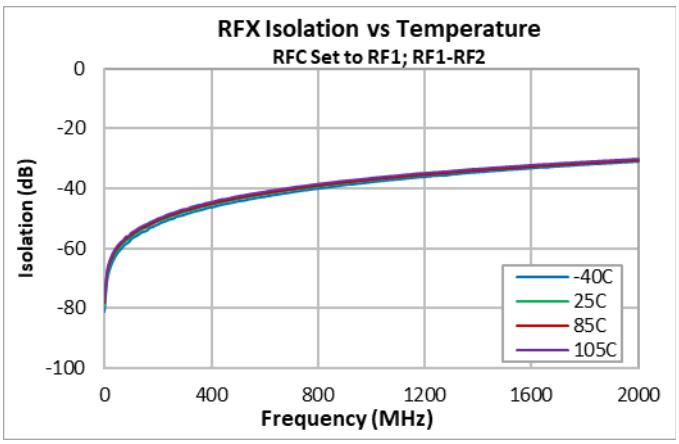








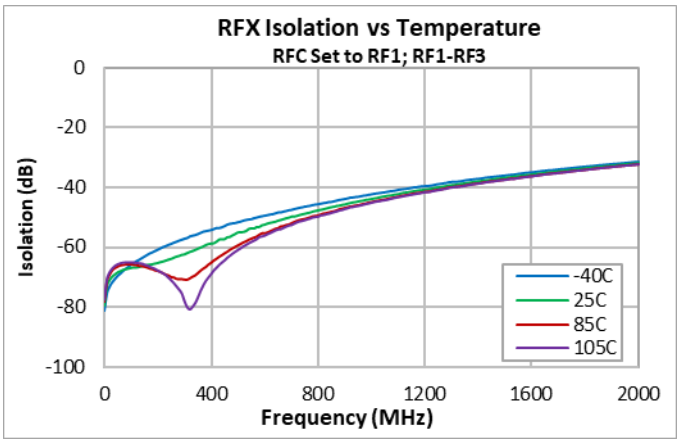


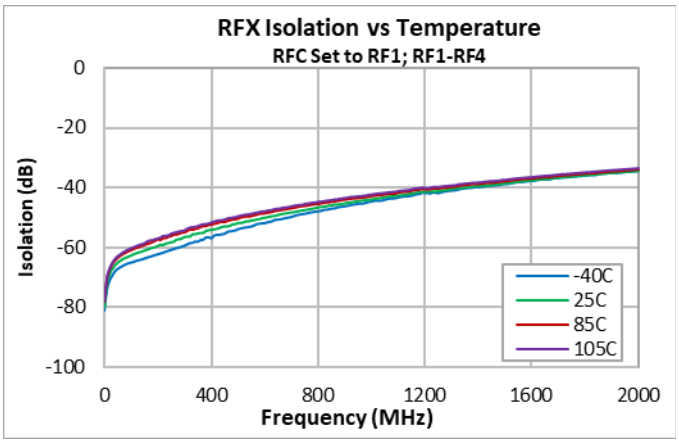


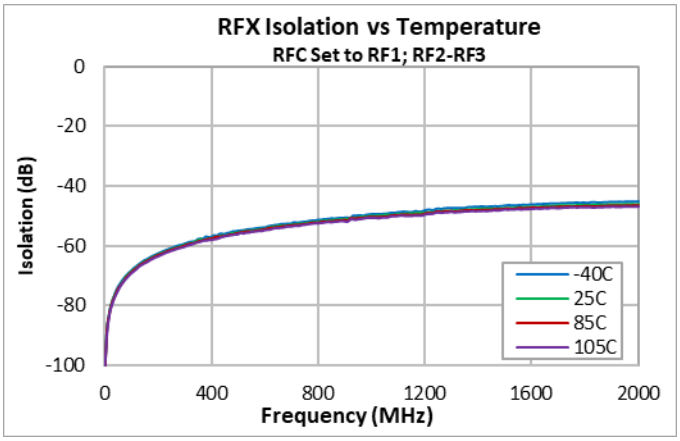
Notes:

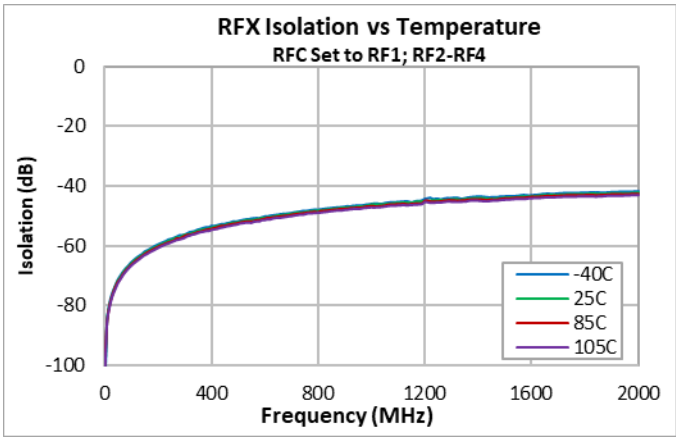
1. VDD =+3.0V, VC2, C1= 0 / 2.5V, Temp= +25°C, Zo = 75Ω

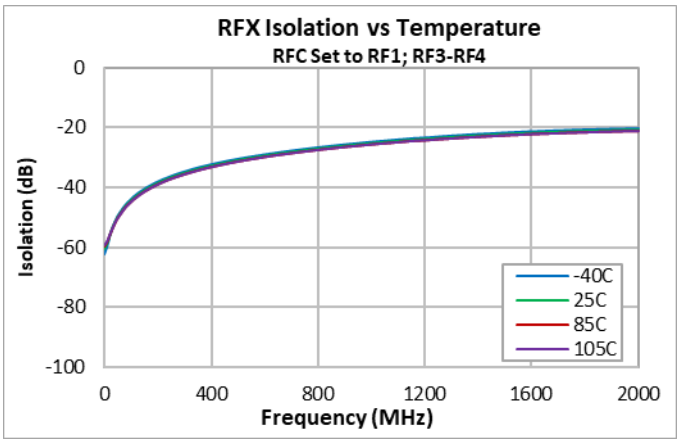
Performance Plots (cont'd.)

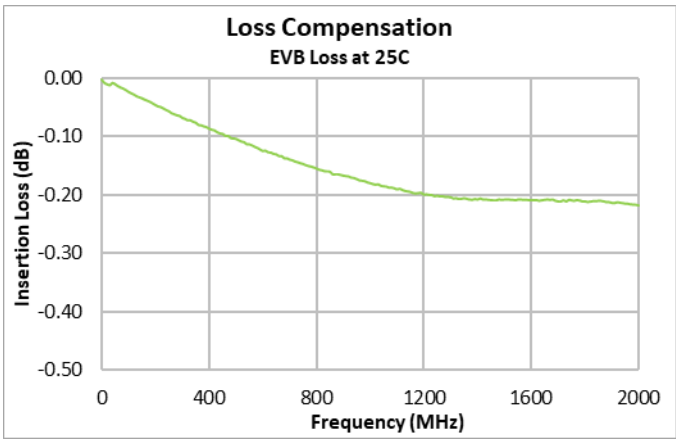








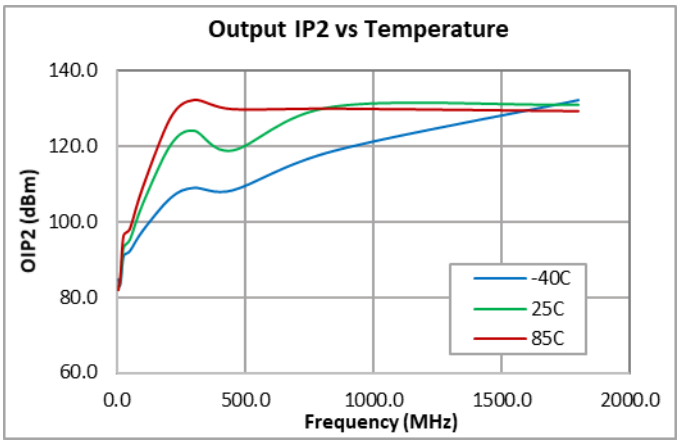


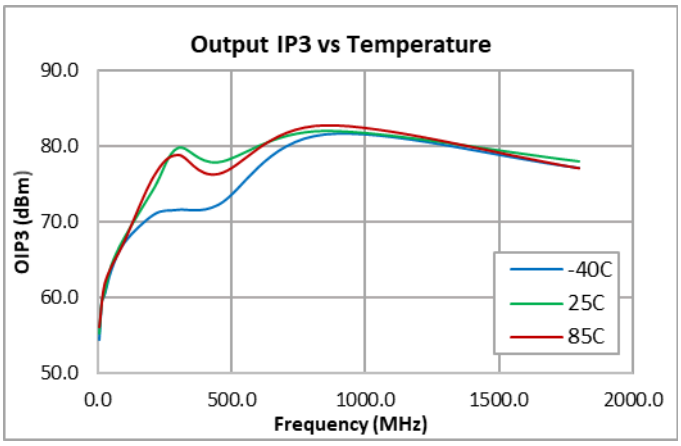


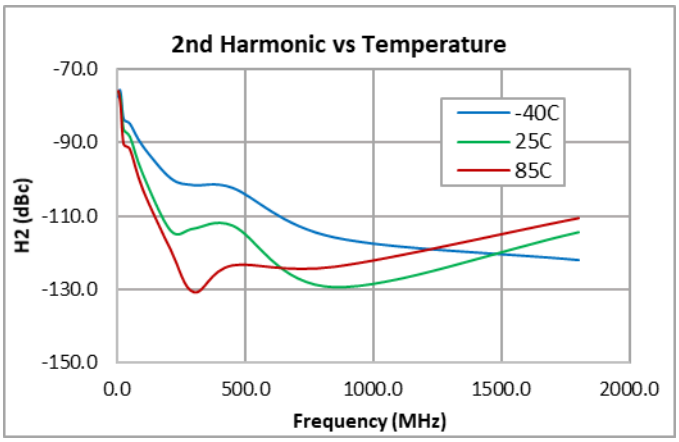
Notes:

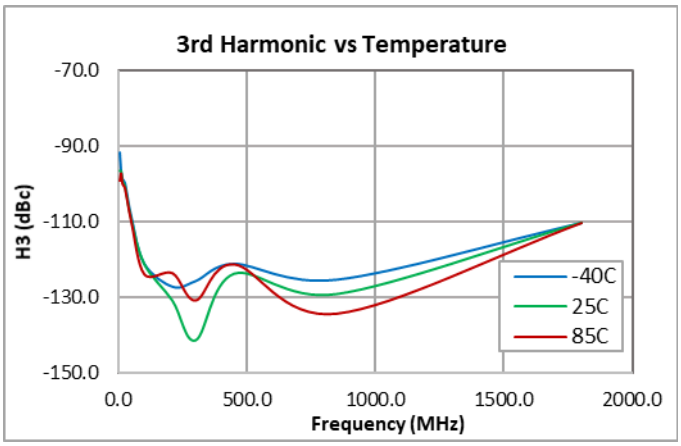
1. VDD =+3.0V, VC2, C1= 0 / 2.5V, Temp= +25°C, Zo = 75Ω

Performance Plots (cont'd.)





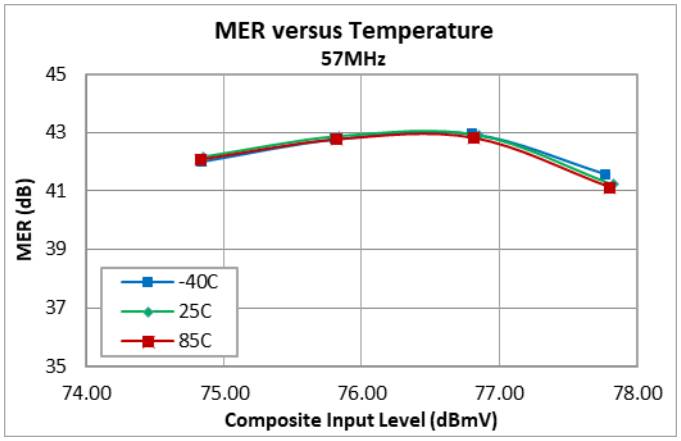


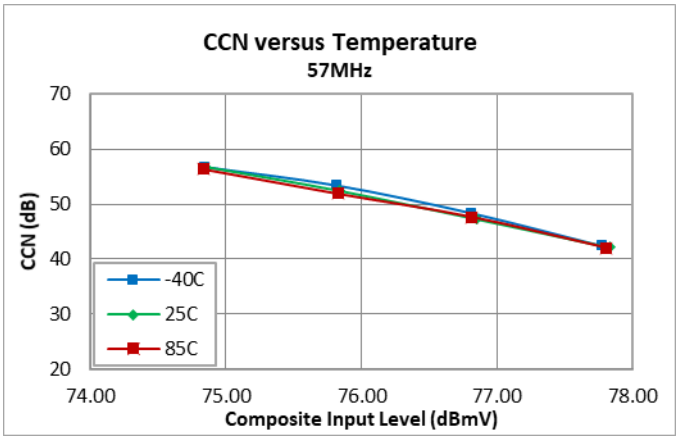


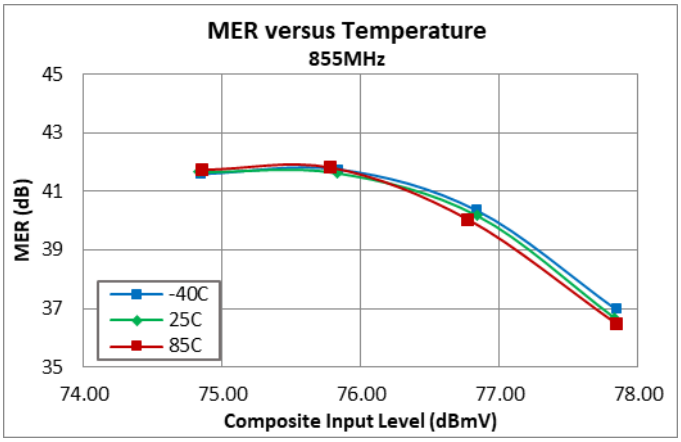
Notes:

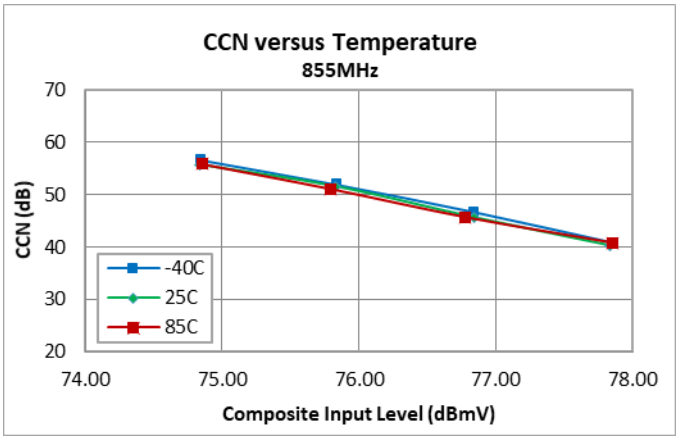
1. VDD =+3.0V, VC2, C1= 0 / 2.5V, Temp= +25°C, Zo = 75Ω
2. +12dBm per tone.

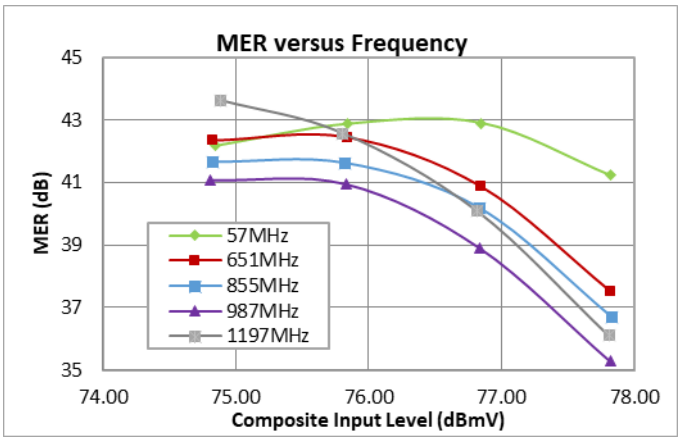
Performance Plots (cont'd.)

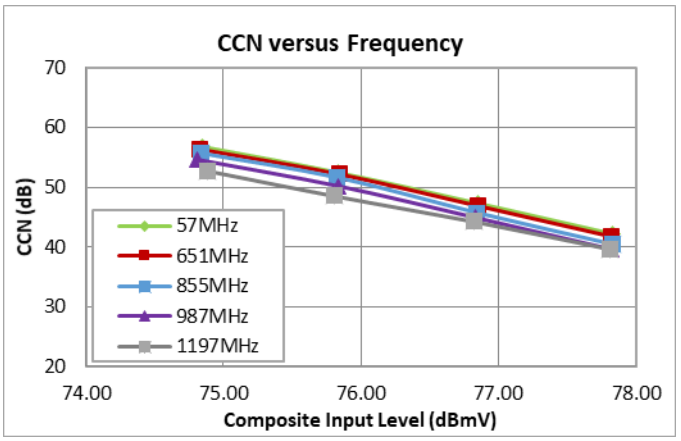








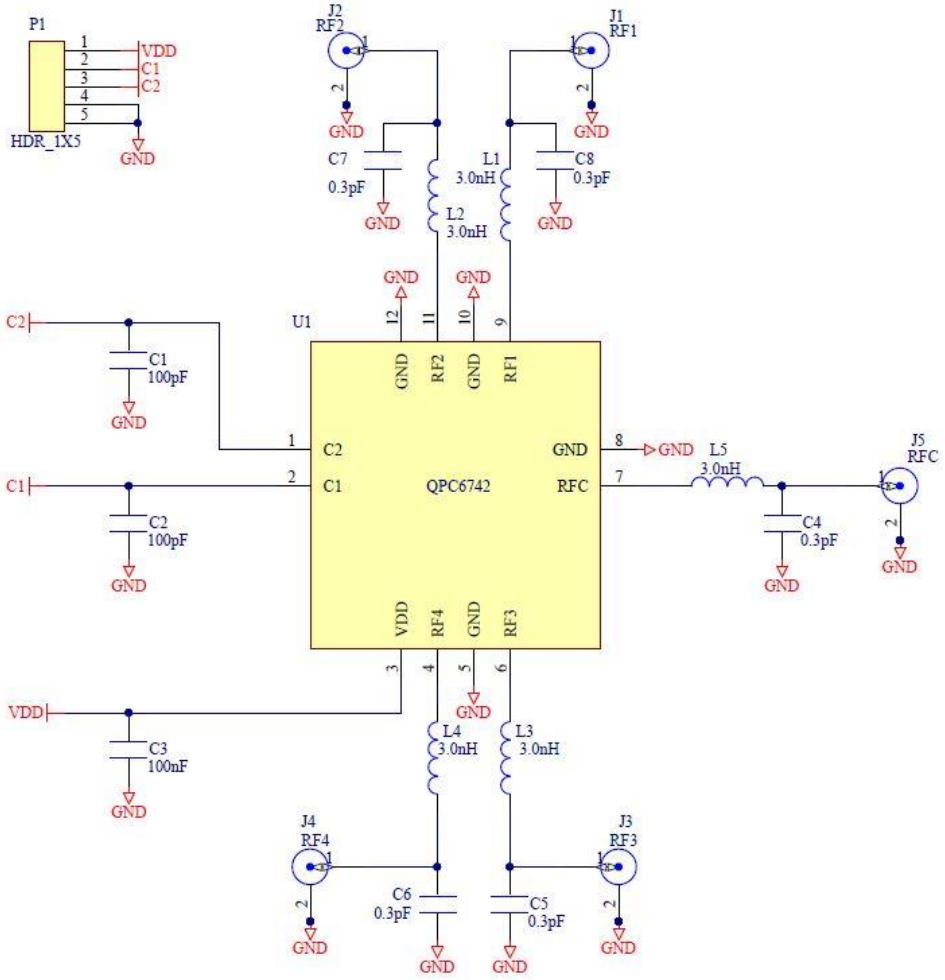




MER/CCN Test Conditions:

1. VDD =+5.0V, VC2, C1= 0 / 2.5V, Temp= +25°C, Zo = 75Ω
2. 190 QAM256 Channels, 57-1215MHz, ITU-T J.83, Annex B
3. CCN test procedure according to ANSI/SCTE 17. System BW 5.36MHz.

Additional Applications; 5-3300MHz (QPC6742-4001A EVB)

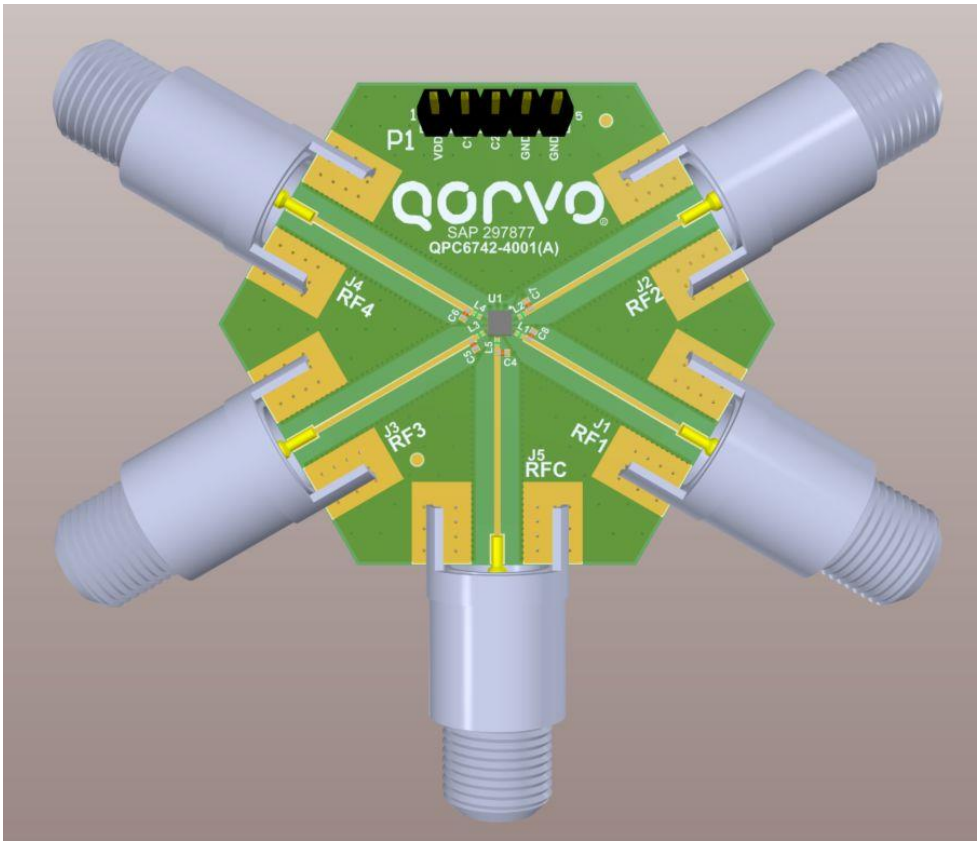


Notes:

1. L1-L5 optimized for return loss for mid band. For applications with F_{MAX} < 1.8GHz, reduce the value of L1-L5 to 2.2nH or less. Depending on application return loss limits, it may also be acceptable to use a single series inductor on RFC.
2. C4-C8 optimized to trim return loss at 3.3GHz. For applications with F_{MAX} of 1.8GHz or lower, C4-C8 should be deleted.
3. Isolation can be optimized by maximizing ground between RF Ports and using coplanar RF tracks to U1.

Ref. Designator	Description	Manufacturer	Part Number
PCB	Evaluation Board PCB	Viasystems	QPC6742-4001A
U1	75ohm SP4T Switch	Qorvo	QPC6742
J1, J2, J3, J4, J5	F Connector, Edge Mount, 75 Ω, 0.065"	Genesis Technology	GT20-300204
P1	CONN, HDR, ST, PLRZD, 5-PIN, 0.100"	ITW Pancon	MPSS100-5-C
C3	CAP, 0.1uF, 10%, 16V, X7R, 0402	Kemet	C0402C104K4RACTU
C4, C5, C6, C7, C8	Cap0402 0.3pF ROHS	Johanson Technology	500R07S0R3AV4T
L1, L2, L3, L4, L5	IND, 3.0nH, +/-0.2nH, T/F, HI-Q, 0201	Murata	LQP03TN3N0C02D
C1, C2	CAP, 100pF, 10%, 16V, COG, 0402	Kemet	C0402C101K4GACTU

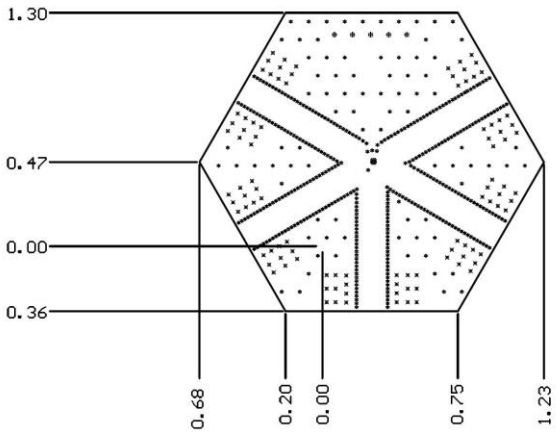
Additional Applications; 5-3300MHz (QPC6742-4001A EVB)



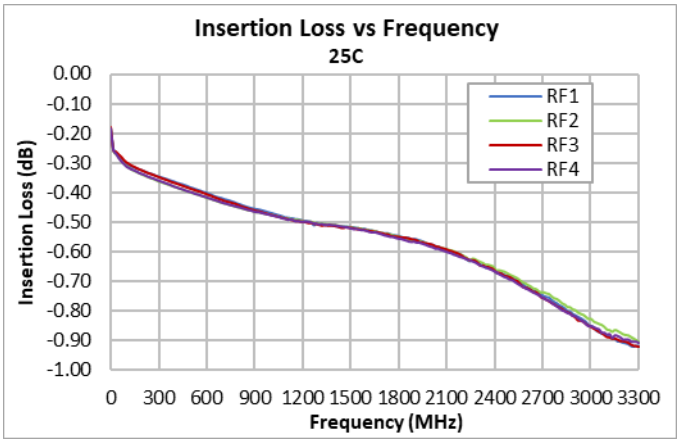
EVB PCB Material and Stack-up

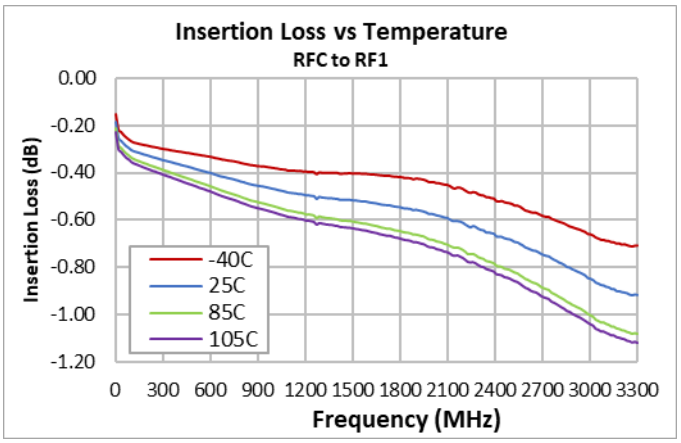
Board Material: 0.020" RO4003C, ε_r=3.38
Final Plating: 0.5oz Copper
Board Dimension: 1.1" x 2.55"
Total Thickness: 50.2 mils

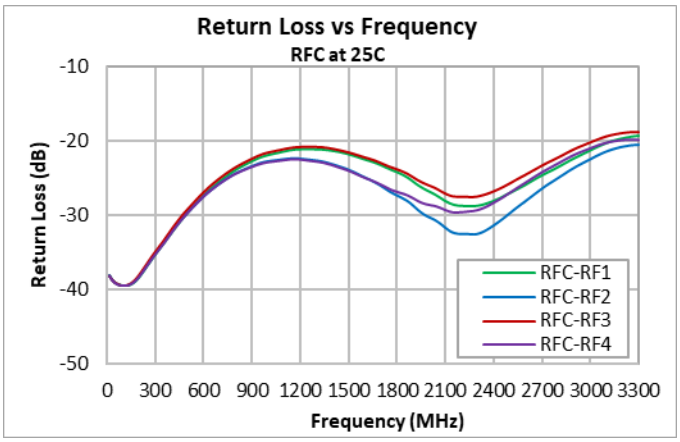
Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	0.70mil		
4	Dielectric1	RO4003C	20.00mil	3.38	
5	MidLayer1	Copper	1.40mil		
6	Dielectric2	370HR	4.22mil	3.7	
7	MidLayer2	Copper	1.40mil		
8	Dielectric3	370HR	21.00mil	4.34	
9	Bottom Layer	Copper	0.70mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				

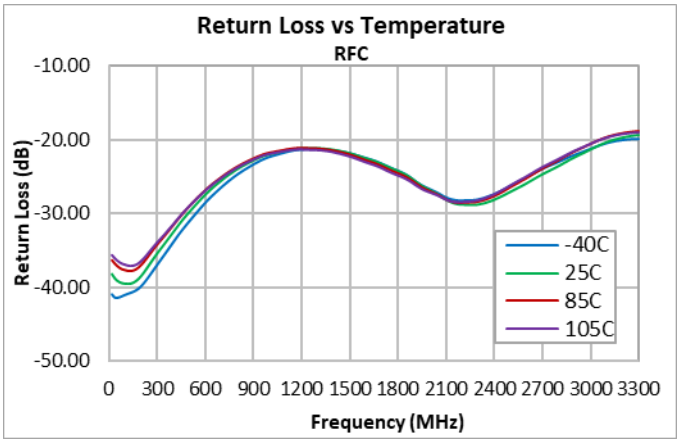


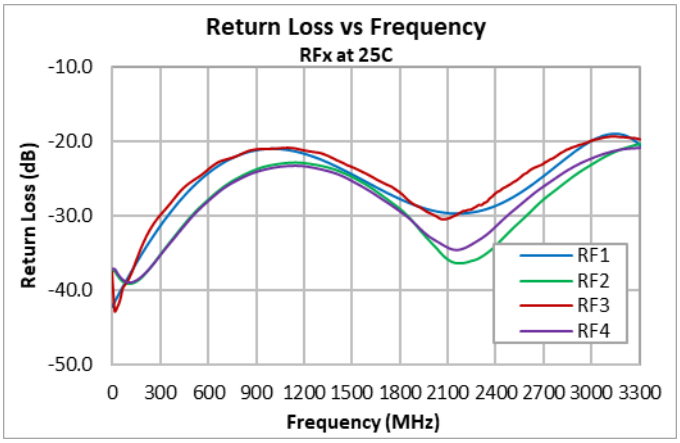
Additional Applications; Performance Plots (QPC6742-4001A EVB)

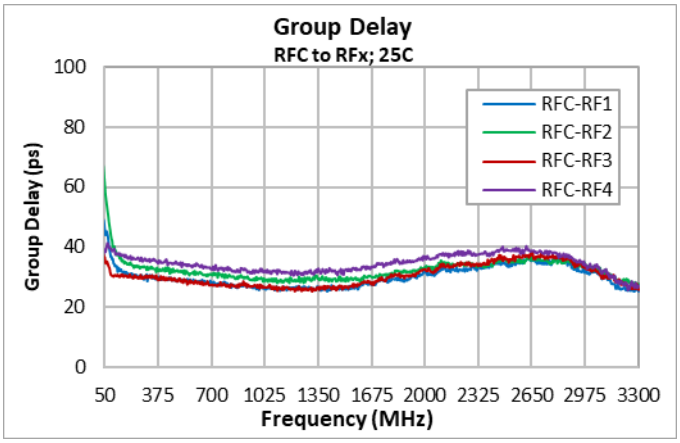








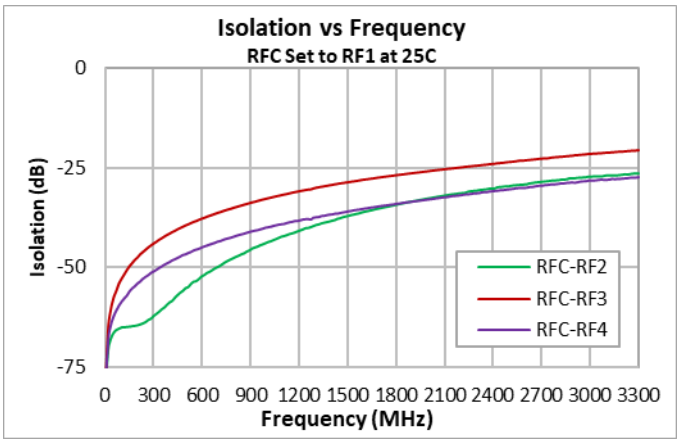


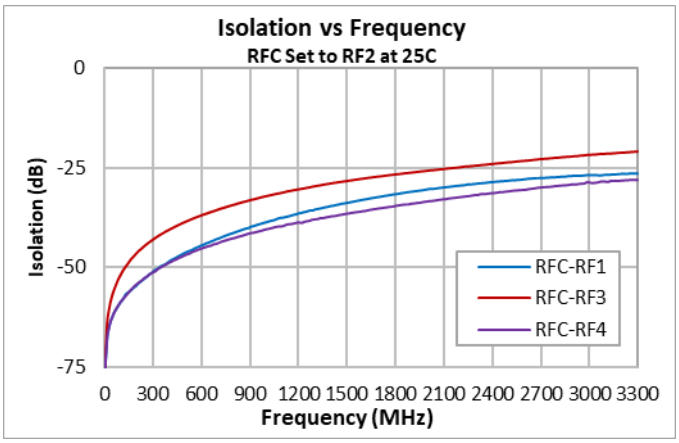


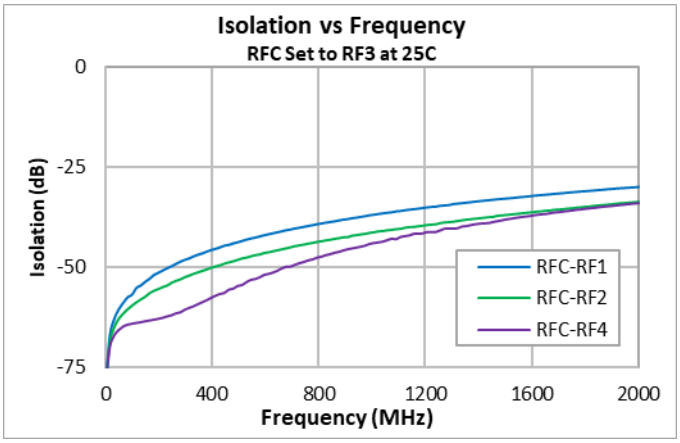
Notes:

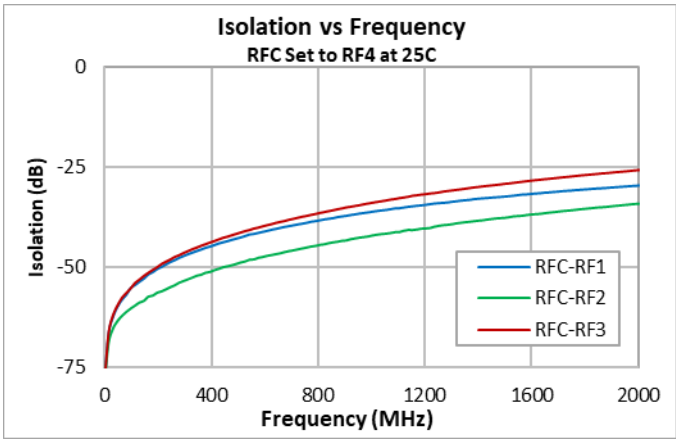
1. VDD =+3.0V, VC2, C1= 0 / 2.5V, Temp= +25°C, Zo = 75Ω
2. Insertion Loss plots are loss compensated to remove effects of EVB.
3. Group Delay is deembedded to remove effects of EVB and matching elements.

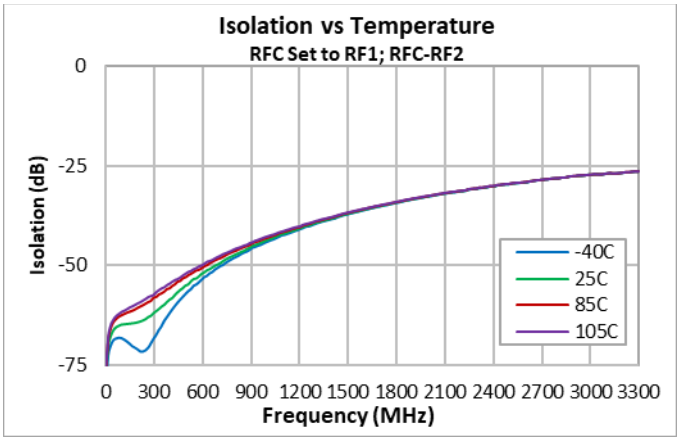
Additional Applications; Performance Plots (QPC6742-4001A EVB)

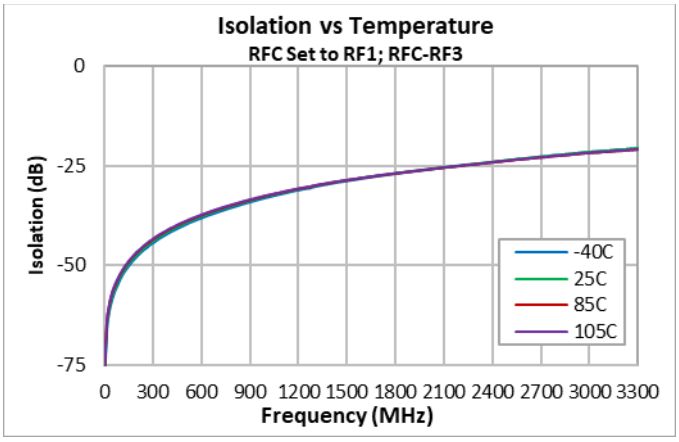












Notes:

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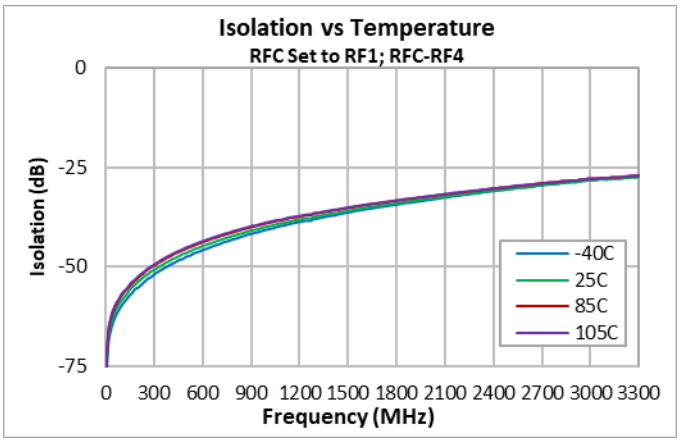
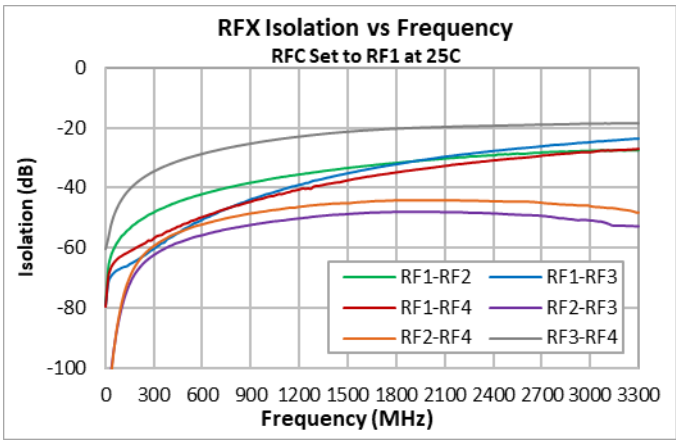
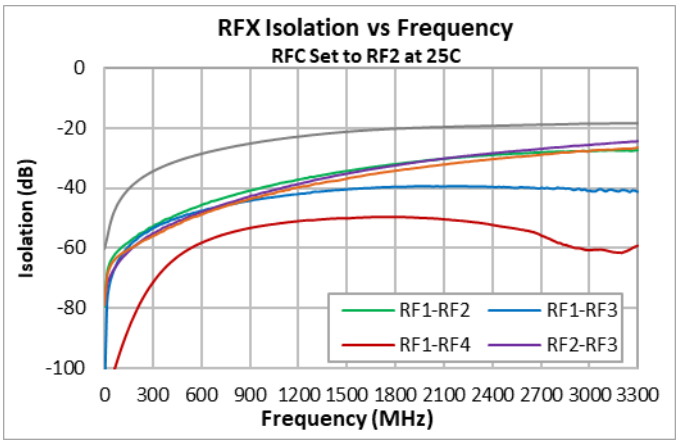
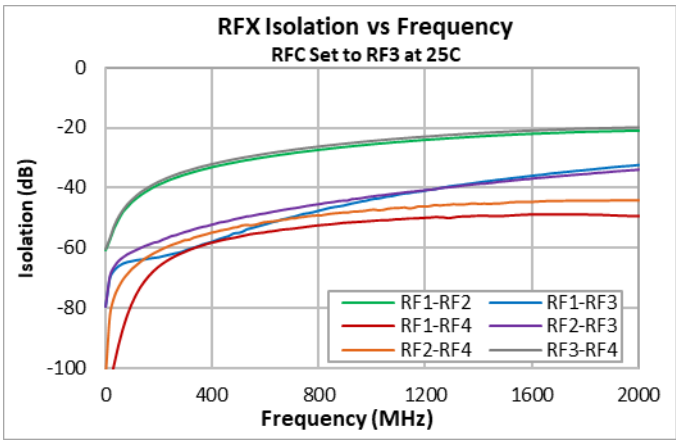
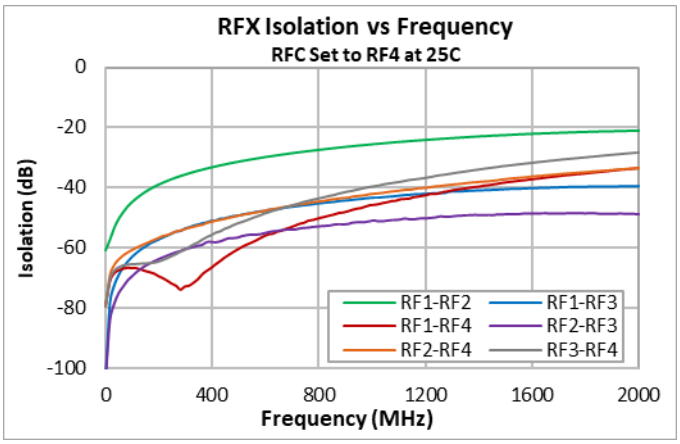
Additional Applications; Performance Plots (QPC6742-4001A EVB)

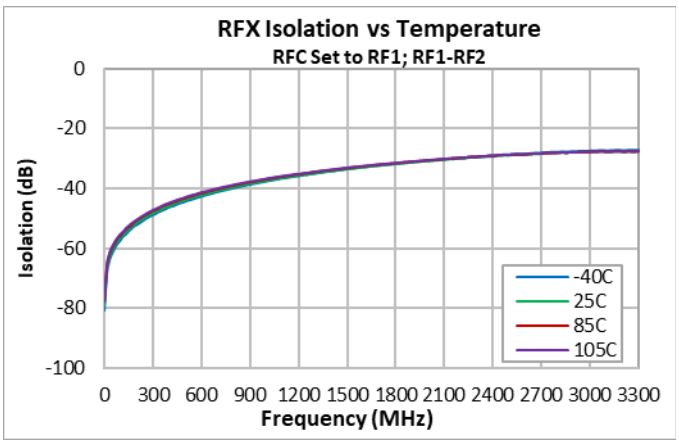












Notes:

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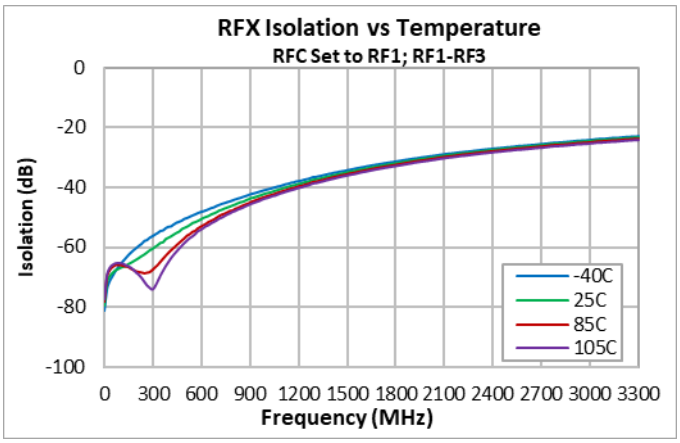
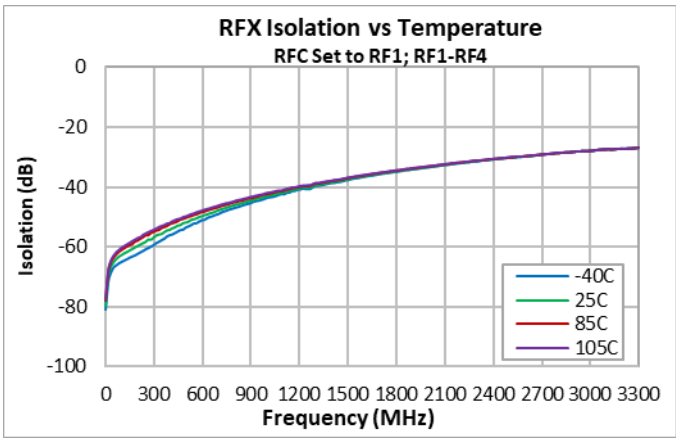
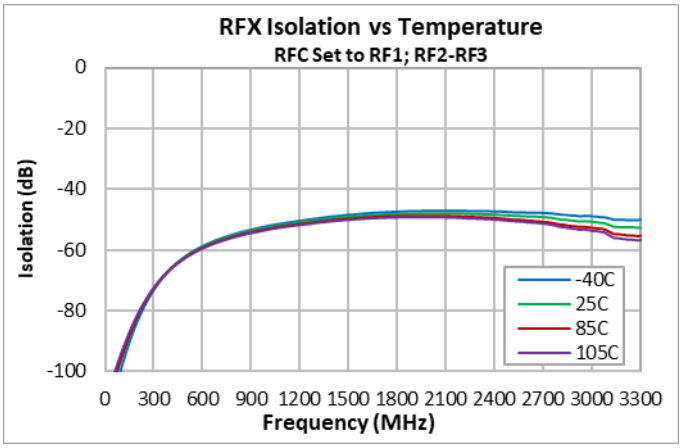
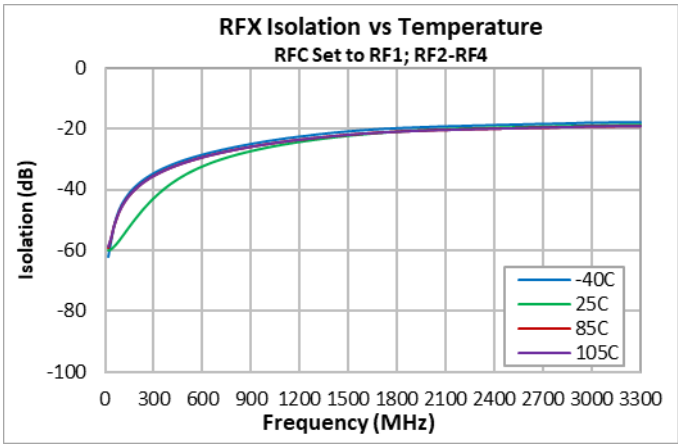
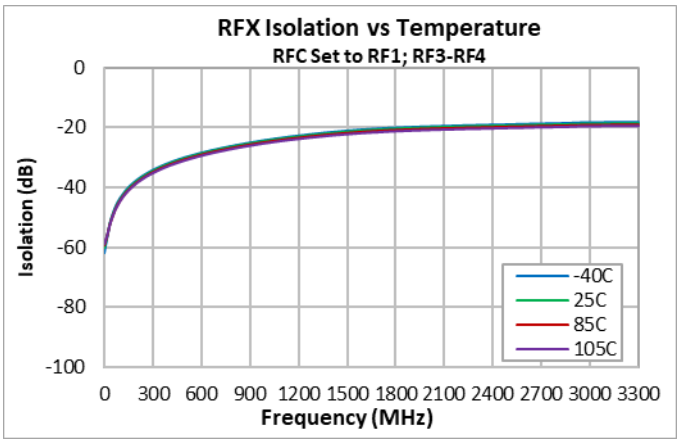
Additional Applications; Performance Plots (QPC6742-4001A EVB)

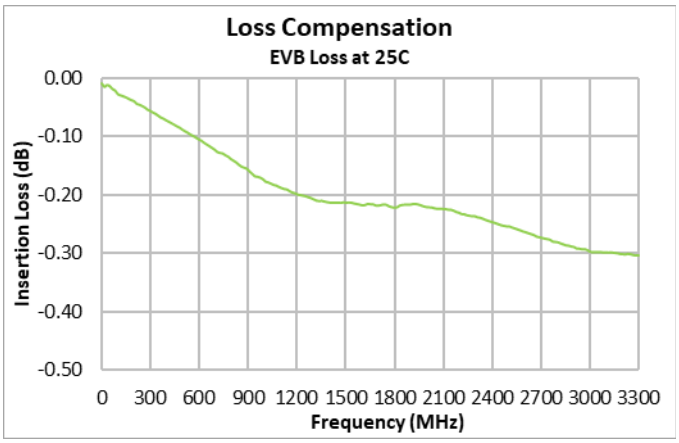








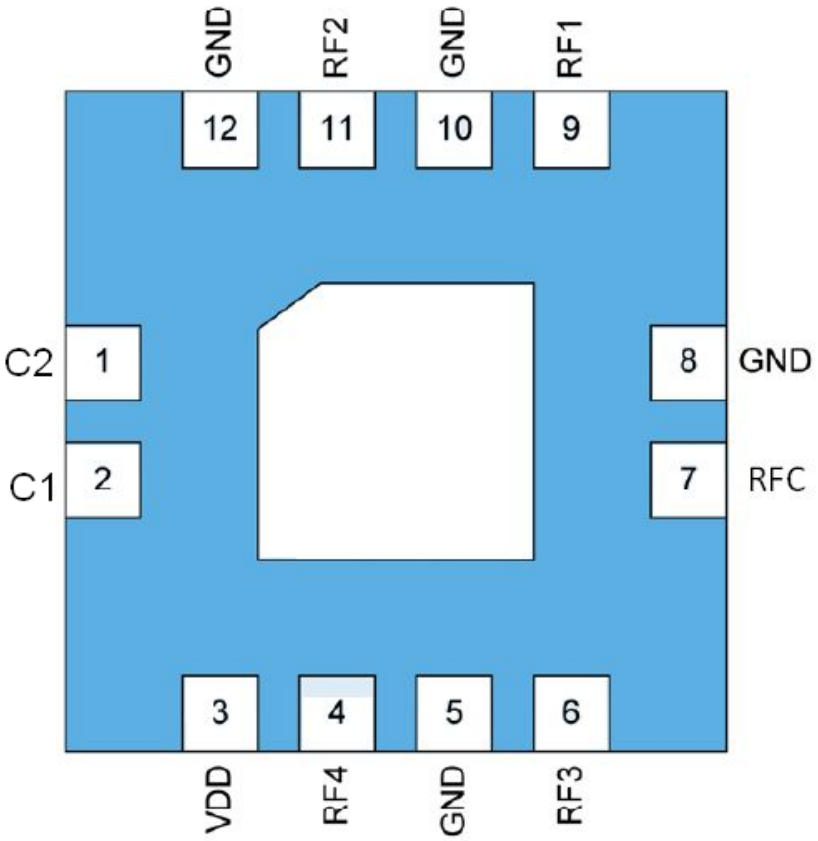




Notes:

1. VDD =+3.0V, VC2, C1= 0 / 2.5V, Temp= +25°C, Zo = 75Ω

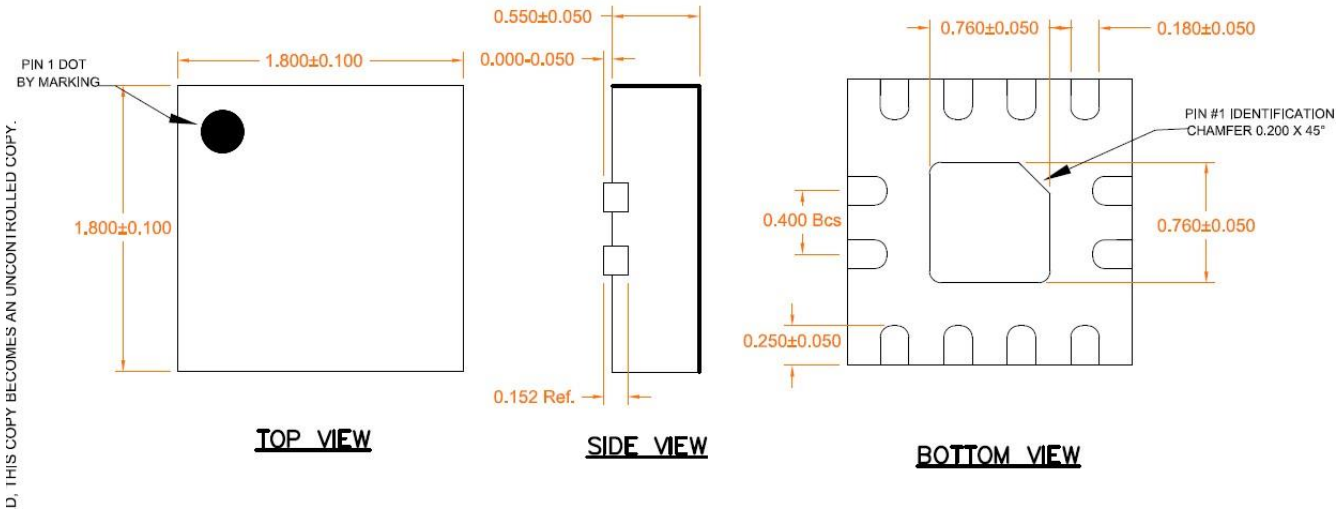
Pin Configuration and Description



Top View

Pad No.	Label	Description
1	C2	Switch Logic Control 2
2	C1	Switch Logic Control 1
3	VDD	Supply Voltage
4	RF4	RF Output Port
5	GND	Ground
6	RF3	RF Output Port
7	RFC	RF Input Port
8	GND	Ground
9	RF1	RF Output Port
10	GND	Ground
11	RF2	RF Output Port
12	GND	Ground

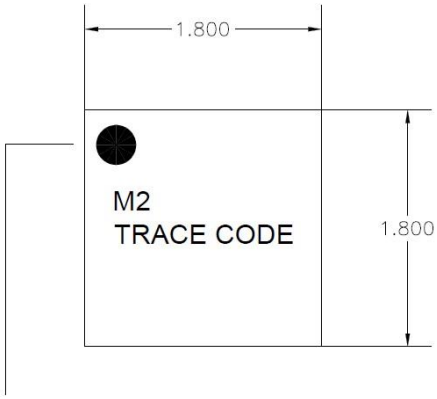
Package Dimensions



Notes:

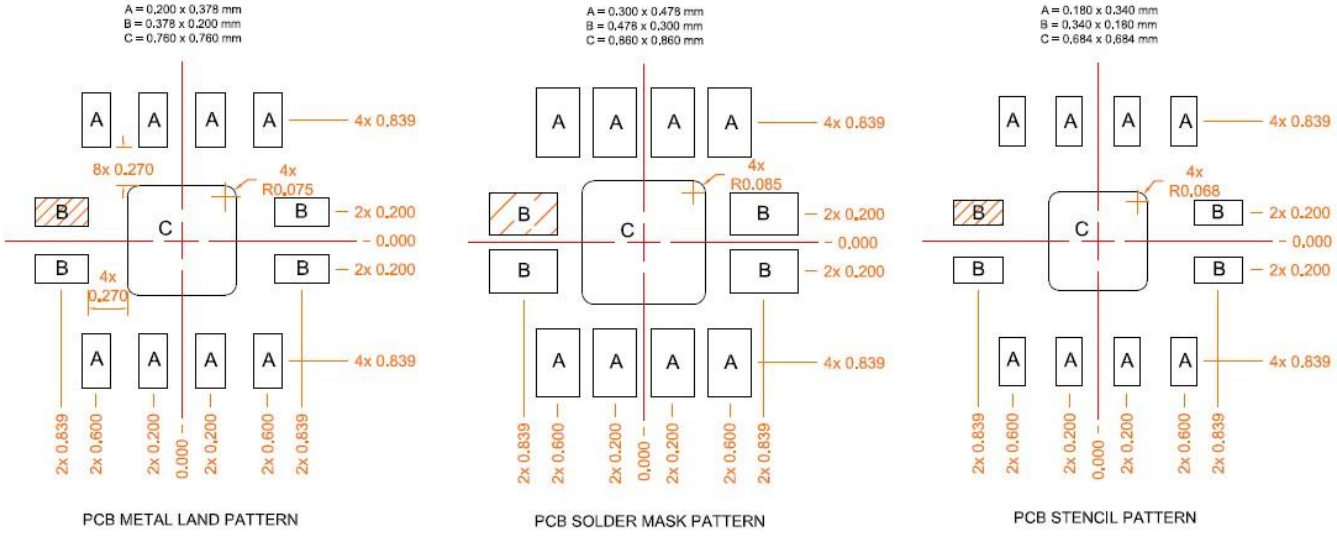
1. All dimensions are in millimeters. Angles are in degrees.
2. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.
3. Contact plating: Matte Sn

Package Marking



Pin 1 Indicator
Trace Code to be assigned by SubCon

Recommended Footprint



Notes:

1. All dimensions are in millimeters. Angles are in degrees.