QPC7332

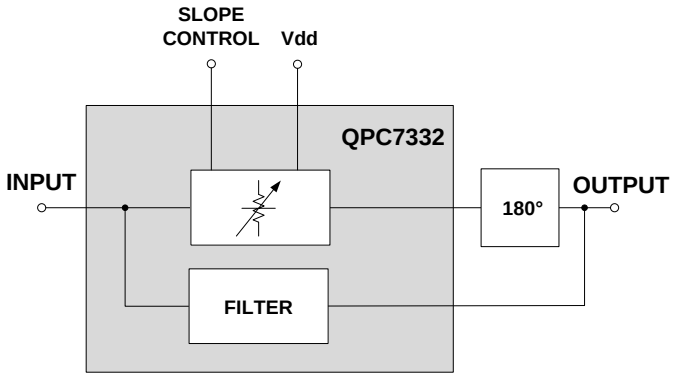
45MHz to 1218MHz Variable Cable Slope Equalizer

Product Description

The QPC7332 is a voltage controlled variable equalizer employing SOI attenuator, optimized for cable loss compensation between 45MHz and 1218MHz.

14 pin, 6.0 mm x 6.0 mm x 1.375 mm package

Functional Block Diagram



Product Features

- 45 – 1218 MHz Operational Bandwidth
- Inverse cable loss frequency response
- 20dB slope range
- Low insertion loss
- High linearity
- 75Ohm impedance for CATV applications
- 5V single supply voltage
- Low power consumption

Applications

CATV amplifier and transmission systems

Ordering Information

Part No.	Description
QPC7332SB	Sample bag 5 pcs
QPC7332SR	7” Reel with 100 pcs
QPC7332TR7	7” Reel with 500 pcs
QPC7332PCBA-410	Fully assembled Evaluation Board

Absolute Maximum Ratings

Parameter	Value / Range
Supply Voltage (Vdd)	-0.5 to +6V
Control Voltage (Vc)	-0.5 to +6V
Control Voltage 2 (Vc2)	-2 to +24V
MODE	-0.5 to +6V
Storage Temperature	−40 to 100 °C
RF Input Power	+30 dBm

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Supply Voltage (Vdd)		+5		V
Junction Temperature			+125	°C
Operating Temperature	-30		+100	°C

Electrical specifications are measured at specified test conditions in application circuit. Specifications are not guaranteed over all recommended operating conditions.

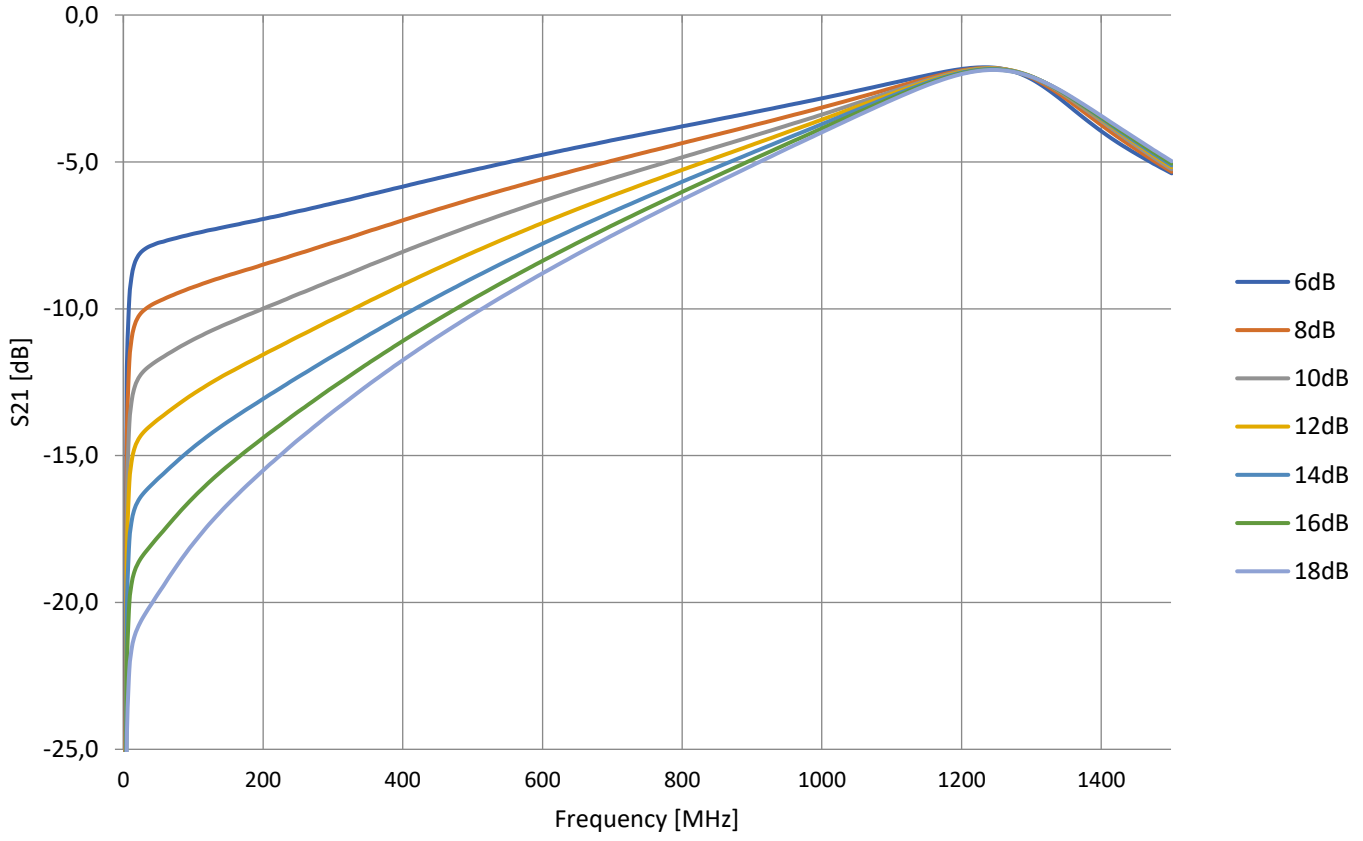
Electrical Specifications – Tested in Evaluation Circuit

Parameter	Conditions (Vdd=5V, T_{MB}=25°C, Z_S=Z_L=75Ω)	Min	Typ	Max	Units
General Performance					
Supply Current (I_{dd})			2.7	3	mA
Thermal Resistance			70		K/W
RF Input Power				27	dBm
Frequency Range		45		1218	MHz
Minimum Slope [1]	f= 45 to 1218MHz		0.3		dB
Maximum Slope [1]	f= 45 to 1218MHz		20		dB
RF Performance, slope set between 8dB and 18dB					
Insertion Loss (S21)	f= 1218MHz		2.2	2.5	dB
Flatness [2]	f= 45 to 1218MHz		<0.7	0.75	dB
Input Return Loss (S11)	f= 45 to 1218MHz		-17		dB
Output Return Loss (S22)	f= 45 to 1218MHz		-16		dB
Input IP3	P_{IN} + ($IM3_{dBc}$/2) 6MHz tone spacing at 15dBm/tone		50		dBm
Input IP2	P_{IN} + $IM2_{dBc}$, IM2 is F1 + F2 6MHz tone spacing at 15dBm/tone		80		dBm
RF Performance, slope set between 1dB and 20dB					
Insertion Loss (S21)	f= 1218MHz		2.3		dB
Flatness [2]	f= 45 to 1218MHz		<1.2	1.3	dB
Input Return Loss (S11)	f= 45 to 1218MHz		-15		dB
Output Return Loss (S22)	f= 45 to 1218MHz		-16		dB

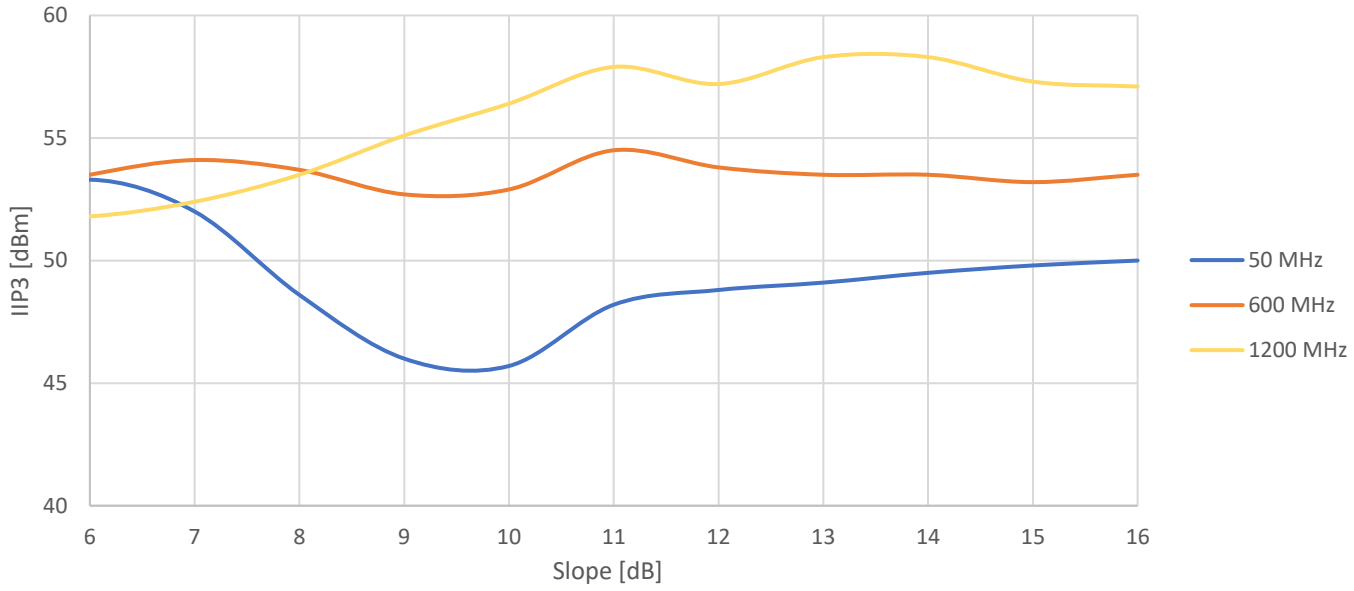
Parameter	Conditions (Vdd=5V, T_{MB}=25°C, Z_S=Z_L=75Ω)	Min	Typ	Max	Units
Control					
Control Voltage (Vc) [3], positive slope control gradient	MODE = 0V, minimum slope at Vc = 0V	0	1 to 3	5	V
Control Voltage (Vc) [3], negative slope control gradient	MODE = 5V, minimum slope at Vc = 5V	0	2 to 4	5	V
Control Voltage 2 (Vc2) [3], positive slope control gradient	MODE = 0V, minimum slope at Vc2 = 0V	0	4 to 12	20	V
Control Voltage 2 (Vc2) [3], negative slope control gradient	MODE = 5V, minimum slope at Vc2 = 20V	0	8 to 16	20	V
MODE Pin Logic Low				0.4	V
MODE Pin Logic High		1			V

Notes:
1. Slope is defined as the difference between the gain at the start frequency and the gain at the stop frequency.
2. Flatness is defined as sum of positive and negative deviation from a polynomial (inverse of typical coaxial cable loss over frequency) between gain at start frequency and gain at stop frequency.
3. Either Vc or Vc2 can be used to set slope, internal 1:4 voltage divider between Vc and Vc2.

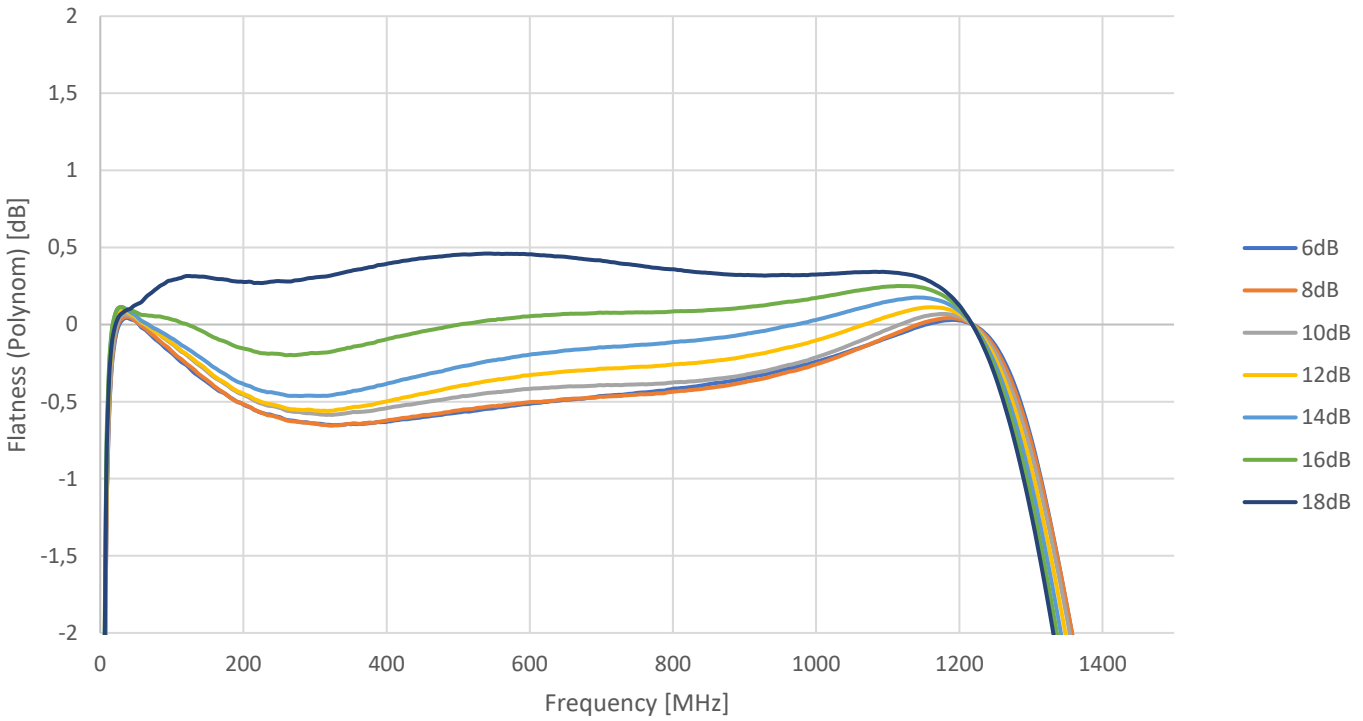
QPC7332 Slope vs. Frequency, typical



QPC7332 Input IP3 vs. Slope, typical

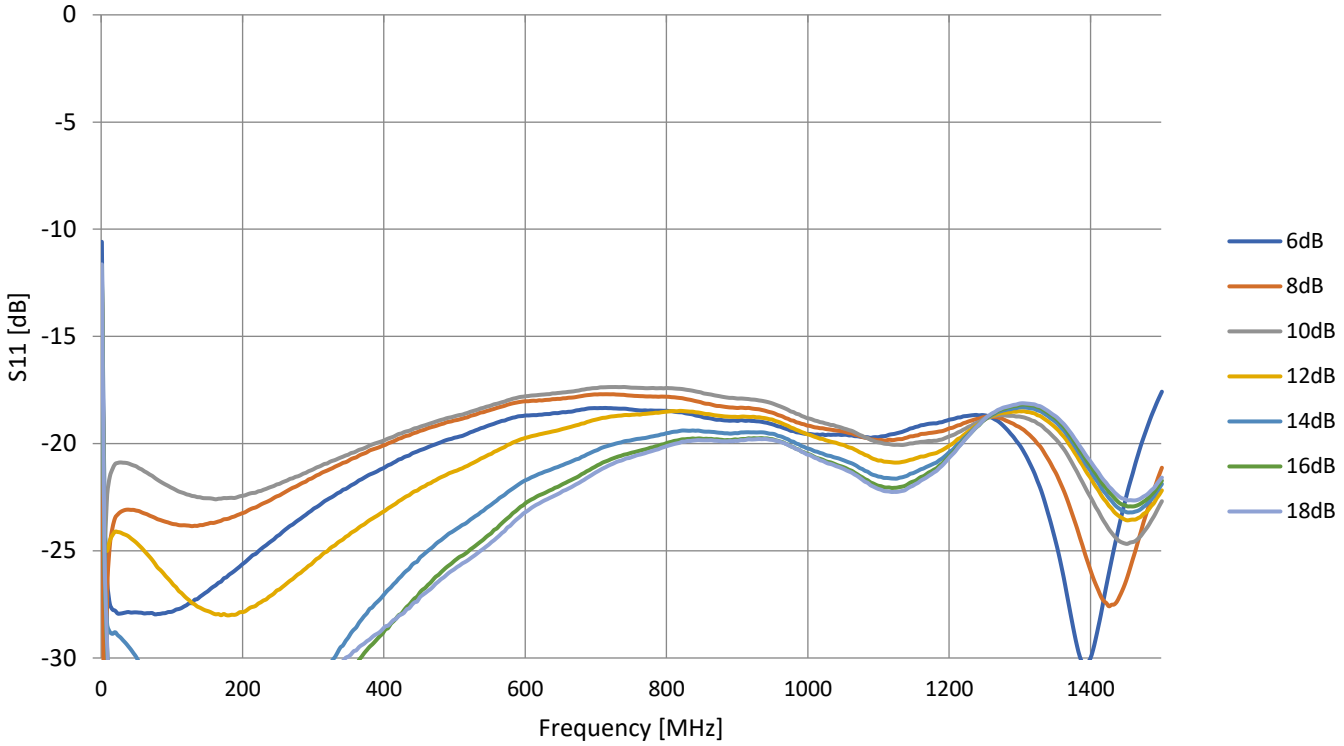


QPC7332 Flatness vs. Slope, typical

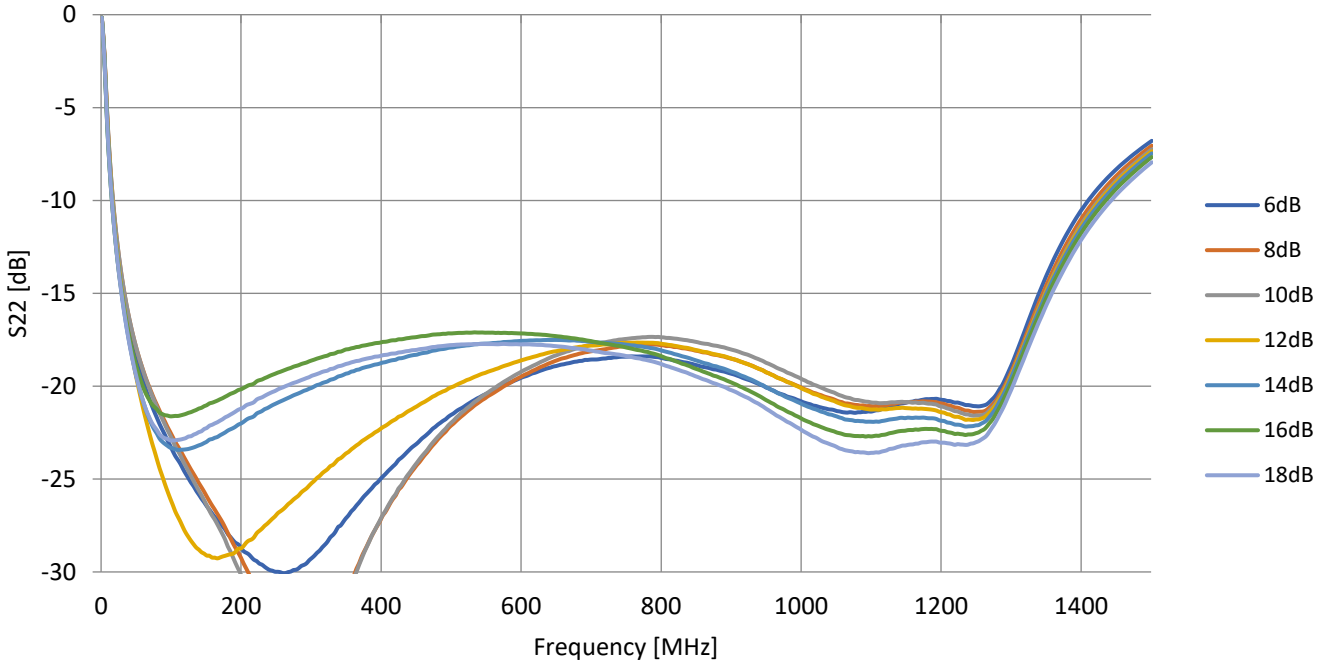


Flatness is measured against a polynomial inverse to the typical cable loss/100ft of -(0.175*$\sqrt{f[MHz]}$+0.001*f[MHz])

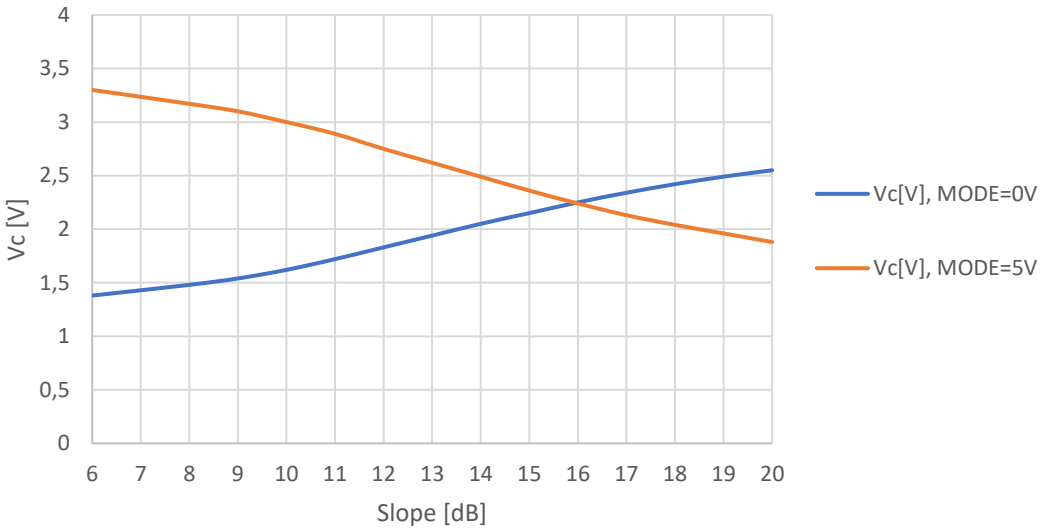
QPC7332 S11 vs. Slope, typical



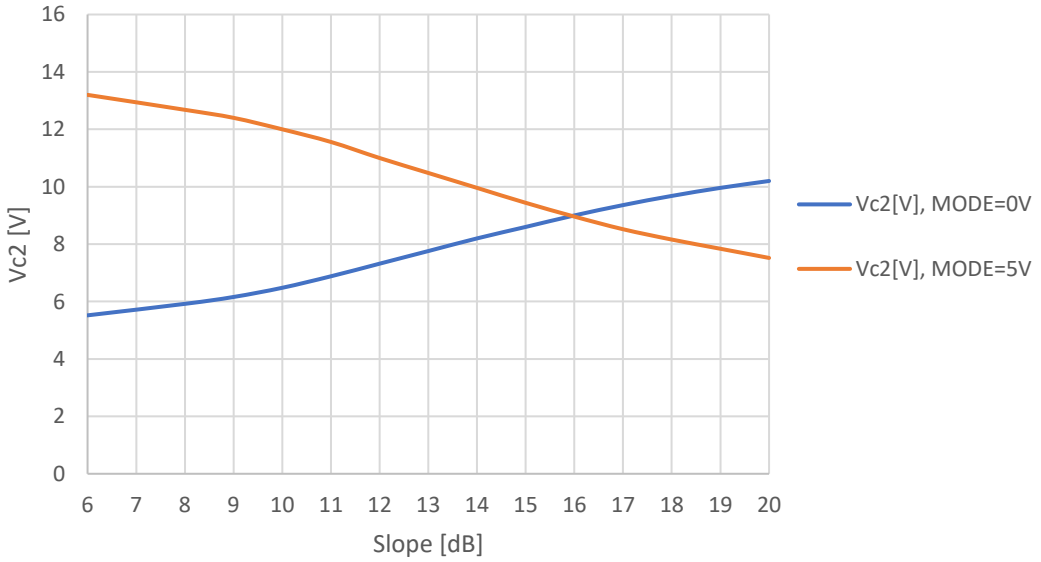
QPC7332 S22 vs. Slope, typical



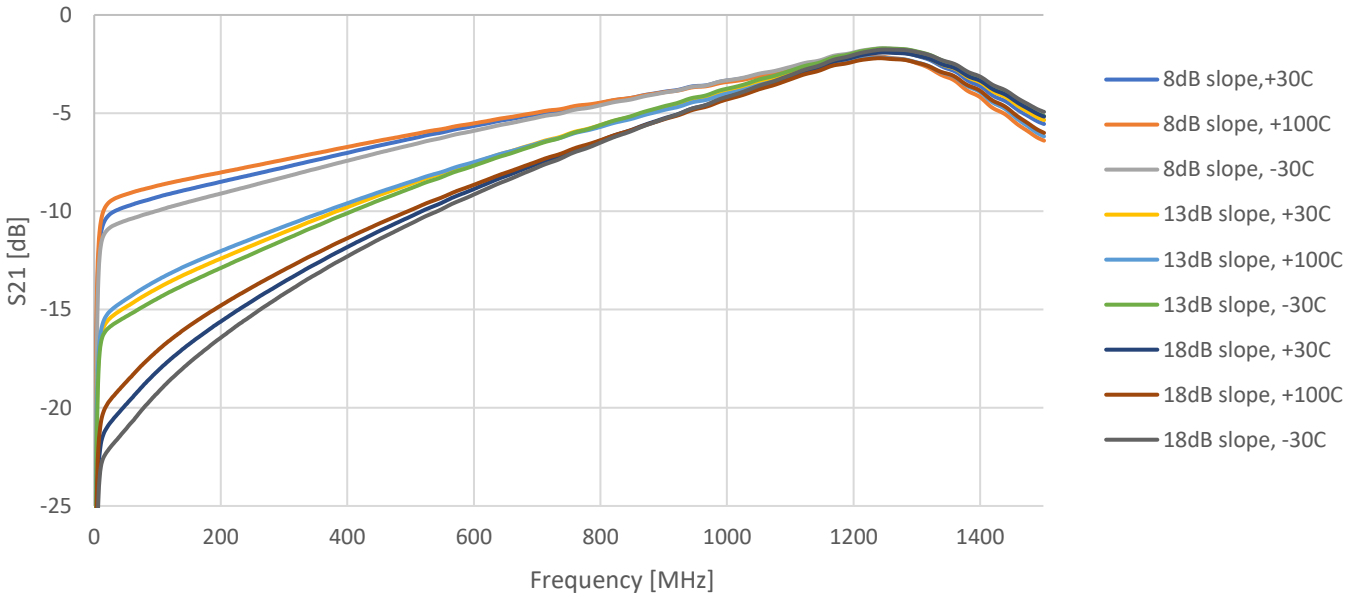
QPC7332 Slope vs. Vc, typical



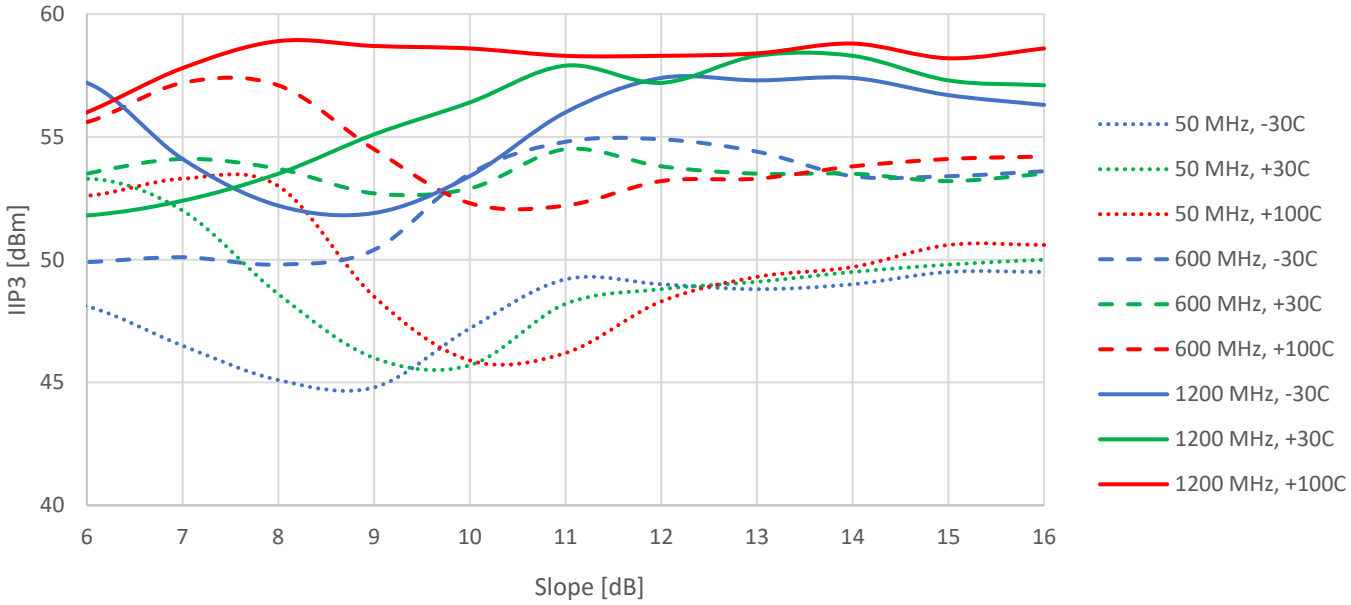
QPC7332 Slope vs. Vc2, typical



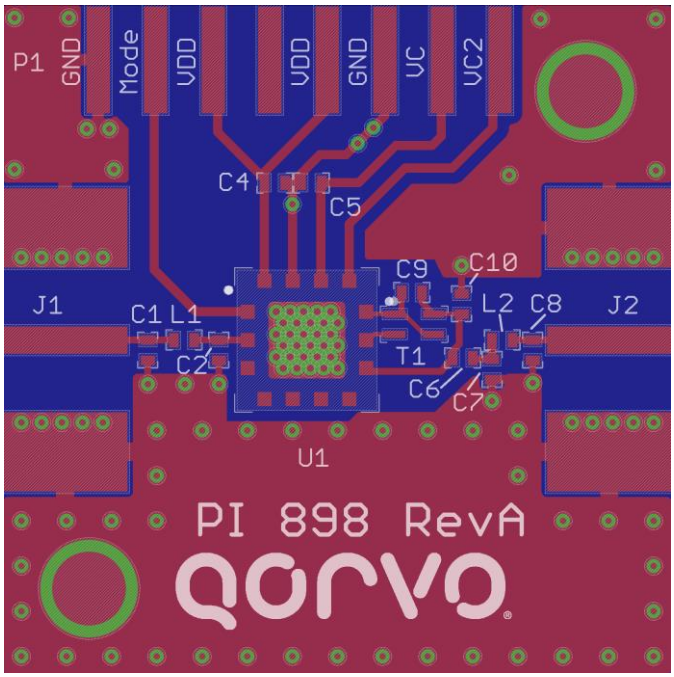
QPC7332 Slope vs. Temperature, typical



QPC7332 Input IP3 vs. Temperature, typical



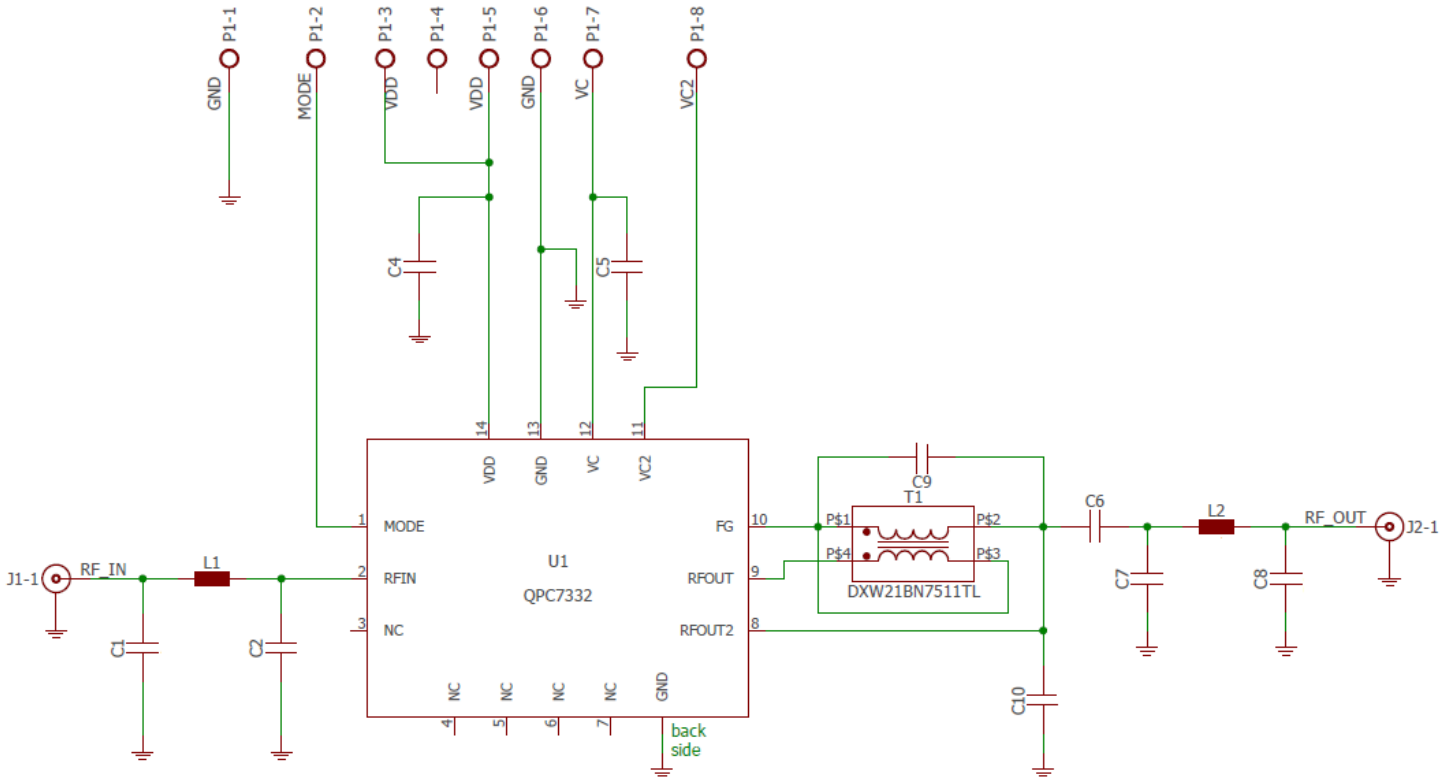
Evaluation Board Assembly Drawing



The ground plane of the QPC7332 module should be soldered onto a board equipped with thermal vias. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25mm (0.010").
In any case the module backside temperature should not exceed 110 °C.

Evaluation board PCB: FR4, double sided, 1.5mm, 35um Cu

Evaluation Board Schematic



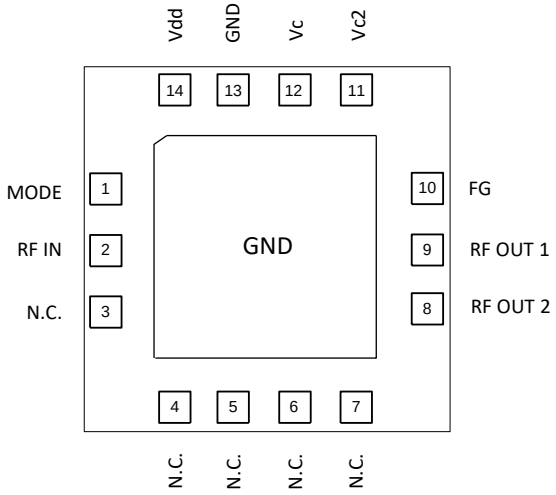
Evaluation Board Bill of Materials (BOM)

Ref. Designator	Value, package	Description	Manufacturer	Part Number
C1	0.7pF, C0G, 0402	Chip capacitor	MURATA, TAIYO YUDEN	
C2, C7, C8	DNI			
C4, C5	4.7nF, X7R, 0402	Chip capacitor	MURATA, TAIYO YUDEN	
C6	1nF, X7R, 0402	Chip capacitor	MURATA, TAIYO YUDEN	
C9	1.2pF, C0G, 0402	Chip capacitor	MURATA, TAIYO YUDEN	
C10	0.2pF, C0G, 0402	Chip capacitor	MURATA, TAIYO YUDEN	
L1, L2	4.7nH, 0402	Chip inductor	TAIYO YUDEN MURATA	HK1005 4N7S LQG15HS4N7S
T1		Transformer	Murata	DXW21BN7511TL
J1, J2		Connector F-type, female	Amphenol	222181
P1		Connector, 2.54mm pin spacing, optional	various	
U1		Variable equalizer	QORVO	QPC7332

Notes: C1, L1, C2, C7, L2 and C8 may be modified in target application circuit for S11 and S22 optimization

Pin Configuration

Top view

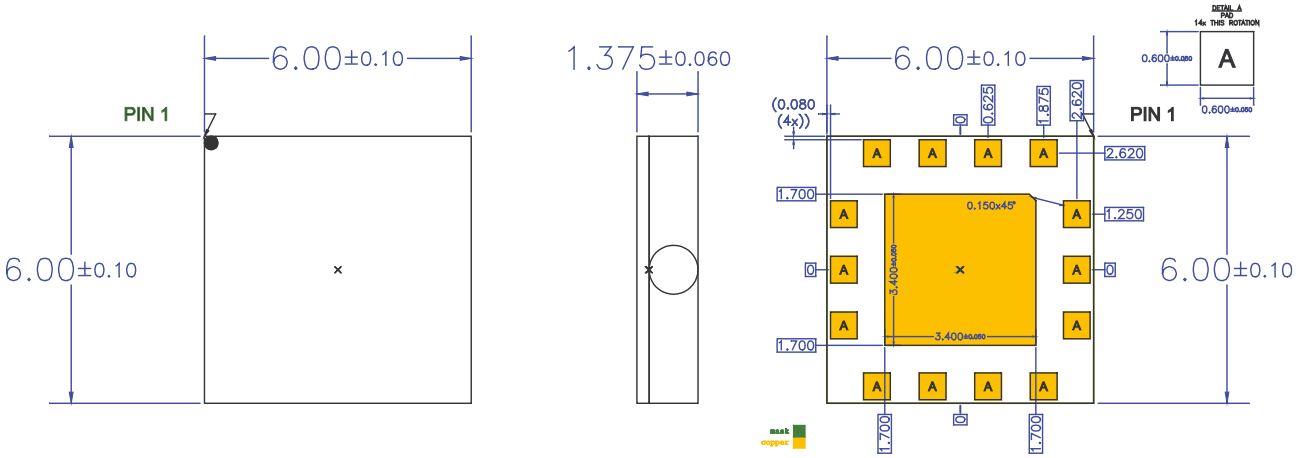


Pin Description

Pin No.	Label	Description
1	MODE	Slope control gradient (0V: positive slope control gradient or 5V: negative slope control gradient)
2	RF IN	RF input signal, AC coupled
8	RF OUT 2	Connection to balun and circuit output
9	RF OUT 1	Connection to balun
10	FG	Floating ground, connection to balun
11	Vc2	Control voltage 2
12	Vc	Control voltage
13, GND	GND	Ground
14	Vdd	+5V supply voltage
3, 4, 5, 6, 7	N.C.	Not connected

Notes: Either Pin11 or Pin12 can be used to set slope, internal 1:4 voltage divider between Pin11 and Pin12

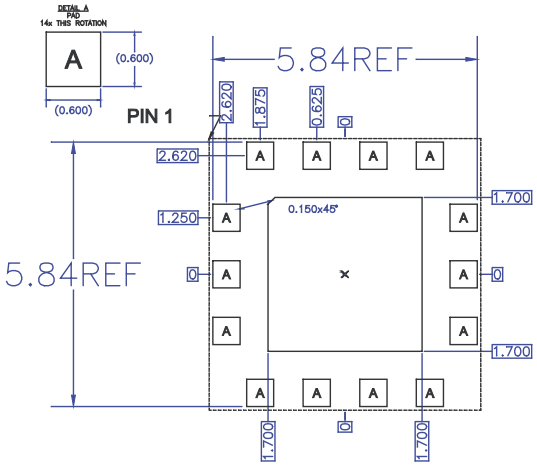
Package Outline Drawing (Dimensions in millimeters)



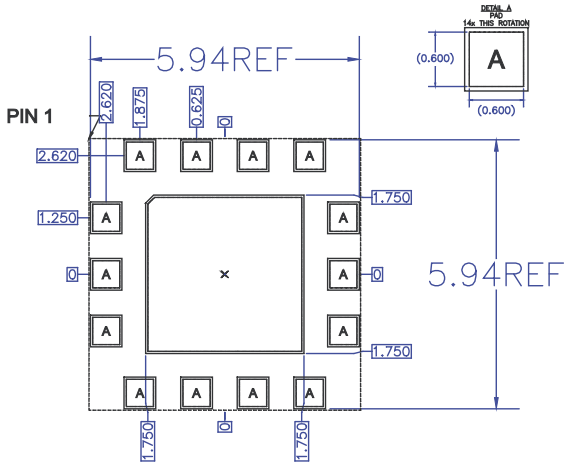
TOP VIEW SIDE VIEW BOTTOM VIEW

Notes:
1. Dimension and tolerance formats conform to ASME Y14.5M-1994.
2. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.
3. Co-planarity applies to the exposed ground/thermal pad as well as the contact pins.
4. Package body length/width does not include plastic flash protrusion across mold parting line.

PCB Metal Land Pattern (Dimensions in millimeters)



RECOMMENDED
LAND PATTERN



RECOMMENDED
LAND PATTERN MASK

All dimensions are in millimeters. Angles are in degrees.