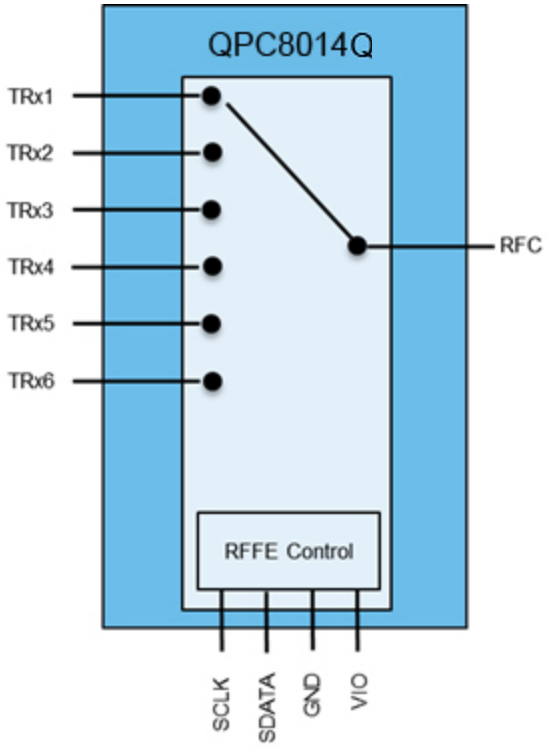
QPC8014Q

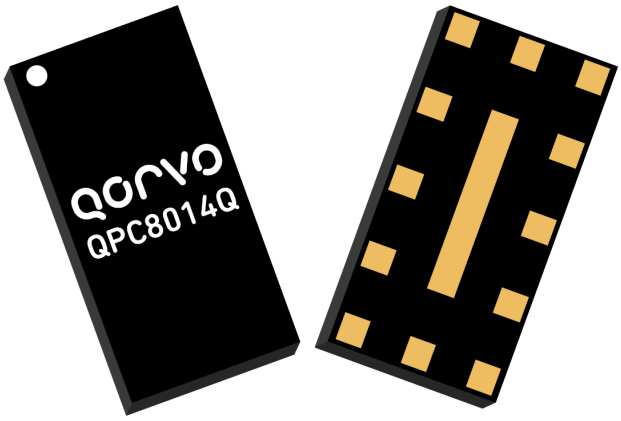
SP6T Switch For LTE Applications

Product Description

The QPC8014Q is a low loss, high isolation SP6T switch with performance optimized for LTE and diversity applications. The QPC8014Q is packaged in an ultra compact 1.1mm x 1.9mm x 0.44mm, 13-pin, Module package which allows for the smallest solution size with no need for external DC blocking capacitors (when no external DC is applied to the device ports).

Functional Block Diagram





13 Pin 1.1 x 1.9 x 0.44 mm Module Package

Feature Overview

- Qualified to AEC-Q100 Grade 3
- Excellent insertion loss and isolation performance
  - 0.33dB Typ IL, Band 5
  - 45dB Typ Isolation, Band 5
- Multi-Band operation from 617MHz to 6000MHz
- RFFE 2.0 compatible
- DC blocking capacitors are not required in typical applications

Applications

- Automotive Telematics Modules
  LTE and Diversity Applications

Ordering Information

PART NO.	DESCRIPTION
QPC8014QSB	5-pc Sample Bag
QPC8014QSR	100-pc, 7” Reel
QPC8014QTR13	10,000-pc, 13” Reel
QPC8014QDK	Design Kit including EVB + SB

Absolute Maximum Ratings

PARAMETER	RATING
Storage Temperature	-45 to +125 °C
V_{IO}	2.5 V
SDATA, SCLK	2.5 V
Maximum Input Power (Electrical point of view)	37 dBm , 1:1 VSWR. 100% Duty Cycle, CW, +105C 34 dBm, 3:1 VSWR, 100% Duty Cycle, CW, +105C
Maximum Input Power (Thermal point of view)	35 dBm , 1:1 VSWR. 100% Duty Cycle, CW, +85C, Tj=125C
Maximum Input Power (Thermal point of view)	32 dBm , 1:1 VSWR. 100% Duty Cycle, CW, +105C, Tj=125C

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

PARAMETER	MIN.	TYP.	MAX.	UNITS
Operating Ambient Temperature(1)	-40	+25	+85	˚C
V_{IO} Supply Voltage	1.65	1.8	1.95	V
V_{IO} Supply Current (Active Mode)		27	35	µA
V_{IO} Supply Current (Low Power Mode)		4	6	µA
SDATA, SCLK Logic Low (Input)	0.00	0.00	0.3 x VIO	V
SDATA, SCLK Logic High (Input)	0.7 x VIO	1.8	VIO	V
SDATA Logic Low (Output)	0.00	0.00	0.2 x VIO	V
SDATA Logic High (Output)	0.8 x VIO	1.8	VIO	V
SDATA, SCLK Logic High Current		0.1	5	µA
Turn-On Time			20	µs
Switching Speed		3.2		µs

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

1)Case temperature allows 10˚C max rise over Ambient.

Electrical Specifications[1]

Test conditions unless otherwise stated: all unused RF ports terminated in 50Ω, Input and Output = 50Ω, T = 25°C, V_{IO} = 1.8V

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Insertion Loss					
RFx to RFC	617MHz to 960MHz		0.33	0.5	dB
RFx to RFC	1710MHz to 2170MHz		0.44	0.65	dB
RFx to RFC	2300MHz to 2690MHz		0.54	0.9	dB
RFx to RFC	3300MHz to 4200MHz		0.75		dB
RFx to RFC	4400MHz to 5000MHz		0.85		dB
RFx to RFC	5100MHz to 6000MHz		1.25		dB
RFx to RFC*	5100MHz to 6000MHz		0.83		dB
Isolation					
RFx to RFx	See Isolation Matrix				
RFx to RFC	See Isolation Matrix				
Harmonics					
Low Band, 2fo	Pin = +26dBm, 50Ω, f_0= 824MHz		-81	-70	dBm
Low Band, 3fo	Pin = +26dBm, 50Ω, f_0= 824MHz		-69	-60	dBm
Mid Band, 2fo	Pin = +26dBm, 50Ω, f_0= 1980MHz		-75	-57	dBm
Mid Band, 3fo	Pin = +26dBm, 50Ω, f_0= 1980MHz		-67	-60	dBm
High Band, 2fo	Pin = +26dBm, 50Ω, f_0= 2570MHz		-72	-60	dBm
High Band, 3fo	Pin = +26dBm, 50Ω, f_0= 2570MHz		-66	-60	dBm
IMD2					
Low Band	TX Carrier @ 897.5MHz at +21dBm CW Blocker @ 1840 MHz at -15dBm Measured RX frequency @ 942.5MHz		-117		dBm
High Band	TX Carrier @ 1880MHz at +21dBm CW Blocker @ 3840 MHz at -15dBm Measured RX frequency @ 1960MHz		-118		dBm
IMD3					
Low Band	TX Carrier @ 897.5MHz at +21dBm CW Blocker @ 852.5MHz at -15dBm Measured RX frequency @ 942.5MHz		-121		dBm
High Band	TX Carrier @ 1880MHz at +21dBm CW Blocker @ 1800MHz at -15dBm Measured RX frequency @ 1960MHz		-110		dBm

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
VSWR					
	617 MHz to 960 MHz		1.1		:1
	1710 MHz to 2170 MHz		1.35		:1
	2300 MHz to 2690 MHz		1.55		:1
	3300 MHz to 4200 MHz		1.6		:1
	4400 MHz to 5000 MHz		1.55		:1
	5100 MHz to 6000 MHz		1.7		:1

* See tuning schematic for 5000MHz to 6000MHz insertion loss
[1)] Recommended EVB schematic / layout / BOM / PCB should be followed in order to achieve specified performance.

Isolation Matrix Low Band (617MHz – 960MHz)

STATE	INSERTION PORT	ISOLATION, TYPICAL (dB)					
		RF1	RF2	RF3	RF4	RF5	RF6
RF1	RF1		45	36	53	48	54
RF2	RF2	46		53	36	52	47
RF3	RF3	35	49		54	38	55
RF4	RF4	50	36	55		53	37
RF5	RF5	43	51	36	53		54
RF6	RF6	52	43	54	36	54	
RF1	RFC		54	40	52	49	44
RF2	RFC	54		51	40	43	50
RF3	RFC	39	55		51	43	45
RF4	RFC	54	39	50		43	43
RF5	RFC	50	53	40	52		46
RF6	RFC	53	49	51	40	45	

Isolation Matrix Mid Band (1710MHz – 2170MHz)

STATE	INSERTION PORT	ISOLATION, TYPICAL (dB)					
		RF1	RF2	RF3	RF4	RF5	RF6
RF1	RF1		36	28	41	37	42
RF2	RF2	36		41	28	42	36
RF3	RF3	27	39		42	28	42
RF4	RF4	39	27	41		41	29
RF5	RF5	35	40	28	41		40
RF6	RF6	40	35	41	28	40	
RF1	RFC		40	32	39	36	35
RF2	RFC	41		39	32	34	36
RF3	RFC	31	41		39	33	35
RF4	RFC	41	31	39		34	33
RF5	RFC	38	40	32	40		36
RF6	RFC	40	38	39	32	35	

Isolation Matrix High Band (2300MHz – 2690MHz)

STATE	INSERTION PORT	ISOLATION, TYPICAL (dB)					
		RF1	RF2	RF3	RF4	RF5	RF6
RF1	RF1		33	25	37	33	39
RF2	RF2	33		37	26	38	33
RF3	RF3	24	35		38	25	38
RF4	RF4	35	25	37		38	25
RF5	RF5	32	36	25	37		36
RF6	RF6	36	32	37	25	36	
RF1	RFC		37	30	36	32	32
RF2	RFC	37		35	30	31	32
RF3	RFC	28	37		36	29	32
RF4	RFC	37	29	35		31	29
RF5	RFC	35	37	30	36		33
RF6	RFC	36	35	36	30	32	

Isolation Matrix Ultra High Band (3200MHz – 3800MHz)

STATE	INSERTION PORT	ISOLATION, TYPICAL (dB)					
		RF1	RF2	RF3	RF4	RF5	RF6
RF1	RF1		28	21	32	28	34
RF2	RF2	28		32	22	33	28
RF3	RF3	20	31		33	21	33
RF4	RF4	30	21	32		33	21
RF5	RF5	27	31	22	32		31
RF6	RF6	31	28	32	22	31	
RF1	RFC		32	27	31	27	27
RF2	RFC	32		30	27	27	27
RF3	RFC	25	32		31	24	28
RF4	RFC	32	26	31		27	25
RF5	RFC	29	31	27	31		28
RF6	RFC	31	30	31	27	27	

Isolation Matrix LTE-U Band (5000MHz – 6000MHz)

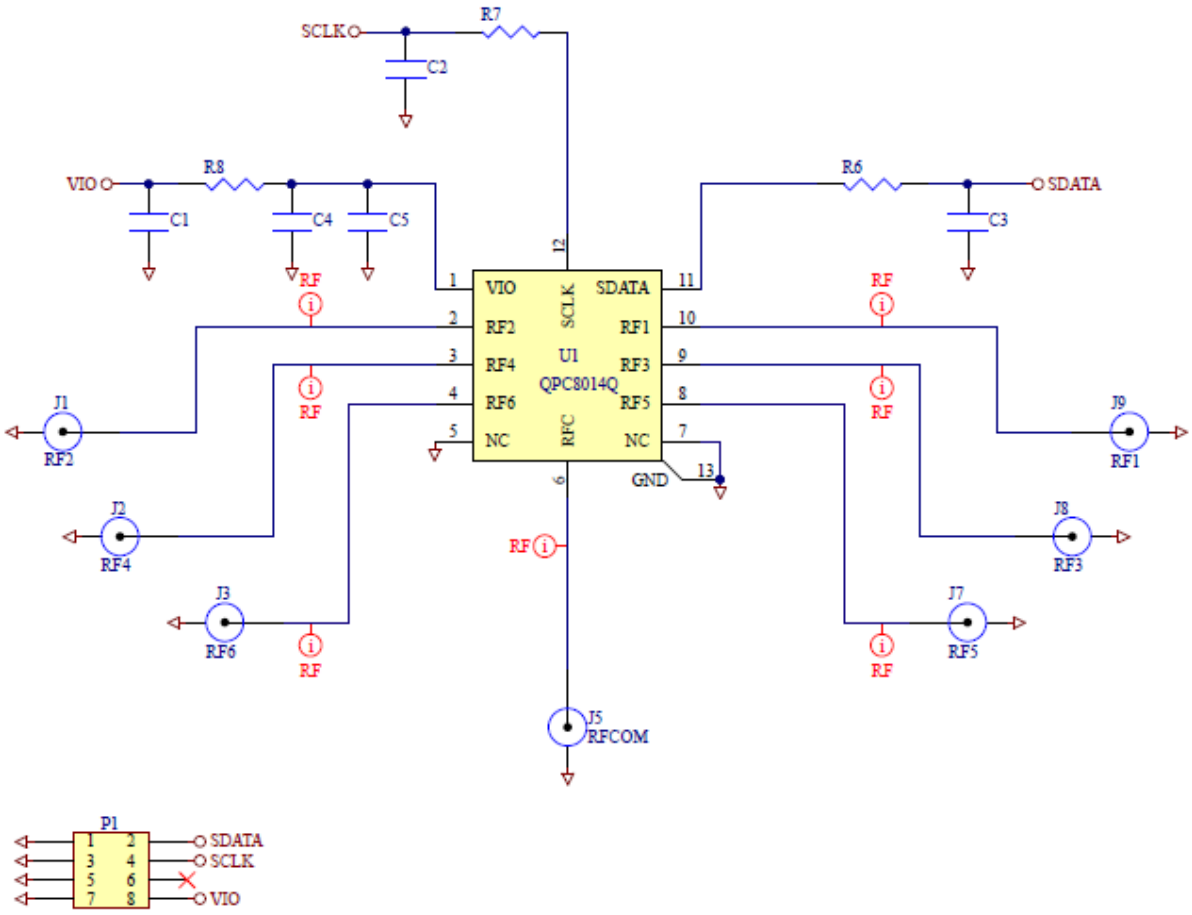
STATE	INSERTION PORT	ISOLATION, TYPICAL (dB)					
		RF1	RF2	RF3	RF4	RF5	RF6
RF1	RF1		22	16	26	22	27
RF2	RF2	22		26	17	27	22
RF3	RF3	15	24		27	16	27
RF4	RF4	24	16	26		27	16
RF5	RF5	22	25	17	26		25
RF6	RF6	24	22	25	17	24	
RF1	RFC		26	22	25	20	22
RF2	RFC	26		25	24	21	22
RF3	RFC	22	26		25	19	22
RF4	RFC	26	22	25		21	20
RF5	RFC	23	25	23	25		22
RF6	RFC	25	23	25	23	21	

Evaluation Board PCB Information

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	0.70mil		
4	Dielectric1	Rogers 4003	8.00mil	3.55	
5	Signal Layer 1	Copper	0.70mil		
6	Dielectric 3	FR4	8.00mil	4.2	
7	Signal Layer 2	Copper	0.70mil		
8	Dielectric 4	FR4	24.00mil	4.2	
9	Signal Layer 3	Copper	0.70mil		
10	Dielectric 5	FR4	8.00mil	4.2	
11	Signal Layer 4	Copper	0.70mil		
12	Dielectric 2	FR4	8.00mil	4.2	
13	Bottom Layer	Copper	1.40mil		
14	Bottom Solder	Solder Resist	0.40mil	3.5	
15	Bottom Overlay				

Total Thickness: 62mil +/- 10%

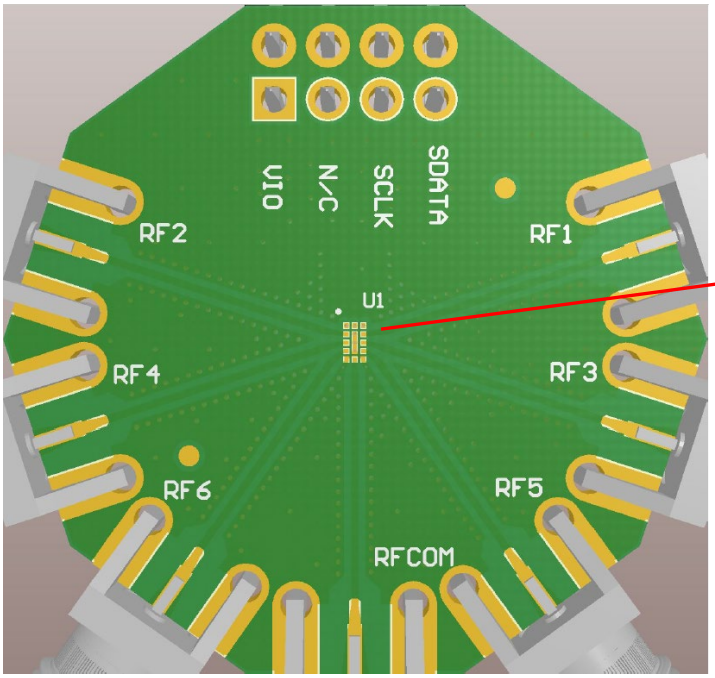
Application Circuit Schematic

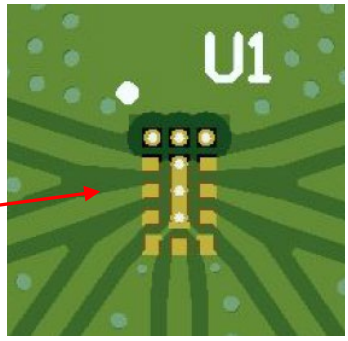


Evaluation Board BOM

Qty	Ref Des	Description	UOM
1	U1	Automotive RFFE LTE SP6T Switch	EA
1	PCB	PCB, QPC8014Q	EA
1	C4	CAP, 100pF, 5%, 25V, C0G, 0201	EA
3	R6,R7,R8	RES, 0 OHM, 5%, 1/20W, 0201	EA
7	RF1,RF2,RF3,RF4,RF5,RF6,RFCOM	CONN, SMA, EL MINI FLT 0.068" SPE-000303	EA
1	P1	CONN, HDR, SHRD, RT-ANG, 2x4, 0.100"	EA
4	C1,C2,C3,C5	NOT POPULATED ITEM-1	EA

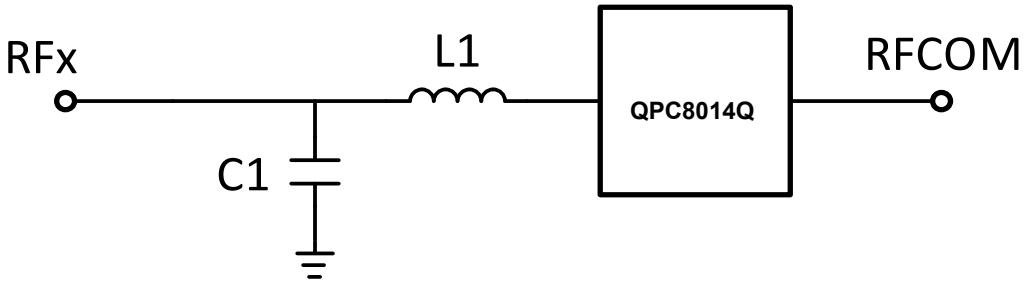
Evaluation Board





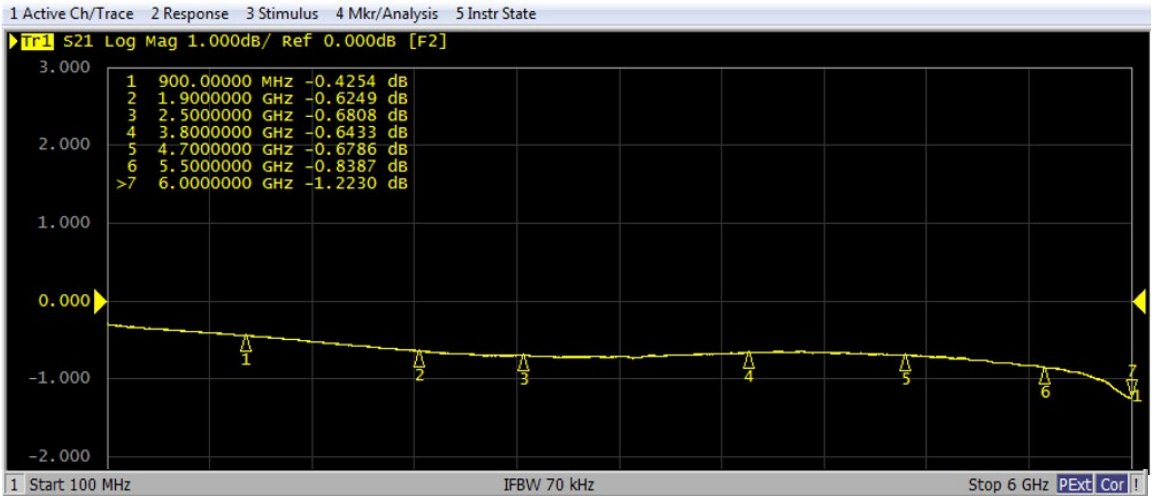
3 vias placed on center pad for thermal conduction

Tuning Schematic and Plot for 5000MHz – 6000MHz

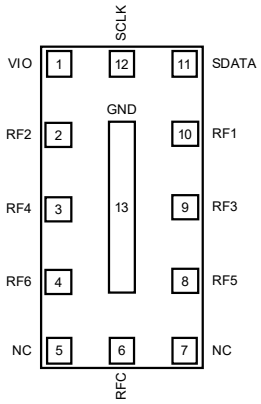


NAME	VALUE	PACKAGE	DESCRIPTION
C1	0.4pF	0201	Matching for optimized RF performance*
L1	1.1nH	0201	Matching for optimized RF performance*

* Matching elements are subject to change based on specific system application



Pin Configuration and Description



Top View

PIN NO.	LABEL	DESCRIPTION
1	VIO	Voltage Supply
2	RF2	RF Port
3	RF4	RF Port
4	RF6	RF Port
5	NC	No Connect
6	RFC	RF Common Port
7	NC	No Connect
8	RF5	RF Port
9	RF3	RF Port
10	RF1	RF Port
11	SDATA	RFFE Data Signal
12	SCLK	RFFE Data Signal
13	GND	Ground

RFFE Register Map

Register 0x0000 – SW_CTRL0

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:6	SPARE	Reserved for future use	0x0	No	0 - 2	R/W
5:0	SW_CTRL	0x00: Isolation 0x01: RF1 - RFC 0x02: RF2 - RFC 0x04: RF3 - RFC 0x08: RF4 - RFC 0x10: RF5 - RFC 0x20: RF6 - RFC	0x00	No	0 - 2	R/W

Register 0x0001 – SPARE

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	SPARE	Reserved for future use	0x00	No	0 - 2	R/W

Register 0x001A – RFFE_STATUS

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7	UDR_RST	Setting this bit initiates a software reset *Note: On software reset, this register and all User Defined registers (UDRs) are reset. This bit will always read as 0.*	0	No	No	W
6	CMD_FR_P_ERR	Command Frame received with a parity error	0	No	No	R/W
5	CMD_LEN_ERR	Command Sequence received with an incorrect length	0	No	No	R/W
4	ADDR_FR_P_ERR	Address Frame received with a parity error	0	No	No	R/W
3	DATA_FR_P_ERR	Data Frame received with a parity error	0	No	No	R/W
2	RD_INVLD_ADDR	Read Command Sequence received with an invalid address	0	No	No	R/W
1	WR_INVLD_ADDR	Write Command Sequence received with an invalid address	0	No	No	R/W
0	BID_GID_ERR	Read Command Sequence received with a BSID or GSID	0	No	No	R/W
		Note: Reading this register resets this register.				

Register 0x001B – GSID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:4	GSID0[3:0]	Group Slave ID0	0x0	No	No	R/W
3:0	GSID1[3:0]	Group Slave ID1	0x0	No	No	R/W

Register 0x001C — PM_TRIG

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:6	PWR_MODE[1:0]	00: ACTIVE - Normal Operation 01: STARTUP - Reset all registers to default settings 10: ACTIVE - Low Power - Antenna in isolation 11: STARTUP - Reset all registers to default settings *Note: Setting PWR_MODE to STARTUP is identical to a hardware reset initiated by the VIO signal.*	0b10	B/G	No	R/W
5:3	TriggerMask[2:0]	Setting bit TriggerMask[N] disables Trigger[N] TriggerMask[N] updates before Trigger[N] is processed *Note: When Trigger[N] is disabled, writing to a register associated with Trigger[N] sends data directly to that register.* *If a register is associated with multiple triggers, then all associated triggers must be disabled to allow direct writes to the associated register.*	0b000	No	No	R/W
2:0	Trigger[2:0]	Setting bit Trigger[N] loads Trigger[N]'s associated registers *Note: When Trigger[N] is enabled, writing to a register associated with Trigger[N] sends data to that register's shadow. Setting the Trigger[N] bit loads data from shadow. All triggers are processed immediately and simultaneously and then cleared. Trigger[0], [1], and [2] will always read as 0.*	0b000	B/G	No	W

Register 0x001D — PRODUCT_ID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	PROD_ID[7:0]	Lower eight bits of Product Number *Note: These are read-only registers. However, as part of the special programming sequence for writing USID, a write command sequence is performed on one or both registers, but does not update them. See MIPI 6.6.2 for details.*	0x18	No	No	R

Register 0x001E — MANUFACTURER_ID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	MFG_ID[7:0]	Lower eight bits of MIPI Manufacturer ID *Note: These are read-only registers. However, as part of the special programming sequence for writing USID, a write command sequence is performed on one or both registers, but does not update them. See MIPI 6.6.2 for details.*	0x34	No	No	R

Register 0x001F – MAN_USID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:6	RESERVED	Reserved for future use	0b00	No	No	R
5:4	MFG_ID[9:8]	Upper two bits of MIPI Manufacturer ID *Note: This is a read-only register. However, as part of the special programming sequence for writing USID, a write command sequence is performed on this register, but does not update it. See MIPI 6.6.2 for details.*	0b01	No	No	R
3:0	USID[3:0]	Programmable Unique Slave ID *Note: USID is only writeable using a special programming sequence. See MIPI 6.6.2 for details.*	0x9	No	No	R/W

Register 0x0020 – EXT_PRODUCT_ID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	PROD_ID[15:8]	Upper eight bits of Product Number *Note: These are read-only registers. However, as part of the special programming sequence for writing USID, a write command sequence is performed on one or both registers, but does not update them. See MIPI 6.6.2 for details.*	0x00	No	No	R

Register 0x0021 – REVISION_ID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:6	MAJOR_REV[1:0]	Major Revisions - all layer	0b00	No	No	R
5:4	MINOR_REV[1:0]	Minor Revisions - metal only	0b00	No	No	R
3:0	MISC_REV[3:0]	Misc Revisions - mask variants	0b0001	No	No	R
		Note: The REVISION_ID register contains this product's revision number which is set by Qorvo according to manufacture date. The value may change throughout the product life cycle.				

Register 0x0022 – GSID0-1

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:4	GSID0[3:0]	Group Slave ID0	0x0	No	No	R/W
3:0	GSID1[3:0]	Group Slave ID1	0x0	No	No	R/W

Register 0x0023 – UDR_RST

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7	UDR_RST	Setting this bit initiates a software reset *Note: On software reset, this register and all User Defined registers (UDRs) are reset. This bit will always read as 0.*	0	B/G	No	W
6:0	RESERVED		0x00	No	No	R

Register 0x0024 – ERR_SUM

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7	SPARE	Reserved for future use	0	No	No	R/W
6	CMD_FR_P_ERR	Command Frame received with a parity error	0	No	No	R/W
5	CMD_LEN_ERR	Command Sequence received with an incorrect length	0	No	No	R/W
4	ADDR_FR_P_ERR	Address Frame received with a parity error	0	No	No	R/W
3	DATA_FR_P_ERR	Data Frame received with a parity error	0	No	No	R/W
2	RD_INVLD_ADDR	Read Command Sequence received with an invalid address	0	No	No	R/W
1	WR_INVLD_ADDR	Write Command Sequence received with an invalid address	0	No	No	R/W
0	BID_GID_ERR	Read Command Sequence received with a BSID or GSID	0	No	No	R/W
		Note: Reading this register resets this register.				

Register 0x002C – TEST_PATT

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	TEST_PATT[7:0]	Test Pattern	0xD2	No	No	R

Power On and Off Sequence

It is very important that the user adheres to the correct timing sequences in order to avoid damaging the device. Figures are NOT drawn to scale.

1. Once VIO is powered down to 0V, wait a minimum of 10 µs to reapply power to VIO. (see figure 1)

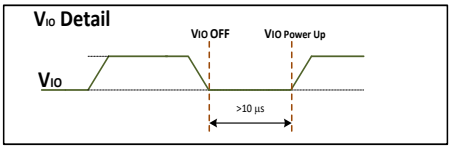


Figure 1 Digital Supply Detail

2. VIO must be applied for a minimum of 120 ns before sending SDATA/SCLK to ensure correct data transmission. (see fig 2)
3. VIO must be applied for a minimum of 15 µs before applying RF power. (see figure 2)
4. Wait a minimum of 5 µs after RFFE bus is idle to apply an RF signal. (see figure 2)

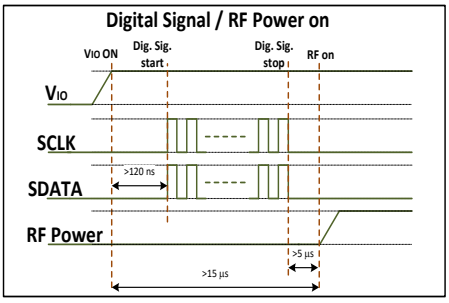


Figure 2 Digital Signal / RF Power-On Detail

5. RF power must not be applied during switching events. To ensure this, remove RF power before completing a register write that will change the switch mode. (see figure 3)

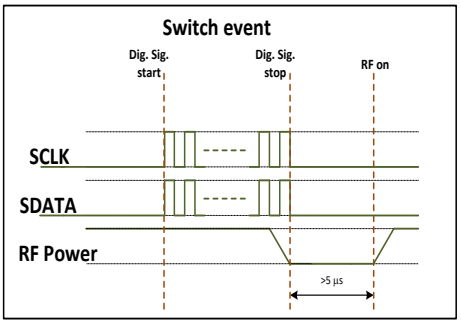


Figure 3 Switch Event Timing

6. If “Low Power Mode” is utilized, there must be a delay of 10 µs before exiting “Low Power Mode”. (see figure 4)

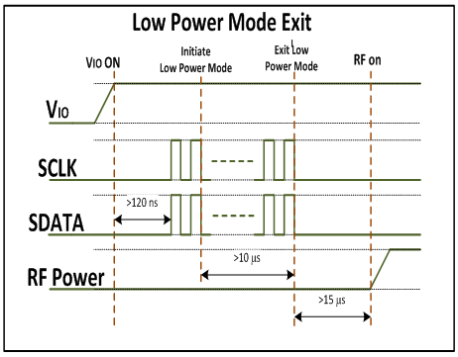
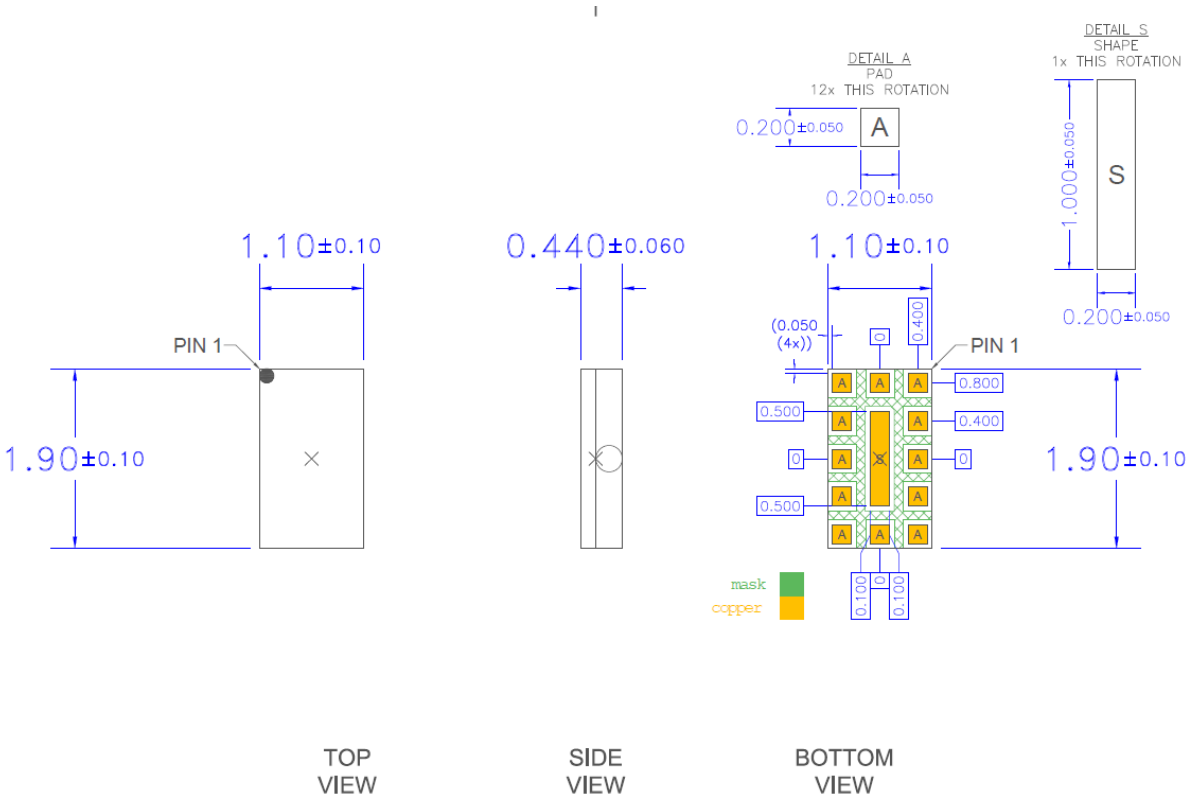


Figure 4 Low Power Mode Exit Timing

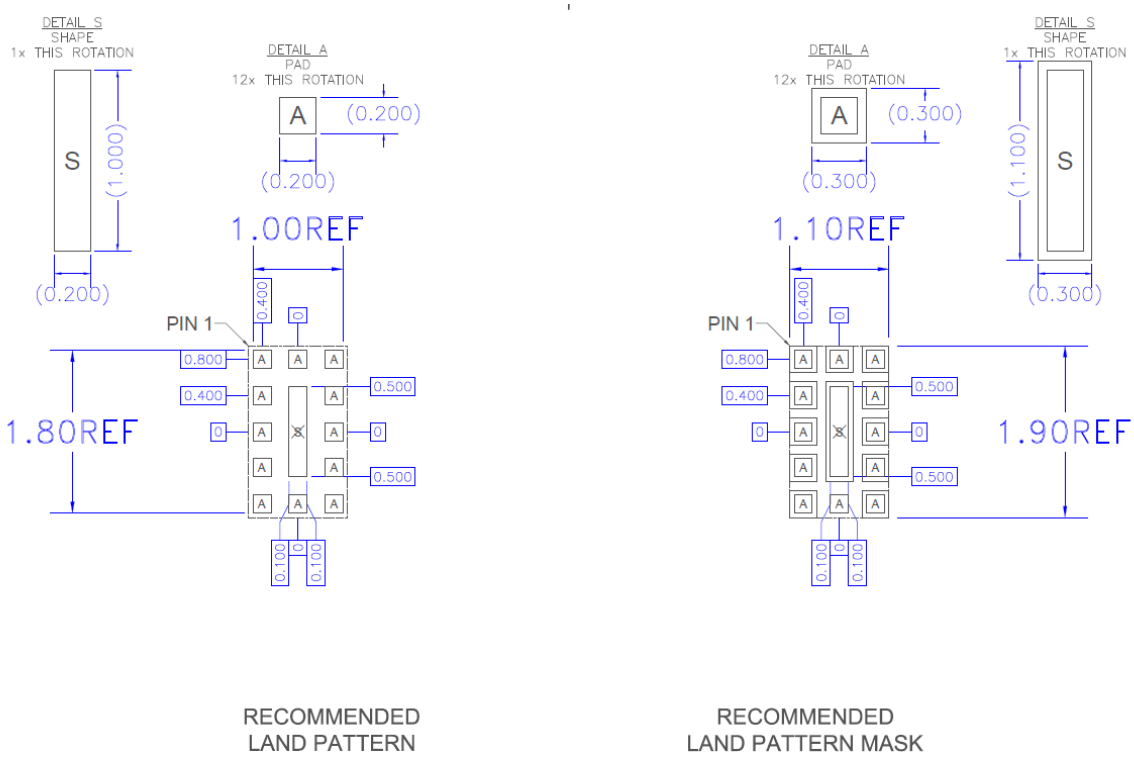
Mechanical Information

Package Drawing



TOP VIEW SIDE VIEW BOTTOM VIEW

PCB Design Requirements

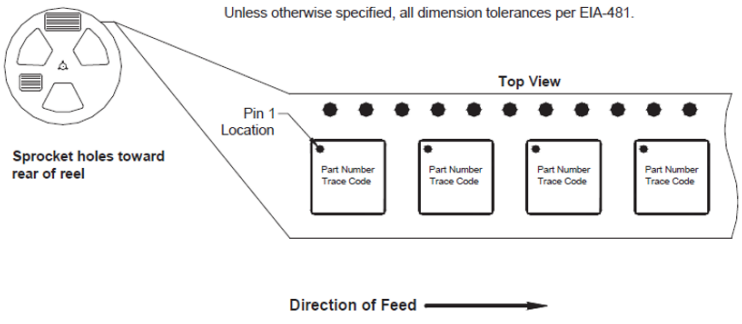


Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

Tape and Reel Information

Table 1. Tape and Reel

Qorvo Part Number	Reel Diameter Inch (mm)	Hub Diameter Inch (mm)	Width (mm)	Pocket Pitch (mm)	Feed	Units Per Reel
QPC8014QTR13	13 (330)	4 (102)	8	4	Single	5000
QPC8014QSR	7 (178)	2.5 (63)	8	4	Single	100



1.10 mm x 1.90 mm (Carrier Tape Drawing with Part Orientation).

PARAMETER	RATING	STANDARD
ESD – Human Body Model (HBM)	Class 2 (2000V)	ESDA/JEDEC JS-001-2012
CDM – Charge Device Model (CDM)	Class C3 (1000V)	ESDA/JEDEC JS-002
MSL – Moisture Sensitivity Level	MSL 3	IPC/JEDEC J-STD-020

Caution!

ESD sensitive device

Solderability

Compatible with both lead-free (260 °C max. reflow temperature) and tin/lead (245 °C max. reflow temperature) soldering processes.

Package lead plating: ENEPIG

RoHS Compliance

This part is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- SVHC Free
- PFOS Free