QPD0006

13.5 W, 48 V, 2.5 – 5.0 GHz, GaN RF Transistor

Product Overview

The QPD0006 is a single-path discrete GaN on SiC HEMT in a plastic overmold DFN package which operates from 2.5 to 5.0 GHz. It is a single-stage, unmatched transistor capable of delivering P3dB of 13.5 W at +48 V operation.

Lead free and RoHS compliant.

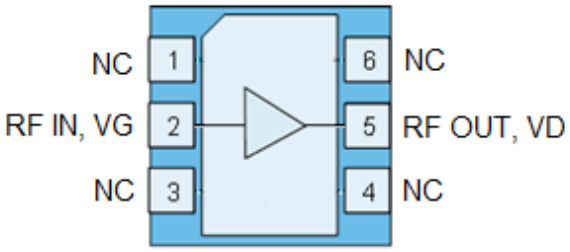
6 Pin 4.5 x 4.0 mm DFN Package

Key Features

- Operating Frequency Range: 2.5 – 5.0 GHz
- Operating Drain Voltage: +48 V
- Maximum Output Power (P3dB): 13.5 W (1)
- Maximum Drain Efficiency: 75% (1)
- Efficiency-Tuned P3dB Gain: 16 dB (1)
- 4.5 x 4.0 mm DFN Package

Notes:
1. Load pull data at 3.6 GHz.

Functional Block Diagram



Applications

- WCDMA / LTE
- Macrocell Base Station
- Microcell Base Station
- Small Cell
- Active Antenna
- 5G Massive MIMO
- General Purpose Applications

Ordering Information

Part No.	Description
QPD0006SR	Short Reel – 100 Pieces
QPD0006EVB1	3.4 – 3.6 GHz Evaluation Board

Absolute Maximum Ratings

Parameter	Rating
Breakdown Voltage (BV_{DG})	+165 V
Gate Voltage Range (V_G)	−7 to +2 V
Drain Voltage (V_D)	+55 V
Peak RF Input Power, Pulsed CW	34 dBm
VSWR Mismatch, P1dB Pulse (20% Duty Cycle, 100 µs Width), T = +25°C	10:1
Storage Temperature	−65 to +150°C

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Gate Voltage (V_G)		−2.6		V
Drain Voltage (V_D)		+48		V
Quiescent Drain Current (I_{DQ})		40		mA

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		3400		3600	MHz
Quiescent Drain Current (I_{DQ})			40.0		mA
Gain	P_{OUT} = 27 dBm	15.8	17.2		dB
Peak Output Power	P_{OUT} = 30.5 dBm, 10 dB PAR signal	38.5	39.5		dBm
Drain Efficiency	P_{OUT} = 27 dBm	12.6	15.1		%
Adjacent Power Ratio	P_{OUT} = 27 dBm		-35.7	-31.0	dBc
Gate Leakage	V_D = +48 V, V_G = −7 V	-1.5			mA

Test conditions unless otherwise noted: V_D = +48 V, I_{DQ} = 40 mA, T = +25°C, using an LTE 20 MHz signal with 8 dB PAR at 3600 MHz on a 3400 – 3600 MHz production test fixture.

Thermal Information

Parameter	Conditions	Values	Units
Thermal Resistance, Peak IR Surface Temperature at Average Power (θ_{JC})	T_{CASE} = +85°C, T_{CH} = 106°C CW: P_{DISS} = 1.8 W, P_{OUT} = 0.3 W	11.7	°C/W

Notes:

1. Thermal resistance is measured to package backside.
2. Refer to the following document: GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates

Power-Matched Load Pull Performance

Frequency (MHz)	Source Impedance (Ω)	Load Impedance (Ω)	P3dB (dBm)	Drain Efficiency (%)	G3dB (dB)
2500	9.0 – j4.0	30.0 + j3.3	41.8	68.0	17.7
2600	8.9 - j4.0	30.5 + j17.0	41.8	67.5	17.5
2700	8.9 - j5.4	30.4 + j17.0	41.3	64.2	17.3
3300	9.2 - j10.0	25.2 + j2.6	41.4	54.9	14.9
3400	9.2 - j11.8	25.1 + j2.7	41.4	55.3	14.5
3500	9.5 - j 11.8	25.2 + j2.7	41.4	57.0	14.5
3600	9.5 - j12.7	25.2 + j2.6	41.3	56.0	14.3
3800	9.7 - j15.2	23.7 + j3.9	41.3	60.1	14.0

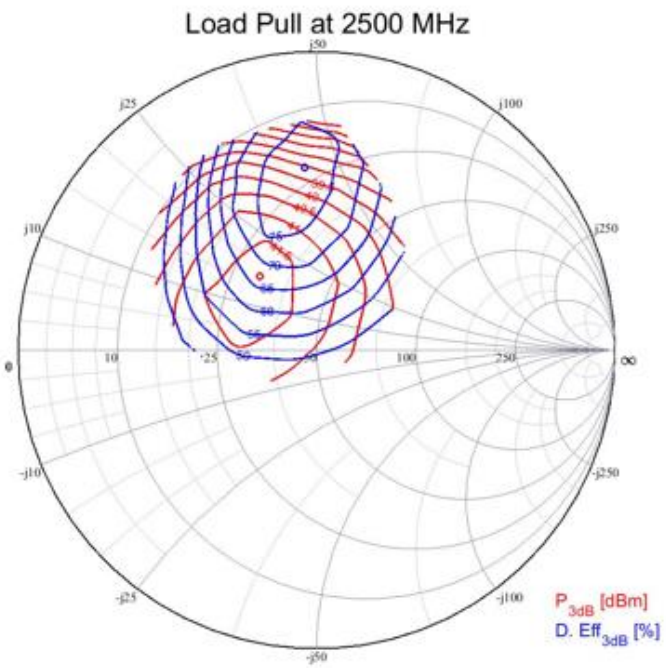
Test conditions unless otherwise noted: V_D = +48 V, I_{DQ} = 40 mA, T = +25°C, Pulse CW (10% duty cycle, 100 µs width).

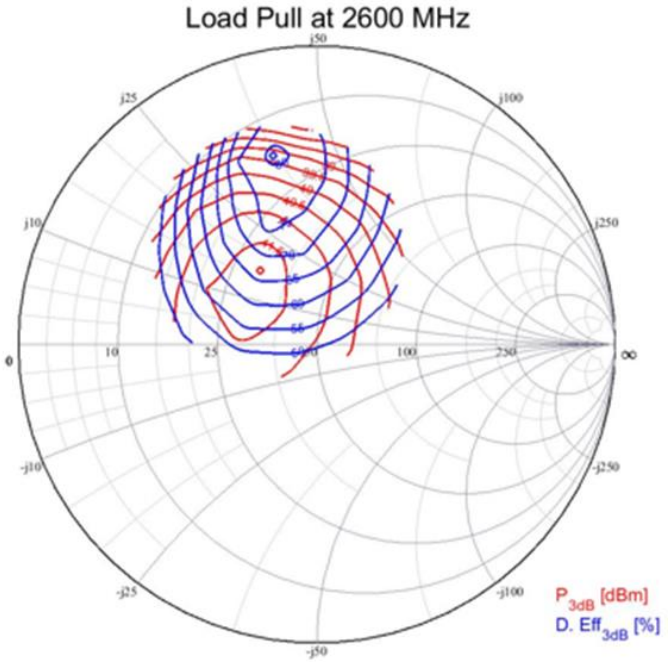
Efficiency-Matched Load Pull Performance

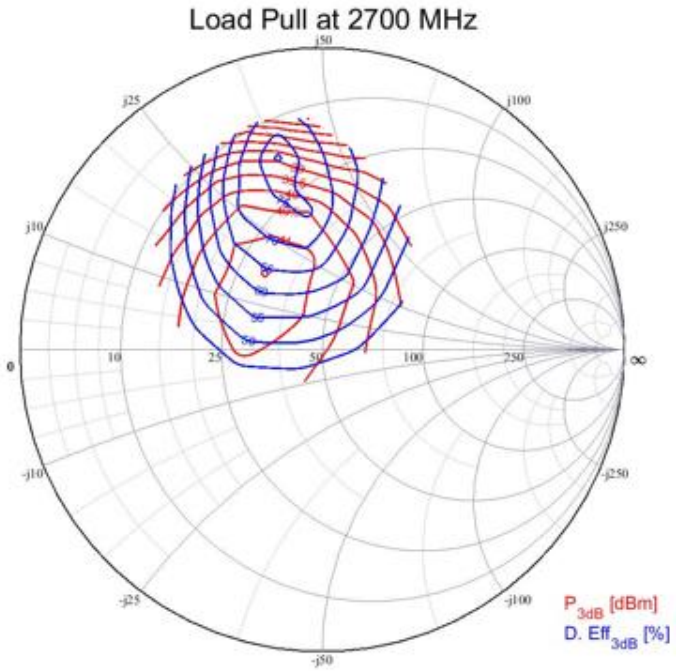
Frequency (MHz)	Source Impedance (Ω)	Load Impedance (Ω)	P3dB (dBm)	Drain Efficiency (%)	G3dB (dB)
2500	9.0 – j4.0	21.6 + j42.2	39.1	78.0	19.0
2600	8.9 - j4.0	16.6 + j36.8	39.3	81.5	18.9
2700	8.9 - j5.4	16.6 + j36.8	38.9	79.3	18.6
3300	9.2 - j10.0	11.6 + j23.4	38.9	73.3	16.7
3400	9.2 - j11.8	11.6 + j23.3	38.8	73.1	16.4
3500	9.5 - j 11.8	15.7 + j19.0	40.3	76.5	16.1
3600	9.5 - j12.7	7.3 + j19.0	38.2	75.9	16.0
3800	9.7 - j15.2	11.1 + j15.2	39.3	72.8	15.2

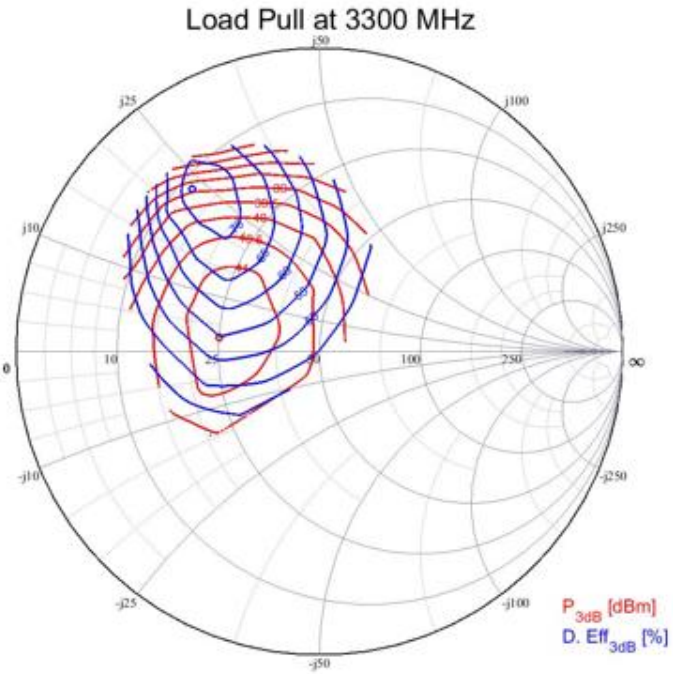
Test conditions unless otherwise noted: V_D = +48 V, I_{DQ} = 40 mA, T = +25°C, Pulse CW (10% duty cycle, 100 µs width).

Load Pull Contours









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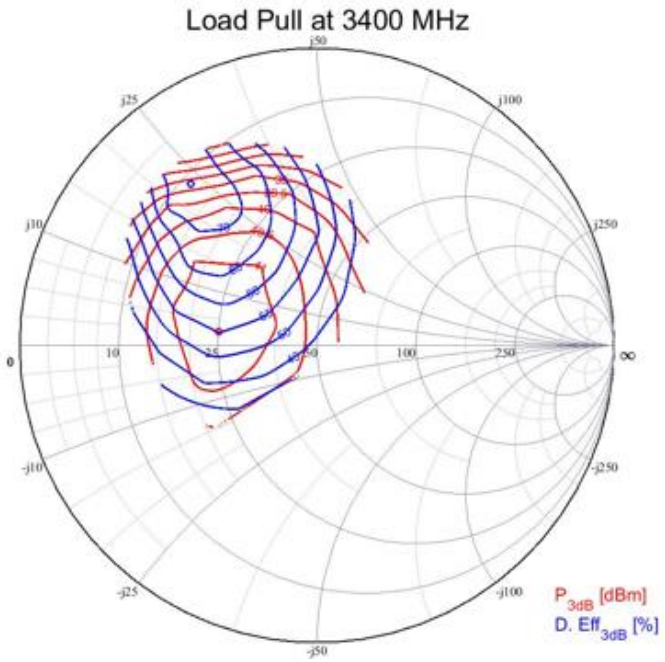
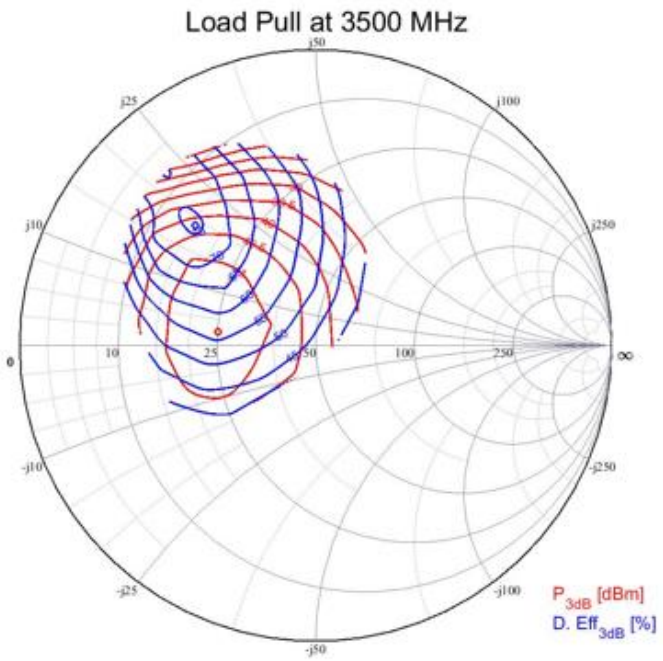
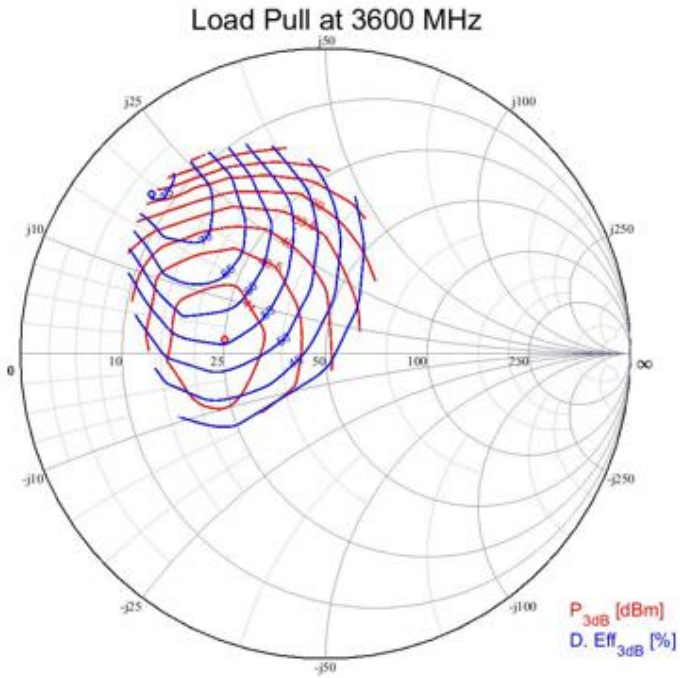
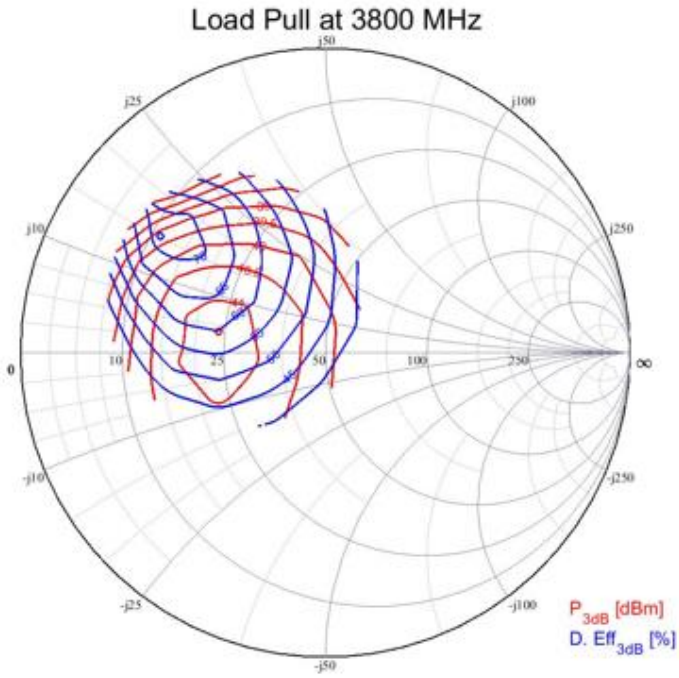


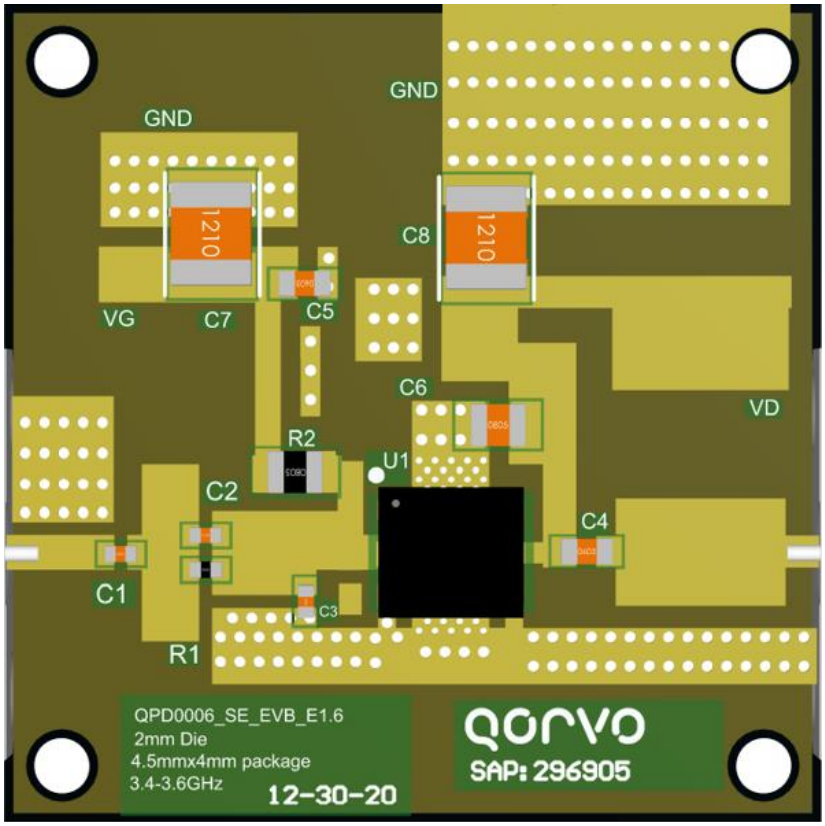






Test Conditions unless otherwise noted: V_D = +48 V, I_{DQ} = 40 mA, T = +25°C, Pulse CW (10% duty cycle, 100 µs width).

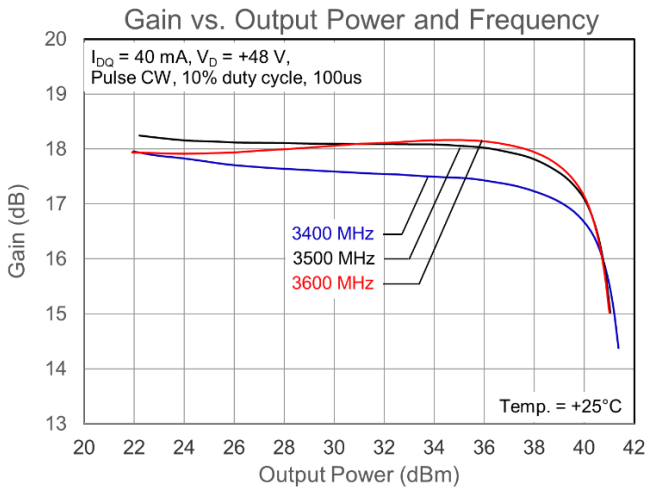
QPD0006EVB1 Layout – 3400 – 3600 MHz Reference Design

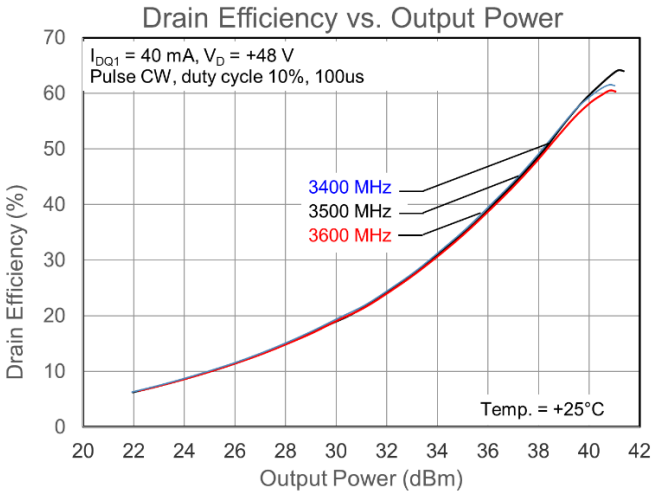


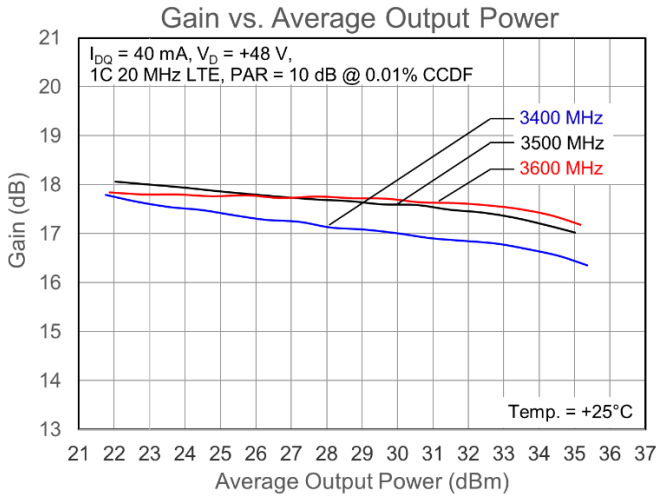
QPD0006EVB1 Bill of Materials – 3400 – 3600 MHz Reference Design

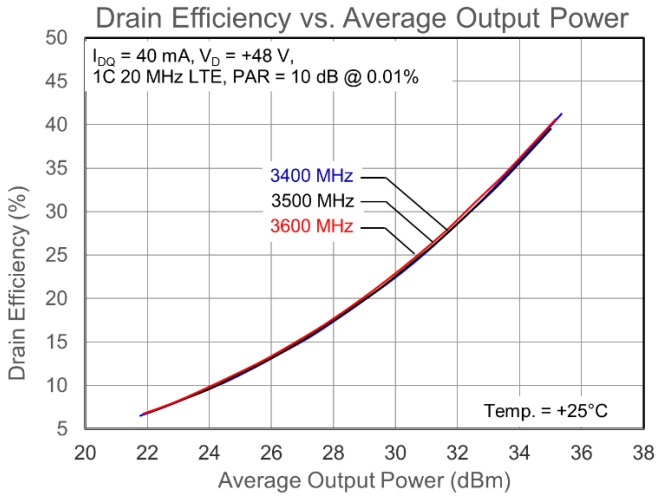
Reference Des.	Value	Description	Manuf.	Part Number
C1	2.4pF	CAP, 2.4pF, ±0.1pF, 200V, C0G, HI-Q 0402	ATC	600L2R4BT200T
C2	1.0pF	CAP, 1pF, ±0.1pF, 200V, C0G, 0402	ATC	600L1R0BT200T
C3	0.2pF	CAP, 0.2pF, ±0.1pF, 200V, HI-Q, 0402	AVX	UQCL2A0R2BAT2A\500
C4	6.2pF	CAP, 6.2pF, +/-0.1pF, 250V, HI-Q, 0603	ATC	600S6R2BT250XT
C5	8.2pF	CAP, 8.2pF, 0.25pF, 250V, 0603	ATC	600S8R2CT250XT
C6	15pF	CAP, 15pF, 5%, 250V, HI-Q, 0805	Murata	GQM2195C2E150JB12D
C7,C8	10uF	CAP, 10uF, 10%, 100V, X7S, 1210	Murata	GRM32EC72A106KE05L
R1	590 Ohm	RES, 590 OHM, 1%, 1/20W, 0402	State Of The Art	M55342K11B590DS
R2	10 Ohm	RES, 15OHM, 2%, 50W, 0805	International Manufacturing	ND3-0805WA15R0G
U1	-	2.5-5GHz, 12W, 50V GaN transistor.	Qorvo	QPD0006
J1, J2 (not pictured)	-	CONNECTOR, SMA (PSF-S00-000)	Powell	PSF-S00-000

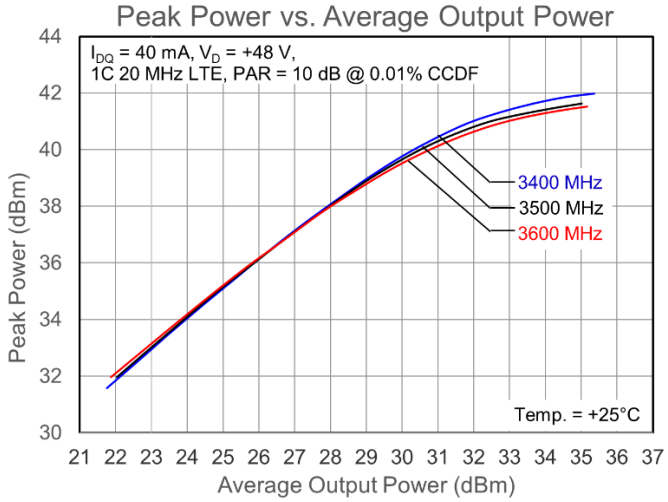
QPD0006EVB1 Performance Plots – 3400 – 3600 MHz Reference Design

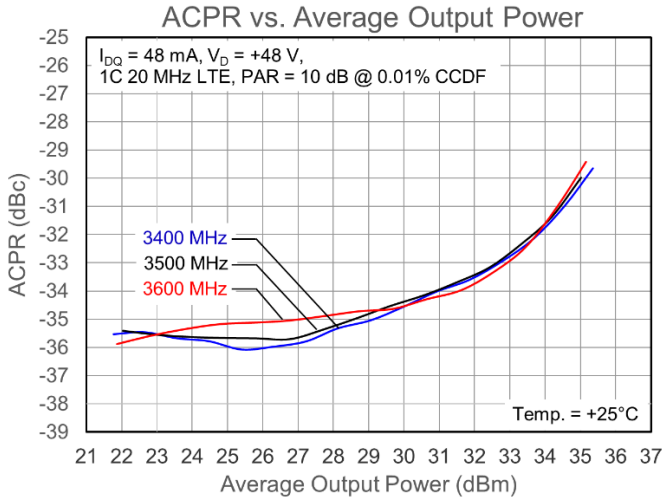






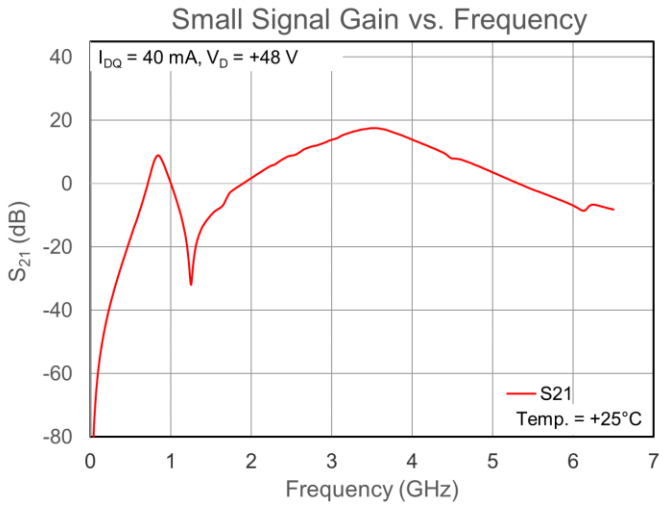


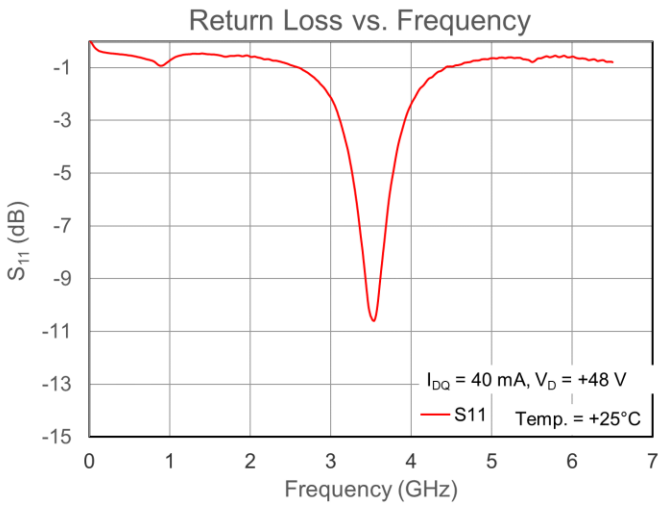




Test conditions unless otherwise noted: V_D = +48 V, I_{DQ} = 40 mA, T = +25°C on a reference design fixture tuned for 3400 – 3600 MHz.

QPD0006EVB1 Performance Plots – 3400 – 3600 MHz Reference Design





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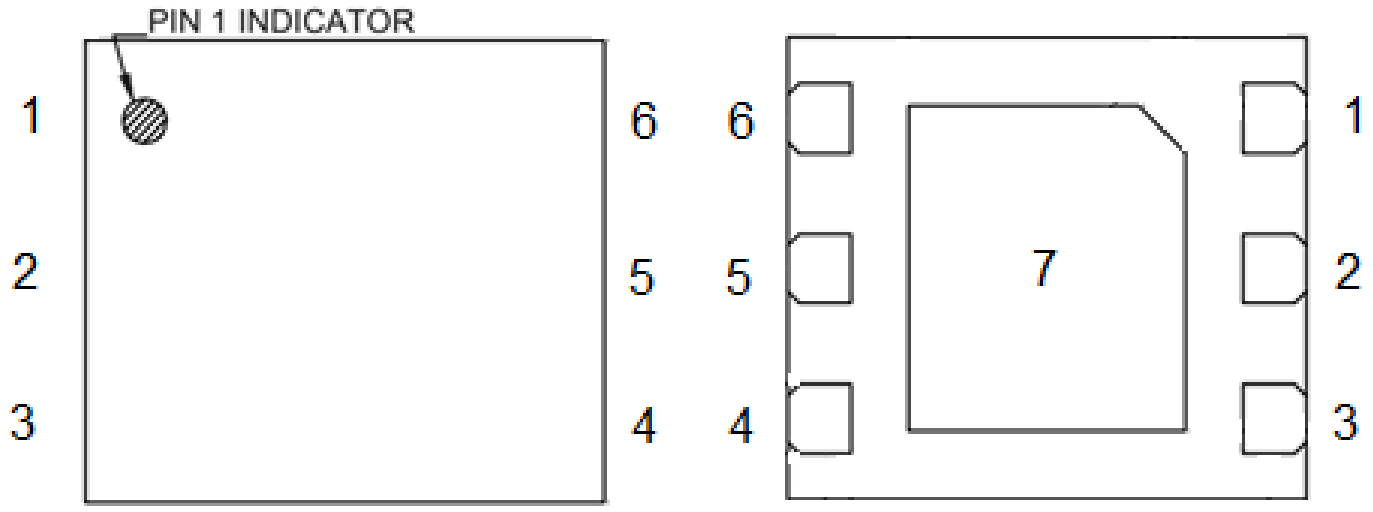
Pin Configuration and Description



Bottom View

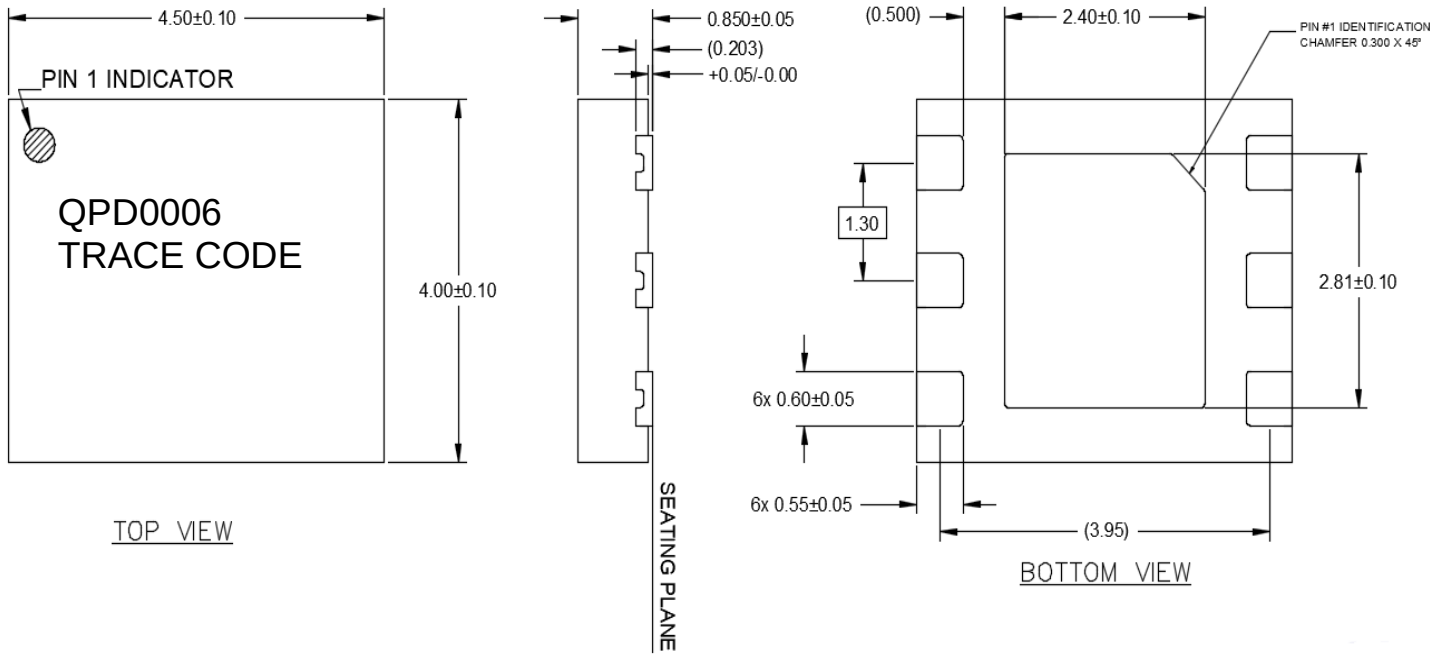
Pin No.	Label	Description
1	NC	No Connect
2	RF IN, VG	RF Input, Gate Bias
3	NC	No Connect
4	NC	No Connect
5	RF OUT, VD	RF Output, Drain Bias
6	NC	No Connect
7 (Backside Paddle)	GND	Ground

Biasing Procedure

Bias On	Bias Off
1. Turn ON V_G to −5 V. 2. Turn ON V_D to +48 V. 3. Slowly adjust V_G until I_D = 40 mA. (Typically, V_G = −2.6 V.) 4. Turn ON RF.	1. Turn OFF RF. 2. Adjust V_G to −5 V. 3. Turn OFF V_D. 4. Wait two (2) seconds to allow drain capacitors to discharge. 5. Turn OFF V_G.

Package Marking and Dimensions

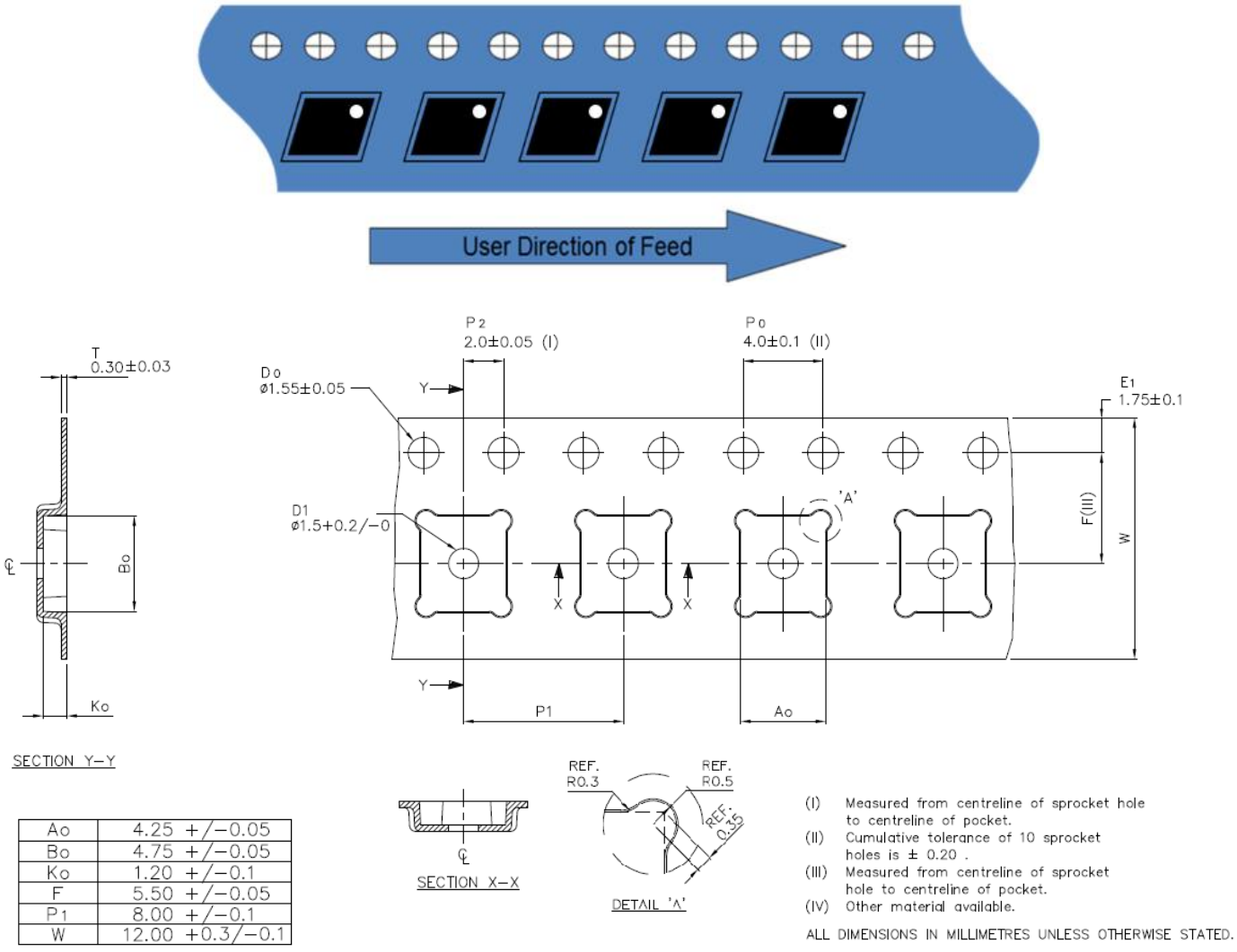
Marking: Qorvo Logo
Part Number – QPD0006
Trace Code – To be assigned by subcontractor.



Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. General tolerance is ±0.05 unless otherwise shown.
3. Part is overmold encapsulated.
4. Contact plating is NiPdAu. Au thickness is 0.00254 to 0.01501 µm.

Tape and Reel Information – Carrier and Cover Tape Dimensions

Tape and reel specifications for this part are also available on the Qorvo website.
Standard T/R size = 2500 pieces on a 13” reel.

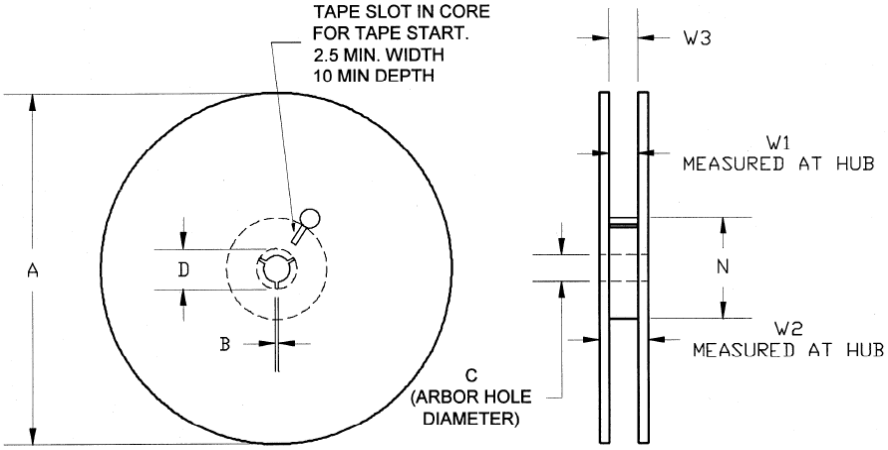


Ao	4.25 +/−0.05
Bo	4.75 +/−0.05
Ko	1.20 +/−0.1
F	5.50 +/−0.05
P1	8.00 +/−0.1
W	12.00 +0.3/−0.1

Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.167	4.25
	Width	B0	0.187	4.75
	Depth	K0	0.047	1.20
	Pitch	P1	0.315	8.00
Centerline Distance	Cavity to Perforation - Length Direction	P2	0.079	2.00
	Cavity to Perforation - Width Direction	F	0.217	5.50
Cover Tape	Width	C	0.362	9.2
Carrier Tape	Width	W	0.472	12.00

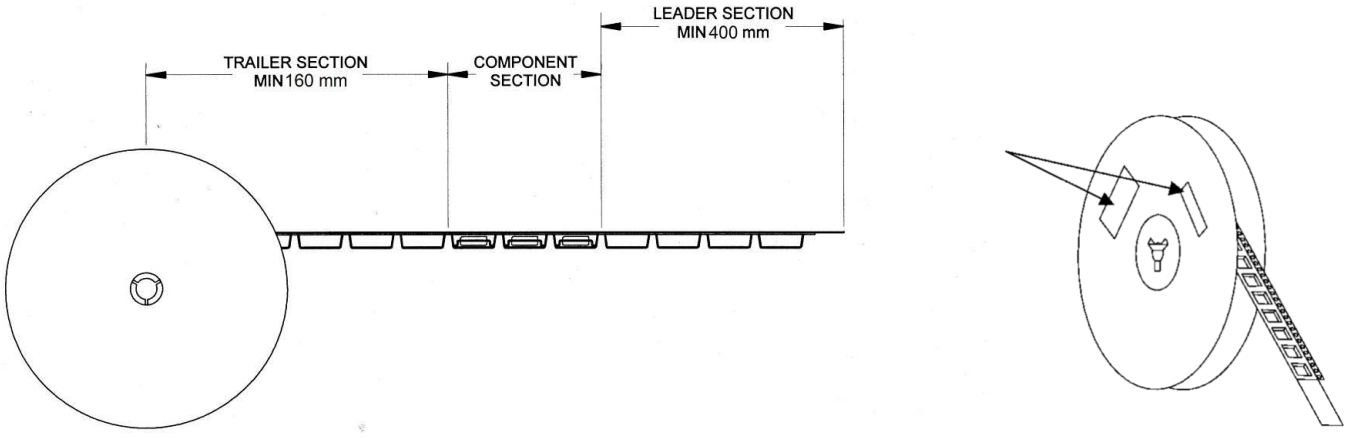
Tape and Reel Information – Reel Dimensions

Packaging reels are used to prevent damage to devices during shipping and storage, loaded carrier tape is typically wound onto a plastic take-up reel. The reel size is 13" diameter. The reels are made from high-impact injection-molded polystyrene (HIPS), which offers mechanical and ESD protection to packaged devices.



Feature	Measure	Symbol	Size (in)	Size (mm)
Flange	Diameter	A	12.992	330.0
	Thickness	W2	0.717	18.2
	Space Between Flange	W1	0.504	12.8
Hub	Outer Diameter	N	4.016	102.0
	Arbor Hole Diameter	C	0.512	13.0
	Key Slit Width	B	0.079	2.0
	Key Slit Diameter	D	0.787	20.0

Tape and Reel Information – Tape Length and Label Placement



Notes:
1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481.
2. Labels are placed on the flange opposite the sprockets in the carrier tape.

Recommended Solder Temperature Profile