QPD0050

75 W, 48 V, DC to 3.6 GHz, GaN RF Power Transistor

Product Overview

The QPD0050 is a wide band plastic over-molded QFN discrete power amplifier. The device is a single stage unmatched power amplifier transistor.

The QPD0050 can be used in Doherty architecture for the final stage of a base station power amplifier for small cell, microcell, and active antenna systems. The QPD0050 can also be used as a driver in a macrocell base station power amplifier.

The wide bandwidth of the QPD0050 makes it suitable for many different applications from DC to 3.6 GHz. QPD0050 can deliver P_{SAT} of 79.4 W at +48 V operation at 2.1 GHz.

Lead-free and ROHS compliant.

6 Pin 6.6 x 7.7 mm DFN Package

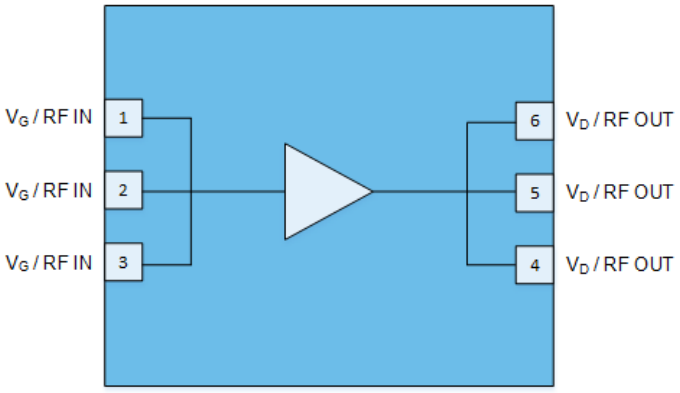
Key Features

- Operating Frequency Range: DC to 3.6 GHz
- Operating Drain Voltage: +48 V
- Maximum Output Power (P_{SAT}): 79.4 W (1)
- Maximum Drain Efficiency: 77.9% (1)
- Efficiency-Tuned P3dB Gain: 19.4 dB (1)
- Surface Mount Plastic Package

Notes:

1. Load pull performance at 2.1 GHz.

Functional Block Diagram



Applications

- W-CDMA / LTE
- Macrocell Base Station Driver
- Microcell Base Station
- Small Cell Final Stage
- Active Antenna
- General Purpose Applications

Ordering Information

Part Number	Description
QPD0050SR	Short Reel – 100 Pieces
QPD0050TR7	7” Reel – 500 Pieces
QPD0050PCB4B01	2110 – 2170 MHz Evaluation Board

Absolute Maximum Ratings

Parameter	Rating
Breakdown Voltage (BV_{DG})	+165 V
Gate Voltage Range (V_G)	−7 to +2 V
Drain Voltage (V_D)	+55 V
Peak RF Input Power	35 dBm
VSWR Mismatch, P1dB Pulse (20% Duty Cycle, 100 µs Width), T = +25°C	10:1

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Gate Voltage (V_G)		−2.7		V
Drain Voltage (V_D)		+48		V
Quiescent Drain Current (I_{DQ})		130		mA

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		2110		2170	MHz
Quiescent Drain Current (I_{DQ})			130		mA
Gain	3 dB Compression	17.5	19.5		dB
Power (P_{SAT})	3 dB Compression	46.5	47.7		dBm
Drain Efficiency	3 dB Compression	60.0	72.7		%
Gate Leakage	Vg = -3.8V, Vd = +10V	-11.6			mA

Test conditions unless otherwise noted: V_D = +48 V, I_{DQ} = 130 mA, T = +25°C, Pulse signal (20% Duty Cycle, 100 µs Width) at 2140 MHz on a Class AB single-ended reference design tuned for 2110-2170 MHz.

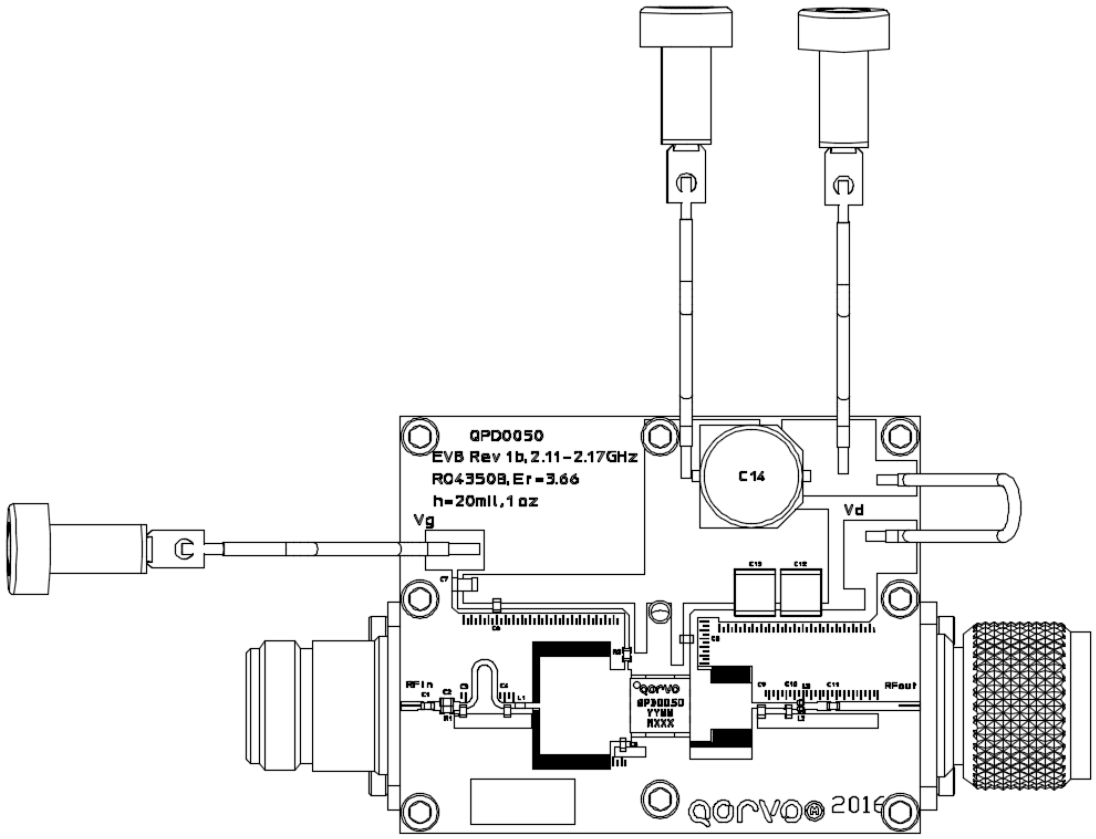
Thermal Information

Parameter	Conditions	Values	Units
Doherty Thermal Resistance, Peak IR Surface Temperature at Average Power (θ_{JC}) (1) (2)	T_{CASE} = +105°C, T_{CH} = 113°C CW: P_{DISS} = 8.5 W, P_{OUT} = 12.7 W	0.9	°C/W
Device Thermal Resistance, Peak IR Surface Temperature at Average Power (θ_{JC})	T_{CASE} = +105°C, T_{CH} = 122°C CW: P_{DISS} = 13.4 W, P_{OUT} = 3.5 W	1.3	°C/W

Notes:

1. Based on expected carrier amplifier efficiency of Doherty.
2. P_{OUT} assumes 20% peaking amplifier contribution of total average Doherty rated power.
3. Thermal resistance is measured to package backside.
4. Refer to the following document: GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates

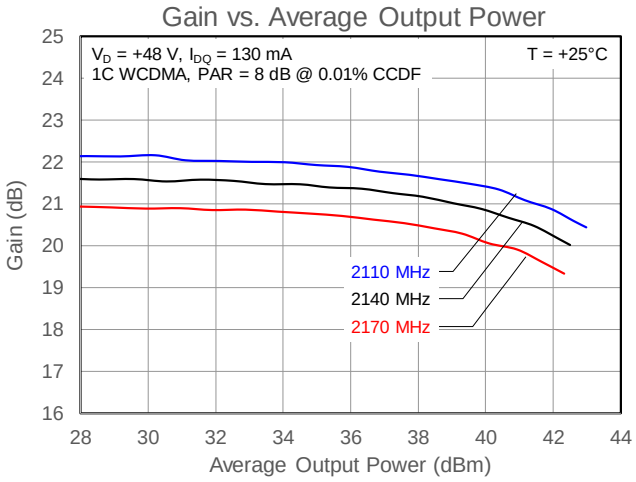
QPD0050PCB4B01 Layout – 2110 – 2170 MHz Reference Design

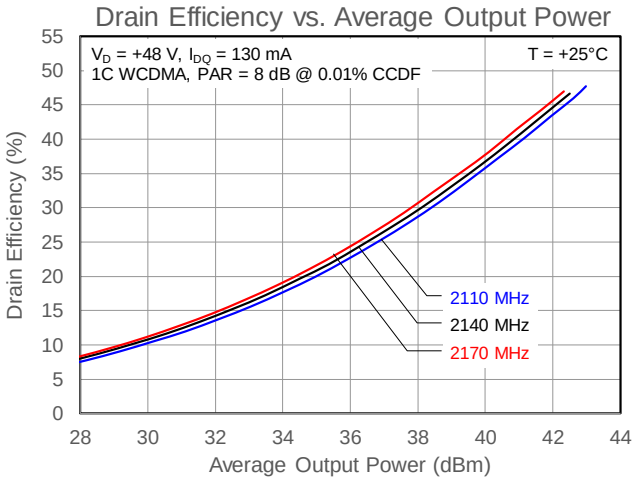


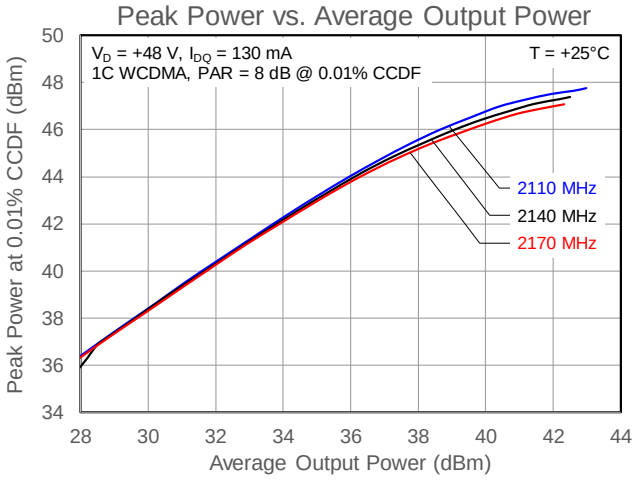
QPD0050PCB4B01 Bill of Materials

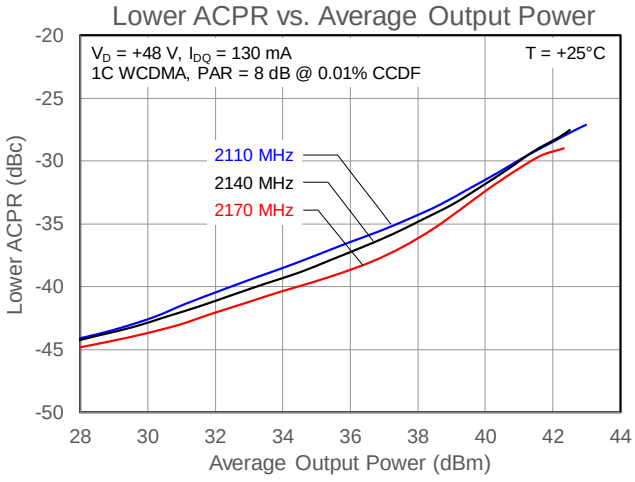
Reference Des.	Value	Description	Manufacturer	Part Number
C1, C2, C6, C8, C11	18 pF	Capacitor, 18 pF, ±1%, 250 V, C0G, 0603	ATC	600S180FT250XT
C3	2 pF	Capacitor, 2 pF, ±0.05 pF, 250 V, C0G, 0603	ATC	600S2R0AT250X
C4	1.6 pF	Capacitor, 1.6 pF, ±0.05 pF, 250 V, HI-Q, 0603	ATC	600S1R6AT250XT
C5	2.4 pF	Capacitor, 2.4 pF, ±0.1 pF, 250 V, C0G, 0603	ATC	600S2R4BT250XT
C7	4.7 µF	Capacitor, 4.7 µF, 50 V, X7R, 1206	Kemet	C1206C475K5RACTU
C9	2.7 pF	Capacitor, 2.7 pF, ±0.1 pF, 250 V, HI-Q, 0603	ATC	600S2R7BW250XT
C10	1.5 pF	Capacitor, 1.5 pF, 250 V, 0603	ATC	600S1R5GT250XT
C12, C13	10 µF	Capacitor, 10 µF, 20%, 100 V, X7S, 2220	TDK	C5750X7S2A106M230KB
C14	100 µF	Capacitor, 100 µF, 20%, 100 V, Electrolytic	Vishay	MAL215099907E3
L1	4.3 nH	Inductor, 4.3 nH, ±5%, 0.7 A, 0402	Coilcraft	0402CS-4N3XJL
L2, L3 (In Parallel)	0.67 nH	Inductor, 0.67 nH, ±10%, 1.6 A, WW, 0302	Coilcraft	0302CS-N67XKLW
R1	1 Ω	Resistor, 1 Ω, 0603	Vishay	CRCW06031R00JNEA
R2	10 Ω	Resistor, 10 Ω, 0603	Vishay	CRCW060310R0

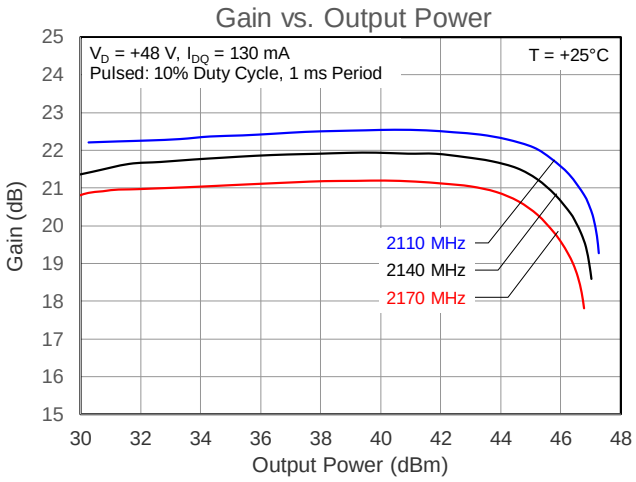
Performance Plots

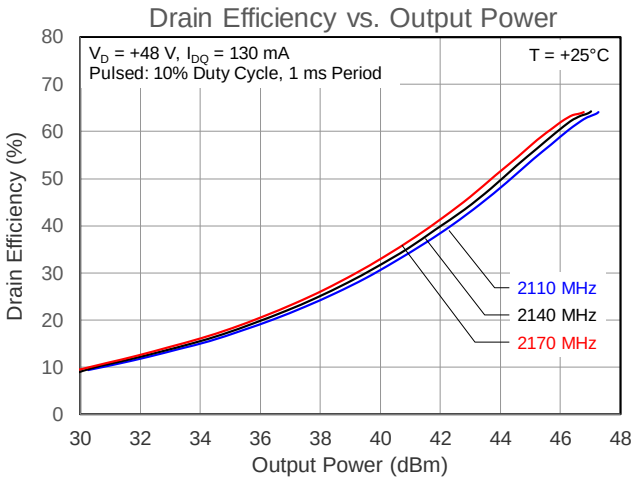






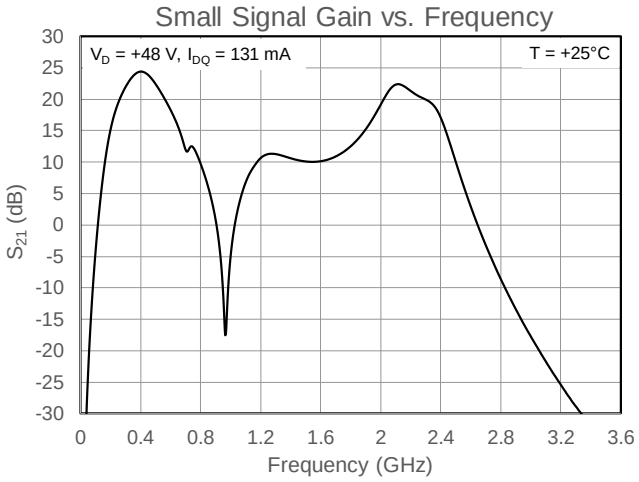


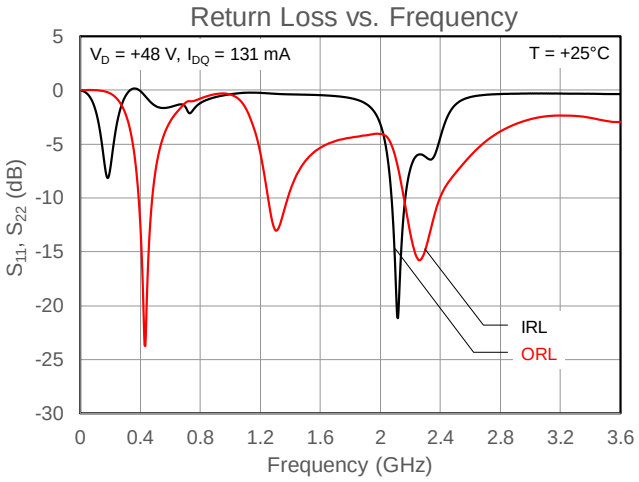




Test conditions unless otherwise noted: V_D = +48 V, I_{DQ} = 130 mA, T = +25°C, on a 2110 – 2170 MHz reference design fixture.

Performance Plots





Test conditions unless otherwise noted: V_D = +48 V, I_{DQ} = 130 mA, T = +25°C, on a 2110 – 2170 MHz reference design fixture.

Power-Matched Load Pull Performance

Frequency (MHz)	Source Impedance (Ω)	Load Impedance (Ω)	P3dB (dBm)	Drain Efficiency (%)	G3dB (dB)
1800	1.5 – j1.6	5.9 + j3.1	48.8	68.7	20.1
1900	1.5 – j2.3	5.7 + j1.9	48.9	64.9	19.3
2100	1.7 – j3.6	5.6 + j0.9	49.0	64.2	18.0
2200	1.6 – j3.9	5.8 + j1.2	49.1	65.5	17.9
2600	1.9 – j5.7	4.5 – j0.5	48.9	62.2	16.5
3500	2.6 – j8.8	3.8 – j4.8	48.5	53.7	13.5

Test conditions unless otherwise noted: V_D = +48 V, I_{DQ} = 130 mA, T = +25°C, Pulse (10% Duty Cycle, 100 µs Width).

Efficiency-Matched Load Pull Performance

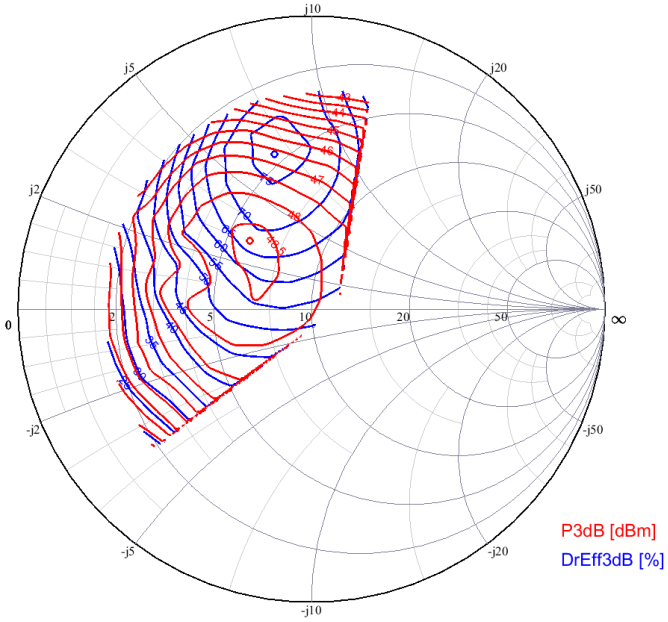
Frequency (MHz)	Source Impedance (Ω)	Load Impedance (Ω)	P3dB (dBm)	Drain Efficiency (%)	G3dB (dB)
1800	1.5 – j1.6	4.6 + j6.8	46.7	77.1	20.9
1900	1.5 – j1.6	4.3 + j5.7	47.1	77.4	20.5
2100	1.7 – j3.6	3.6 + j5.2	46.6	77.9	19.4
2200	1.6 – j3.9	3.7 + j5.2	46.9	76.3	19.1
2600	1.9 – j5.7	2.9 + j2.2	47.1	73.8	17.5
3500	2.6 – j8.8	1.8 – j2.4	46.5	66.7	14.7

Test conditions unless otherwise noted: V_D = +48 V, I_{DQ} = 130 mA, T = +25°C, Pulse (10% Duty Cycle, 100 µs Width).

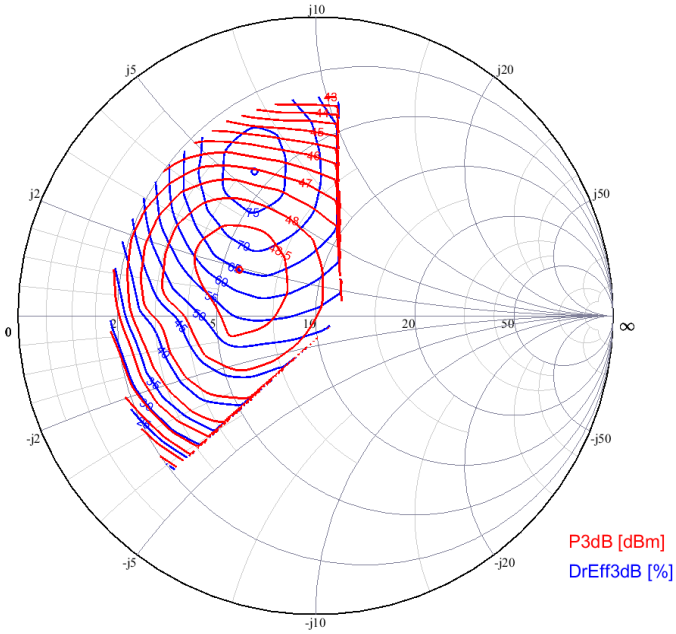
Load Pull Contours

Test Conditions unless otherwise noted: V_D = +48 V, I_{DQ} = 130 mA, T = +25°C, Pulse (10% Duty Cycle, 100 µs Width).

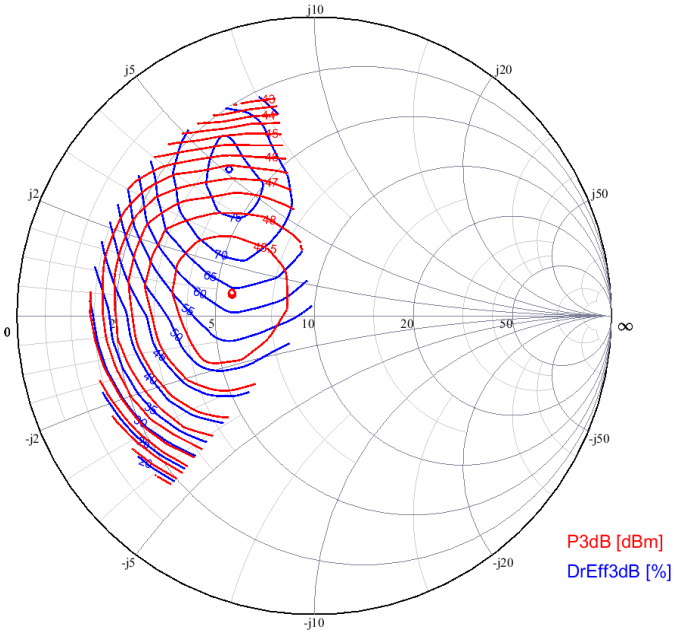
Load Pull at 1.8 GHz



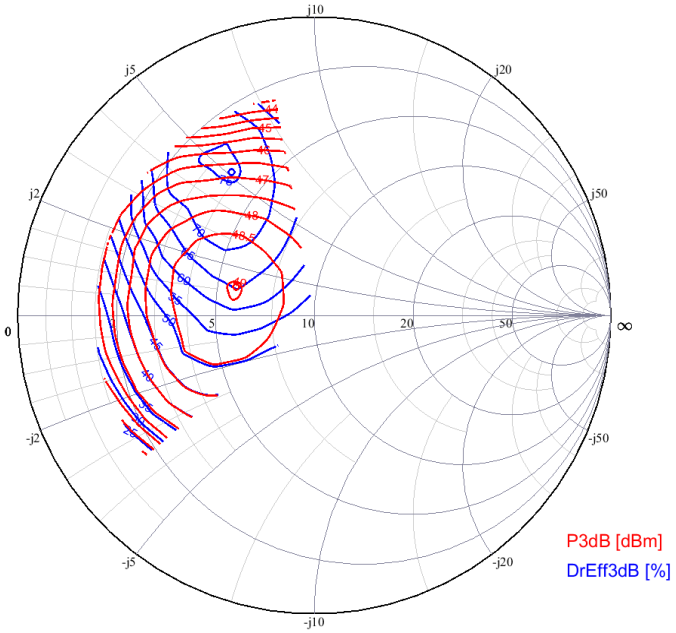
Load Pull at 1.9 GHz



Load Pull at 2.1 GHz



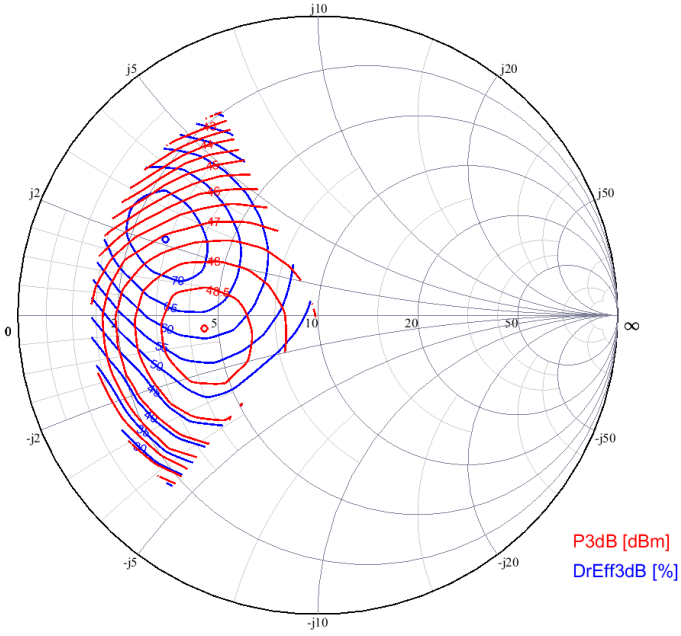
Load Pull at 2.2 GHz



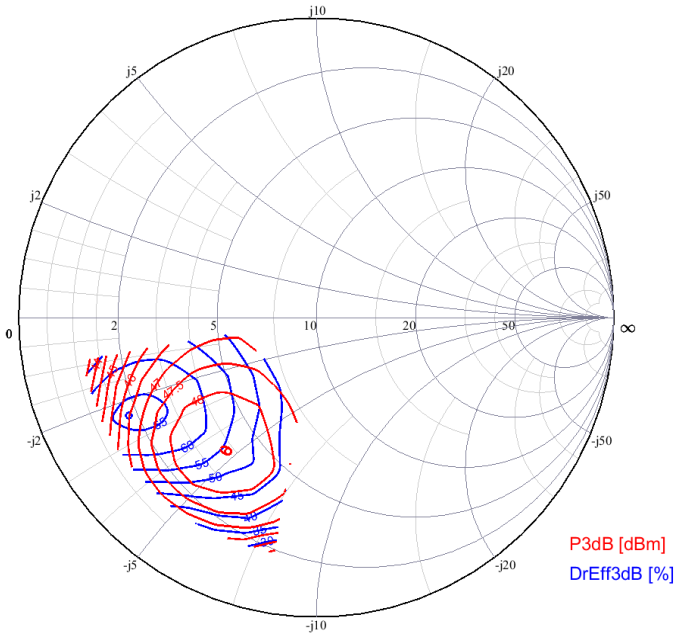
Load Pull Contours

Test Conditions unless otherwise noted: V_D = +48 V, I_{DQ} = 130 mA, T = +25°C, Pulse (10% Duty Cycle, 100 µs Width).

Load Pull at 2.6 GHz

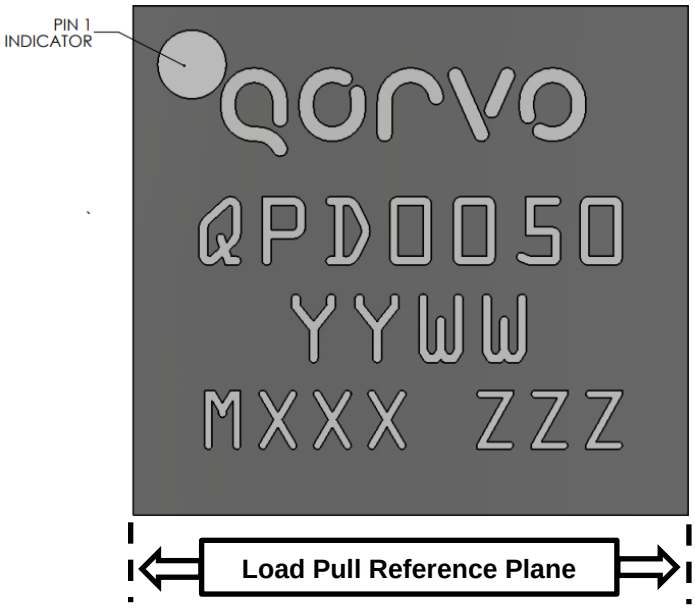


Load Pull at 3.5 GHz

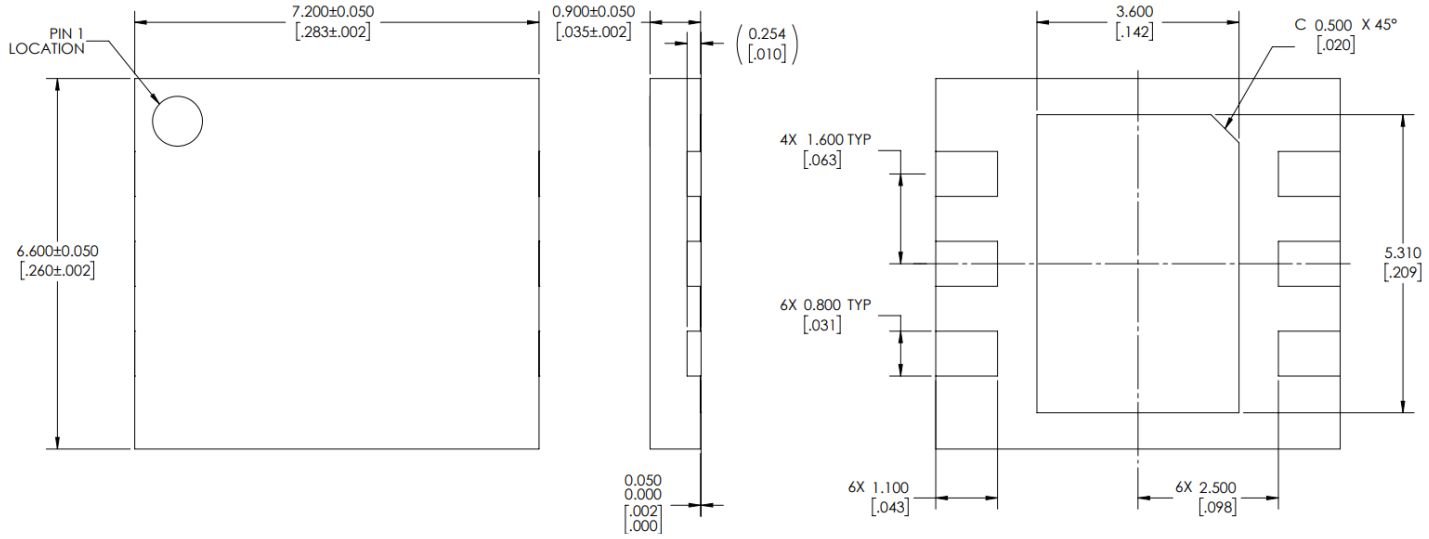


Package Markings

Marking: Qorvo Logo
Part Number – QPD0050
Date Code – YYWW
Lot Code – MXXX
Serial Number – ZZZ

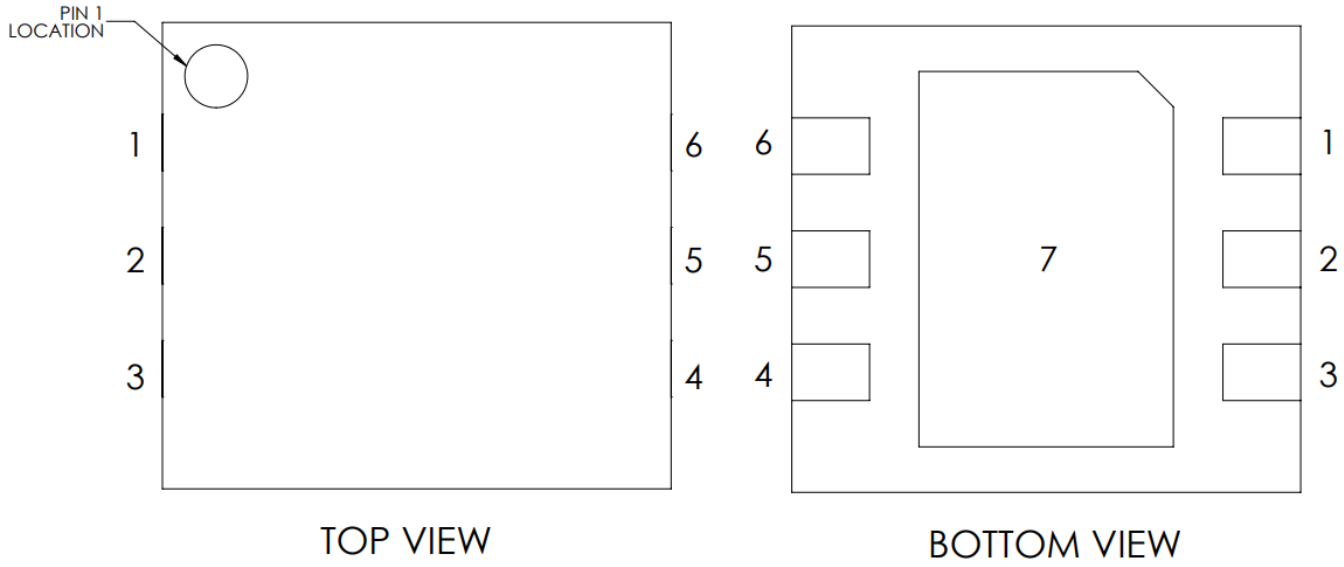


Package Dimensions



Notes:
1. Dimensions are in millimeters [inches]. Angles are in degrees.
2. Part is overmold encapsulated.
3. Contact plating is NiPdAu. Au thickness is 0.00254 to 0.01501 µm.

Pin Configuration and Description



Pin No.	Label	Description
1, 2, 3	RF IN, V_G	RF Input, Gate Bias
4, 5, 6	RF OUT, V_D	RF Output, Drain Bias
7 (Backside Paddle)	RF/DC GND	RF/DC Ground

Bias Procedure

Bias On	Bias Off
1. Turn ON V_G to –4 V. 2. Turn ON V_D to +48 V. 3. Slowly adjust V_G until I_D is set to 130 mA. (Typically, V_G = −2.7 V.) 4. Turn ON RF.	1. Turn OFF RF. 2. Adjust V_G to −5 V. 3. Turn OFF V_D. 4. Wait two (2) seconds to allow drain capacitor to discharge. 5. Turn off V_G.

Recommended Solder Temperature Profile