QPD1020

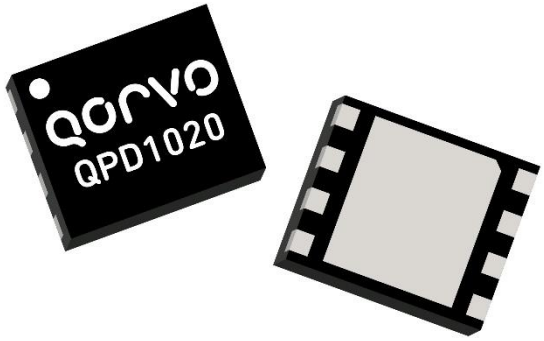
2.7 – 3.5 GHz, 50 V, 30 W GaN RF Input-Matched Transistor

Product Overview

The Qorvo QPD1020 is a 30 W (P_{3dB}), 50Ω-input matched discrete GaN on SiC HEMT which operates from 2.7 to 3.5 GHz and 50 V supply. The integrated input matching network enables wideband gain and power performance, while the output can be matched on board to optimize power and efficiency for any region within the band.

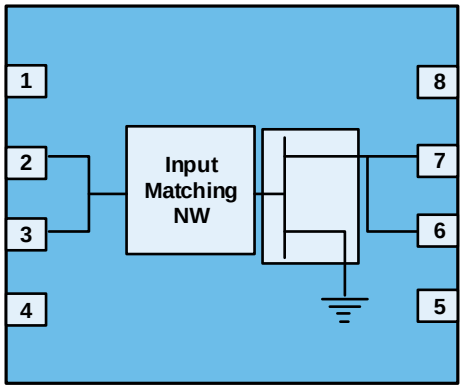
Lead-free and ROHS compliant.

Evaluation boards are available upon request.



6 x 5 x 1.09 mm DFN

Functional Block Diagram



Key Features

- Frequency: 2.7 to 3.5 GHz
- Output Power (P_{3dB})[1]: 31 W
- Linear Gain[1]: 18.4 dB
- Typical $DEFF_{3dB}$[1]: 65 %
- Operating Voltage: 50 V
- CW and Pulse capable

Note 1: @ 3.1 GHz Load Pull

Applications

- Military radar
- Civilian radar
- Test instrumentation

Ordering info

Part No.	Description
QPD1020S2	Sample of 2 QPD1020
QPD1020SQ	Sample of 25 QPD1020
QPD1020SR	Sample of 100 QPD1020
QPD1020EVB01	2.7 – 3.1 GHz EVB

Absolute Maximum Ratings[1]

Parameter	Rating	Units
Breakdown Voltage,BV_{DG}	+145	V
Gate Voltage Range, V_G	-7 to +2	V
Drain Current, I_{DMAX}	4.1	A
Gate Current Range, I_G	See page 15.	mA
Power Dissipation, P_{DISS}[2]	30	W
RF Input Power, Pulse, 2.9 GHz, T = 25 °C[2]	+33	dBm
Mounting Temperature (30 Seconds)	320	°C
Storage Temperature	−65 to +150	°C

Notes:
1. Operation of this device outside the parameter ranges given above may cause permanent damage.
2. Pulsed 100uS PW, 20% DC

Recommended Operating Conditions[1]

Parameter	Min	Typ	Max	Units
Operating Temp. Range	−40	+25	+85	°C
Drain Voltage Range, V_D	+32	+50	+55	V
Drain Bias Current, I_{DQ}		52.5		mA
Drain Current, I_D[4]	–	100	–	mA
Gate Voltage, V_G[3]	–	−2.8	–	V
Power Dissipation (P_D), Pulsed[2,4]	–	–	27	W
Power Dissipation (P_D), CW[2]	–	–	18.5	W

Notes:
1. Electrical performance is measured under conditions noted in the electrical specifications table. Specifications are not guaranteed over all recommended operating conditions.
2. Package base at 85 °C
3. To be adjusted to desired I_{DQ}
4. 100uS PW, 20% DC

Measured Load Pull Performance – Power Tuned[1]

Parameter	Typical Values			Units
Frequency, F	2.7	3.1	3.5	GHz
Drain Voltage, V_D	50	50	50	V
Drain Bias Current, I_{DQ}	52.5	52.5	52.5	mA
Output Power at 3dB compression, P_{3dB}	45.2	44.9	45	dBm
Drain Efficiency at 3dB compression, $DEFF_{3dB}$	57	55.3	58.2	%
Gain at 3dB compression, G_{3dB}	14	15.4	15.4	dB

Notes:
1. Pulsed, 100 uS Pulse Width, 20% Duty Cycle
2. Characteristic Impedance, Zo = 33.4 Ω.

Measured Load Pull Performance – Efficiency Tuned[1]

Parameter	Typical Values			Units
Frequency, F	2.7	3.1	3.5	GHz
Drain Voltage, V_D	50	50	50	V
Drain Bias Current, I_{DQ}	52.5	52.5	52.5	mA
Output Power at 3dB compression, P_{3dB}	43.6	43.6	43.9	dBm
Drain Efficiency at 3dB compression, $DEFF_{3dB}$	68	65.1	66.5	%
Gain at 3dB compression, G_{3dB}	16.5	17.5	16.3	dB

Notes:
1. Pulsed, 100 uS Pulse Width, 20% Duty Cycle
2. Characteristic Impedance, Zo = 33.4 Ω.

2.7 – 3.1 GHz EVB 2.9 GHz Performance[1]

Parameter	Min	Typ	Max	Units
Linear Gain, G_{LIN}	–	17	–	dB
Output Power at 3dB compression point, P3dB	–	25	–	W
Drain Efficiency at 3dB compression point, DEFF3dB	–	57.6	–	%
Gain at 3dB compression point, G3dB	–	14	–	dB

Notes:

1. V_D = +50 V, I_{DQ} = 52.5 mA, Temp = +25 °C, Pulse Width = 128 uS, Duty Cycle = 10%

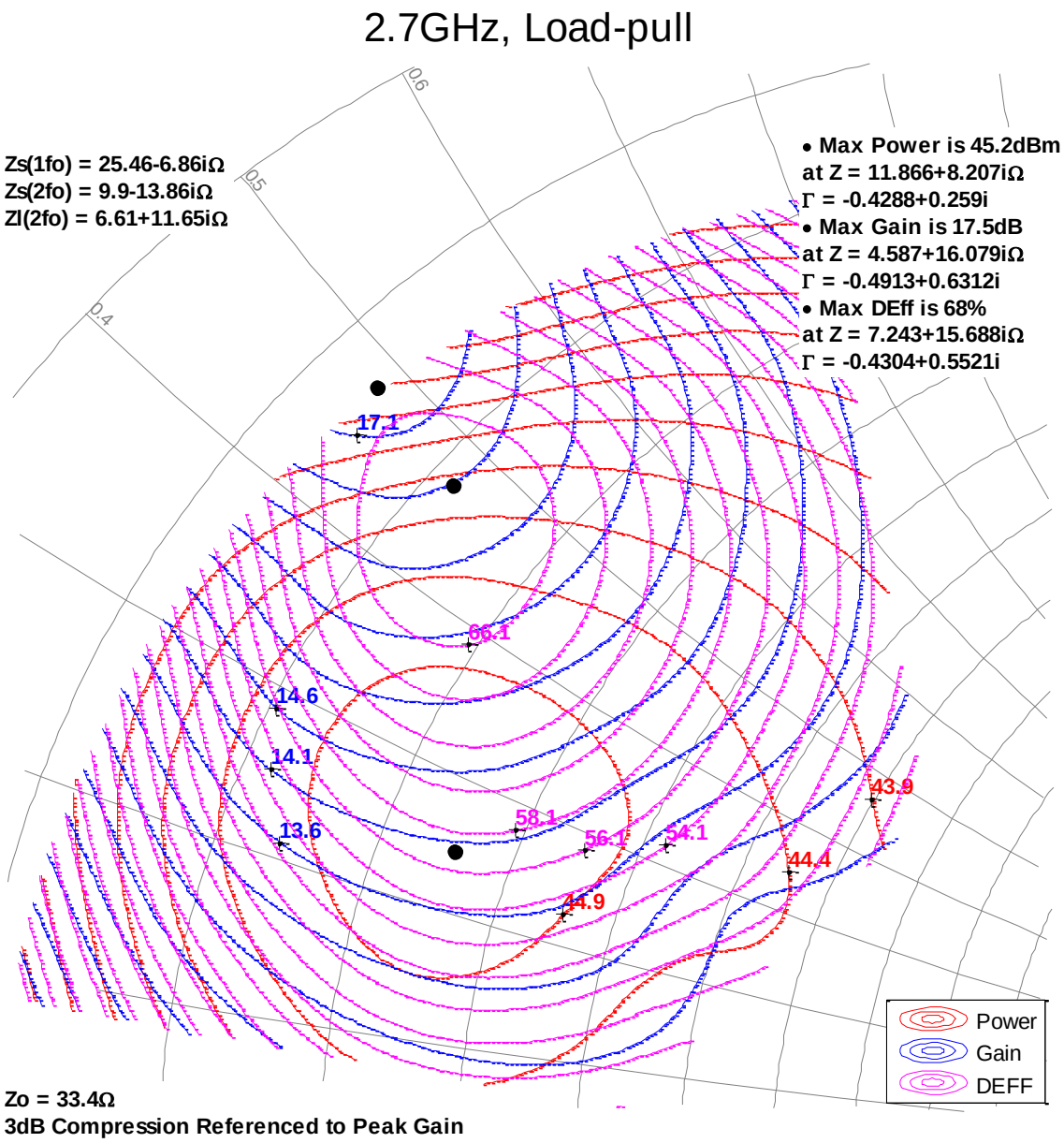
RF Characterization – Mismatch Ruggedness at 2.9 GHz

Symbol	Parameter	dB Compression	Typical
VSWR	Impedance Mismatch Ruggedness	3	10:1

Test conditions unless otherwise noted: T_A = 25 °C, V_D = 50 V, I_{DQ} = 52.5 mA, Pulsed, 128 uS Pulse Width, 10% Duty Cycle
Input drive power is determined at pulsed 3dB compression under matched condition at EVB output connector.

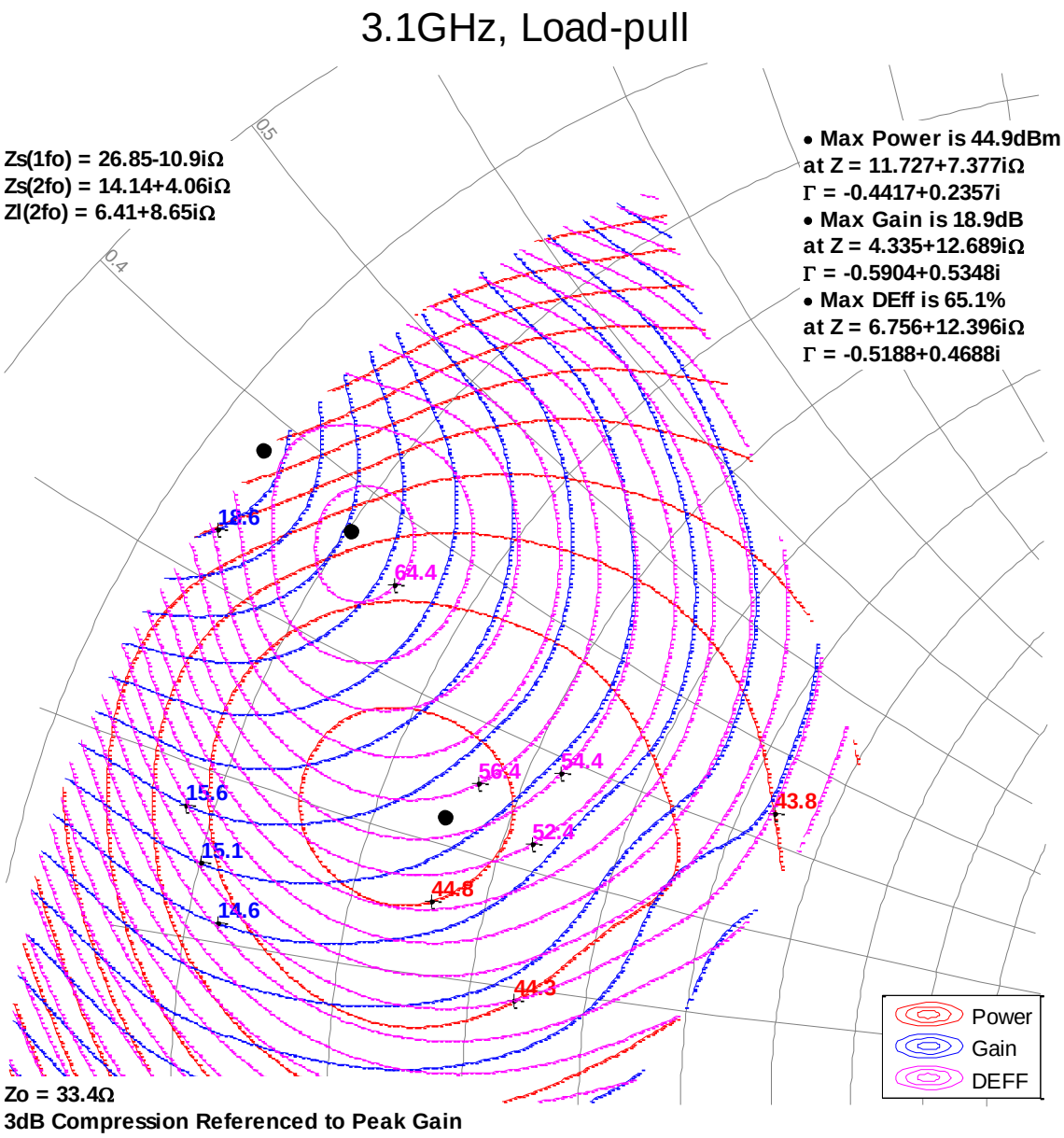
Measured Load-Pull Smith Charts[1, 2]

Notes:
1. Test Conditions: V_D = 50 V, I_{DQ} = 52.5 mA, 100 uS Pulse Width, 20% Duty Cycle
2. See page 15 for load pull reference planes where the performance was measured.



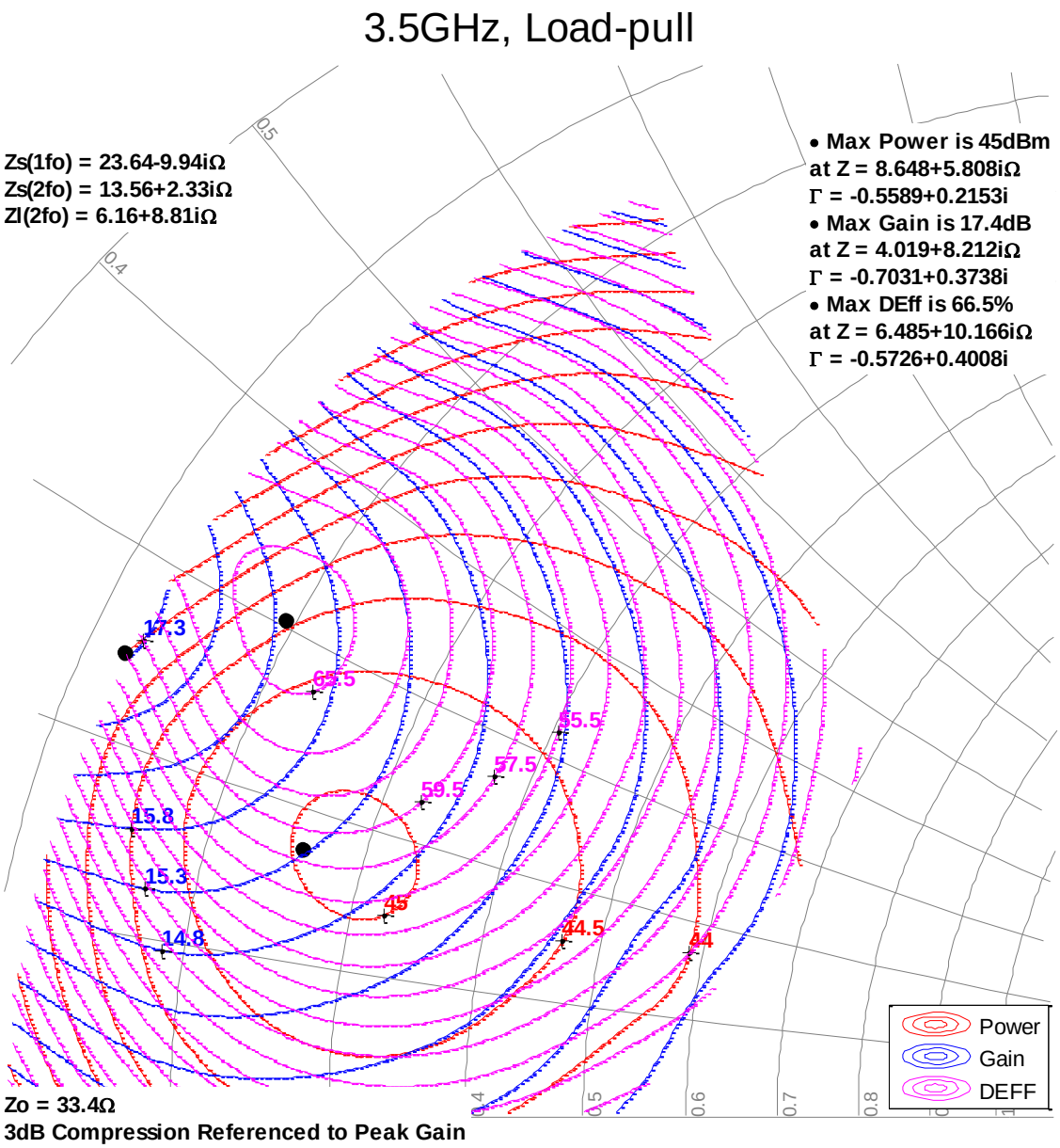
Measured Load-Pull Smith Charts[1, 2]

Notes:
1. Test Conditions: V_D = 50 V, I_{DQ} = 52.5 mA, 100 uS Pulse Width, 20% Duty Cycle
2. See page 15 for load pull reference planes where the performance was measured.



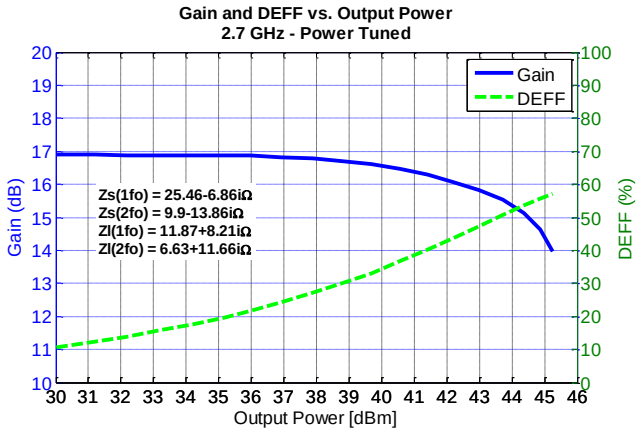
Measured Load-Pull Smith Charts[1, 2]

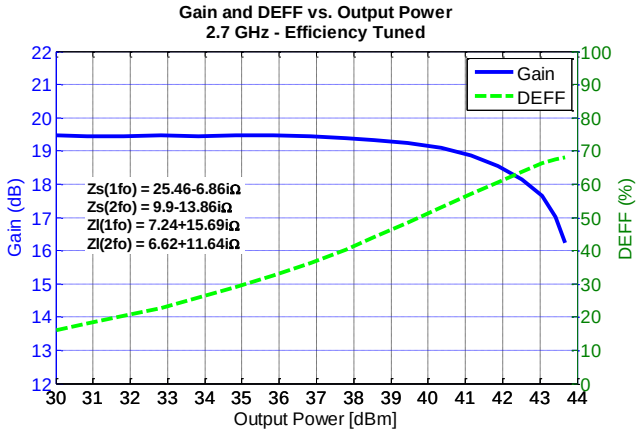
Notes:
1. Test Conditions: V_D = 50 V, I_{DQ} = 52.5 mA, 100 uS Pulse Width, 20% Duty Cycle
2. See page 15 for load pull reference planes where the performance was measured.

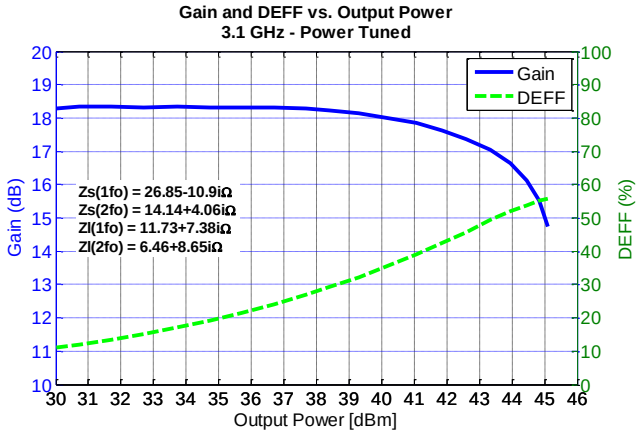


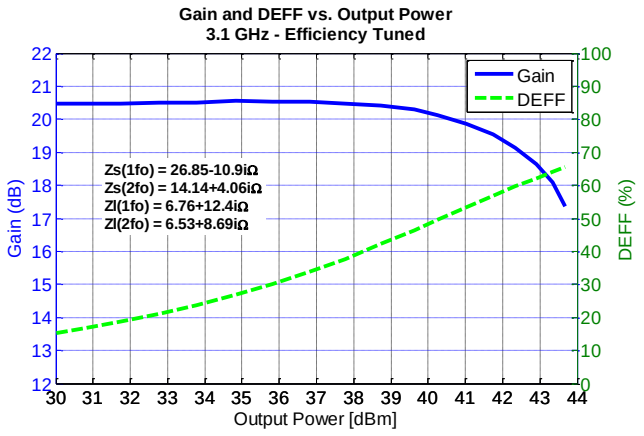
Typical Measured Performance – Load-Pull Drive-up[1, 2]

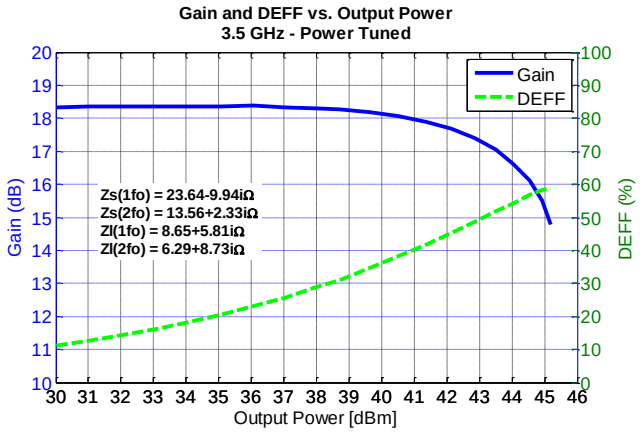
Notes:
1. Test Conditions: V_D = 50 V, I_{DQ} = 52.5 mA, 100 uS Pulse Width, 20% Duty Cycle
2. See page 15 for load-pull and source-pull reference planes where the performance was measured.

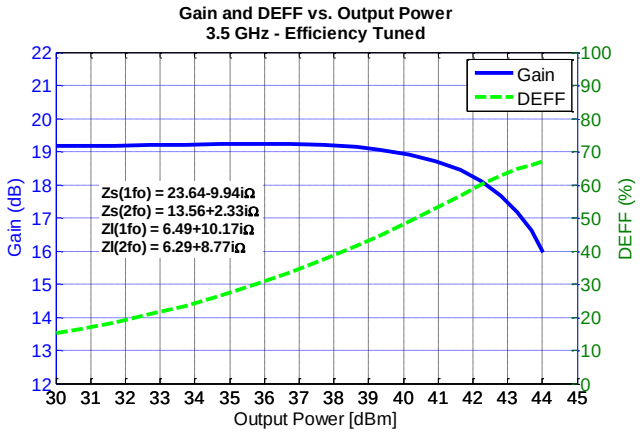






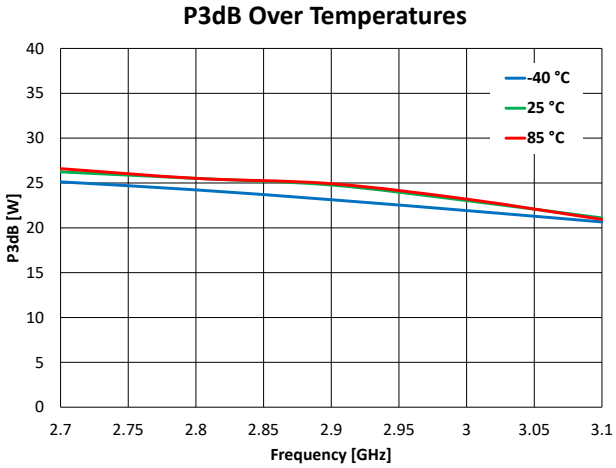


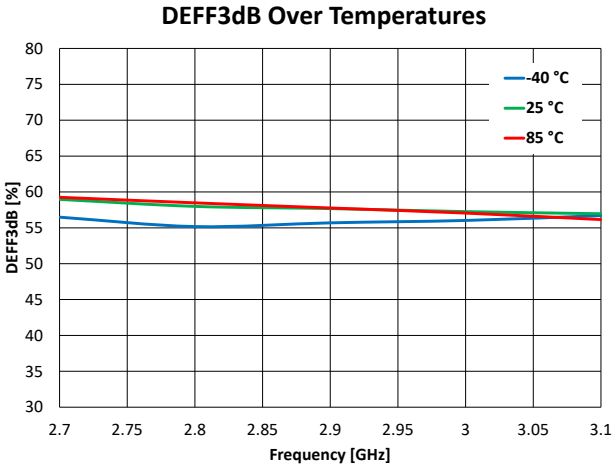


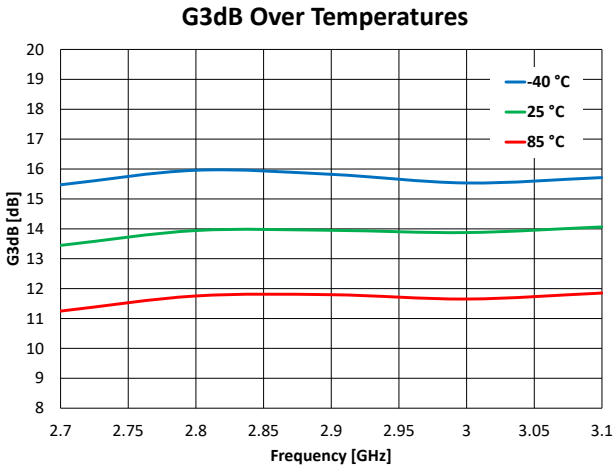


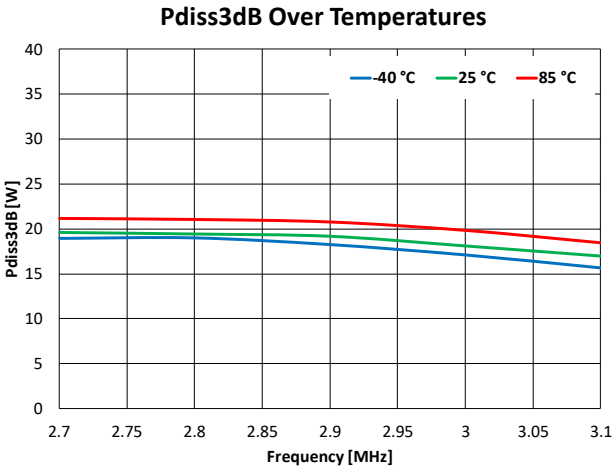
Power Driveup Performance Over Temperatures Of 2.7 – 3.1 GHz EVB[1]

Notes:
1. Test Conditions: V_D = 50 V, I_{DQ} = 52.5 mA, 128 uS Pulse Width, 10% Duty Cycle



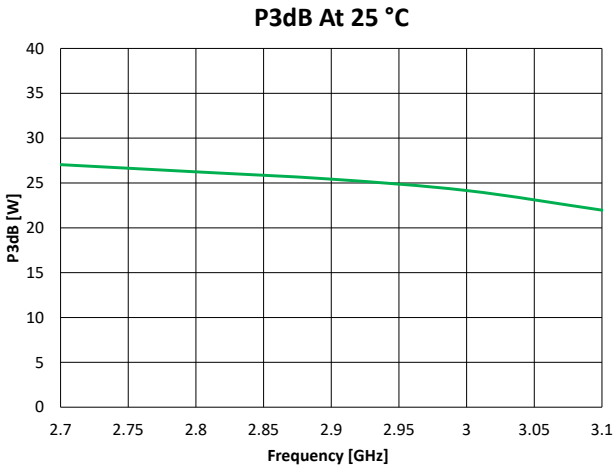


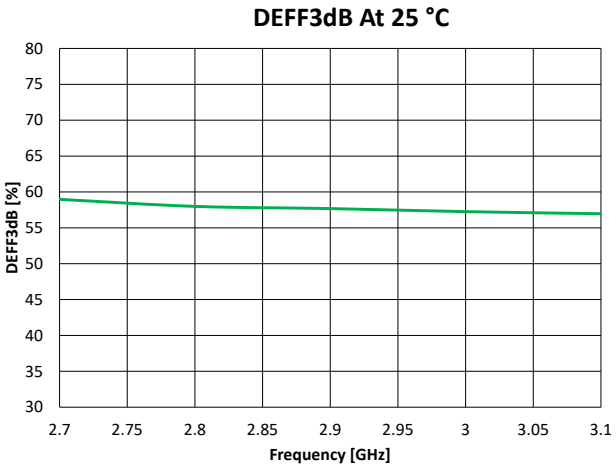


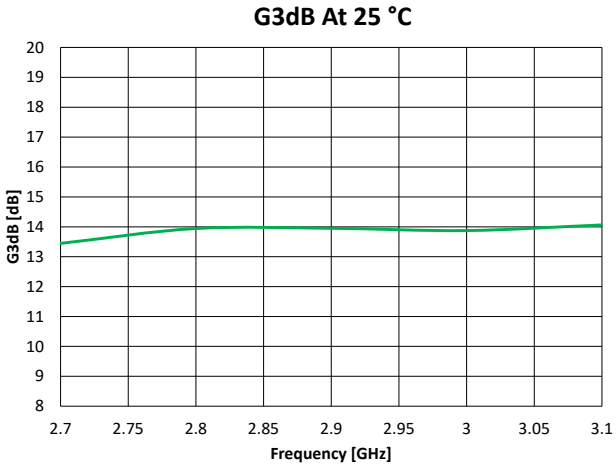


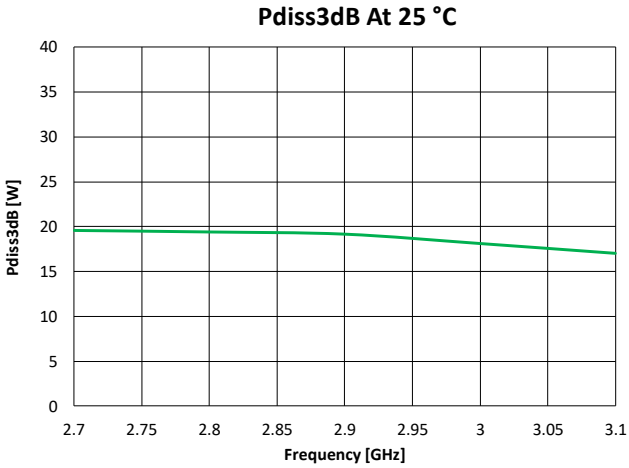
Power Driveup Performance At 25°C Of 2.7 – 3.1 GHz EVB[1, 2]

Notes:
1. Test Conditions: V_D = 50 V, I_{DQ} = 52.5 mA, 128 uS Pulse Width, 10% Duty Cycle



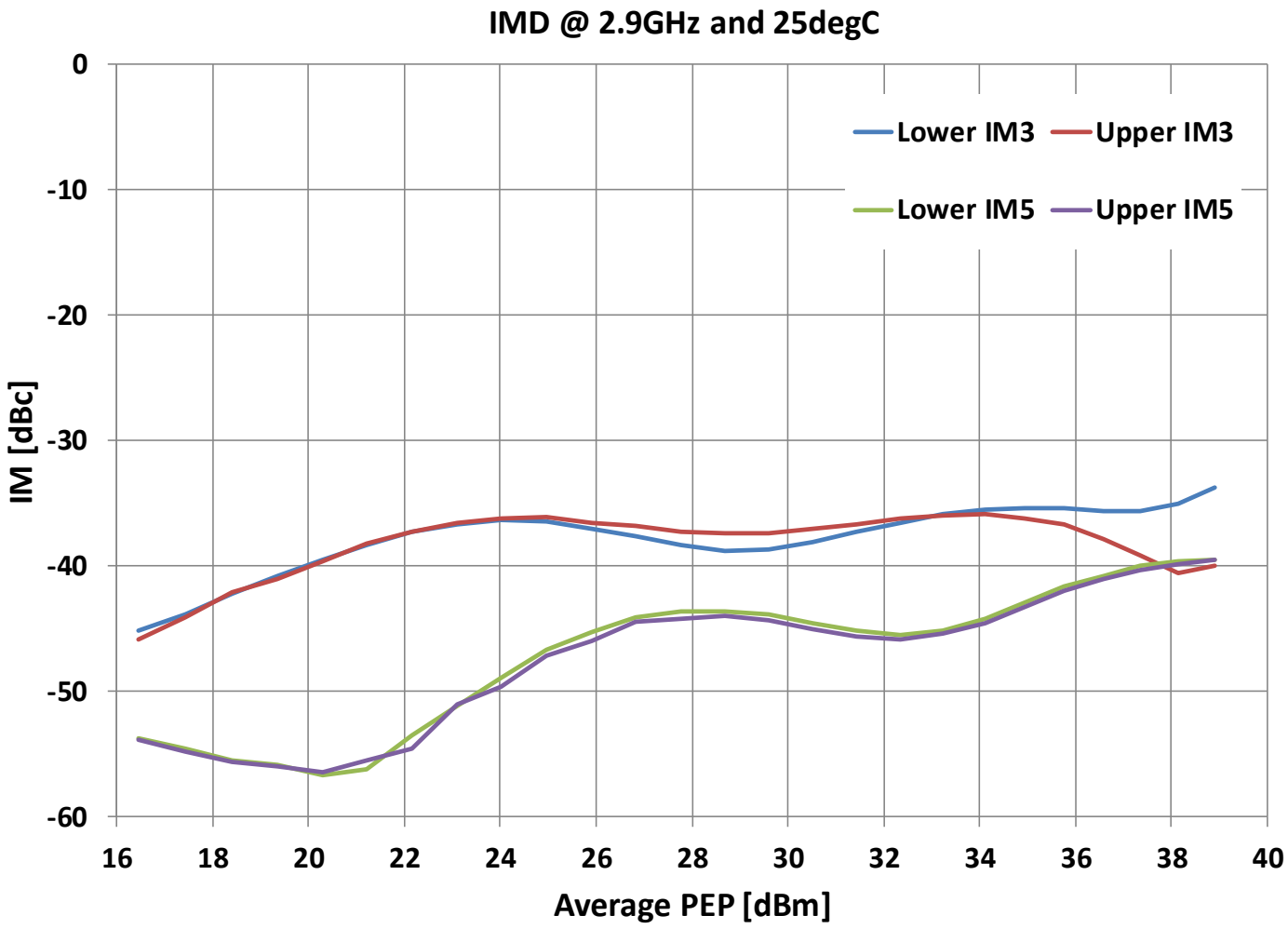






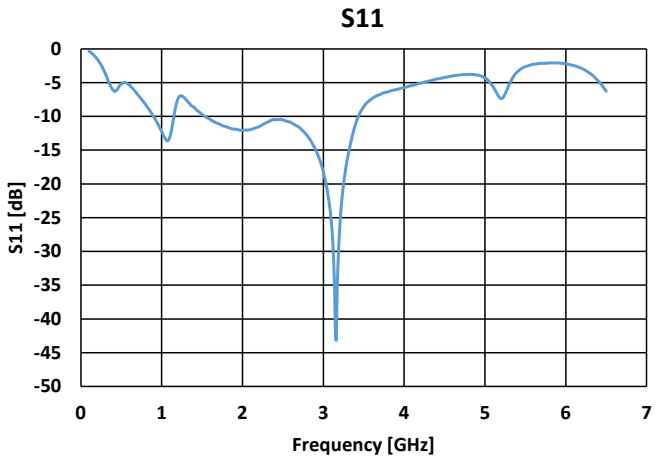
2-Tone 2.9 GHz Performance At 25°C Of 2.7 – 3.1 GHz EVB[1, 2]

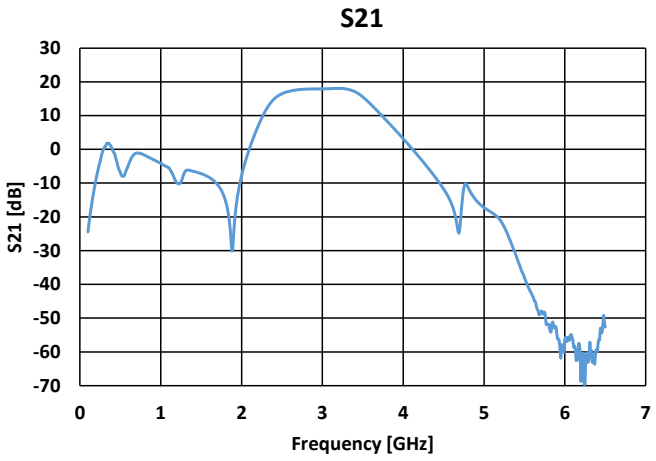
Notes:
1. Test Conditions: V_D = 50 V, I_{DQ} = 52.5 mA
2. Tone spacing = 1 MHz.

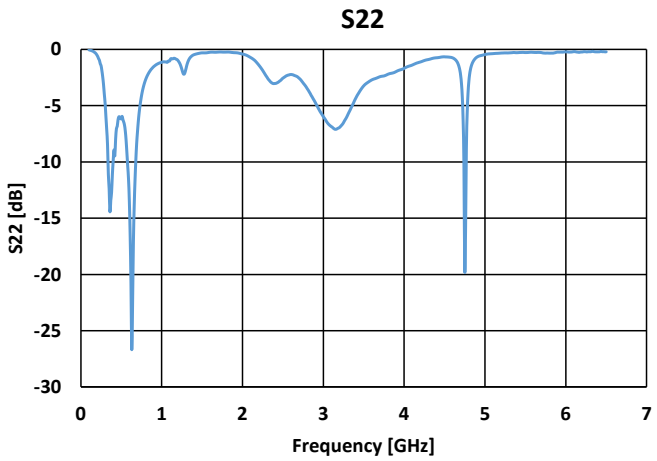


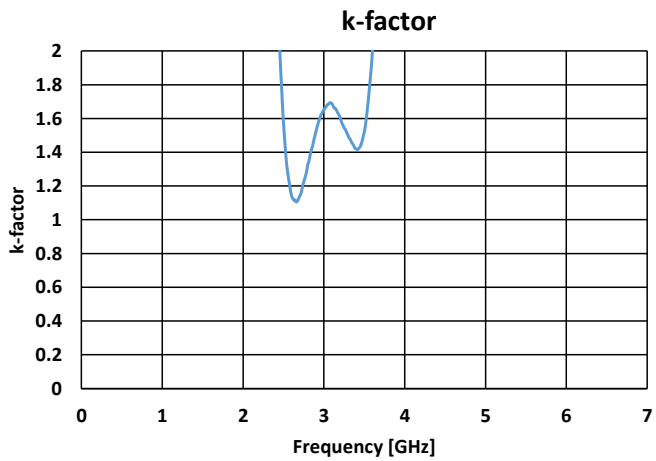
Small Signal Performance At 25°C Of 2.7 – 3.1 GHz EVB[1, 2]

Notes:
1. Test Conditions: V_D = 50 V, I_{DQ} = 52.5 mA
2. K factor > 1 indicates unconditional stability.

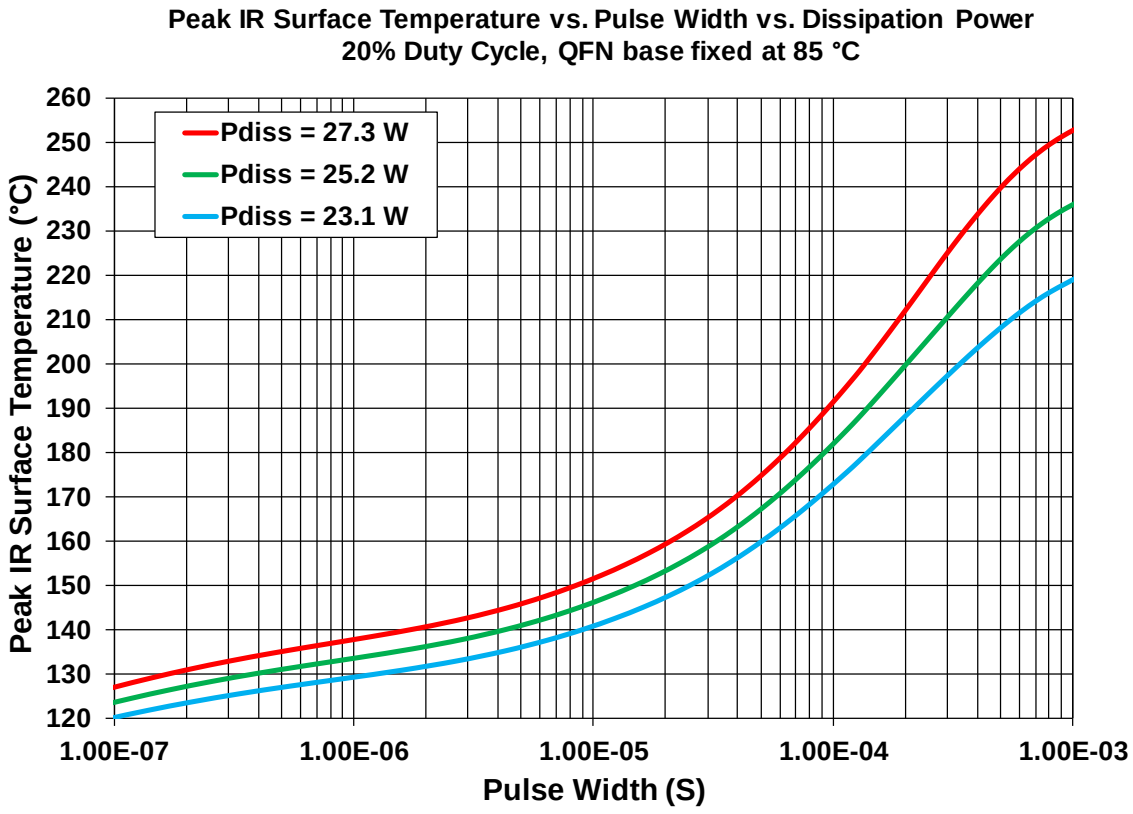








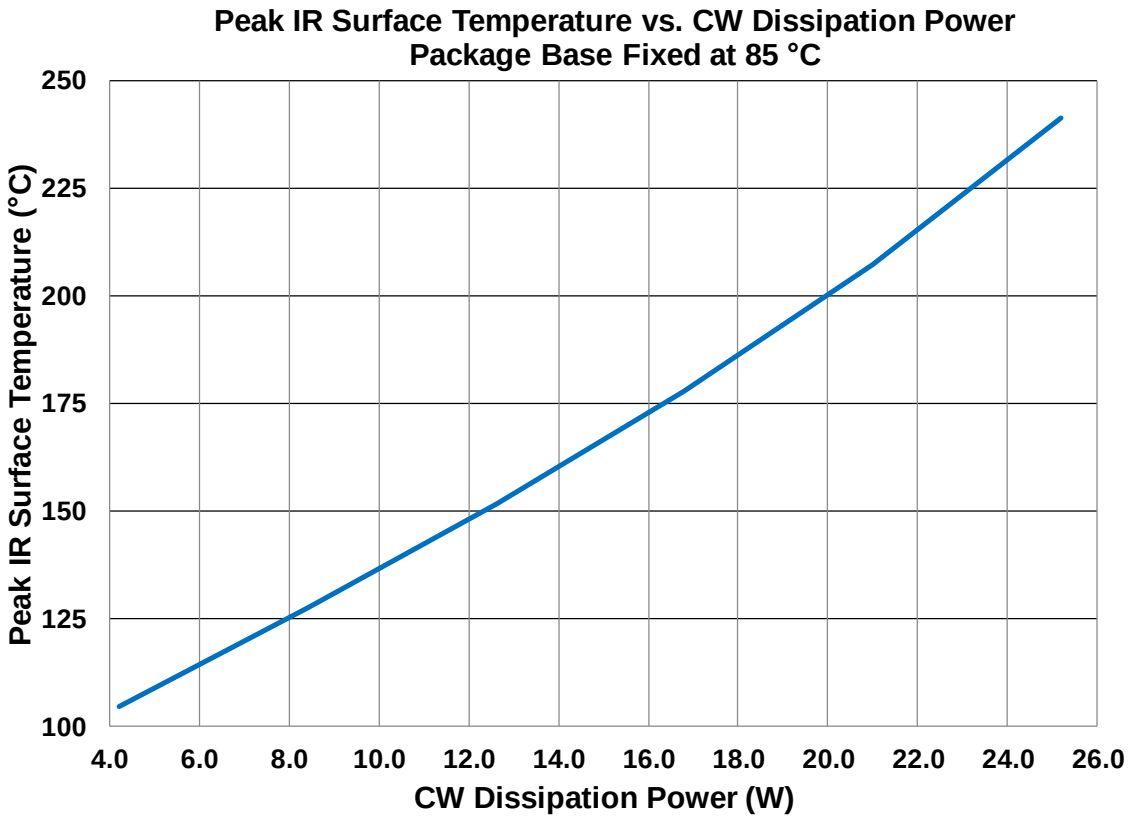
Thermal and Reliability Information – Pulsed



Parameter	Conditions	Values	Units
Thermal Resistance, IR[1] (θ_{JC})	85 °C Case 23.1 W Pdiss, 100 uS PW, 20% DC	3.79	°C/W
Peak IR Surface Temperature[1] (T_{CH})		173	°C
Thermal Resistance, IR[1] (θ_{JC})	85 °C Case 25.2 W Pdiss, 100 uS PW, 20% DC	3.84	°C/W
Peak IR Surface Temperature[1] (T_{CH})		182	°C
Thermal Resistance, IR[1] (θ_{JC})	85 °C Case 27.3 W Pdiss, 100 uS PW, 20% DC	3.89	°C/W
Peak IR Surface Temperature[1] (T_{CH})		191	°C

Notes:
[1]Refer to the following document GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates

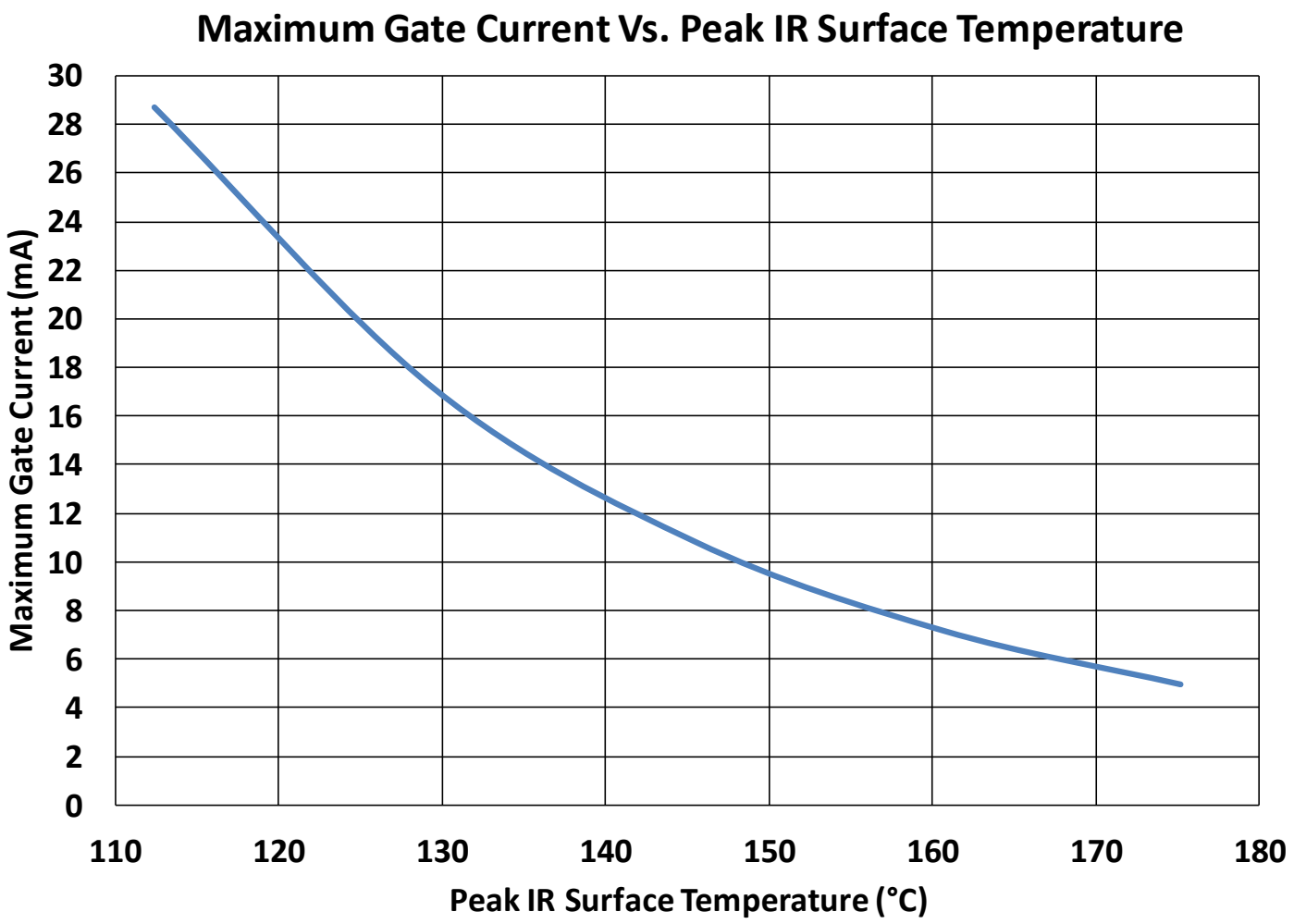
Thermal and Reliability Information - CW



Parameter	Conditions	Values	Units
Thermal Resistance, IR[1] (θ_{JC})	85 °C Case 12.6 W Pdiss, CW	5.29	°C/W
Peak IR Surface Temperature[1] (T_{CH})		152	°C
Thermal Resistance, IR[1] (θ_{JC})	85 °C Case 16.8 W Pdiss, CW	5.52	°C/W
Peak IR Surface Temperature[1] (T_{CH})		178	°C
Thermal Resistance, IR[1] (θ_{JC})	85 °C Case 21 W Pdiss, CW	5.82	°C/W
Peak IR Surface Temperature[1] (T_{CH})		207	°C

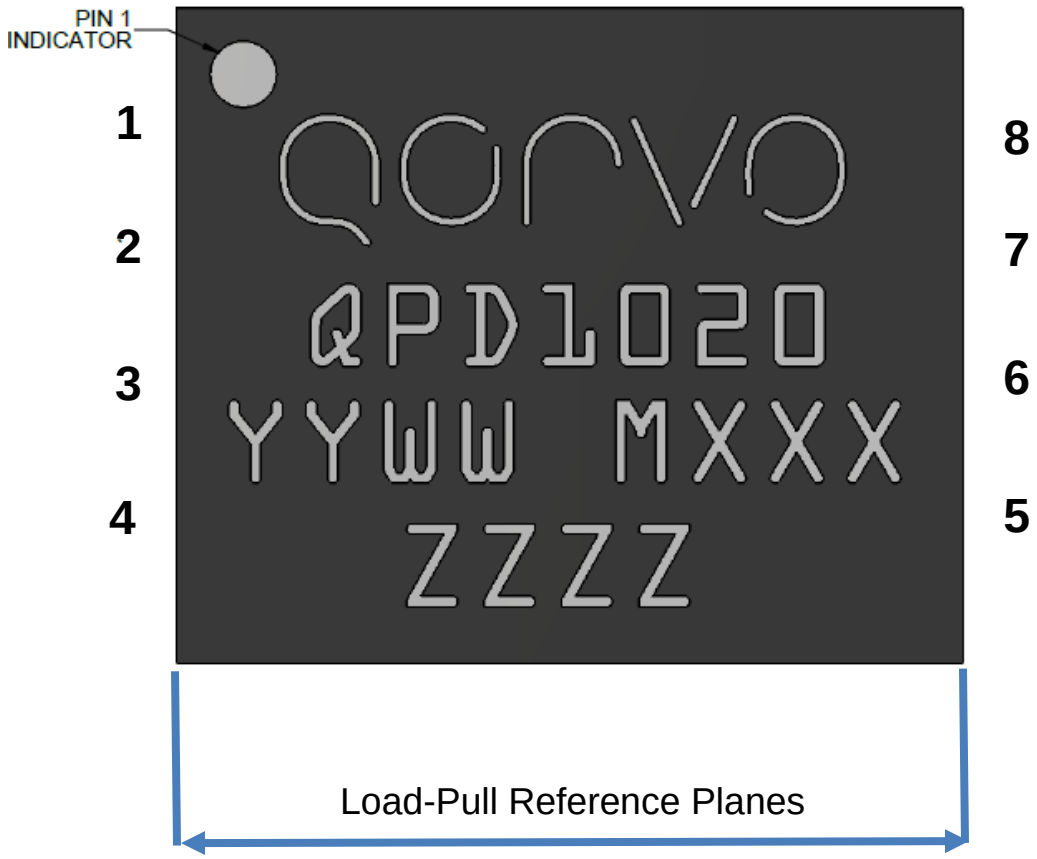
Notes:
[1]Refer to the following document GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates

Maximum Gate Current



Pin Configuration and Description[1]

Note 1: The QPD1020 will be marked with the “QPD1020” designator and a lot code marked below the part designator. The “YY” represents the last two digits of the calendar year the part was manufactured, the “WW” is the work week of the assembly lot start, the MXXX” is the production lot number, and the “ZZZ” is an auto-generated serial number.

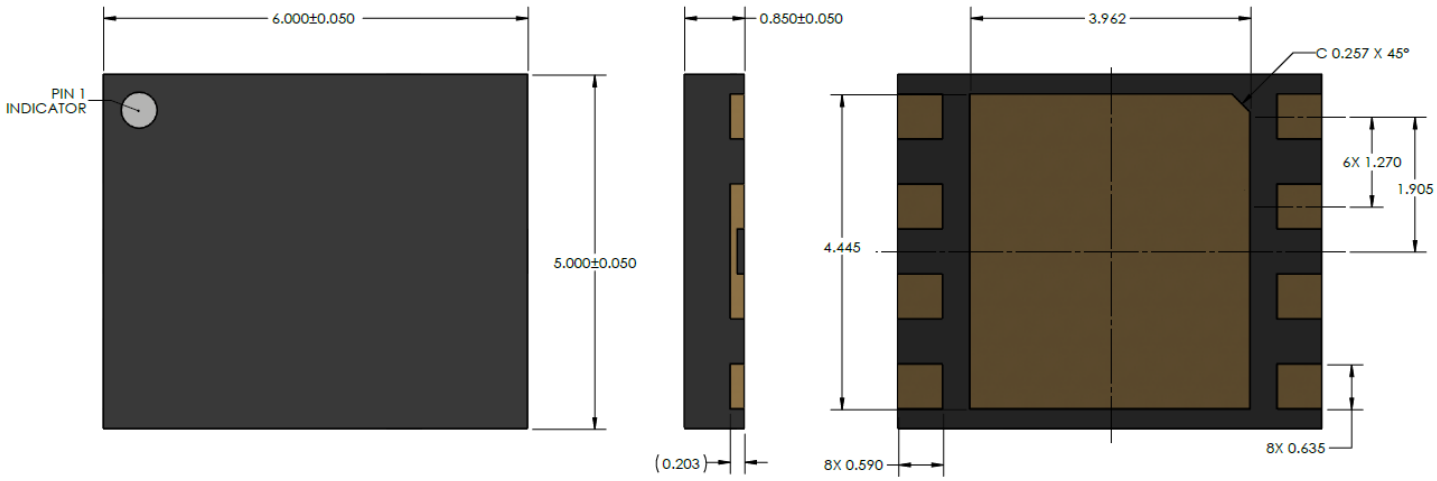


Pin	Symbol	Description
2, 3	RF IN / V_G	Gate
6, 7	RF OUT / V_D	Drain
1, 4, 5, 8	N/C	No Connection
9	Source	Source / Ground / Backside of part (See next page.)

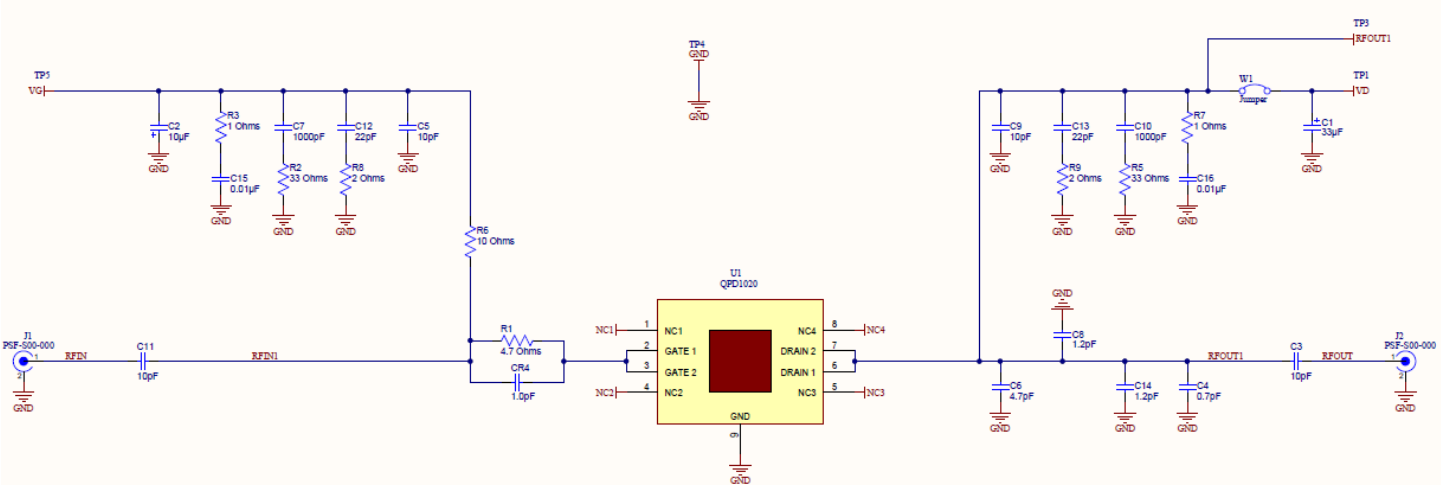
Mechanical Drawing[1]

Note 1:

1. Dimensions are in mm. Dimension tolerance is ± 0.1 mm, unless otherwise noted.
2. Pakage exposed metallization is gold plated.
3. Part is overmold encapsulated.



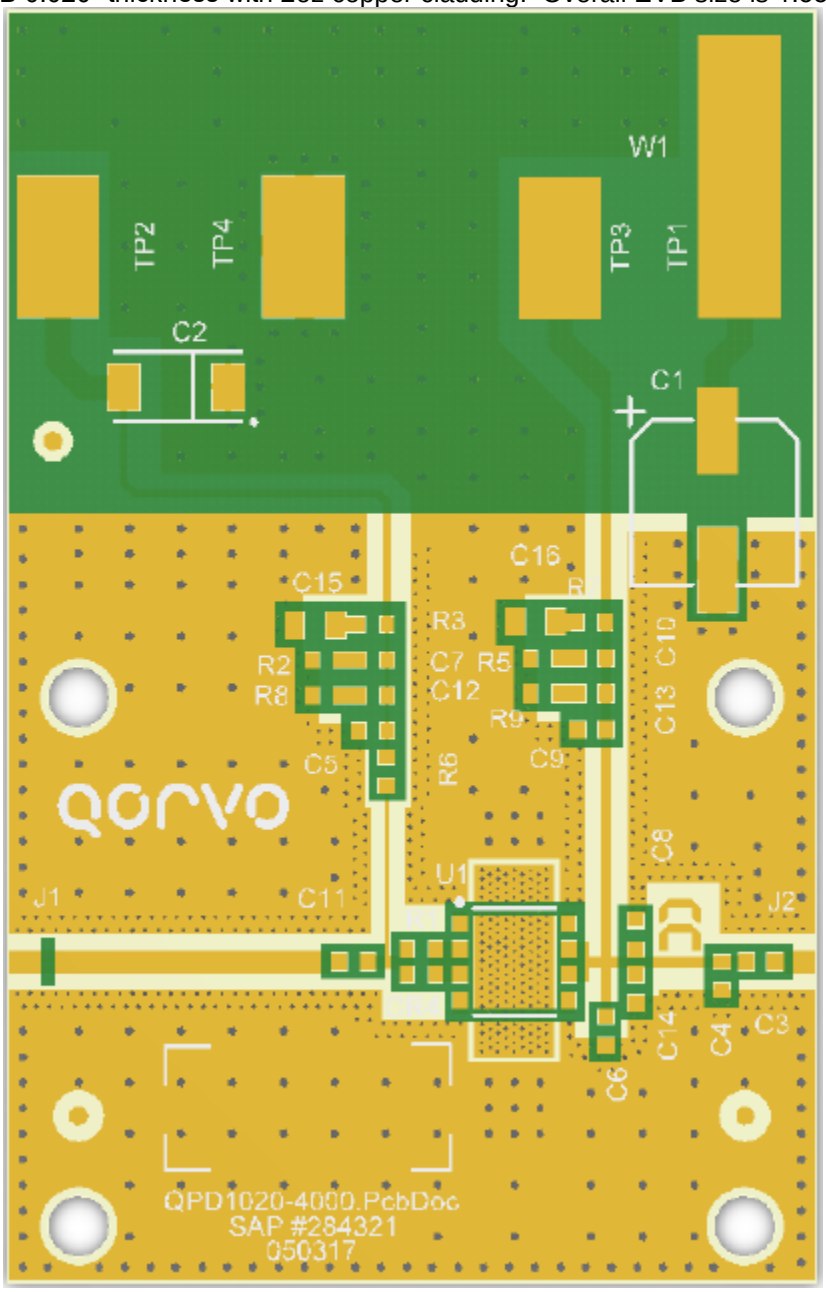
2.7 – 3.1 GHz Application Circuit - Schematic



Bias-up Procedure	Bias-down Procedure
1. Set V_G to -4 V.	1. Turn off RF signal.
2. Set I_D current limit to 60 mA.	2. Turn off V_D
3. Apply 50 V V_D.	3. Wait 2 seconds to allow drain capacitor to discharge
4. Slowly adjust V_G until I_D is set to 52.5 mA.	4. Turn off V_G
5. Set I_D current limit to 120 mA (Pulsed operation)	
6. Apply RF.	

2.7 – 3.1 GHz Application Circuit - Layout

Board material is RO4350B 0.020” thickness with 2oz copper cladding. Overall EVB size is 1.58” x 2.48”.



2.7 – 3.1 GHz Application Circuit - Bill Of material

Description	Ref. Des.	Manufacturer	Part Number
Cap 10 UF +/-10% 16V LOW ESR TANT	C2	AVX	TPSC106K016R0500
CAP, 1000pF,100V, 10%, X7R, 0603	C7, C10	AVX	06031C102KAT2A
CAP 0.01 UF,100V,5%,X7R,LF,0805	C15, C16	TTI	08051C103JAT2A
CAP, 4.7 PF, 250V,0603,LF +/-.1P	C6	ATC	600S4R7BT250XT
CAP, 10PF,250V,1%,0603	C3, C5, C9, C11	ATC	600S100FT250XT
CAP, 1.0pF, +/-0.05pF, 250V, HI-Q	CR4	ATC	600S1R0AT250XT
CAP, 0.7pF, +/-0.05pF, 250V, HI-Q	C4	ATC	600S0R7AT250XT
CAP, 22pF, +/-5%, 250V, HI-Q, 0603	C12, C13	ATC	600S220JT250XT
CAP, 33uF, 20%, 80V, ALUM ELEC,8mm SMD	C1	Panasonic	EEE-FK1K330P
CAP, 1.2pF, +/-0.05pF, 250V, C0G	C8, C14	ATC	600S1R2AT250XT
RES, 2 OHM, 1%, 1/10W, 0603	R8, R9	Vishay	CRCW06032R00FKEA
RES, 1 OHM, 1%, 1/10, 0603	R3, R7	Samsung	RC1608F1R0CS
33 OHM,5%,0.1W,0603,LEAD FREE	R2, R5	KOA	RK73B1JTTD330J
10 OHM,1%,0.1W,0603,LEAD FREE	R6	KOA	RK73H1JTTD10R0F
CONN, SMA, 4-HOLE PANEL MOUNT	J1, J2	Gigalane	PSF-S00-000

Recommended Solder Temperature Profile