QPD1881L

400 W, 50 V, 2.7 – 2.9 GHz, GaN RF Power Transistor

Product Overview

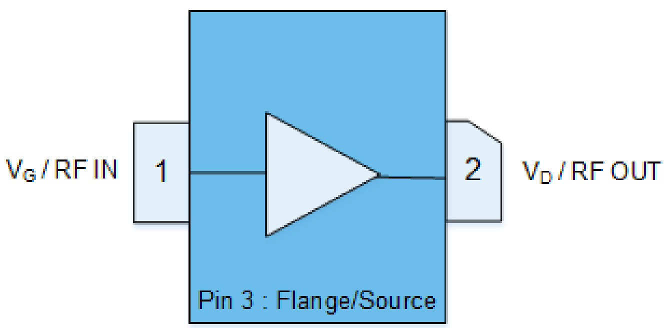
The Qorvo QPD1881L is a 400 W (P_{3dB}) discrete GaN on SiC HEMT which operates from 2.7 to 2.9 GHz. Input pre-match within the package results in ease of external board match and saves board space. The device is in an industry standard air cavity package and is ideally suited for civilian radar, weather radar and test instrumentation. The device can support both CW and pulsed operations.

Lead-free and ROHS compliant

Evaluation boards are available upon request.

2-lead NI-780 Package (Eared)

Functional Block Diagram



Key Features

- Frequency: 2.7 to 2.9 GHz
- Output Power (P_{3dB})[1]: 427 W
- Linear Gain[1]: 21.2 dB
- Typical PAE_{3dB}[1]: 75.1%
- Operating Voltage: 50 V
- CW and Pulse capable

Note 1: @ 2.9 GHz Load Pull

Applications

- Civilian radar
- Weather radar
- Test instrumentation

Ordering info

Part No.	ECCN	Description
QPD1881L	EAR99	2.7 – 2.9 GHz Transistor
QPD1881LS2	EAR99	2 Piece Sample Bag
QPD1881LEVB01	EAR99	2.7 – 2.9 GHz Evaluation Board

Absolute Maximum Ratings [1, 2, 3]

Parameter	Rating	Units
Breakdown Voltage, BV_{DG}	145	V
Gate Voltage Range, V_G	-7 to +2	V
Drain Current, I_{DMAX}	56	A
Drain Voltage, V_D	55	V
Gate Current Range, I_G	See pg. 12	mA
Power Dissipation, Pulsed, P_{DISS} [2]	466	W
Power Dissipation, CW, P_{DISS}	237	W
RF Input Power, Pulsed, P_{IN} [3]	41.9	dBm
Channel Temperature, T_{CH}	275	°C
Mounting Temperature (30 Seconds)	320	°C
Storage Temperature	−65 to +150	°C

Notes:
1. Operation of this device outside the parameter ranges given above may cause permanent damage
2. Pulsed, 100us PW, 10% DC, Package base at 85 °C
3. Pulsed, 100us PW, 10% DC, T = 25 °C

Recommended Operating Conditions [1, 2, 3, 4]

Parameter	Min	Typ	Max	Units
Operating Temp. Range	−40	+25	+85	°C
Drain Voltage Range, V_D	–	+50	–	V
Drain Bias Current, I_{DQ}	–	0.7	–	A
Drain Current, I_D [4]	–	13	–	A
Gate Voltage, V_G [3]	–	−2.8	–	V
Channel Temperature (T_{CH})	–	–	250	°C
Power Dissipation (P_D) [2,4]	–	–	418	W
Power Dissipation (P_D), CW [2]	–	–	213	W

Notes:
1. Electrical performance is measured under conditions noted in the electrical specifications table. Specifications are not guaranteed over all recommended operating conditions
2. Package base at 85 °C
3. To be adjusted to desired I_{DQ}
4. Pulsed, 100us PW, 10% DC

Measured Load Pull Performance – Power Tuned [1, 2]

Parameter	Typical Values		Units
Frequency, F	2.7	2.9	GHz
Output Power at 3dB compression, P_{3dB}	56.2	56.3	dBm
Power Added Efficiency at 3dB compression, PAE_{3dB}	67.8	63.3	%
Gain at 3dB compression, G_{3dB}	17.3	16.6	dB

Notes:
1. Test conditions unless otherwise noted: T_A = 25 °C, V_D = 50 V, I_{DQ} = 700 mA
2. Pulsed, 100 us Pulse Width, 10% Duty Cycle.

Measured Load Pull Performance – Efficiency Tuned [1, 2]

Parameter	Typical Values		Units
Frequency, F	2.7	2.9	GHz
Output Power at 3dB compression, P_{3dB}	55.1	54.4	dBm
Power Added Efficiency at 3dB compression, PAE_{3dB}	73.2	75.1	%
Gain at 3dB compression, G_{3dB}	18.5	18.2	dB

Notes:
1. Test conditions unless otherwise noted: T_A = 25 °C, V_D = 50 V, I_{DQ} = 700 mA
2. Pulsed, 100 us Pulse Width, 10% Duty Cycle.

RF Characterization – 2.7 – 2.9 GHz EVB Performance at 2.8 GHz [1]

Parameter	Min	Typ	Max	Units
Linear Gain, G_{LIN}	–	19.7	–	dB
Output Power at 3dB compression point, P3dB	–	306.4	–	W
Drain Efficiency at 3dB compression point, DEFF3dB	–	66.8	–	%
Gain at 3dB compression point, G3dB	–	16.7	–	dB

Notes:
1. V_D = 50 V, I_{DQ} = 0.7 A, Temp = +25 °C, Pulse Width = 100 us, Duty Cycle = 10%

RF Characterization – Mismatch Ruggedness at 2.8 GHz [1, 2, 3]

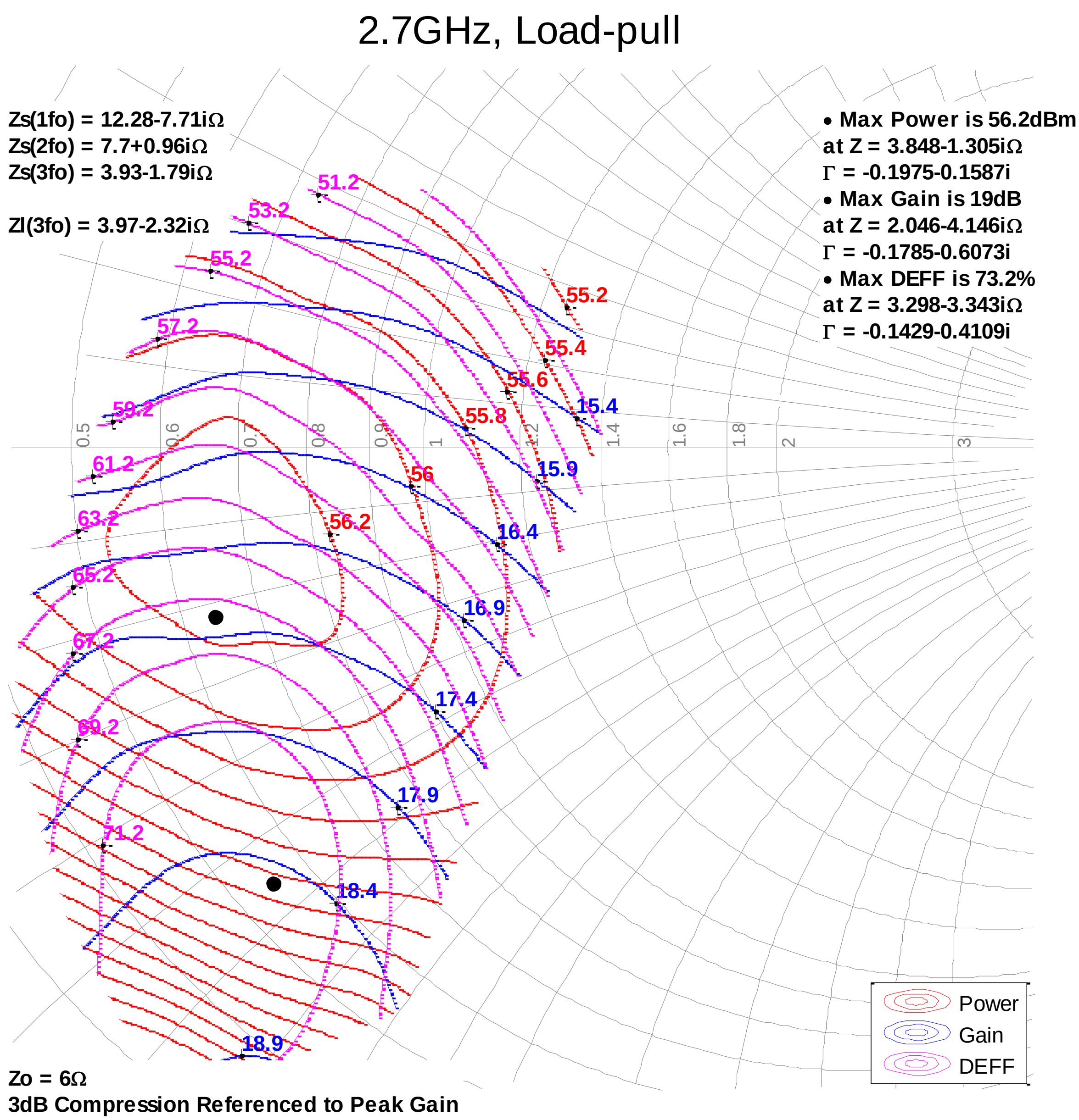
Symbol	Parameter	dB Compression	Typical
VSWR	Impedance Mismatch Ruggedness	3	10:1

Notes:
1. Test conditions unless otherwise noted: T_A = 25 °C, V_D = 50 V, I_{DQ} = 0.7 A
2. Input drive power is determined at pulsed 3dB compression under matched condition at EVB output connector
3. Pulse: 100us, 10% Duty cycle

Measured Load-Pull Smith Charts [1, 2]

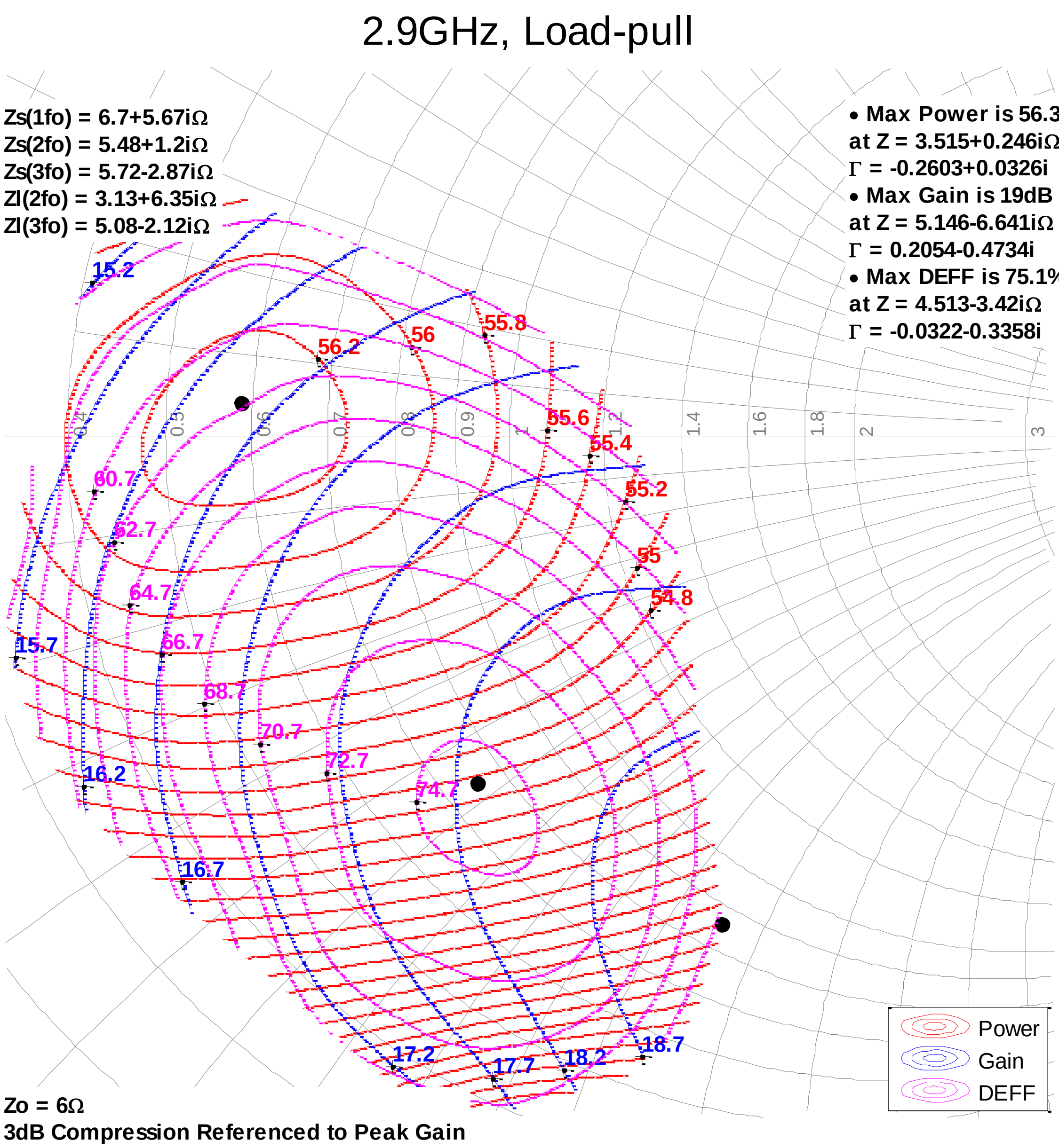
Notes:

1. Test Conditions: V_D = 50 V, I_{DQ} = 700 mA, 100 us Pulse Width, 10% Duty Cycle, Temp = 25°C.
2. See page 13 for load pull reference planes where the performance was measured.



Measured Load-Pull Smith Charts [1, 2]

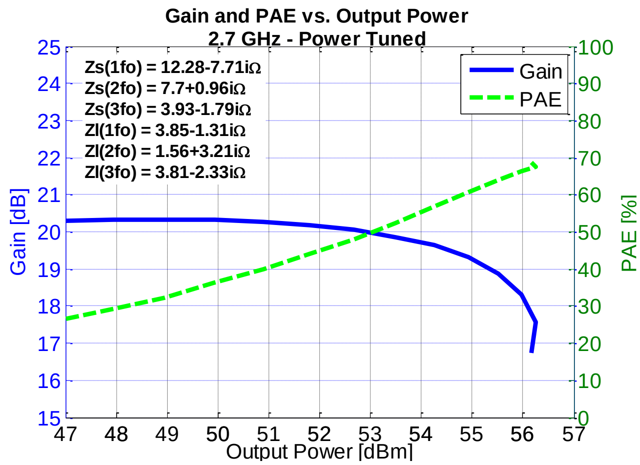
Notes:
1. Test Conditions: V_D = 50 V, I_{DQ} = 700 mA, 100 us Pulse Width, 10% Duty Cycle, Temp = 25°C.
2. See page 13 for load pull reference planes where the performance was measured.

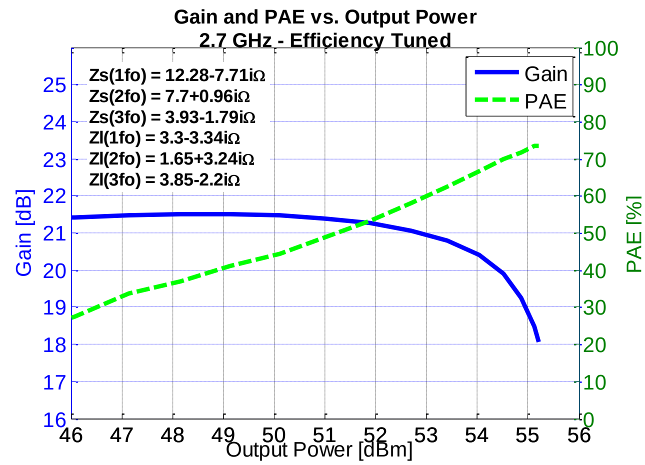


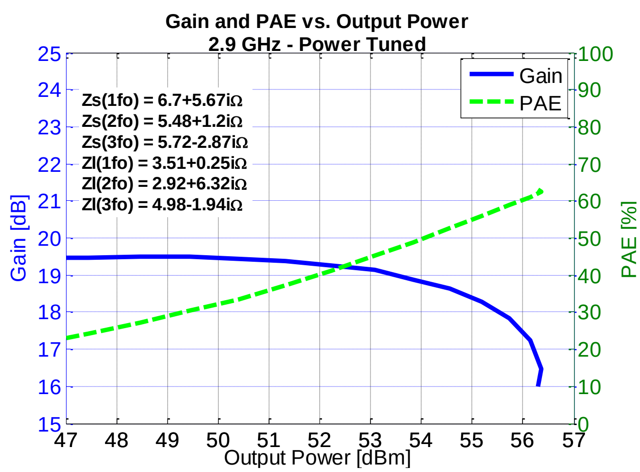
Typical Measured Performance – Load-Pull Drive-up [1, 2]

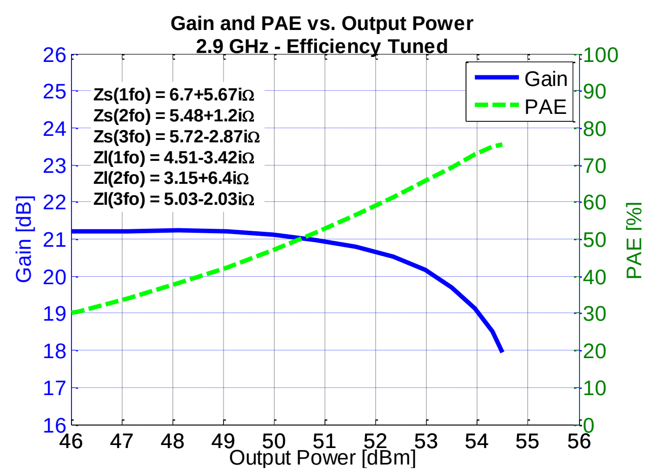
Notes:

1. Test Conditions: V_D = 50 V, I_{DQ} = 700 mA, 100 us Pulse Width, 10% Duty Cycle, Temp = 25°C.
2. See page 13 for load pull reference planes where the performance was measured.



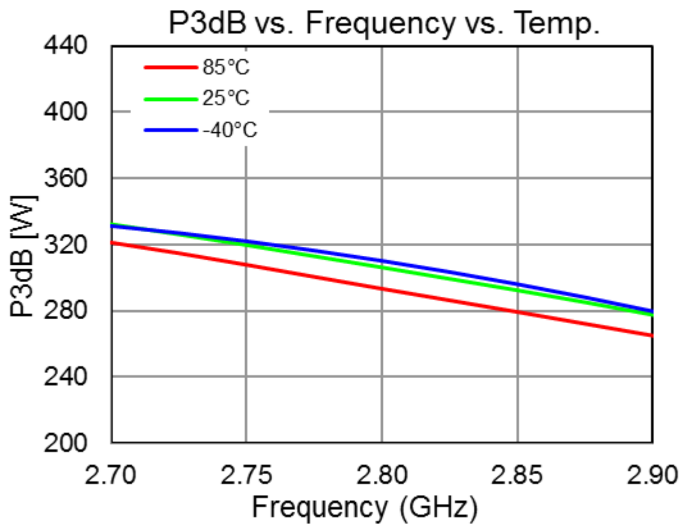


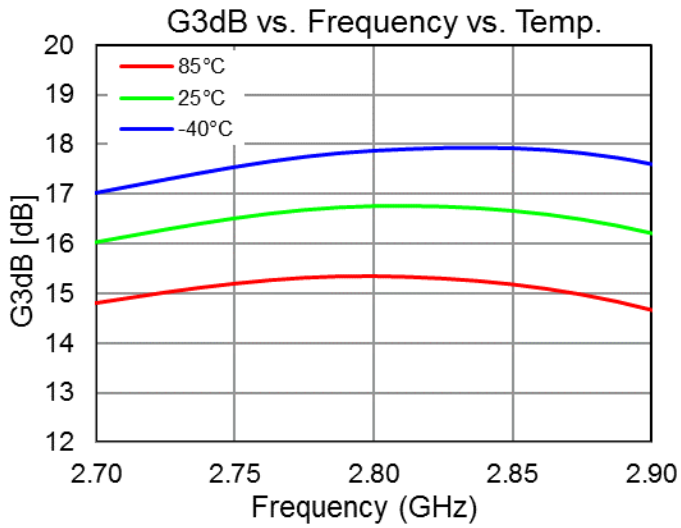


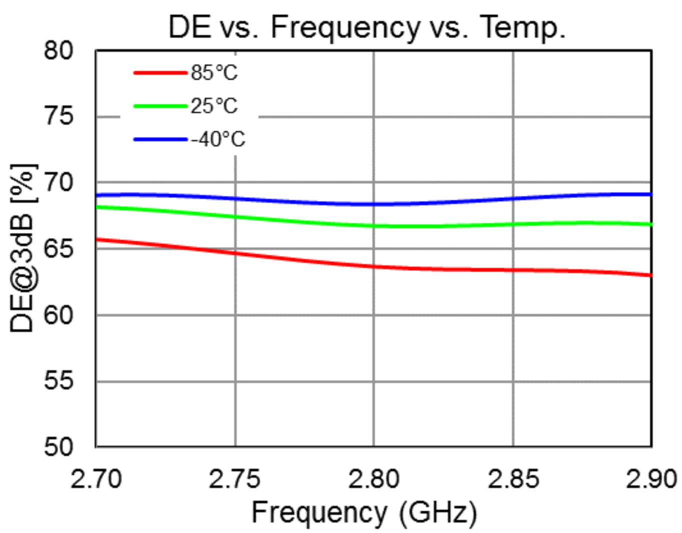


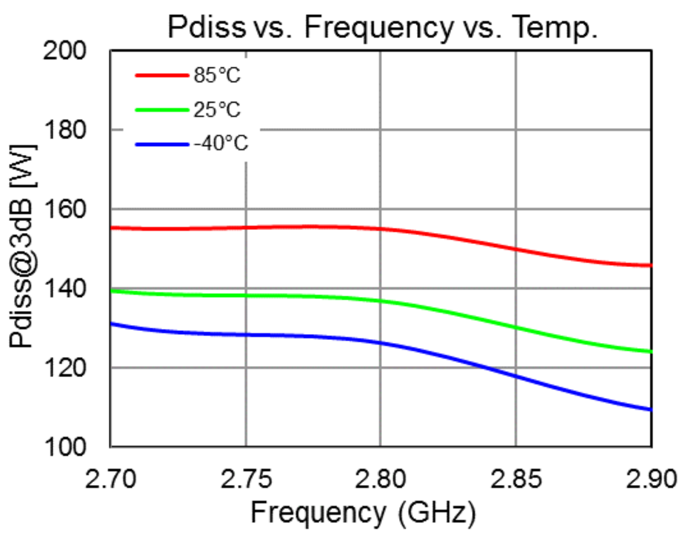
Large signal performance over temperatures of 2.7 – 2.9 GHz EVB [1]

Notes:
1. Test Conditions: V_D = 50 V, I_{DQ} = 0.7 A, 100 us Pulse Width, 10% Duty Cycle.





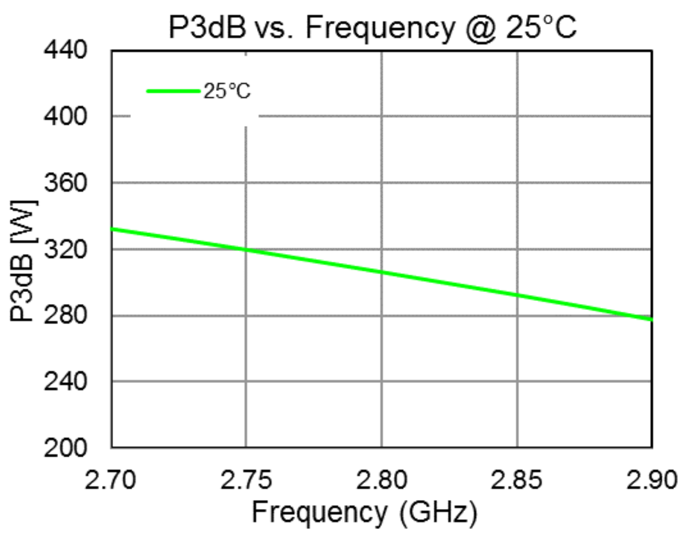


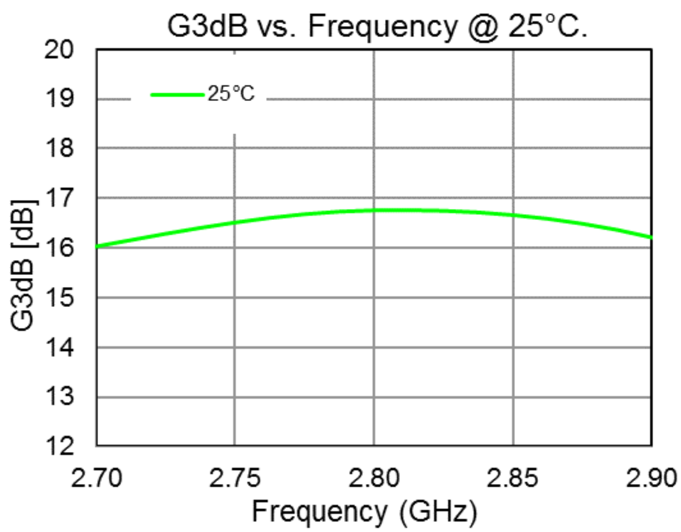


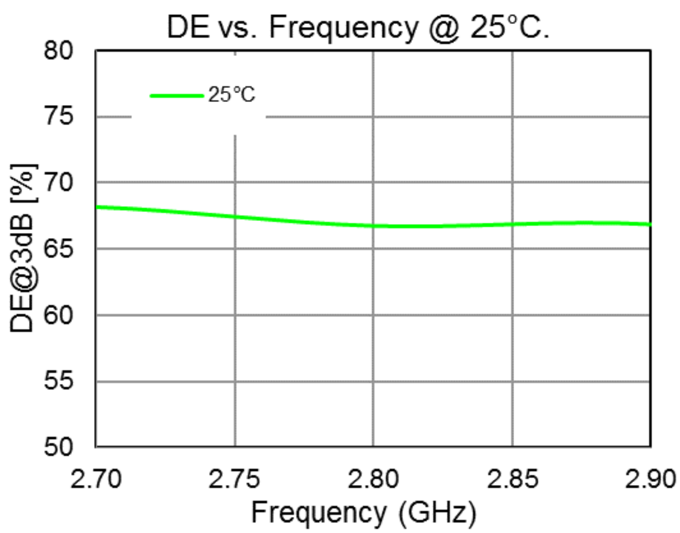
Large signal performance at 25°C of 2.7 – 2.9 GHz EVB [1]

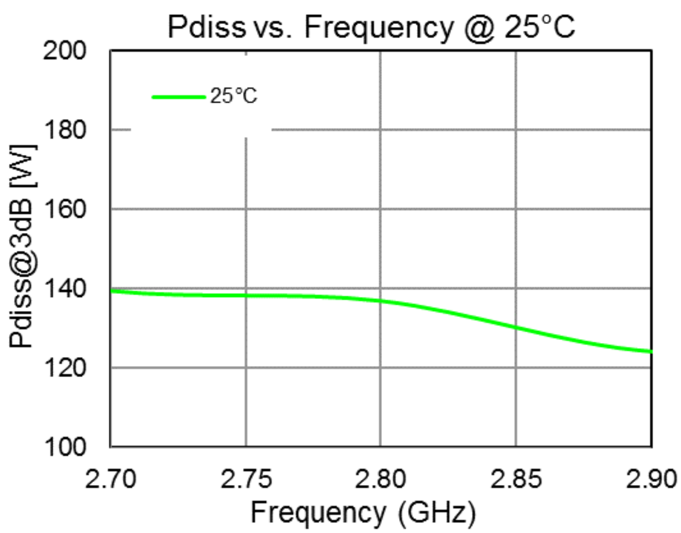
Notes:

1. Test Conditions: V_D = 50 V, I_{DQ} = 0.7 A, 100 us Pulse Width, 10% Duty Cycle.

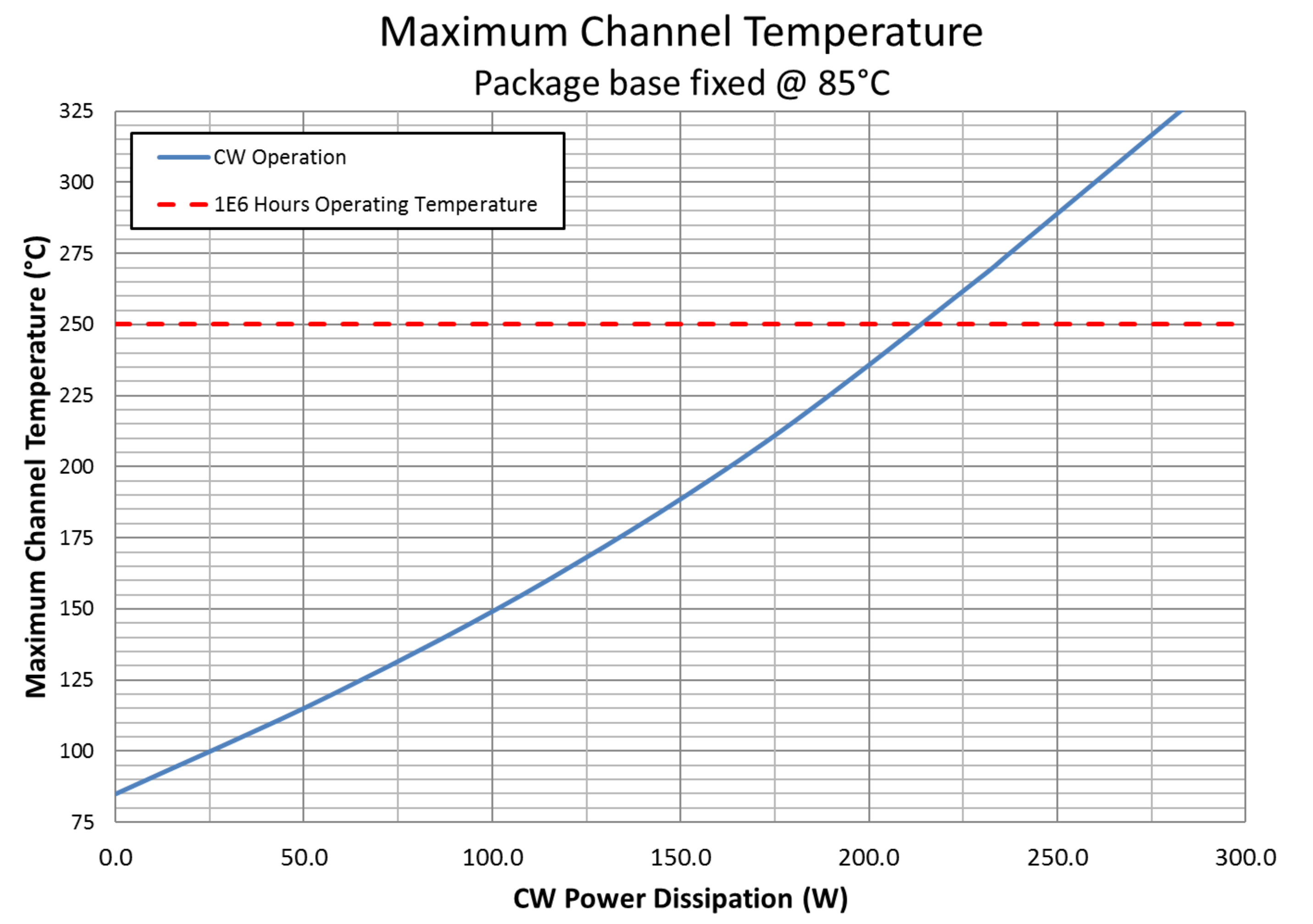








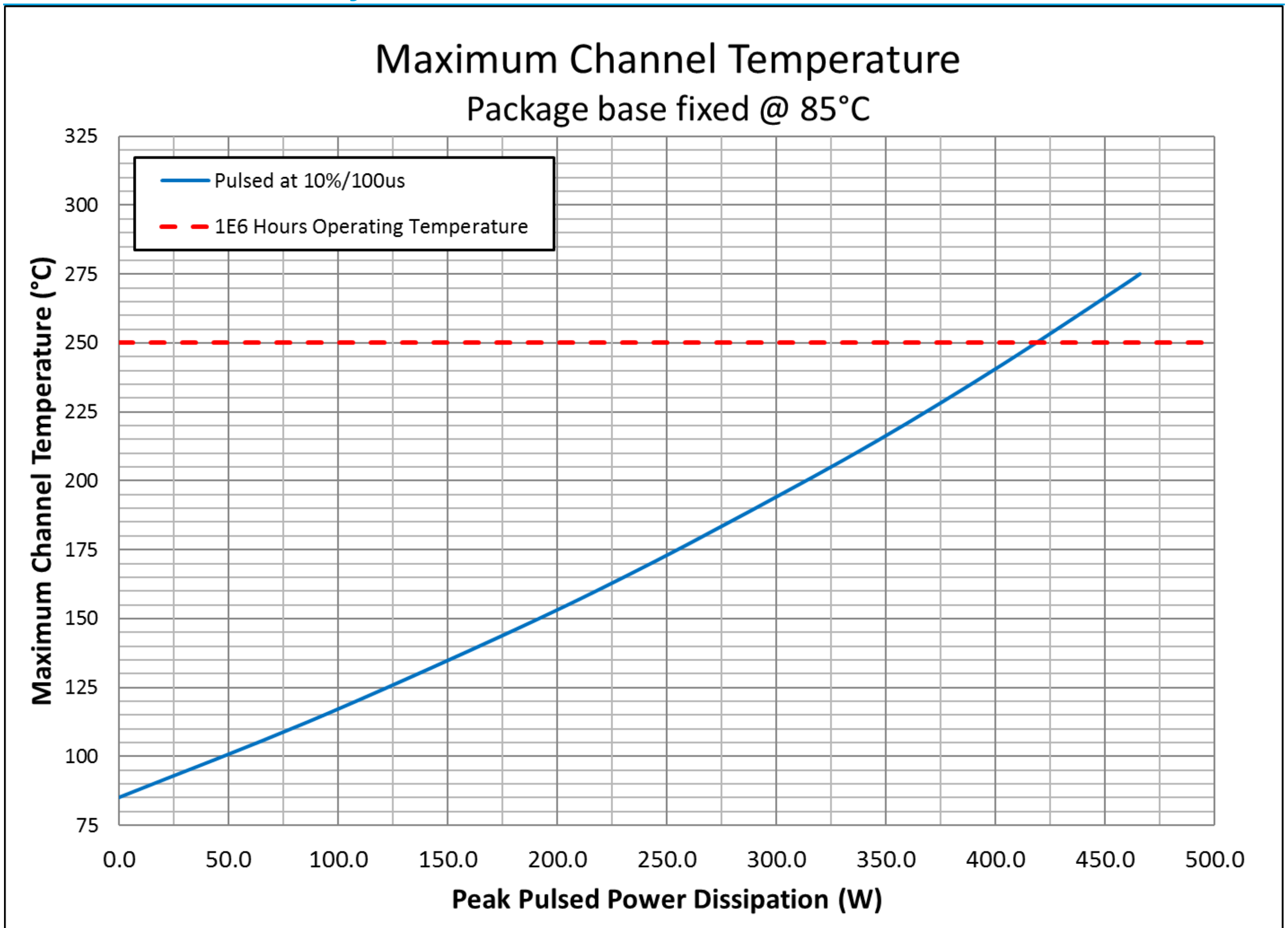
Thermal and Reliability Information – CW [1, 2, 3]



Parameter	Conditions	Values	Units
Thermal Resistance, FEA (θ_{JC}) (1) (3)	85 °C Case Pdiss = 57.6 W CW	0.61	°C/W
Peak Channel Temperature, FEA (T_{CH}) (1)		120	°C
Median Lifetime, FEA (T_M) (1)		1.6E11	Hrs
Peak Channel Temperature, IR (2)		109 (2)	°C
Thermal Resistance, FEA (θ_{JC}) (1) (3)	85 °C Case Pdiss = 115.2 W CW	0.66	°C/W
Peak Channel Temperature, FEA (T_{CH}) (1)		161	°C
Median Lifetime, FEA (T_M) (1)		1.9E9	Hrs
Peak Channel Temperature, IR (2)		137 (2)	°C
Thermal Resistance, FEA (θ_{JC}) (1) (3)	85 °C Case Pdiss = 172.8 W CW	0.72	°C/W
Peak Channel Temperature, FEA (T_{CH}) (1)		209	°C
Median Lifetime, FEA (T_M) (1)		2.0E7	Hrs
Peak Channel Temperature, IR (2)		166 (2)	°C

Notes:
1. Finite Element Analysis (FEA) thermal values shall be used to determine performance and reliability. Unless otherwise noted, all thermal references are FEA.
2. Infrared (IR) thermal values are for reference only and can not be used to determine performance or reliability.
3. Thermal resistance measured to backside of package.

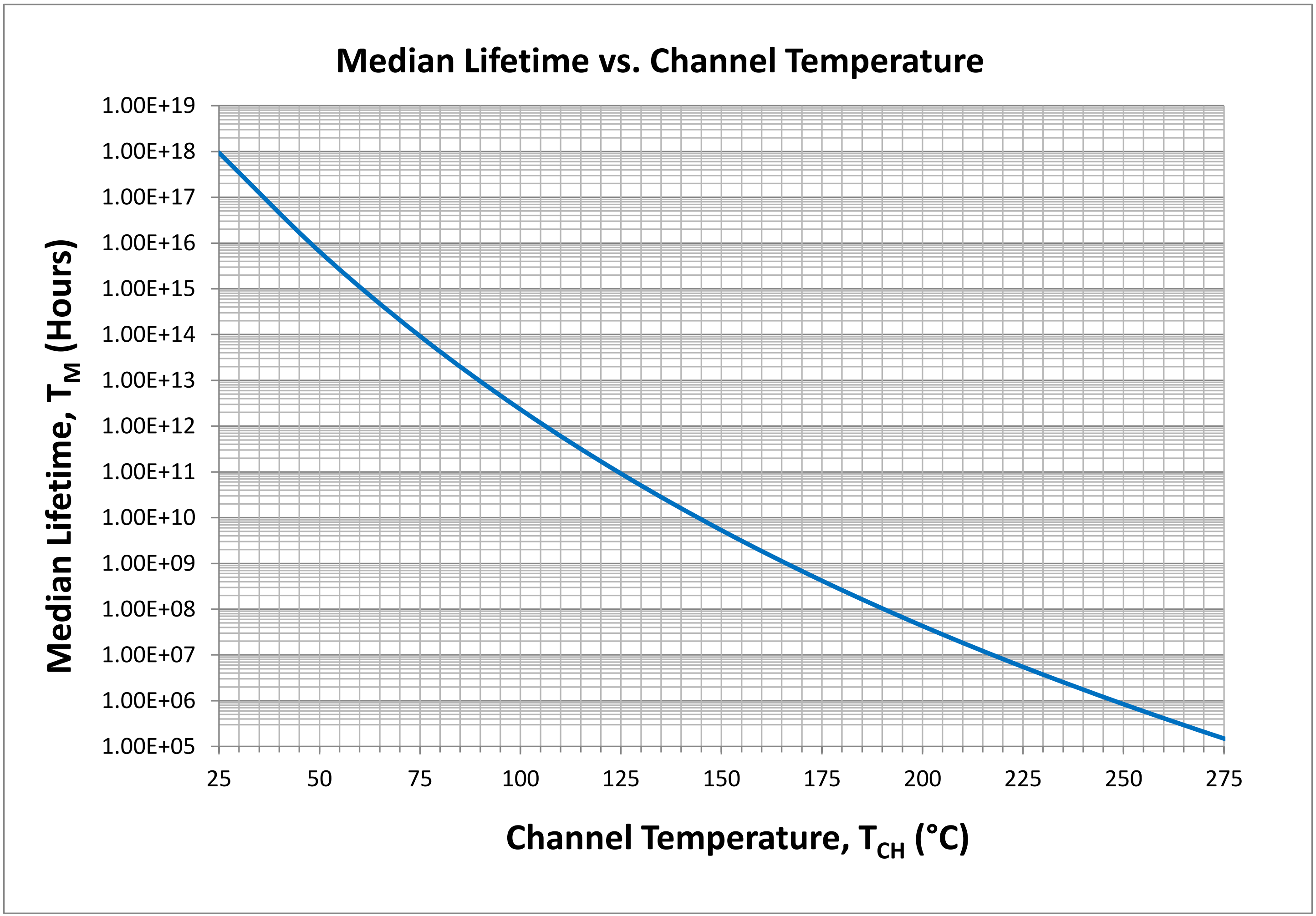
Thermal and Reliability Information – Pulsed [1, 2, 3]



Parameter	Conditions	Values	Units
Thermal Resistance, FEA (θ_{JC}) (1) (3)	85 °C Case Pdiss = 115.2 W Pulse: 100 us PW, 10% DC	0.32	°C/W
Peak Channel Temperature, FEA (T_{CH}) (1)		122	°C
Median Lifetime, FEA (T_M) (1)		1.0E12	Hrs
Peak Channel Temperature, IR (2)		110 (2)	°C
Thermal Resistance, FEA (θ_{JC}) (1) (3)	85 °C Case Pdiss = 172.8 W Pulse: 100 us PW, 10% DC	0.34	°C/W
Peak Channel Temperature, FEA (T_{CH}) (1)		143	°C
Median Lifetime, FEA (T_M) (1)		1.0E11	Hrs
Peak Channel Temperature, IR (2)		125 (2)	°C
Thermal Resistance, FEA (θ_{JC}) (1) (3)	85 °C Case Pdiss = 230.4 W Pulse: 100 us PW, 10% DC	0.35	°C/W
Peak Channel Temperature, FEA (T_{CH}) (1)		165	°C
Median Lifetime, FEA (T_M) (1)		1.0E10	Hrs
Peak Channel Temperature, IR (2)		139 (2)	°C

Notes:
1. Finite Element Analysis (FEA) thermal values shall be used to determine performance and reliability. Unless otherwise noted, all thermal references are FEA.
2. Infrared (IR) thermal values are for reference only and can not be used to determine performance or reliability.
3. Thermal resistance measured to backside of package.

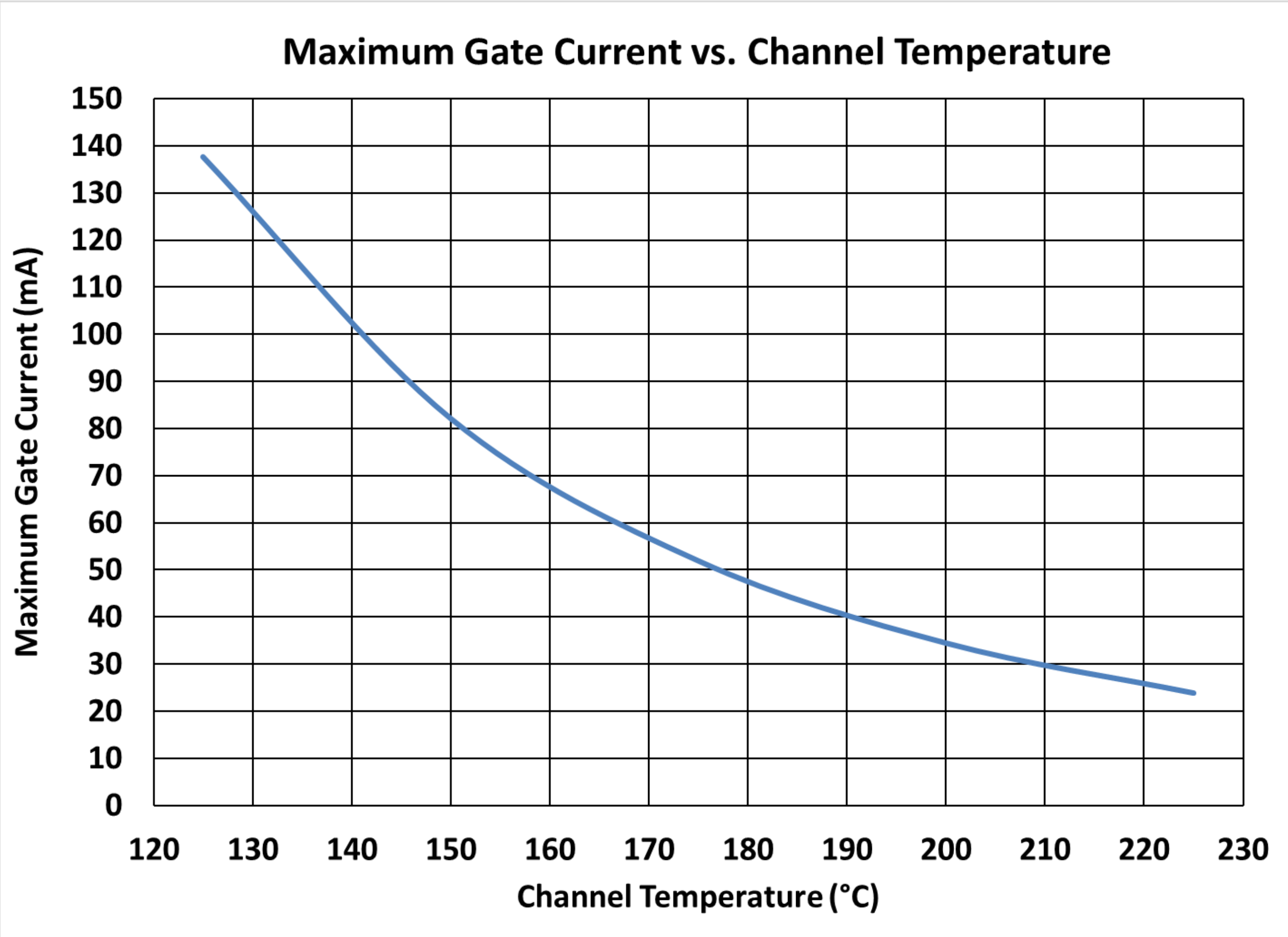
Median Lifetime [1, 2]



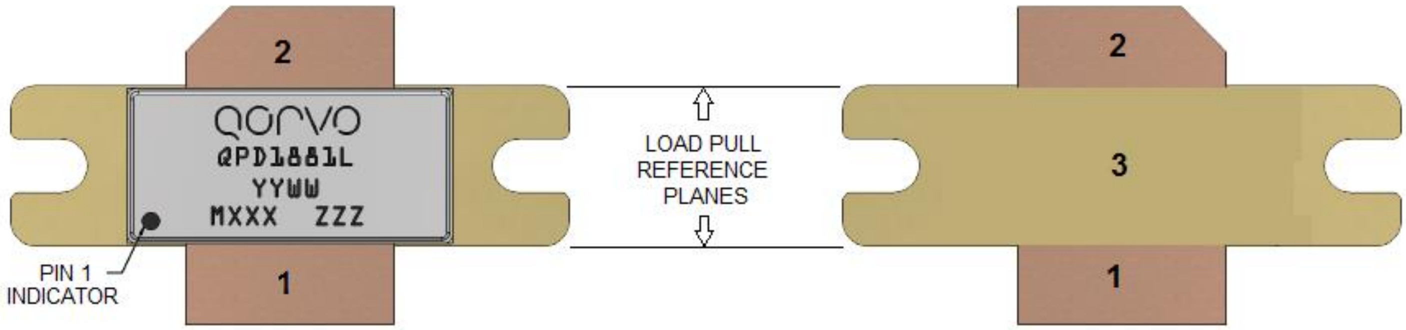
Notes:

1. Test Conditions: V_D = +50 V; Failure Criteria = 10 % reduction in I_{D_MAX} during DC Life Testing.
2. For pulsed signals, average lifetime is average lifetime at maximum channel temperature divided by duty cycle.

Maximum Gate Current



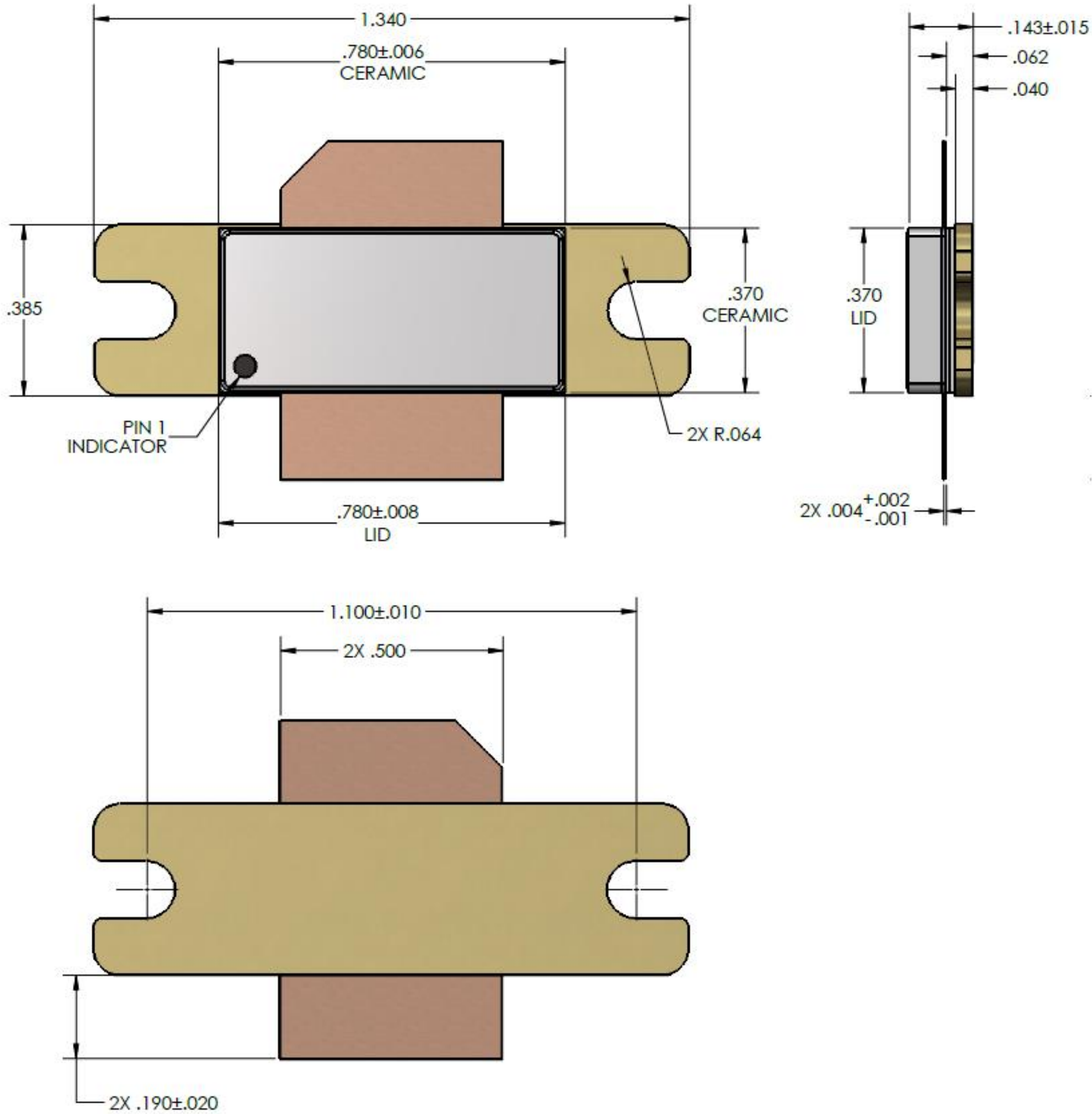
Pin Configuration and Description [1]



Note:
1- The QPD1881L will be marked with the "QPD1881L" designator and a lot code marked below the part designator. The "YY" represents the last two digits of the calendar year the part was manufactured, the "WW" is the work week of the assembly lot start, the "MXXX" is the production lot number, and the "ZZZ" is an auto-generated serial number.

Pin	Symbol	Description
1	RF IN / V_G	Gate
2	RF OUT / V_D	Drain
3	Source	Source / Ground / Backside of part

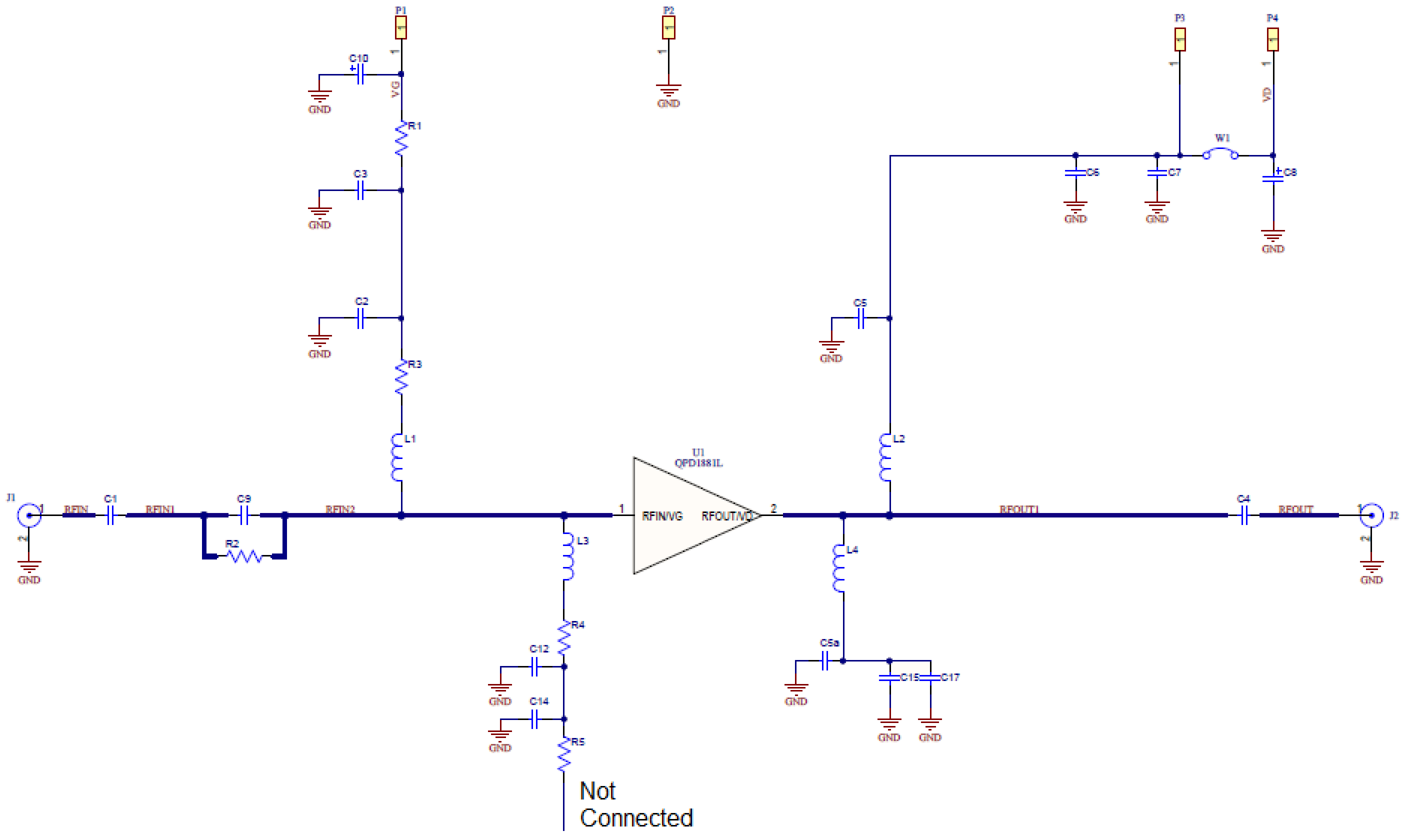
Mechanical Drawing



Notes:

1- ALL DIMENSIONS ARE IN INCHES. DIMENSION TOLERANCE IS ± 0.005 in, UNLESS NOTED OTHERWISE.
2- MATERIAL:
   PACKAGE BASE : METAL/CERAMIC
   PACKAGE LID : CERAMIC
   LEAD : ALLOY 42
3- PACKAGE EXPOSED METAL BASE AND LEADS ARE GOLD PLATED.
4- PART IS EPOXY SEALED.
5- PARTS MEET INDUSTRY NI780 FOOTPRINT.
6- BODY DIMENSIONS DO NOT INCLUDE LID SHIFT OR EPOXY RUN OUT WHICH CAN BE UP TO .020 PER SIDE.

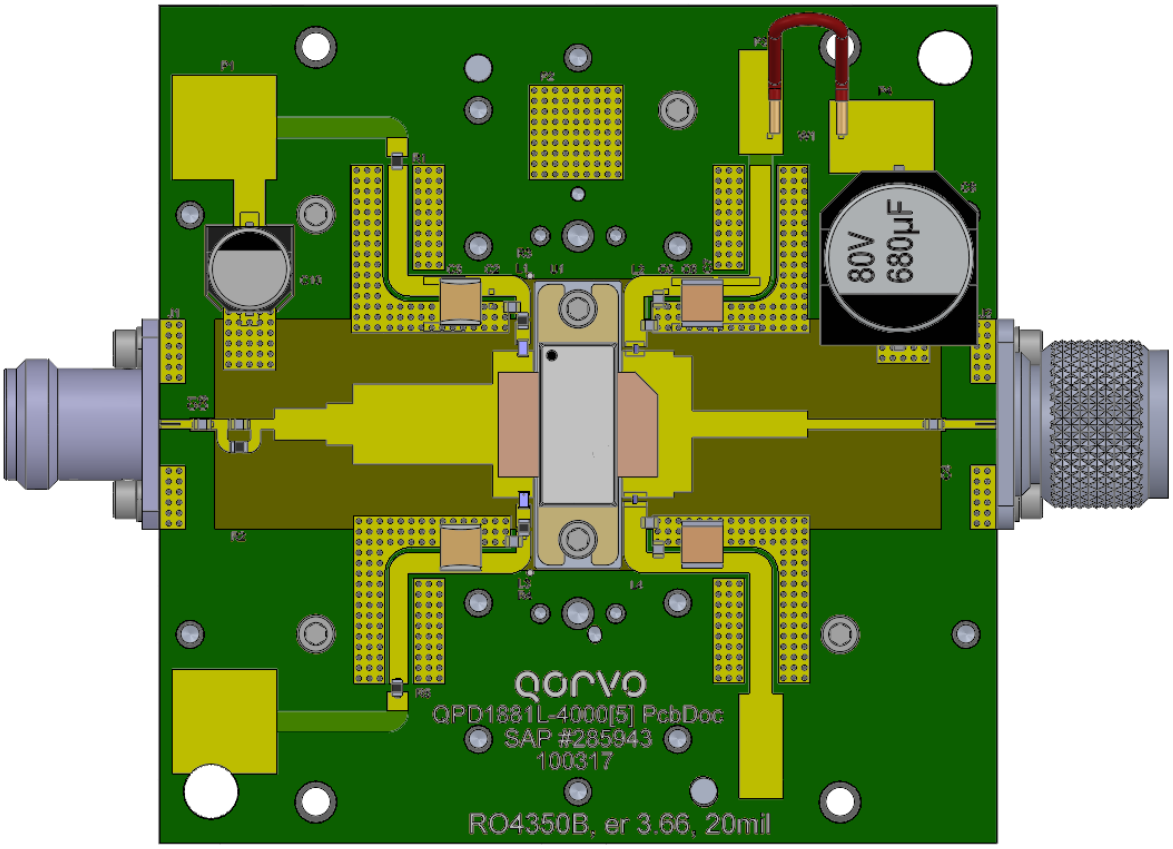
2.7 – 2.9 GHz Application Circuit - Schematic



Bias-up Procedure	Bias-down Procedure
1. Set V_G to -5 V.	1. Turn off RF signal.
2. Set I_D current limit to 2 A.	2. Turn off V_D
3. Apply 50 V V_D.	3. Wait 2 seconds to allow drain capacitor to discharge.
4. Slowly adjust V_G until I_D is set to 0.7 A.	4. Turn off V_G
5. Apply RF.	

2.7 – 2.9 GHz Application Circuit – Layout [1]

Notes:
1. PCB material is RO4350B 0.020” thick, 1 oz. copper each side.



2.7 – 2.9 GHz Application Circuit – Bill of Material

Reference Design	Value	Qty	Manufacturer	Part Number
R1,R5	0 Ohm	2	Kamaya Inc.	RMC1/10JPTP
R2	330 Ohm	1	Panasonic	ERJ-6GEYJ331
R3,R4	10 Ohm	2	Panasonic	ERJ-6ENF10R0V
C1,C4	18 pF	2	American Technical Ceramics	600F180FT250XT
C9,C2,C12,C5,C5A	10 pF	4	American Technical Ceramics	600F100FT250XT
C6,C15	100 pF	2	American Technical Ceramics	600F101JT250XT
C7,C17	10 uF	4	TDK	C5750X7S2A106M230KB
C3,C14	10 uF	4	TDK	C5750X7R1H106K230KB
C10	220 uF	1	United Chemi-Con	EMVY500ADA221MJA0G
C8	680 uF	1	Vishay	MAL215099708E3
L1,L3	8.2 nH	2	Coilcraft Inc.	0805HT-8N2TJRC
L2,L4	8.1 nH	2	Coilcraft Inc.	0908SQ-8N1JLB
Connectors	N-Type	2	Huber+Suhner, Inc.	23_N-50-0-33

Recommended Solder Temperature Profile