QPF4005

37 – 40.5 GHz GaN Dual Channel Front End Module

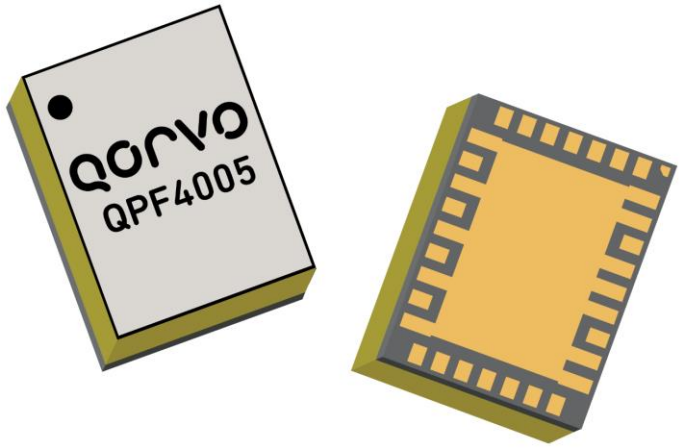
Product Description

The QPF4005 is a dual-channel multi-function Gallium Nitride MMIC front-end module targeted for 39GHz phased array 5G base stations and terminals. For each channel a multi-function MMIC die combines a low noise amplifier, a low insertion-loss high-isolation TR switch, and a high-gain high-efficiency multi-stage PA.

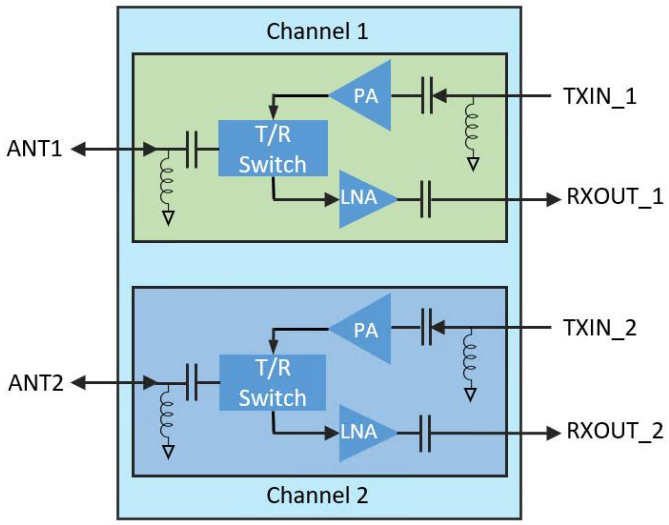
The QPF4005 operates from 37 GHz to 40.5 GHz range. The receive path (LNA + T/R SW) is designed to provide 15dB of gain and a noise figure less than 4.5dB. The transmit path (PA + T/R SW) provides 18 dB of small signal gain and a saturated output power of 2W each channel.

The compact 4.5 mm x 6.0 mm surface mount package configuration is designed to meet the tight lattice spacing requirements and support multi-channel/dual-polarization phased array applications.

The QPF4005 is fabricated on Qorvo's 0.15um GaN on SiC process. It is housed in an air-cavity laminate package with an embedded copper heat slug. The copper slug, coupled with a low thermal resistance die-attach process, allows the QPF4005 to operate at the extreme case temperatures needed in phased array applications.



Functional Block Diagram



Product Features

- Frequency Range: 37 – 40.5 GHz [1]
- RX Noise Figure: 4.2 dB
- RX Small Signal Gain: 18 dB
- RX Saturated Power: 17 dBm
- RX TOI : 20 dBm @ - 5 dBm Pin / tone
- TX Small Signal Gain: 23 dB
- TX Saturated Power: 33 dBm
- TX TOI: 42 dBm @ 24 dBm Pout / tone
- TX ACPR: 32dBc @ 24dBm average Pout [2]
- TX Linearity: 4% EVM @ 24 dBm average Pout [2]
- TX PAE: 7% @ 24 dBm average Pout.
- Package Dimensions: 4.5 x 6.0 x 1.8 mm

1. *Performance is typical at room temperature.*
2. *OFDM, 400 MHz modulation bandwidth, 64QAM.*

Applications

- 5G Wireless Base stations and terminals
- Point to Point Communications

Part No.	Description
QPF4005SR	Tape and Reel, Qty 100
QPF4005EVB03	QPF4005 Evaluation Board, Qty 1

Normal Operating Conditions

Parameter	Value
Drain Voltage (TXVD, RXVD) [1, 2, 5]	20 V
Drain Current (TXIDQ12 / TXIDQ3)	135 mA / 24 mA [4]
Drain Current (RXIDQ)	15 mA
Gate Voltage (TXVG12 / TXVG3) [3]	−2 V / -2.4 V
Gate Voltage (RXVG) [3]	-2 V
Control Voltage (TXSW, RXSW)	TXSW = 0 V, RXSW = 20V (RX on, TX off) TXSW = 20 V, RXSW = 0V (RX off, TX on)
Operating Temperature Range	−40 to 95 °C

1 Electrical specifications are measured at specified test conditions, no guarantee over all recommended operating conditions
2 Suffixes for channel ID removed from pin labels, both channels use the same settings
3 Gate voltages shown are typical, can be adjusted to set required drain current
4 Other current settings: 45 / 60 mA = 105 mA; 90 / 120 mA = 210 mA; 135 / 180 mA = 315 mA (gate controls combined together)
5 When in TX mode, the drain of receive channel is turned off by an internal switch.

Electrical Specifications RX

Test conditions, unless otherwise noted: VD = 20 V, IDQ = 15 mA. Data de-embedded to device reference planes, 25 °C

Parameter	Min	Typical	Max	Units
Frequency	37		40.5	GHz
Small Signal Gain		18		dB
Noise Figure		4.2		dB
Saturated Output Power		17		dBm
Input Return Loss		12		dB
Output Return Loss		15		dB
Output TOI, @ -5 dBm Pin / tone, 10 MHz tone spacing		20		dBm
Gain Temperature Coefficient		−0.056		dB/°C

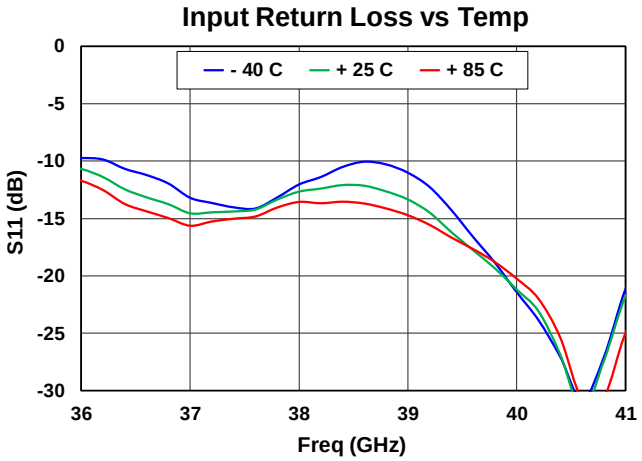
Electrical Specifications TX

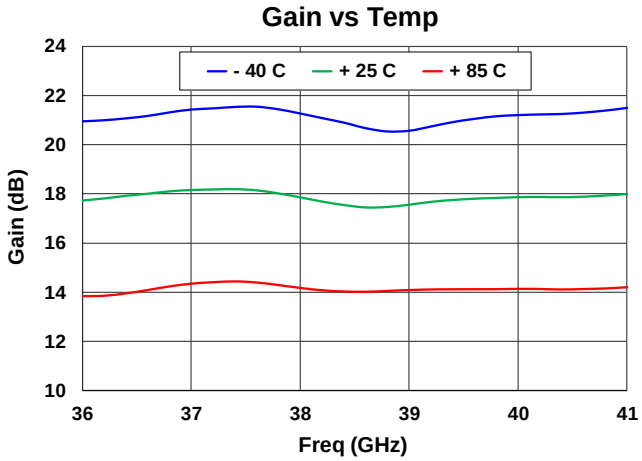
Test conditions unless otherwise noted: VD = 20 V, TXIDQ12 / TXIDQ3 = 135mA / 24 mA
Data de-embedded to device reference planes, 25 °C

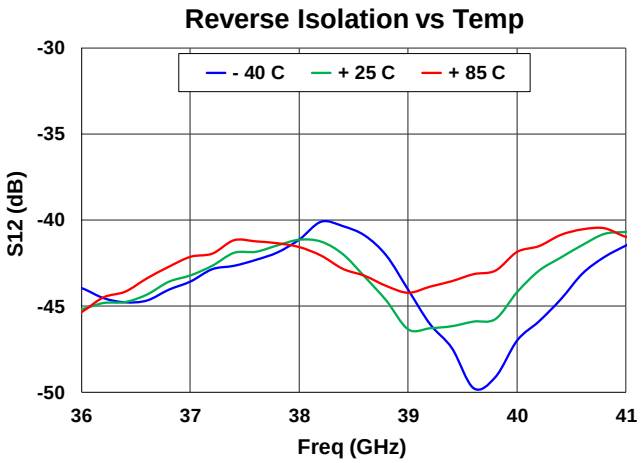
Parameter	Min	Typical	Max	Units
Frequency	37		40.5	GHz
Small Signal Gain		23		dB
Saturated Output Power		33		dBm
Input Return Loss		12		dB
Output Return Loss		13		dB
Output TOI, @ 24dBm Pout / tone, 10 MHz tone spacing		42		dBm
ACPR (24 dBm average power, OFDM, 400MHz, 64QAM)		-32		dBc
EVM (24 dBm average power, OFDM, 400MHz, 64QAM)		4		%
PAE at average output power (24dBm)		7		%
Gain Temperature Coefficient		−0.112		dB/°C

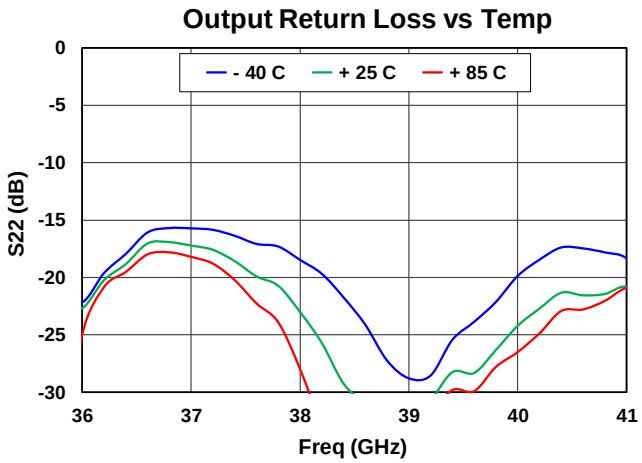
Performance Plots, Small Signal, Receive Path

Test Conditions unless otherwise stated: RXVD = 20 V, RXIDQ = 15 mA, 25C





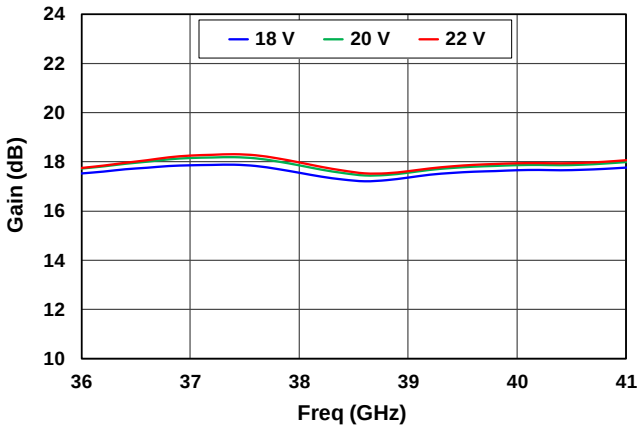




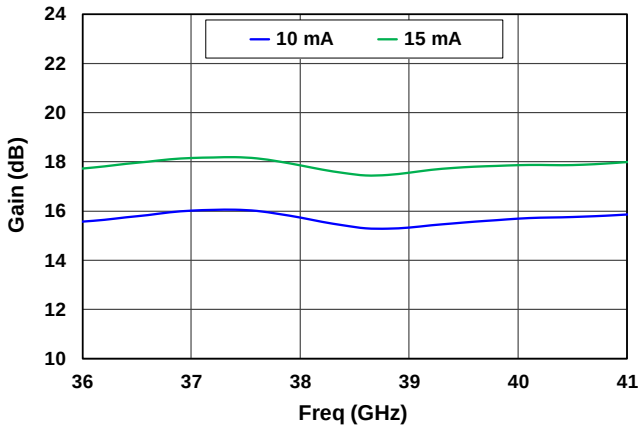
Performance Plots, Small Signal, Receive Path

Test Conditions unless otherwise stated: RXVD = 20 V, RXIDQ = 15 mA, 25 C

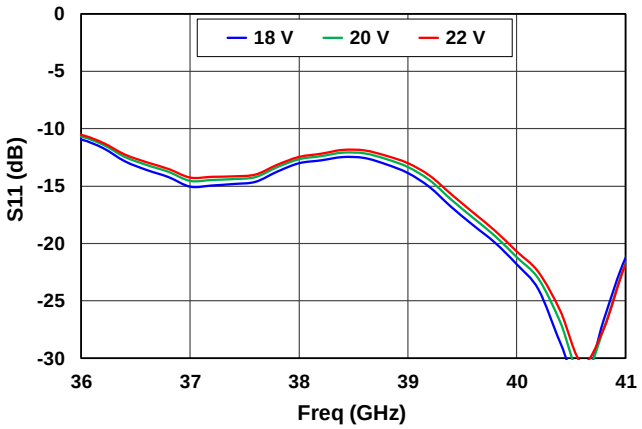
Gain vs Voltage



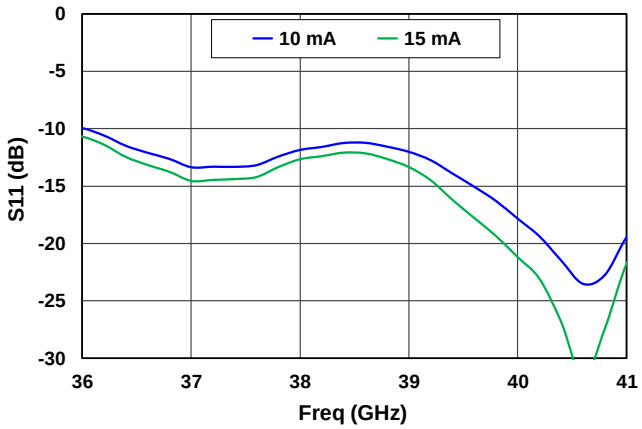
Gain vs Current



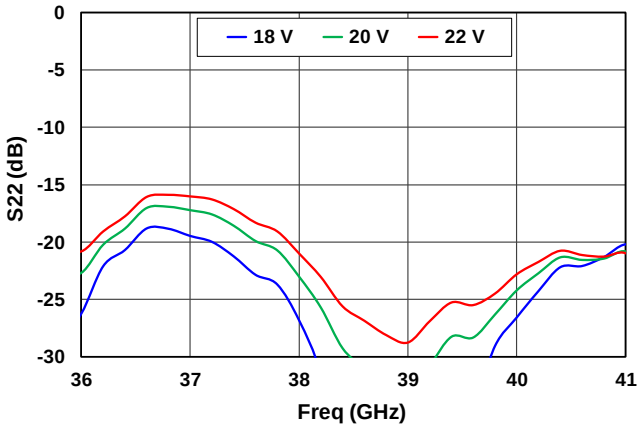
Input Return Loss vs Voltage



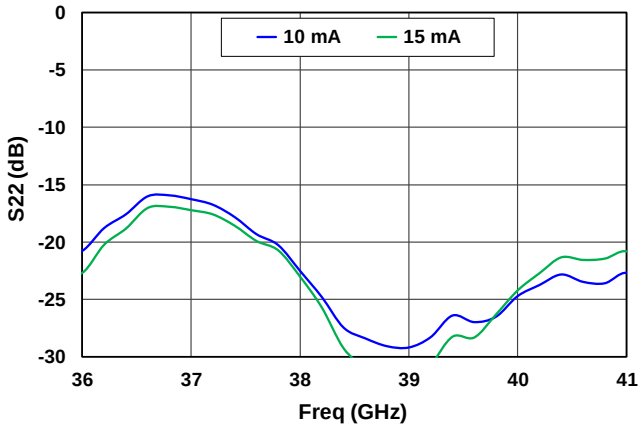
Input Return Loss vs Current



Output Return Loss vs Voltage

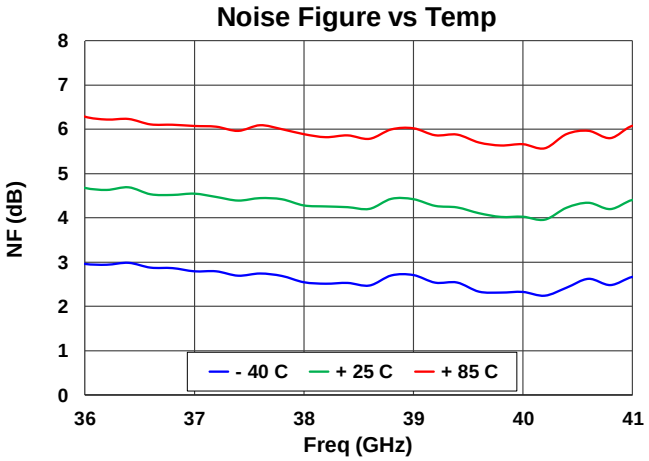


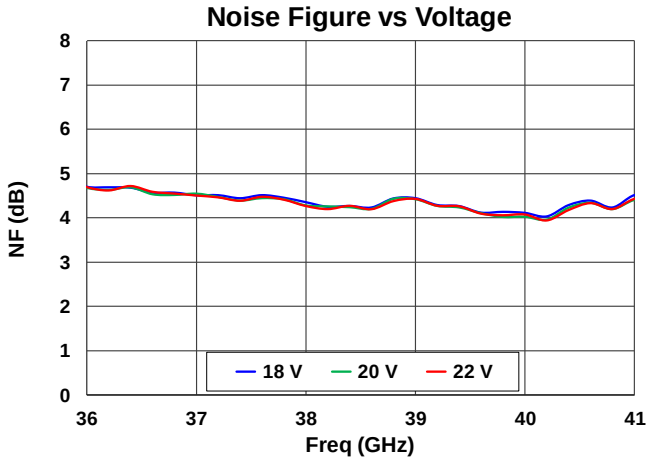
Output Return Loss vs Current

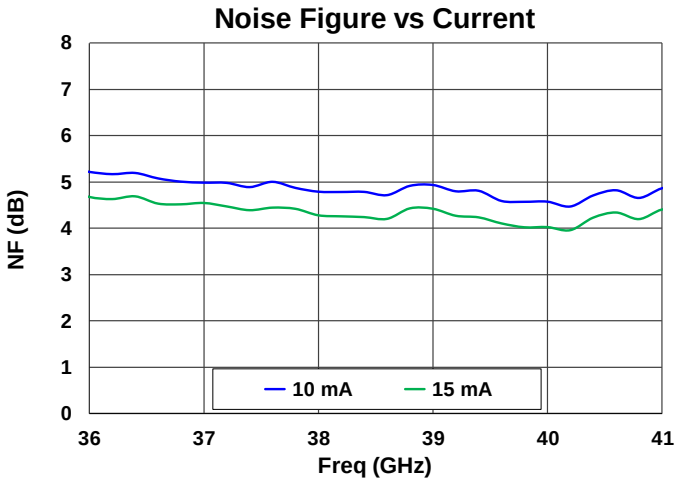


Performance Plots, Noise Figure, Receive Path

Test Conditions unless otherwise stated: RXVD = 20 V, RXIDQ = 15 mA, 25 C

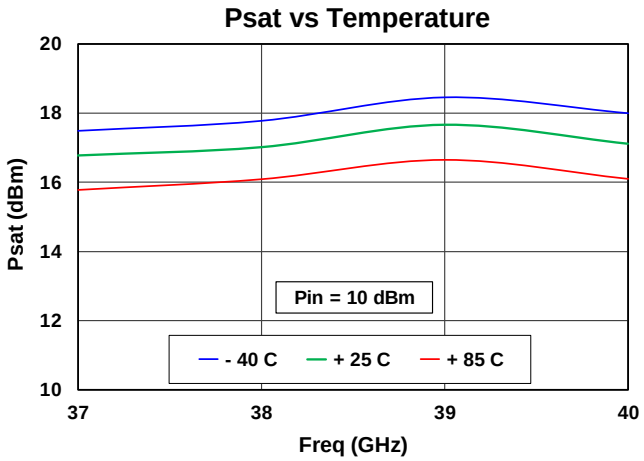


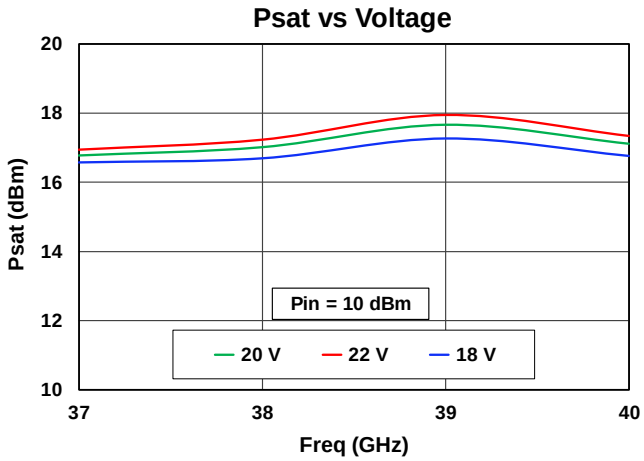


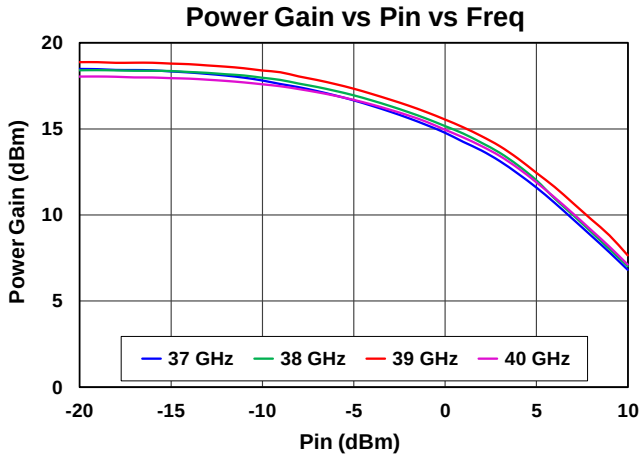


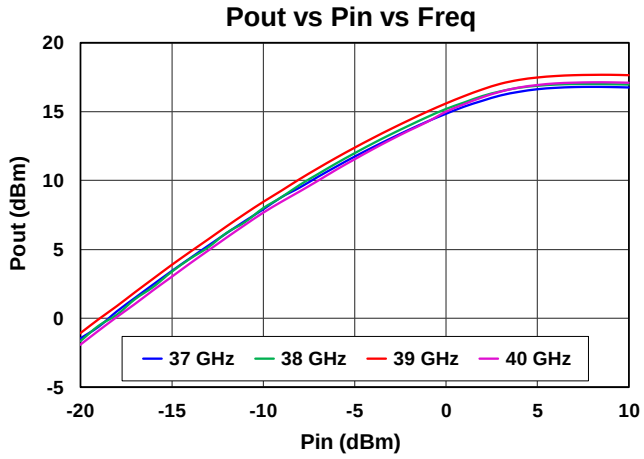
Performance Plots, Large Signal, Receive Path

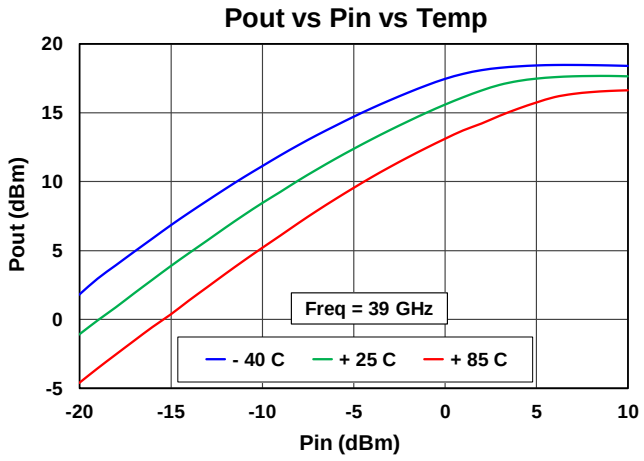
Test Conditions unless otherwise stated: RXVD = 20 V, RXIDQ = 15 mA, CW, 25 C

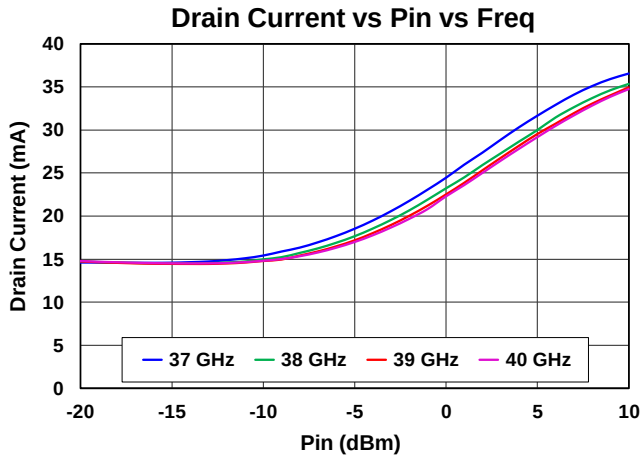






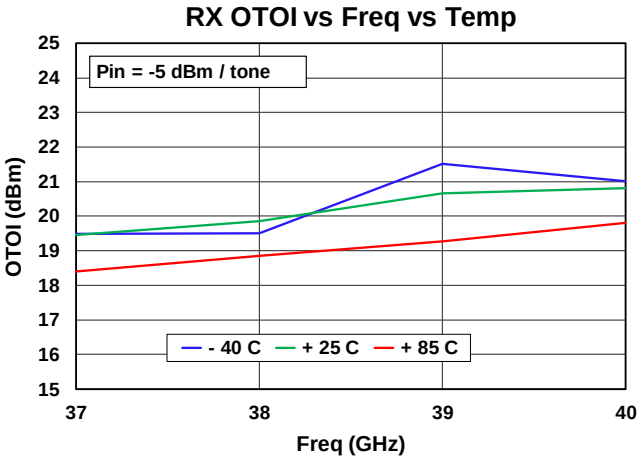


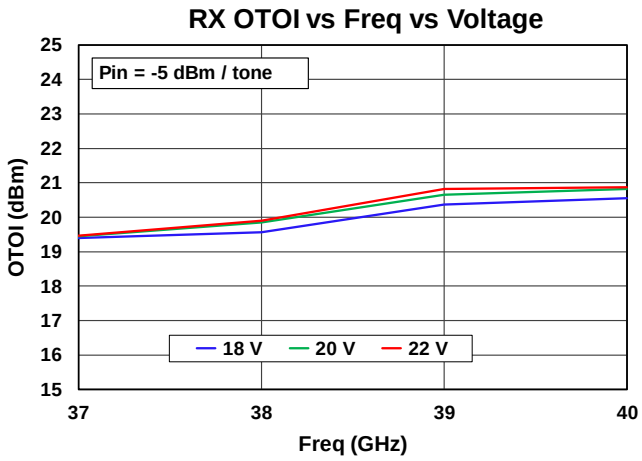


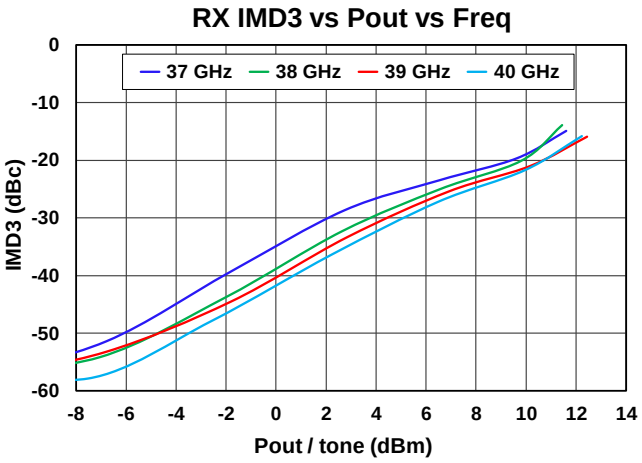


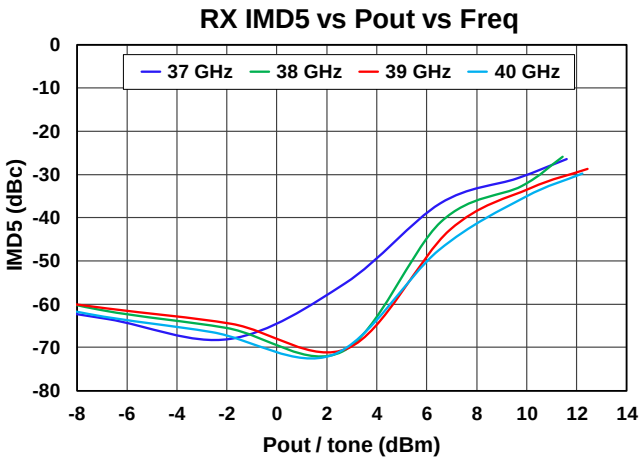
Performance Plots, Linearity, Receive Path

Test Conditions unless otherwise stated: RXVD = 20 V, RXIDQ = 15 mA, Tone spacing: 10 MHz, 25 C



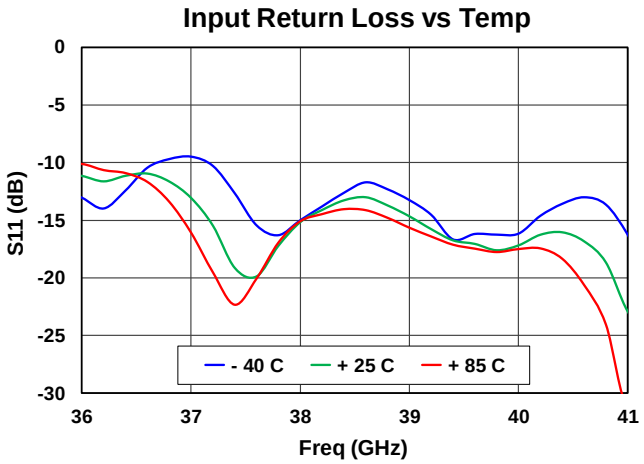


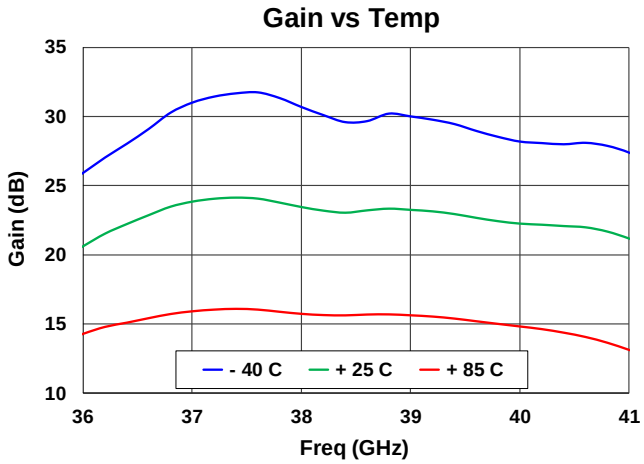


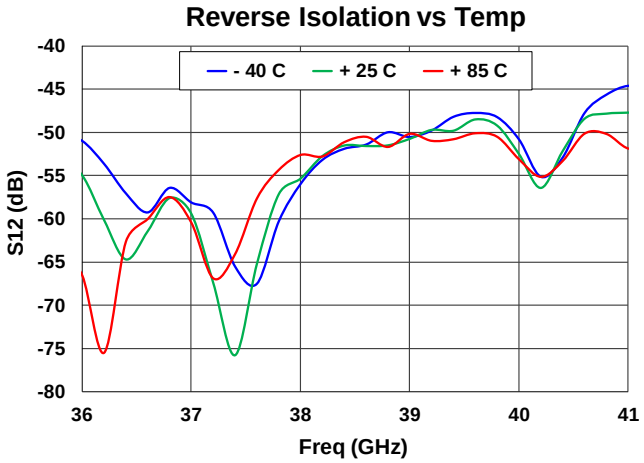


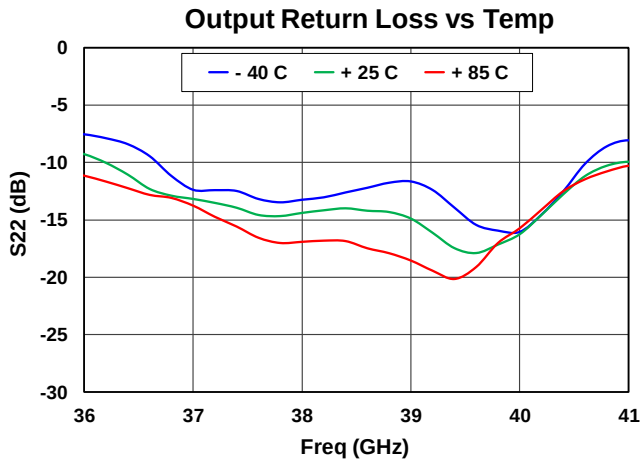
Performance Plots, Small Signal, Transmit Path

Test Conditions unless otherwise stated: TXVD = 20 V, TXIDQ12 = 135 mA, TXIDQ3 = 24 mA





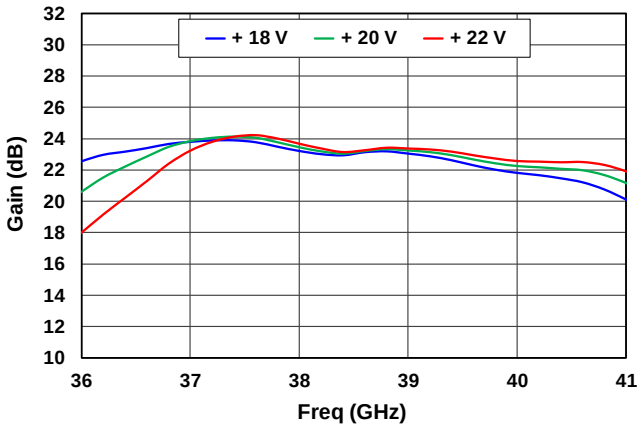




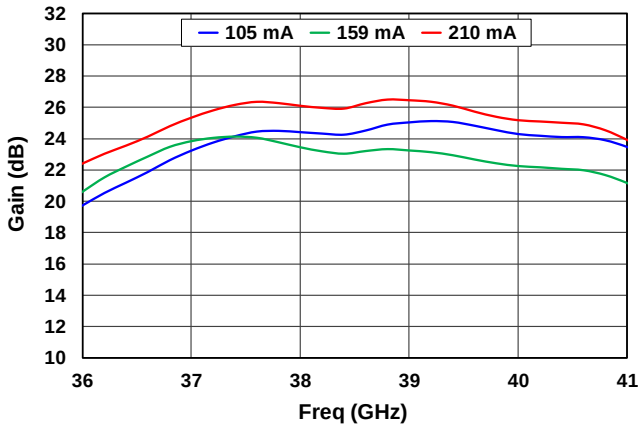
Performance Plots, Small Signal, Transmit Path

Test Conditions unless otherwise stated: TXVD = 20 V, 25 C
TXIDQ12 = 135 mA, TXIDQ3 = 24 mA (159mA), for other bias conditions refer to Nominal Operating Condition table in page 2

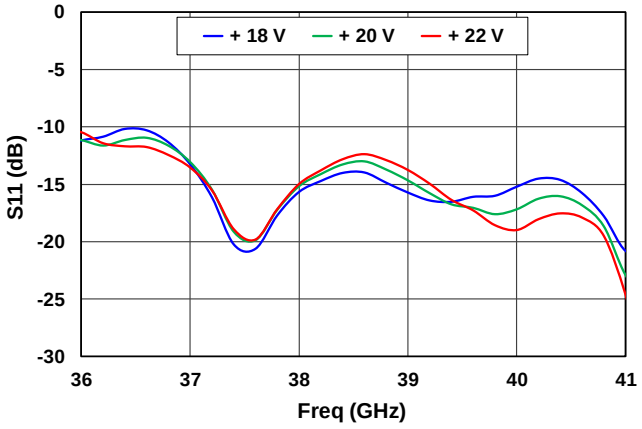
Gain vs Voltage



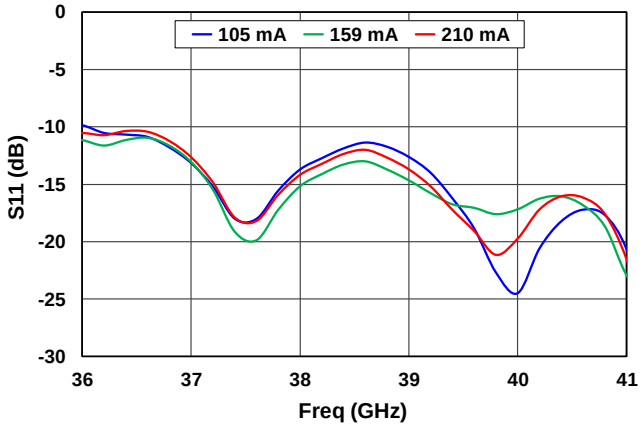
Gain vs Current



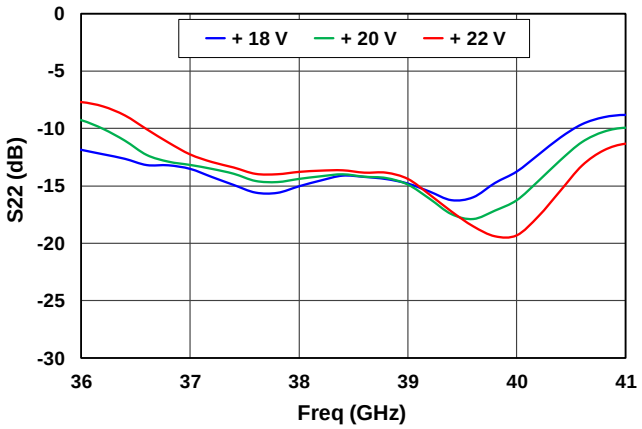
Input Return Loss vs Voltage



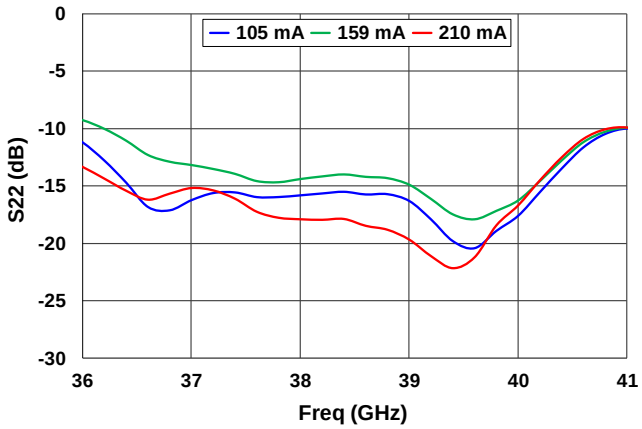
Input Return Loss vs Current



Output Return Loss vs Voltage

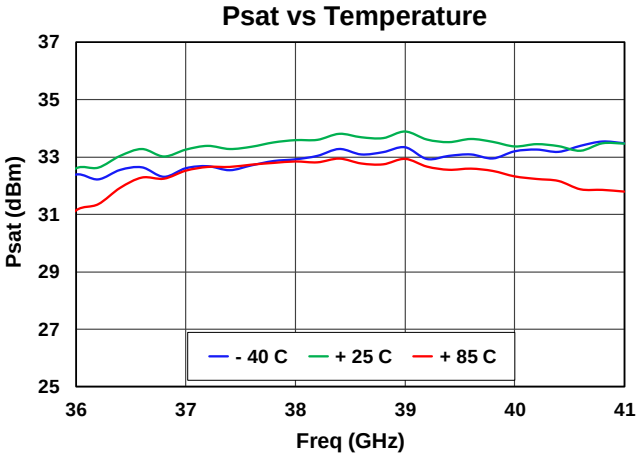


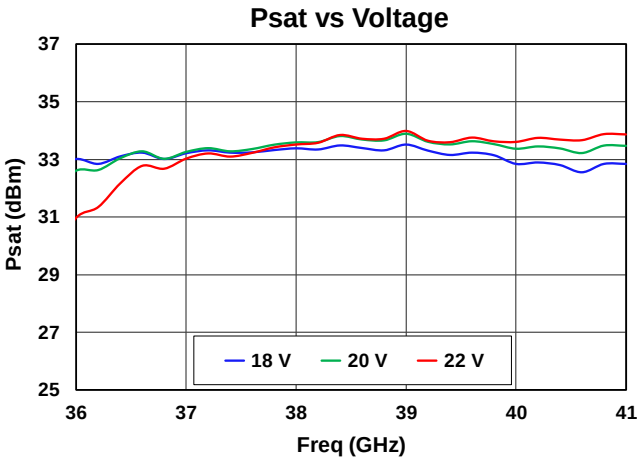
Output Return Loss vs Current

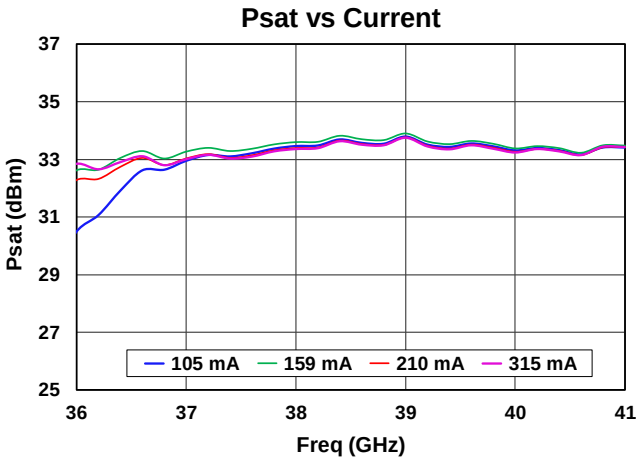


Performance Plots, Large Signal, Transmit Path

Test Conditions unless otherwise stated: TXVD = 20 V, 25 C, Pin = 20 dBm
TXIDQ12 = 135 mA, TXIDQ3 = 24 mA (159mA), for other bias conditions refer to Nominal Operating Condition table in page 2

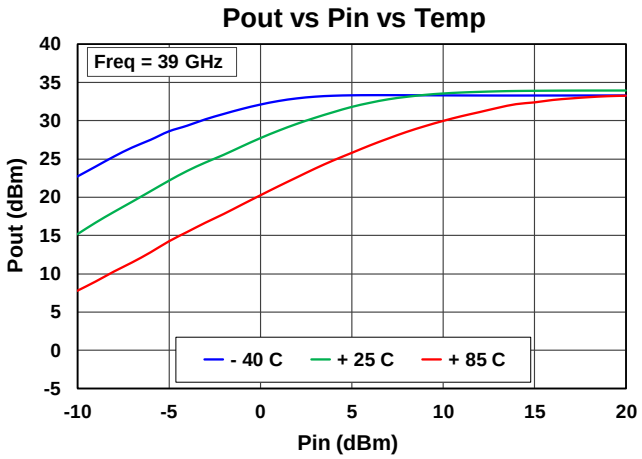


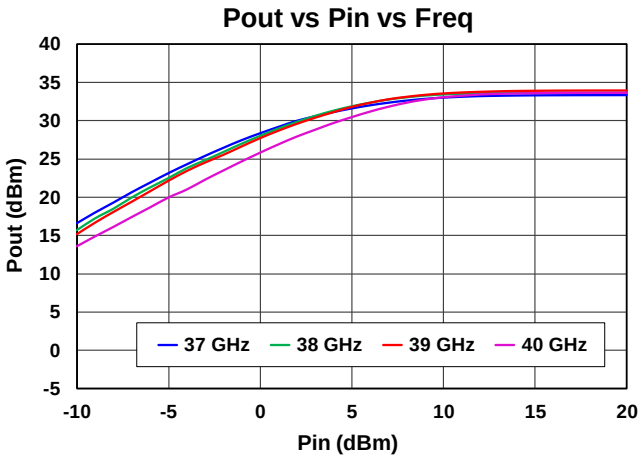


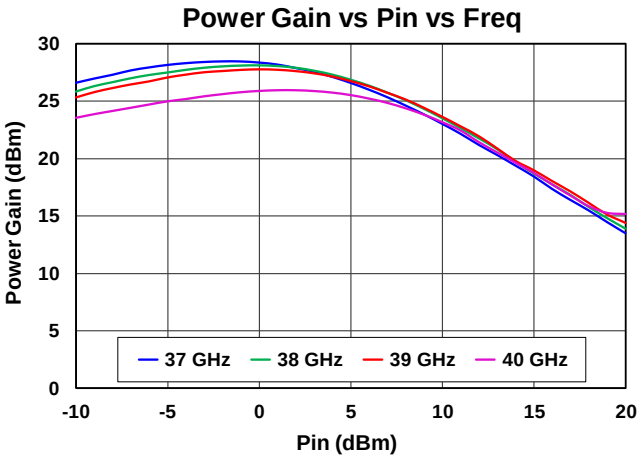


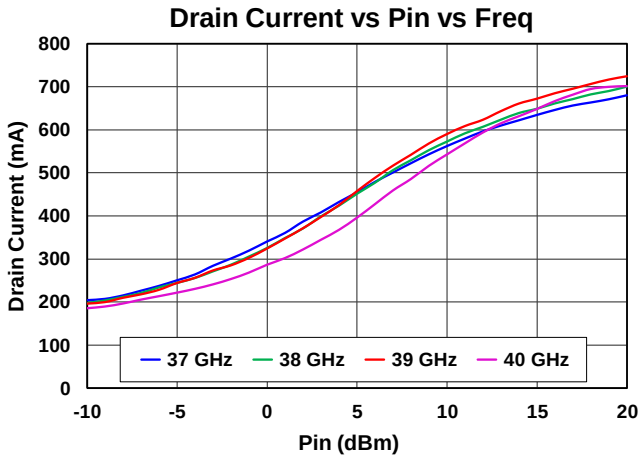
Performance Plots, Large Signal, Transmit Path

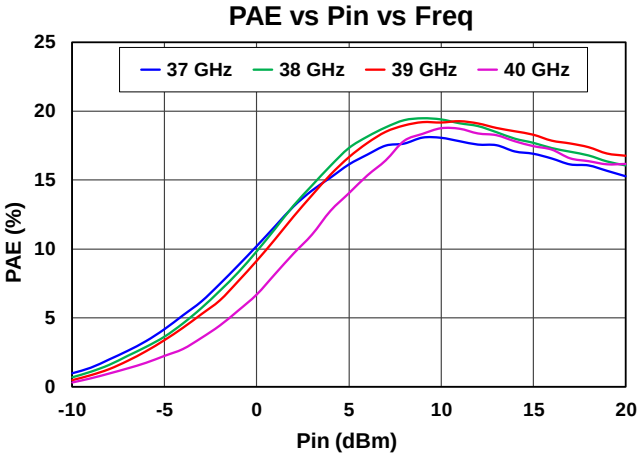
Test Conditions unless otherwise stated: TXVD = 20 V, TXIDQ12 = 135 mA, TXIDQ3 = 24 mA,
Pulse Mode: PW = 100 uS, DC = 10%, 25C

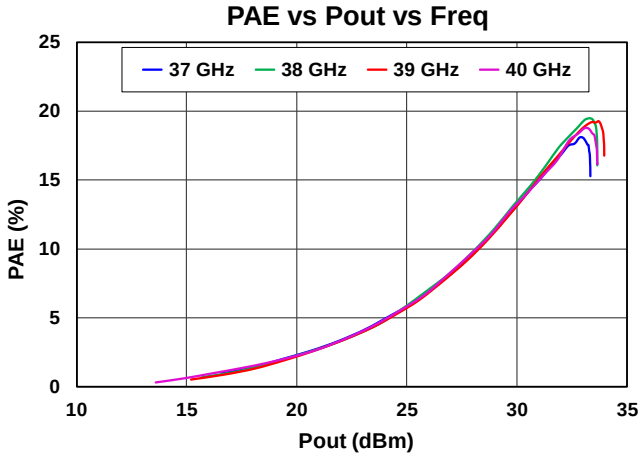






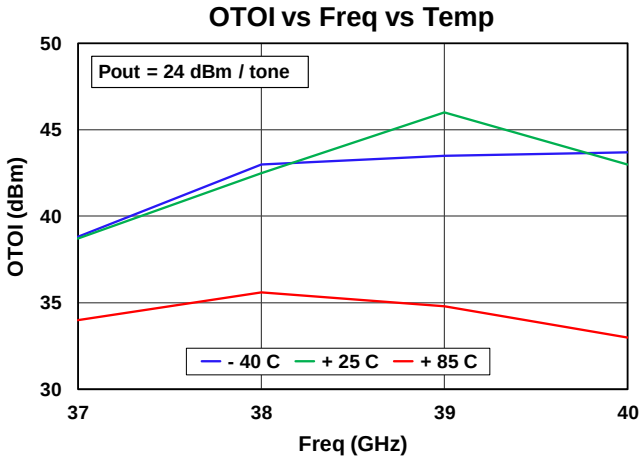


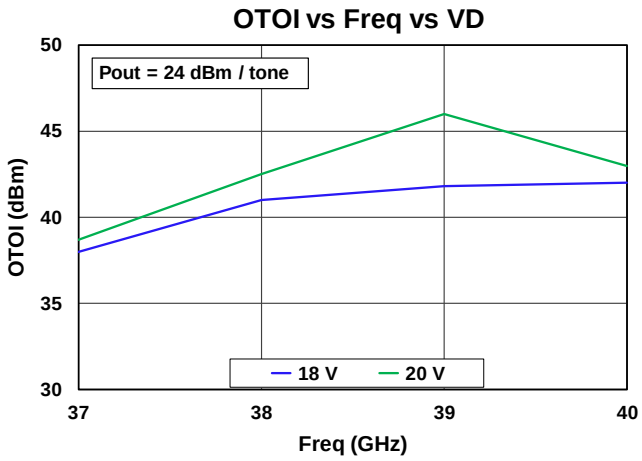


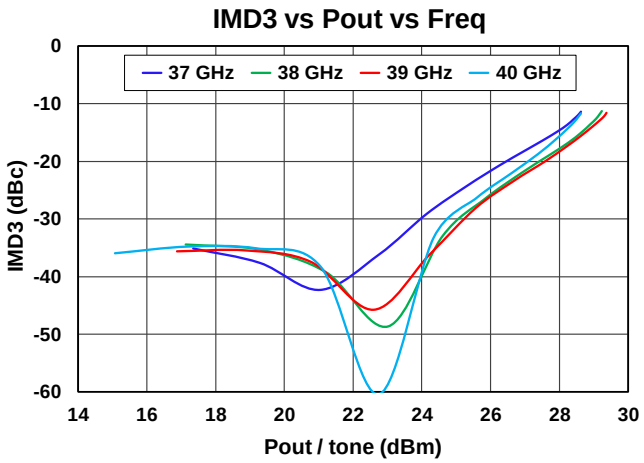


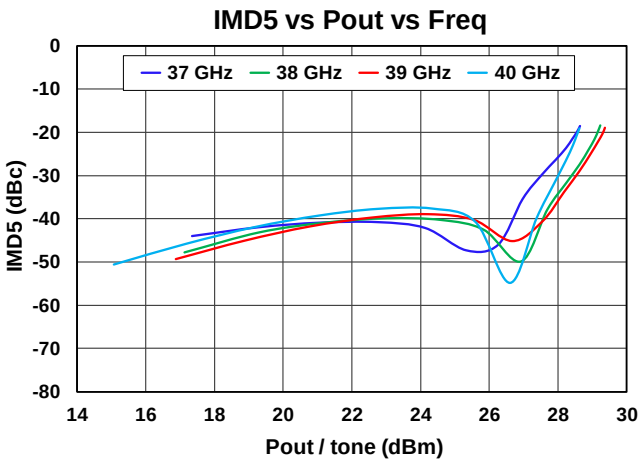
Performance Plots, Linearity, Transmit Path

Test Conditions unless otherwise stated: TXVD = 20 V, TXIDQ12 = 135 mA, TXIDQ3 = 24 mA, Tone Spacing = 10 MHz, 25 C



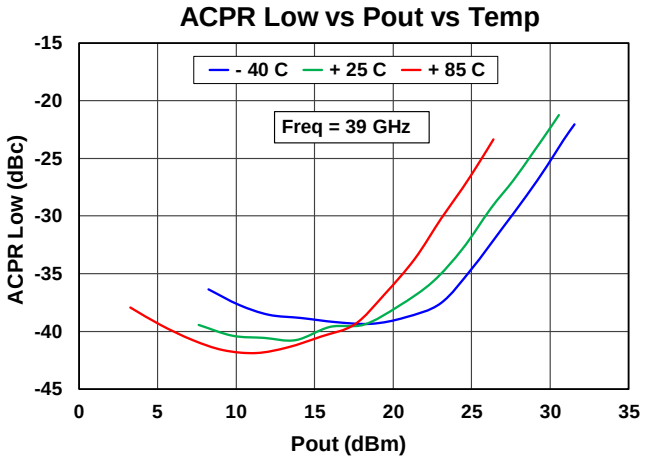


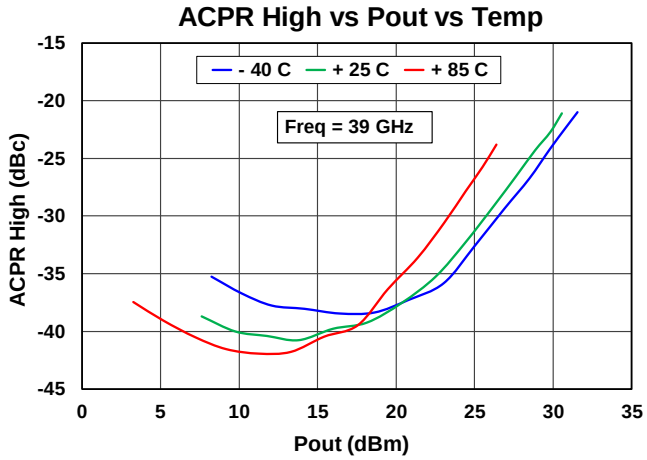


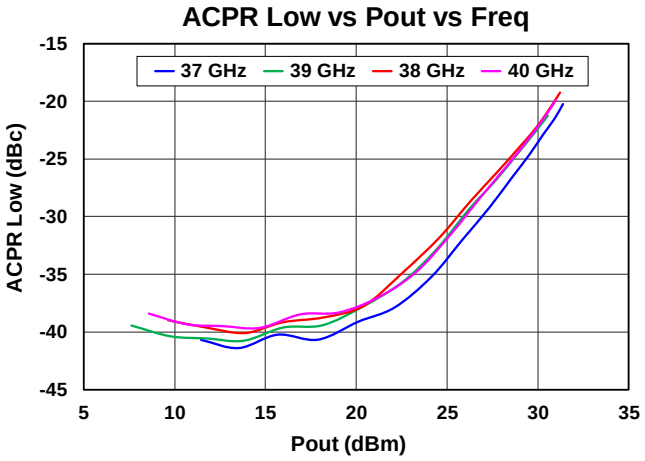


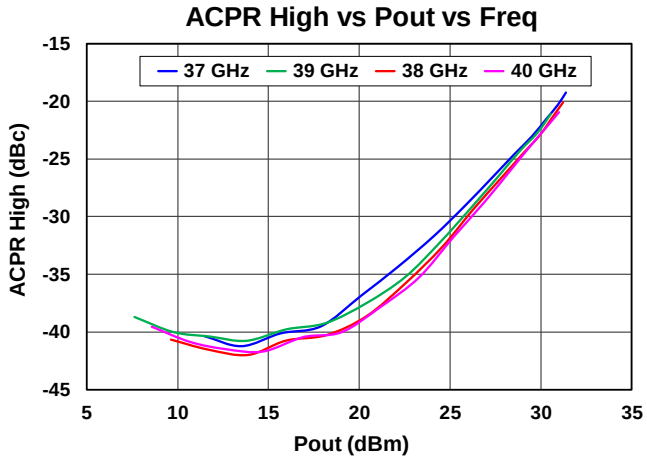
Performance Plots, Modulated Signal, Transmit Path

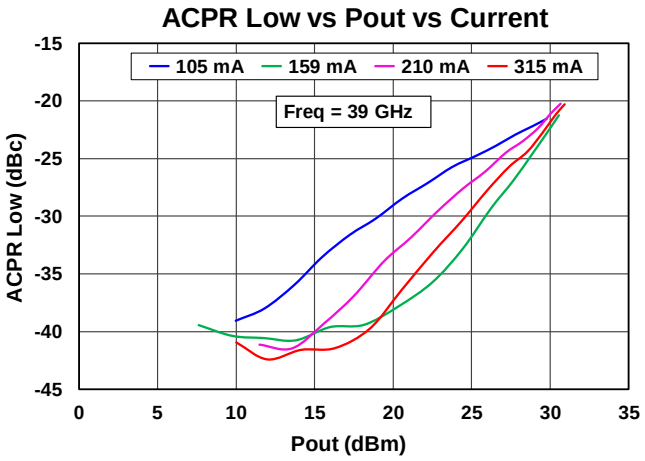
Test Conditions unless otherwise stated: TXVD = 20 V, 25 C
TXIDQ12 = 135 mA, TXIDQ3 = 24 mA (159mA), for other bias conditions refer to Nominal Operating Condition table in page 2

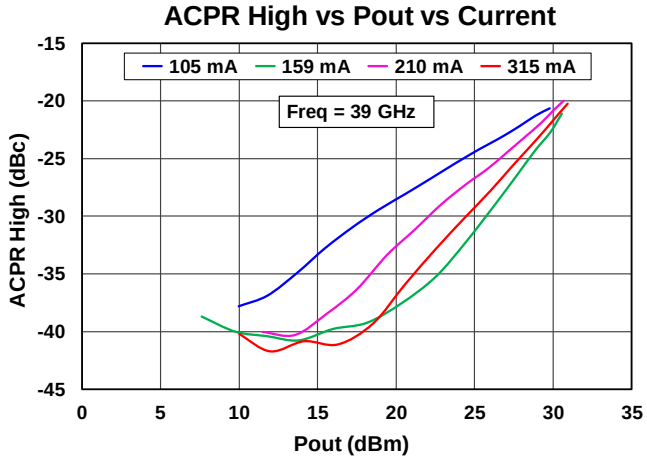






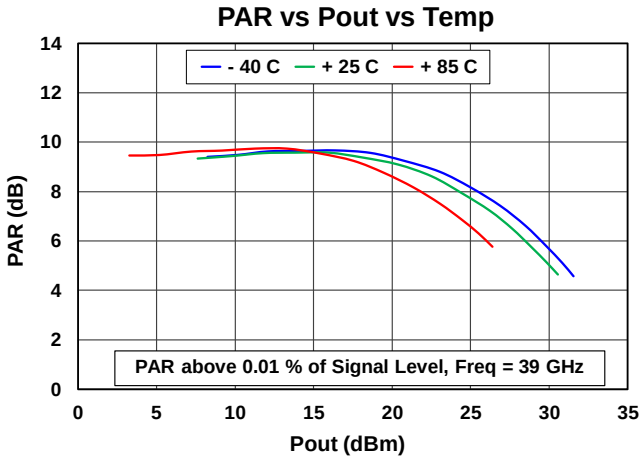


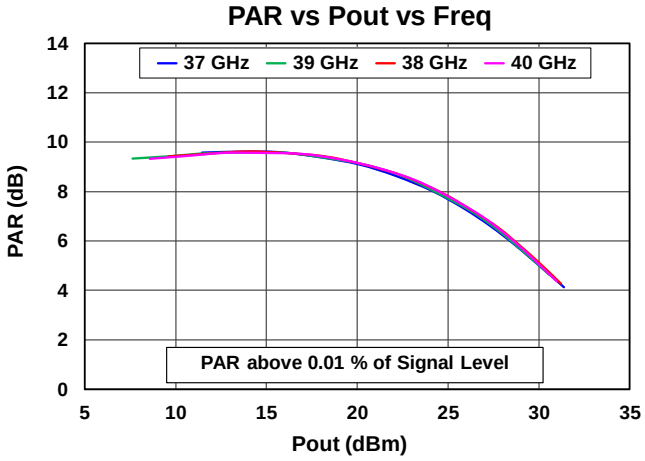


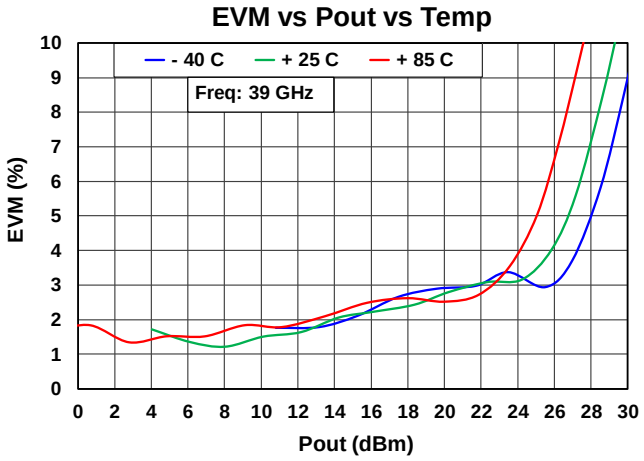


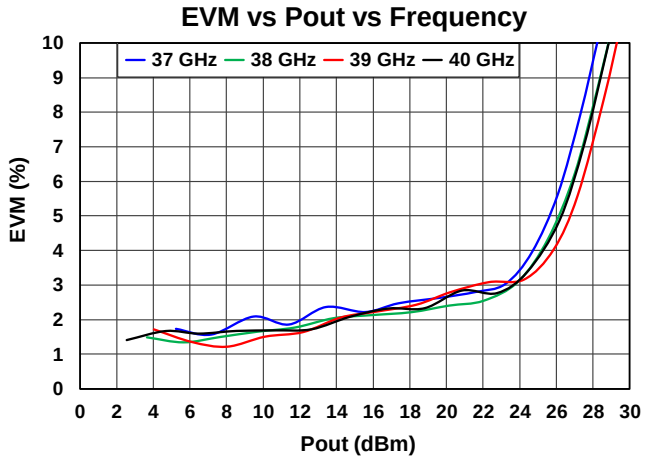
Performance Plots, Modulated Signal, Transmit Path

Test Conditions unless otherwise stated: TXVD = 20 V, TXIDQ12 = 135 mA, TXIDQ3 = 24 mA
Source: 400 MHz OFDM, 64 QAM, 25 C



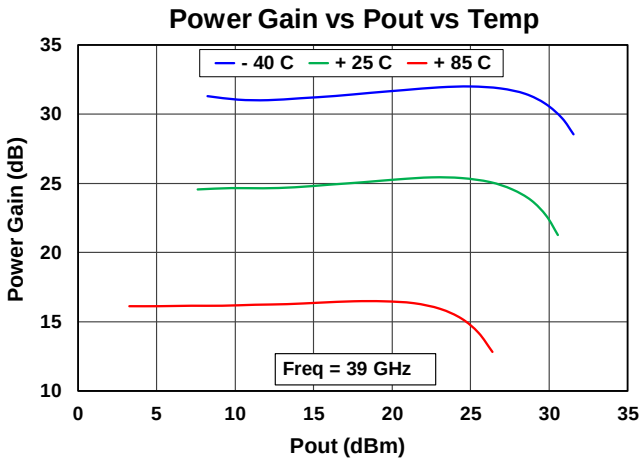


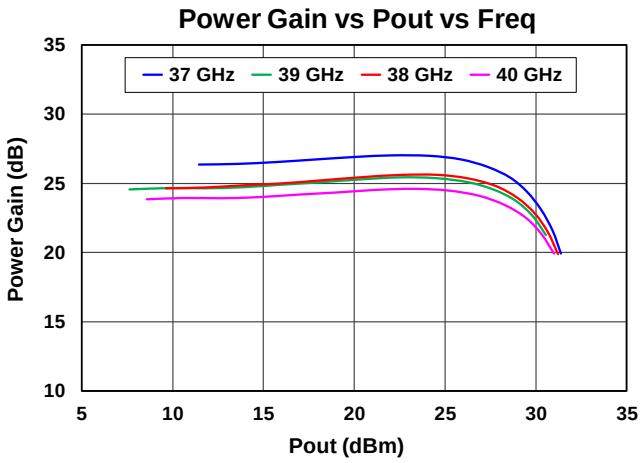


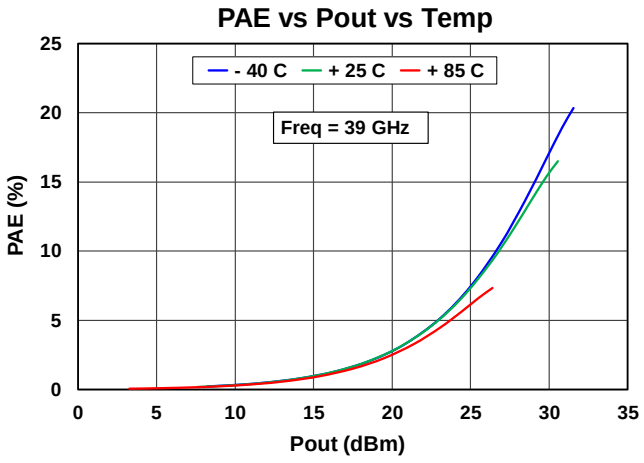


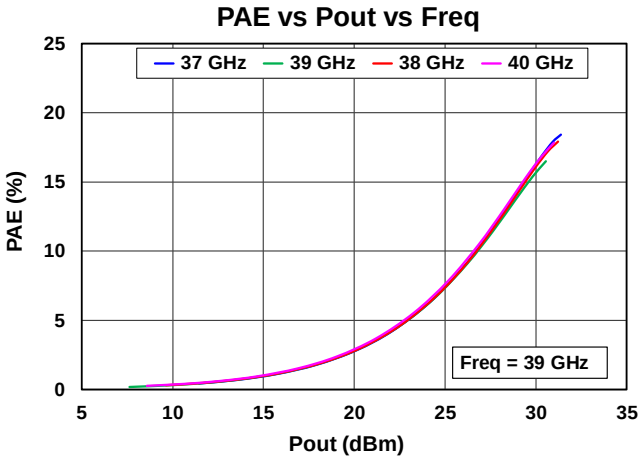
Performance Plots, Modulated Signal, Transmit Path

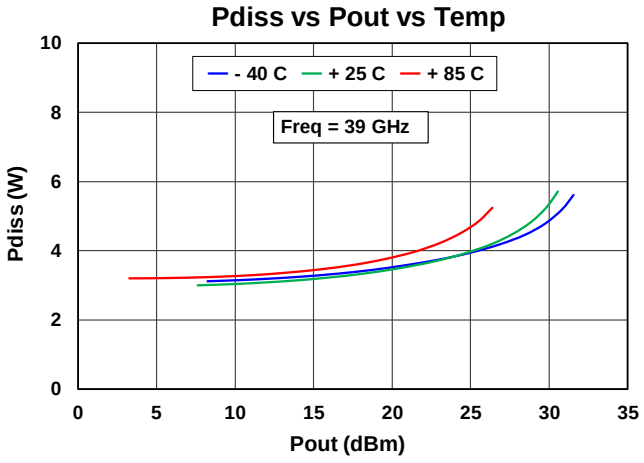
Test Conditions unless otherwise stated: TXVD = 20 V, TXIDQ12 = 135 mA, TXIDQ3 = 24 mA
Source: 400 MHz OFDM, 64 QAM, 25 C

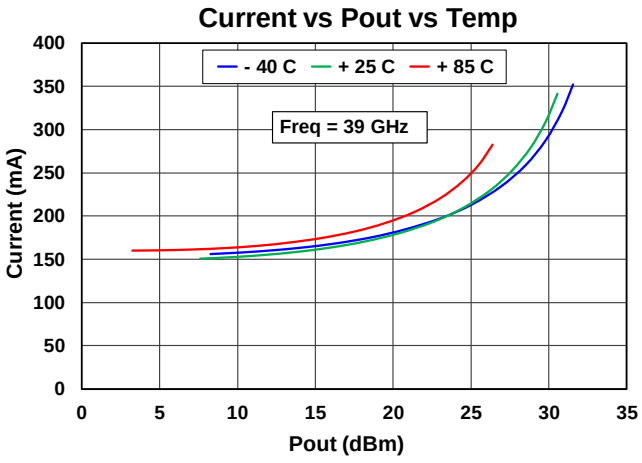








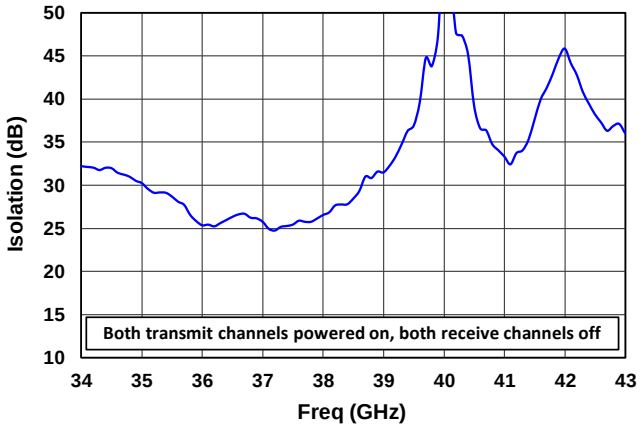




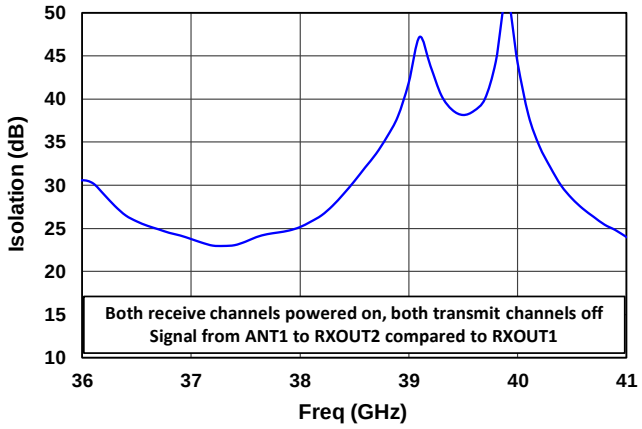
Performance Plots, Channel Isolations

Test Conditions unless otherwise stated: TXVD = 20 V, TXIDQ12 = 135 mA, TXIDQ3 = 24 mA, RXVD = 20 V, RXID = 15 mA
Cable calibration, data not de-embedded, 25 C

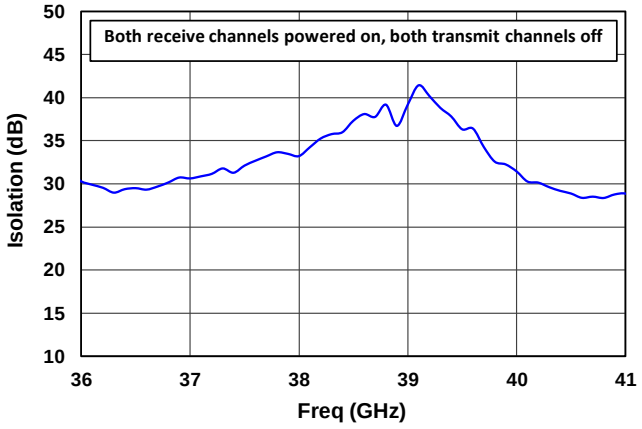
Transmit Port Isolation TX2 - TX1



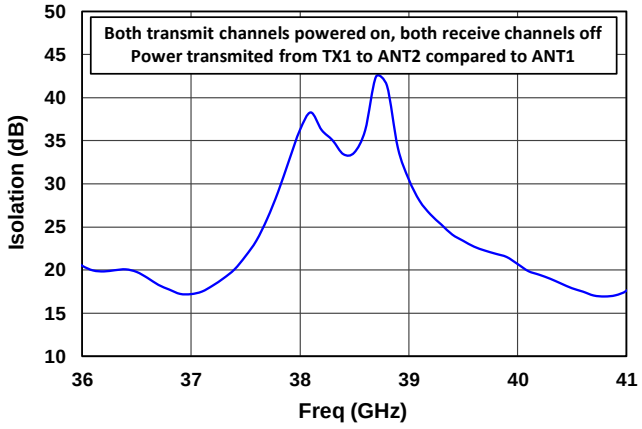
Ant1 to Port RX2 Relative to RX1



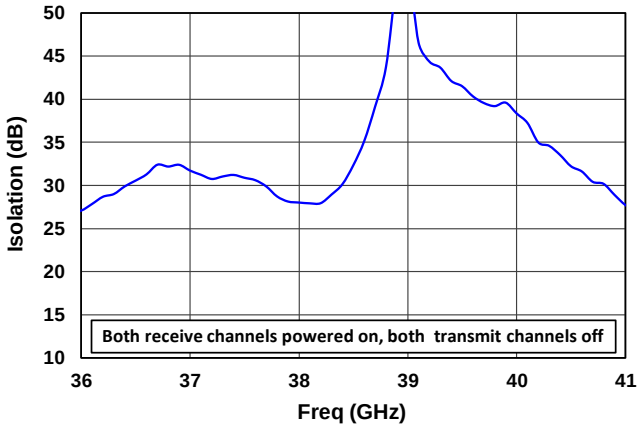
Receive Port Isolation RX2 - RX1



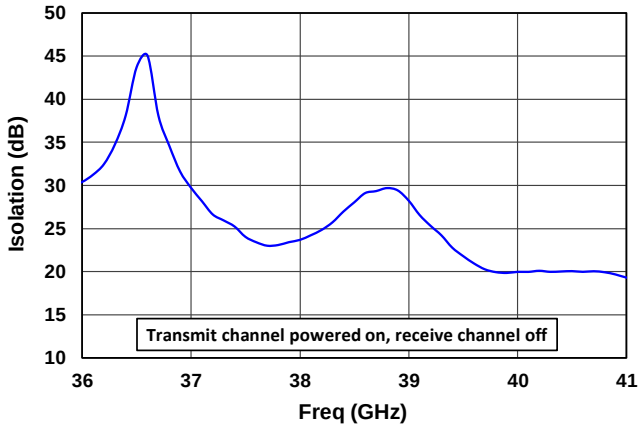
TX1 to Ant2 Relative to ANT1



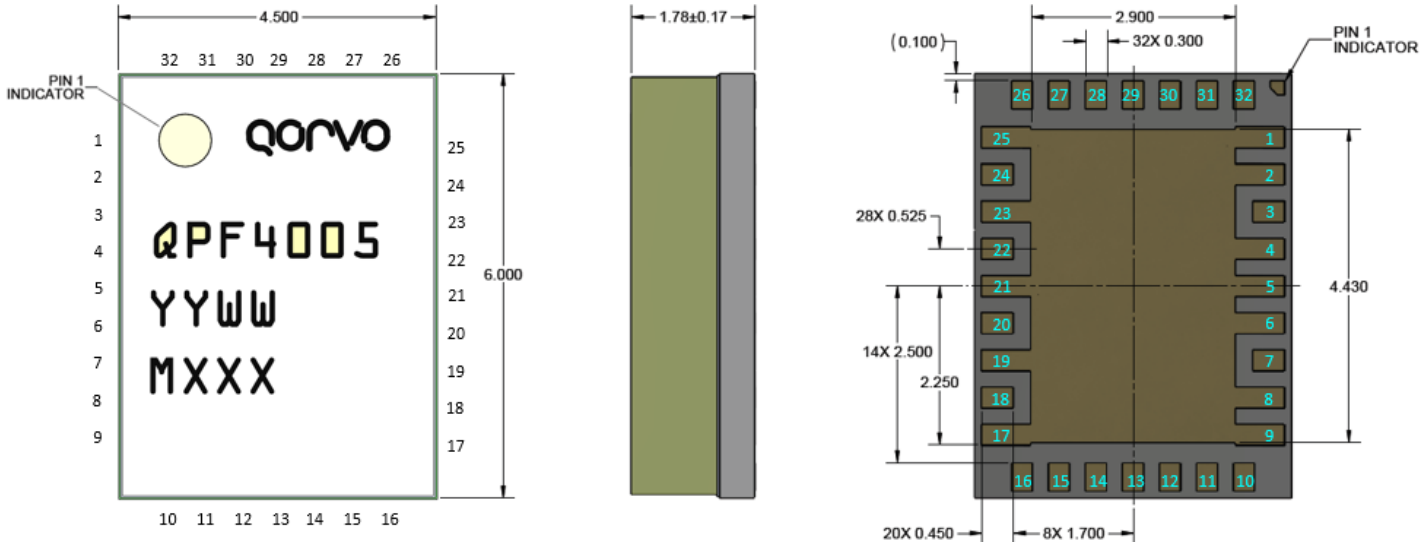
Antenna Port Isolation Ant1 - Ant2



Transmit to Receive Isolation TX1 - RX1



Mechanical Drawings & Pad Descriptions

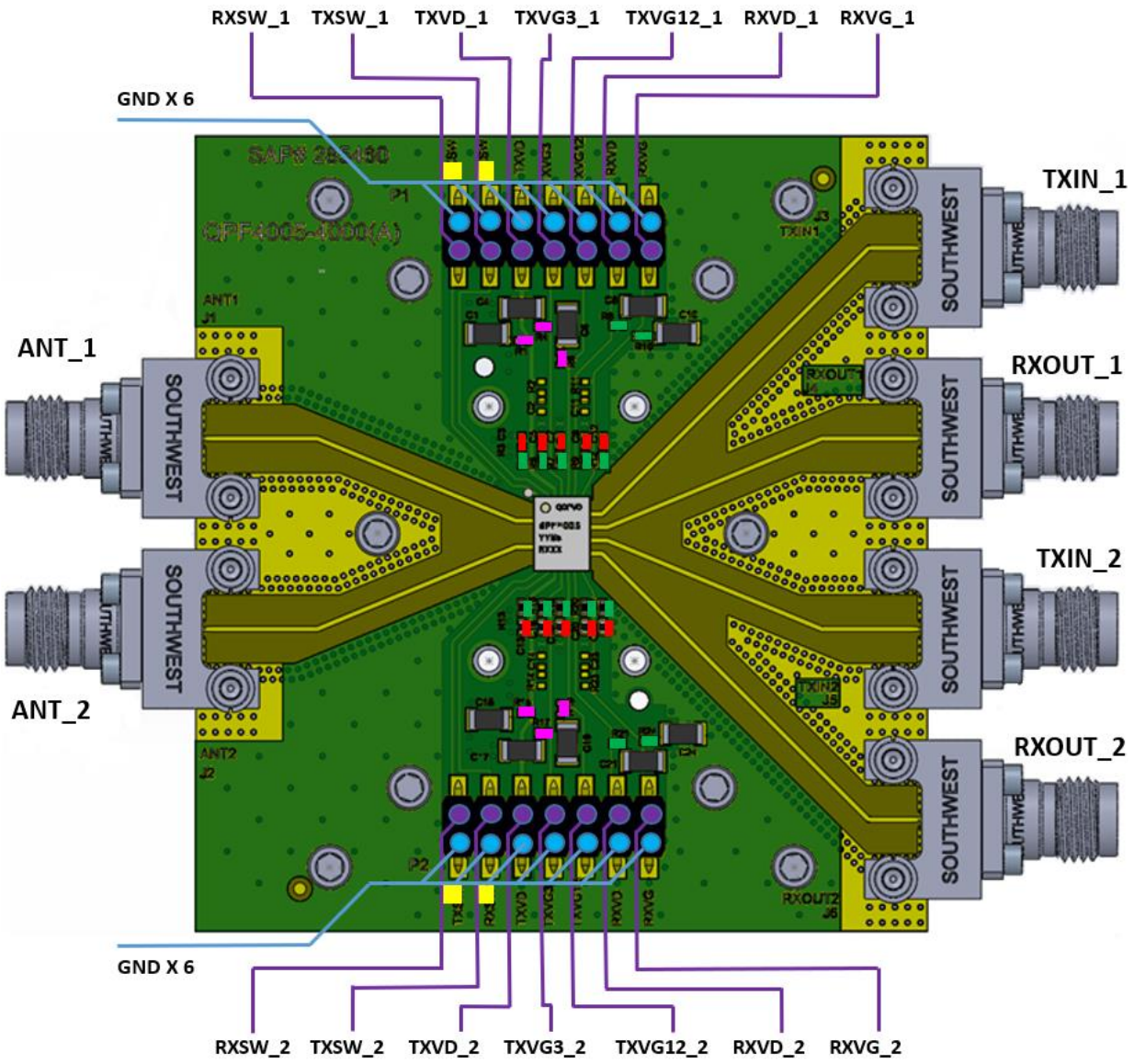


Dimensions in mm

Part Marking: QPF4005: Part Number, YY = Part Assembly Year, WW = Part Assembly Week, MXXX = Batch ID

Pin Number	Label	Description
1, 2, 4, 5, 6, 8, 9	GND	GROUND
3	ANT_1	Channel 1 Antenna, DC Grounded
22	RXOUT_1	Channel 1 Receive Output, DC Blocked
24	TXIN_1	Channel 1 Transmit Input, DC Grounded
26	RXVG_1	Channel 1 Receive VG
27	RXVD_1	Channel 1 Receive VD
28	TXVG12_1	Channel 1 Transmit VG12
29	TXVG3_1	Channel 1 Transmit VG3
30	TXVD_1	Channel 1 Transmit VD
31	TXSW_1	Channel 1 Transmit Switch
32	RXSW_1	Channel 1 Receive Switch
7	ANT_2	Channel 2 Antenna, DC Grounded
10	RXSW_2	Channel 2 Receive Switch
11	TXSW_2	Channel 2 Transmit Switch
12	TXVD_2	Channel 2 Transmit VD
13	TXVG3_2	Channel 2 Transmit VG3
14	TXVG12_2	Channel 2 Transmit VG12
15	RXVD_2	Channel 2 Receive VD
16	RXVG_2	Channel 2 Receive VG
18	RXOUT_2	Channel 2 Receive Output, DC Blocked
20	TXIN_2	Channel 2 Transmit Input, DC Grounded
17, 19, 21, 23, 25, Slug	GND	GROUND

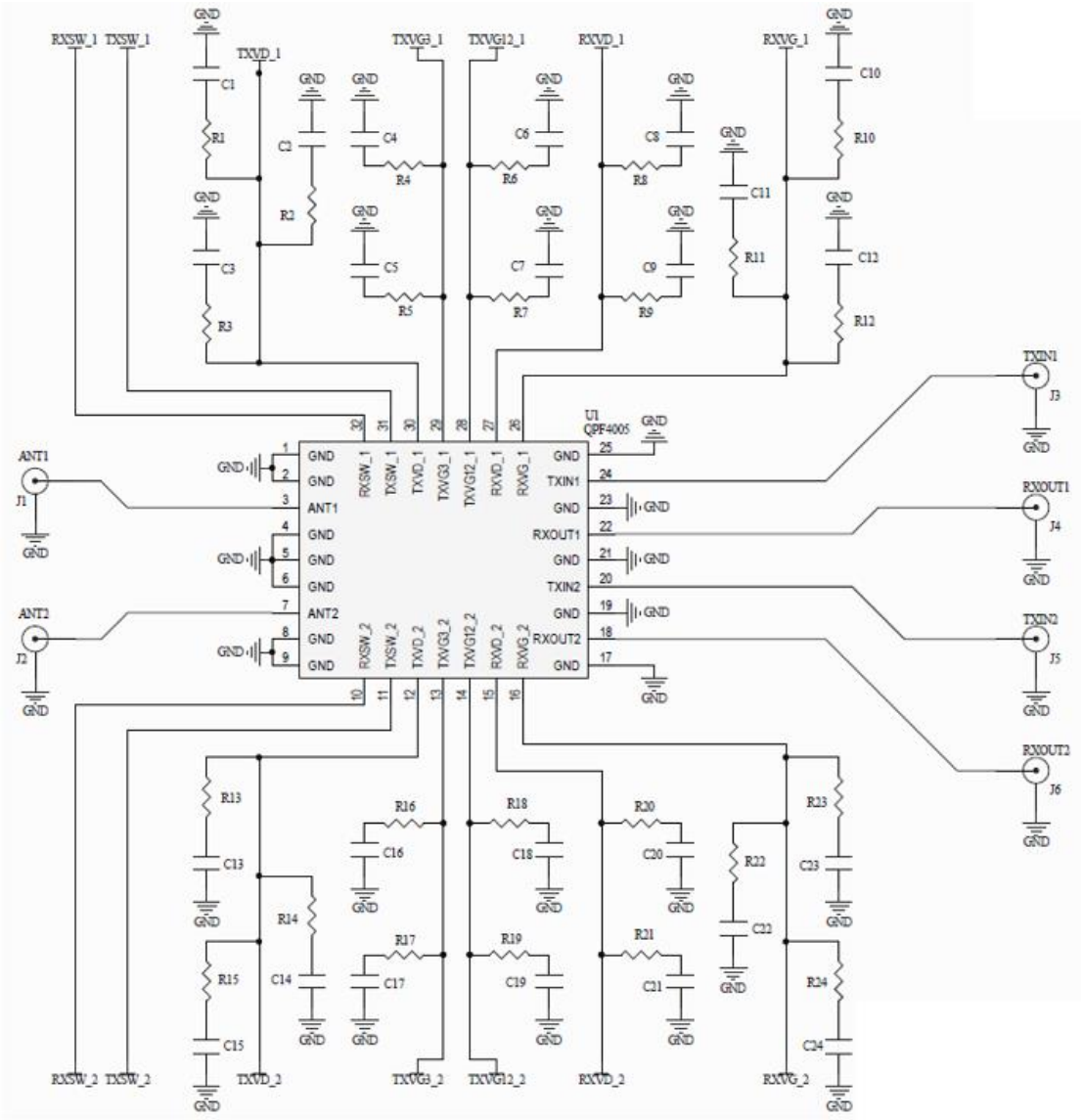
Evaluation Board and Assembly



RF Layer is 0.008” thick Rogers Corp. RO4003C (ε_r = 3.35). Metal layers are 0.5 oz. copper. The microstrip line at the connector interface is optimized for the Southwest Microwave end launch connector 1492-04A-5.

Ref. Des.	Component	Value	Manuf.	Remark
C2, C4, C6, C8, C10	SMT Cap.	CAP, 0402 1000pF +/-10% 50V 0402 X7R ROHS	Various	Red
C1, C3, C5, C7, C9	SMT Cap.	CAP, 1206 1.0uF +/-10% 50V X7R ROHS	Various	Grey
R2, R4, R6 - R10	SMT Res.	RES, 0402 5.1 OHM, 5% 50V, ROHS	Various	Green
R1, R3, R5	SMT Res.	RES, 0402 0 OHM, 5%, ROHS	Various	Pink

Application Circuit



Bias-up Procedure

1. Set drain supply TXVD limit to 700 mA, RXVD limit to 50 mA, gate and control supply limit to 10 mA each.
2. Set TXVG12, TXVG3, RXVG to −5 V
3. Set TXSW = 20 V (or 0 V), RXSW = 0 V (or 20 V)
4. Set VD = +20 V
5. For TX, adjust TXVG12 to get TXID12 current, then adjust TXVG3 to achieve required total drain current; For RX, adjust RXVG to achieve required drain current.
6. Apply RF signal

Bias-down Procedure

1. Turn off RF signal
2. Set TXVG12, TXVG3 and RXVG to −5 V
3. Set VD = 0 V
4. Turn off drain supply
5. Turn off TXSW, RXSW
6. Turn off gate supply

Absolute Maximum Ratings

Parameter	Value
Drain Voltage (TXVD, RXVD)	28 V
Drain Current (TXID3+TXID12)	800 mA
Drain Current (RXID)	60 mA
Gate Voltage (RXVG, TXVG3, TXVG12)	0 to −5 V
Gate Current (RXIG, TXIG3, TXIG12)	20 mA
Switch Control Voltage (TXSW, RXSW)	0 to 28 V
Switch Control Current	20 mA
RF Input Power (All RF ports, 85 °C)	30 dBm
Channel Temperature, T_{CH}	225 °C
Mounting Temperature (30 seconds)	260 °C
Storage Temperature	−55 to 150 °C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Thermal and Reliability Information

Parameter	Values	Units	Conditions
Thermal Resistance (θ_{JC}) (1,2,3), Quiescent, TX	14.9	°C/W	TX on, RX off, CW, V_D = +20 V, I_{DQ} = 159 mA, T_{BASE} = 85 °C RF off, P_{DISS} =3.18 W
Channel Temperature (T_{CH}), Quiescent, TX	132.4	°C	
Thermal Resistance (θ_{JC}) (1,2,3), Under Drive, TX	10.7	°C/W	TX on, RX off, CW, V_D = +20 V, T_{BASE} = 85 °C, Freq = 39 GHz, P_{IN} = 10 dBm, P_{OUT} = 25 dBm, I_{D_DRIVE} = 0.25 A, P_{DISS} = 4.69 W
Channel Temperature (T_{CH}), Under Drive, TX	135.2	°C	
Thermal Resistance (θ_{JC}) (1,2,3), Quiescent, RX	67.0	°C/W	RX on, TX off, CW, V_D = +20 V, I_{DQ} = 15 mA T_{BASE} = 85 °C RF off, P_{DISS} = 0.3 W
Channel Temperature (T_{CH}), Quiescent, RX	105.1	°C	

Notes:
1. Thermal resistance is referenced to package backside
2. Base or ambient temperature is 85 °C
3. Refer to the following document: GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates

Solderability

1. Compatible with the latest version of J-STD-020, Lead-free solder, 260 °C.
2. This package is non-hermetic, and therefore cannot be subjected to aqueous washing. The use of no-clean solder to avoid washing is highly recommended.

Recommended Soldering Temperature Profile