QPL6202Q

Ultra-Low Noise, High Gain LNA

General Description

The QPL6202Q is a flat-gain, high-linearity, ultra-low noise amplifier in a small 2 x 2 mm surface-mount package. At 2.3 GHz, the amplifier typically provides 21.8 dB gain, +39.9 dBm OIP3 at a 55 mA bias setting, and 0.52 dB noise figure. The LNA can be biased from a single positive supply ranging from 3.3 to 5.25 volts. The device is housed in a green/RoHS-compliant industry-standard 2x2 mm package.

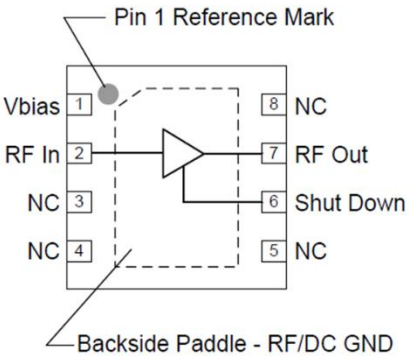
The QPL6202Q uses a high performance E-pHEMT process. The low noise amplifier contains an internal active bias to maintain high performance over temperature. This LNA integrates a shut-down biasing capability to allow for operation in TDD applications.

Package: DFN, 8-pin
2.0mm x 2.0mm x 0.85mm

Product Features

- Tested to AEC-Q100 Grade 2
- Ultra-low noise figure, 0.52 dB NF @ 2.3 GHz
- >20 dB gain across SDARS
- Bias adjustable for linearity optimization
- High input power ruggedness, >32 dBm Pin Max
- +39.9 dBm OIP3 at 55mA I_{DD}
- Unconditionally stable
- Integrated shutdown control pin
- Maintains OFF state with high Pin drive
- +3.3V to +5.25V supply; does not require -Vgg

Functional Block Diagram



Top View

Applications

- SDARS

Ordering Information

Part No.	Description
QPL6202QSB	5 PC SAMPLE BAG
QPL6202QSQ	25 PIECE SAMPLE BAG
QPL6202QSR	100 PIECE 7” SAMPLE REEL
QPL6202QTR7	2500 PIECE 7” SAMPLE REEL
QPL6202QPCK-01	EVALUATION BOARD + 5 PC SAMPLE BAG

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−65 to +150 °C
Supply Voltage	+7V
RF Input Power, CW, 50 Ω, T=25 °C	+33 dBm
RF Input Power, WCDMA, 10dB PAR	+27 dBm
RF Input Power, CW, OFF State	+33 dBm

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Supply Voltage (V_{DD})	3.3	4.5	5.25	V
Bias Voltage (V_{bias})	3.3	3.6	5.25	V
TCASE	−40		+105	°C
Tj for >10^6 hours MTTF			+190	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications at +25˚C

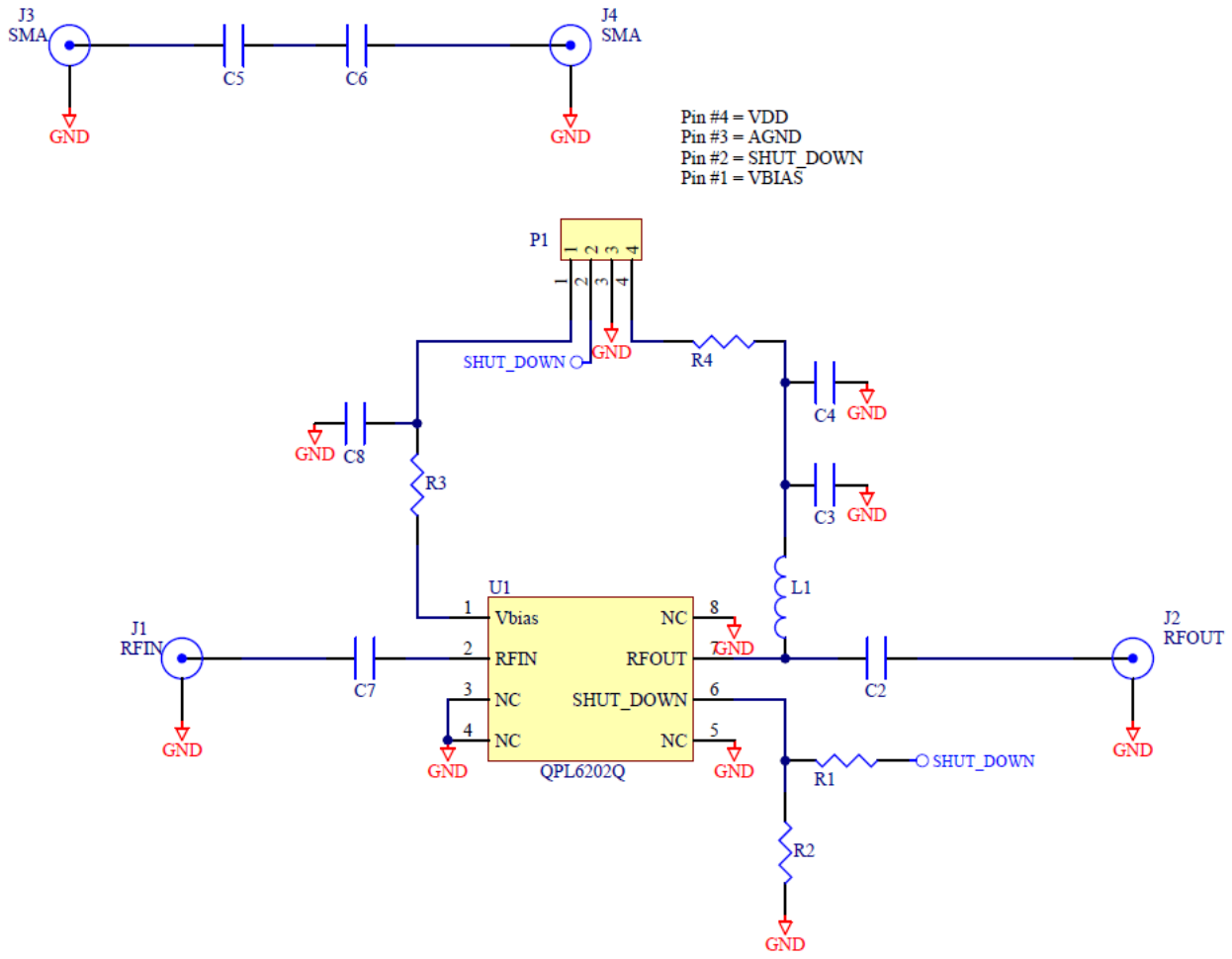
Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		2320		2345	MHz
Test Frequency			2332		MHz
Gain		21.2	21.8	23.5	dB
Input Return Loss			8.5		dB
Output Return Loss			17		dB
Noise Figure[1]			0.52	0.75	dB
Output P1dB		+17	+19.9		dBm
Output IP3	Pout =+2 dBm/tone, Δf=1 MHz	+30	+39.9		dBm
Power Shutdown Control (pin 6)	On state	0		0.63	V
	Off state (Power down)	1.17		V_{DD}	V
Current, I_{DD}[2]	On state	38	55	68	mA
	Off state (Power down)		2.8	5	mA
Shutdown pin current, ISD	VPD ≥ 1.17 V		58		µA
Switching Speed	LNA ON to OFF		583		ns
	LNA OFF to ON		216		ns
Thermal Resistance, θjc	channel to case		48		°C/W

Test conditions unless otherwise noted: VDD = +4.5V, Vbias = +3.6V, Temp=+25°C, 2332MHz, 50 Ω system

Note: **1**) Noise Figure data has input trace loss de-embedded

2) Icq set by external 3.6K resistor

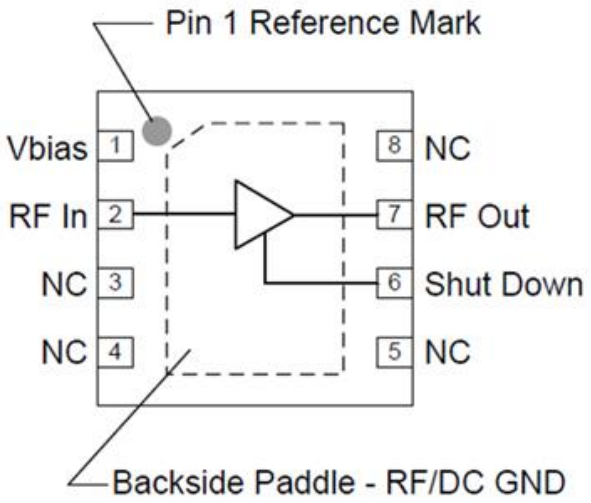
Applications Schematic



Qty	Ref Des	Description	UOM
1	U1	Hi Gain SDARS	EA
1		PCB, QPL6202	EA
5	C2,C5,C6,C7,C8	CAP, 100pF, 5%, 50V, C0G, 0402	EA
1	C3	CAP, 1000pF, 10%, 50V, X7R, 0402	EA
1	C4	CAP, 1uF, 10%, 6.3V, X7R, 0402	EA
2	R1,R4	RES, 0 OHM, 5%, 1/10W, 0402	EA
1	R3	RES, 3.6K, 5%, 1/16W, 0402	EA
1	R2	RES, 20K, 5%, 1/16W, 0402	EA
1	L1	IND, 18nH, 5%, M/L, 0402	EA
4	J1,J2,J3,J4	862000-422 CONN .062 RF SMA F STRT FLANG	EA
1	P1	CONN, HDR, ST, PLRZD, 4-PIN, 0.100"	EA

Vbias=3.6V	**Icq**	40mA	50mA	60mA	70mA	80mA
Vdd=4.5V	**R3**	7K	4.9K	3.5K	2.7K	2.1K

Pin Configuration and Description

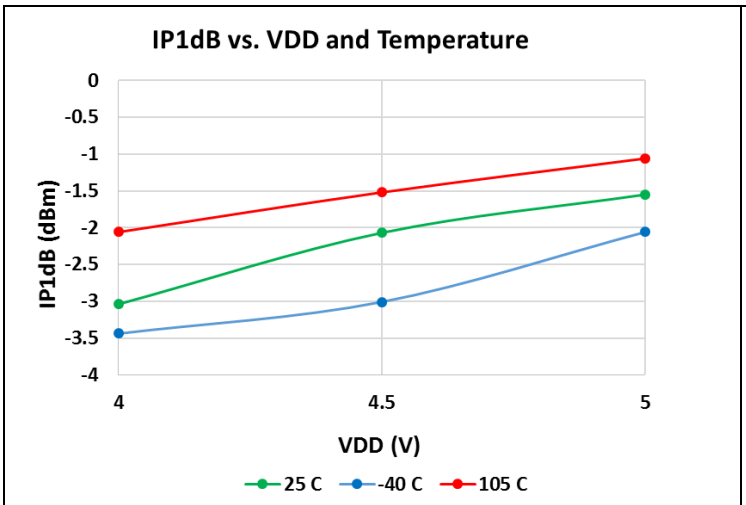


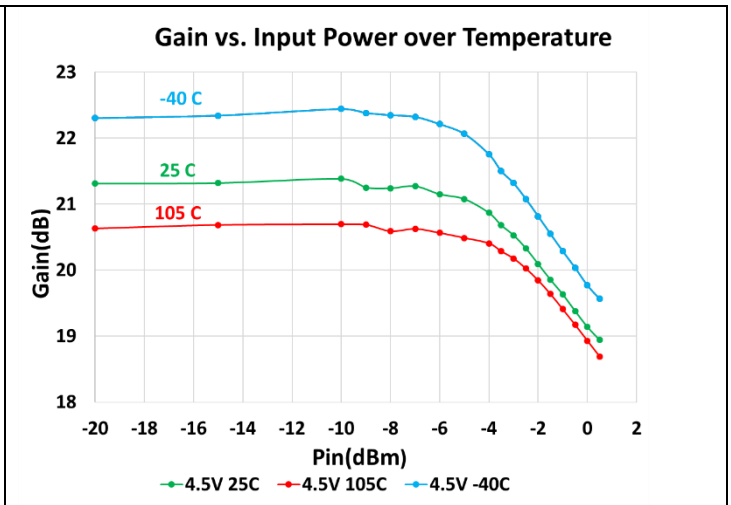
Top View

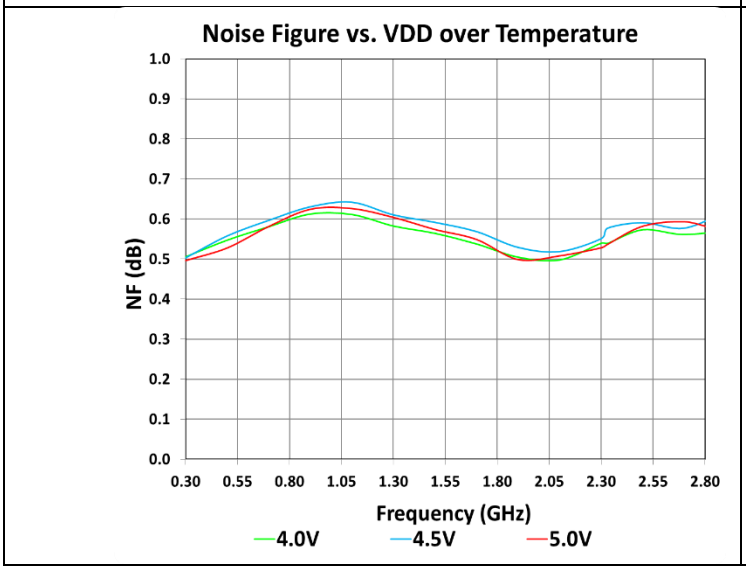
Pad No.	Label	Description
1	Vbias	Sets the Icq bias point for the device.
2	RF In	RF Input pin. A DC Block is required.
6	Shut Down	A high voltage (>1.17V) turns off the device. If the pin is pulled to ground or driven with a voltage less than 0.63V, then the device will operate under LNA ON state.
7	RF Out / DCBias	RF Output pin. DC bias will also need to be injected through a RF bias choke/inductor for operation.
3, 4, 5, 8	NC	No electrical connection. Provide grounded land pads for PCB mounting integrity.
Backside Paddle	RF/DC GND	RF/DC ground. Use recommended via pattern to minimize inductance and thermal resistance; see PCB Mounting Pattern for suggested footprint.

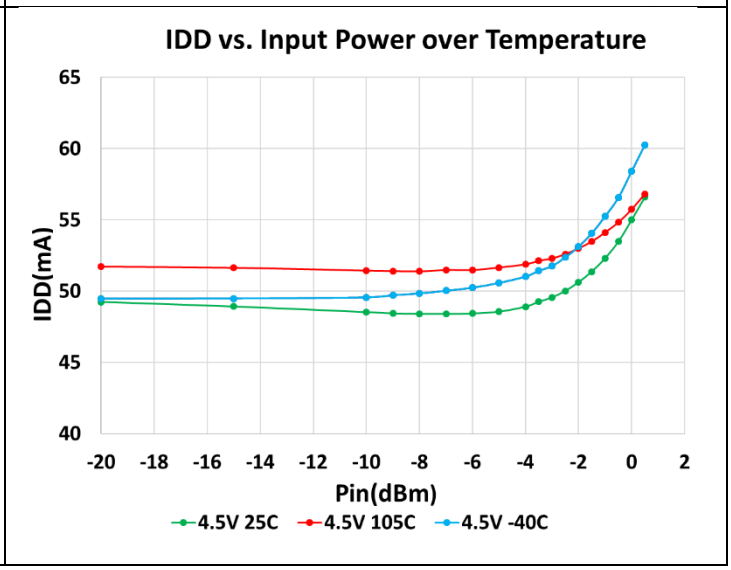
Performance Plots

Test conditions unless otherwise noted: V_{DD}=+4.5 V, I_{DD} = 50mA, Temp=+25°C. Noise figure data has input trace loss de-embedded.





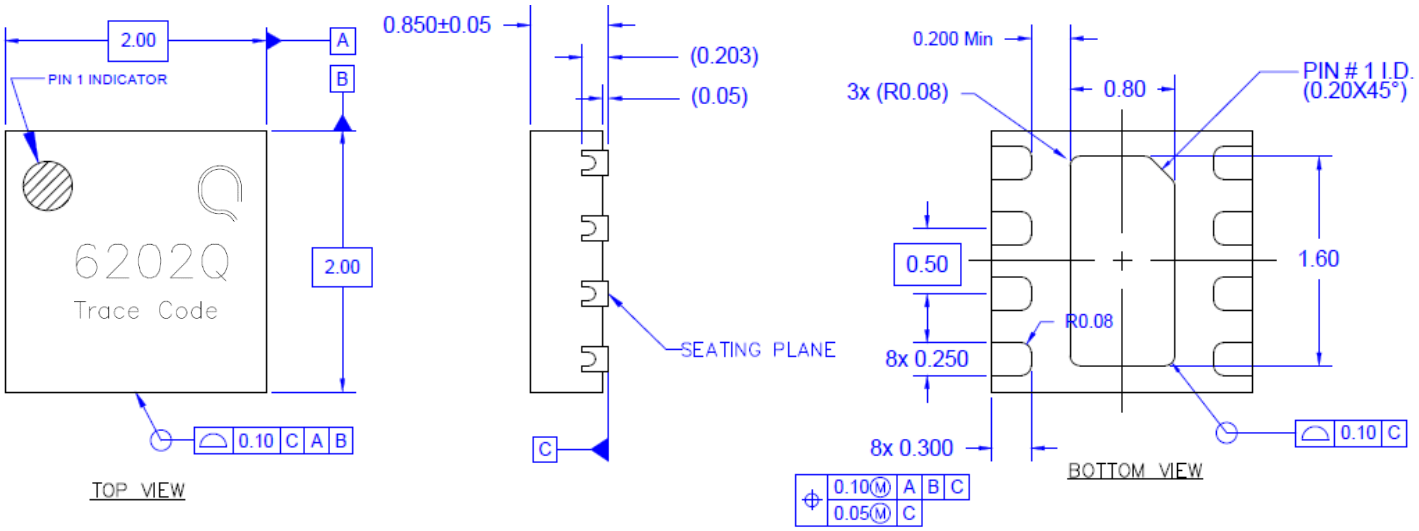




Mechanical Information

Marking: Part number – 6202Q

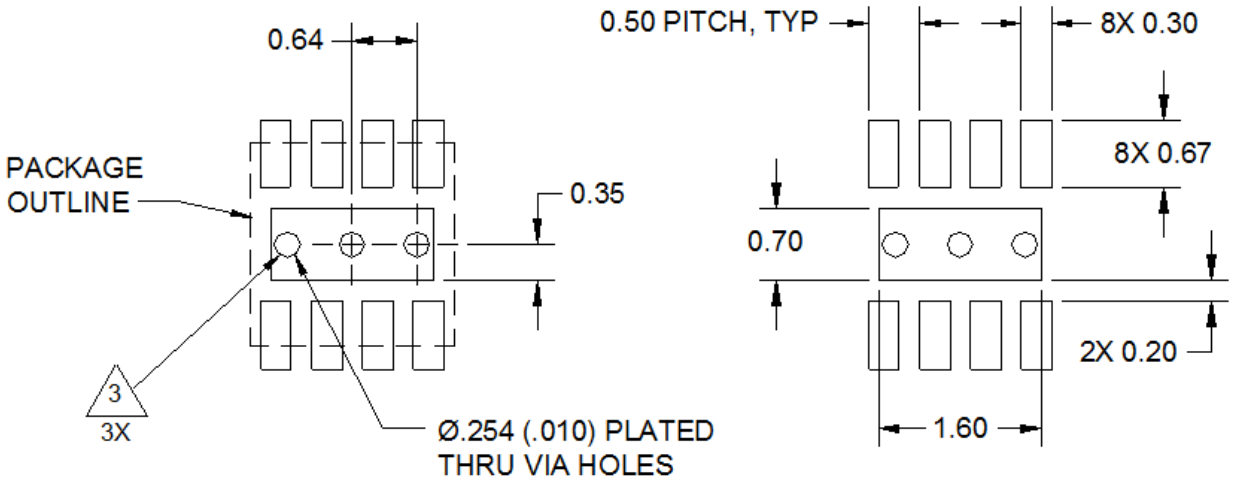
Trace Code – XXXX



NOTES:

1. All dimensions are in millimeters. Angles are in degrees.
2. Except where noted, this part outline conforms to JEDEC standard MO-220, Issue E (Variation VGGC) for thermally enhanced plastic very thin fine pitch quad flat no lead package (QFN).
3. Dimension and tolerance formats conform to ASME Y14.4M-1994.
4. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

PCB Mounting Pattern



Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.10”).
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.