QPL6207Q

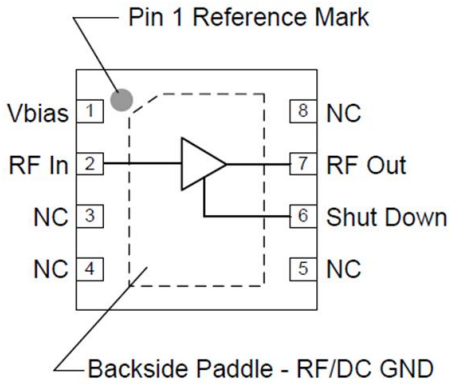
High-Linearity SDARS LNA

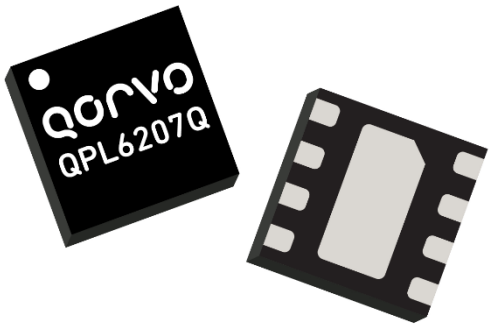
Product Description

The QPL6207Q is a high linearity, ultra-low noise gain block amplifier in a small 2x2 mm surface-mount package. At 2332 MHz, the amplifier typically provides +35 dBm OIP3. The amplifier does not require any negative supplies for operation and can be biased from positive supply rails from 3.3 to 5.25 V. The device is housed in a lead- free/green/RoHS-compliant industry-standard 2x2 mm package.

The QPL6207Q uses a high performance E-pHEMT process. The low noise amplifier contains an internal active bias to maintain high performance over temperature.

Functional Block Diagram





Package: DFN, 8-pin
2.0mm x 2.0mm x 0.85mm

Feature Overview

- Tested in accordance to AEC-100 Grade 2
- High Gain device – Typical value 18.5dB
- Ultra-low noise figure, 0.45 dB NF at 2332 MHz
- High linearity, +35 dBm Output IP3
- High input power ruggedness, >29 dBm PIN, MAX
- Unconditionally stable
- Externally controlled Icq with Vbias
- Integrated shutdown control pin
- 3.3-5.25 V positive supply voltage: −Vgg not required

Applications

- SDARS Active Antenna

Ordering Information

PART NUMBER	DESCRIPTION
QPL6207QSB	5 PIECE SAMPLE BAG
QPL6207QSQ	25 PIECE SAMPLE BAG
QPL6207QSR	100 PIECE 7” REEL
QPL6207QTR7	2500 PIECE 7” REEL
QPL6207QPCK-01	EVALUATION BOARD + 5 PIECE SAMPLE BAG

Absolute Maximum Ratings

PARAMETER	RATING	UNITS
Storage Temperature	-65 to 150°	C
Supply Voltage (V_{DD})	+7	V
RF Input Power, CW, 50Ω,T = 25°C	+30	dBm

Recommended Operating Conditions

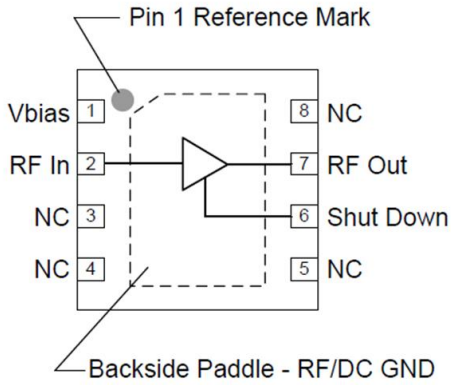
PARAMETER	MIN	TYP	MAX	UNITS
Supply Voltage (V_{DD})	+3.3	+4.5	+5.25	V
Bias Voltage (V_{bias})	+3.3	+3.6	+5.25	V
TCASE	−40		+105	°C
TJ (for >10^6 hours MTTF)			+190	°C

Electrical Specifications at +25˚C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operational Frequency Range		2320	2332	2345	MHz
Test Frequency			2330		MHz
Gain		18.1	18.5	20	dB
Input Return Loss			9.5		dB
Output Return Loss			8.5		dB
Output P1dB		+19.5	+21.5		dBm
Output IP3	Pout=+5 dBm/tone, Δf=1 MHz	+31	+35		dBm
Noise Figure[1]			0.45	0.7	dB
Power Shutdown Control (Pin 6)	On state	0		0.63	V
	Off state (Power down)	1.17	3.3	V_{DD}	V
Current, I_{DD}[2]	On state	38	55	68	mA
	Off state (Power down)		3	5	mA
Shutdown pin current, ISD	VPD ≥ 1.17 V		60	500	µA
Thermal Resistance, θjc	Channel to case		53.4		°C/W

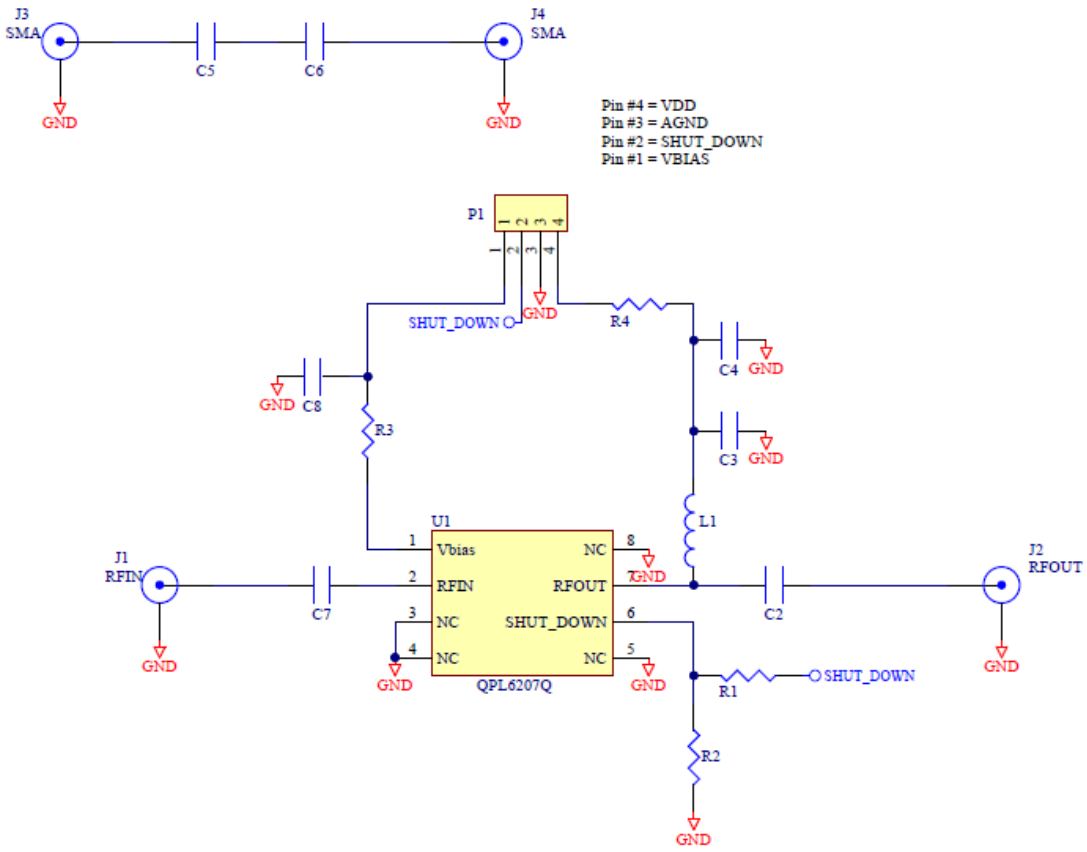
Test conditions unless otherwise noted: VDD = +4.5V, Vbias = +3.6V, Temp=+25°C, 50 Ω system
Note: **1**) Noise Figure data has input trace loss de-embedded
2) Icq set by external 2.7K resistor

Pin Configuration and Description



Pin No.	Label	Description
1	Vbias	Sets the Icq bias point for the device.
2	RF In	RF Input pin. A DC Block is required.
6	Shut Down	A high voltage (>1.17V) turns off the device. If the pin is pulled to ground or driven with a voltage less than 0.63V, then the device will operate under LNA ON state.
7	RF Out / DCBias	RF Output pin. DC bias will also need to be injected through a RF bias choke/inductor for operation.
3, 4, 5, 8	NC	No electrical connection. Provide grounded land pads for PCB mounting integrity.
Backside Paddle	RF/DC GND	RF/DC ground. Use recommended via pattern to minimize inductance and thermal resistance; see PCB Mounting Pattern for suggested footprint.

Applications Schematic

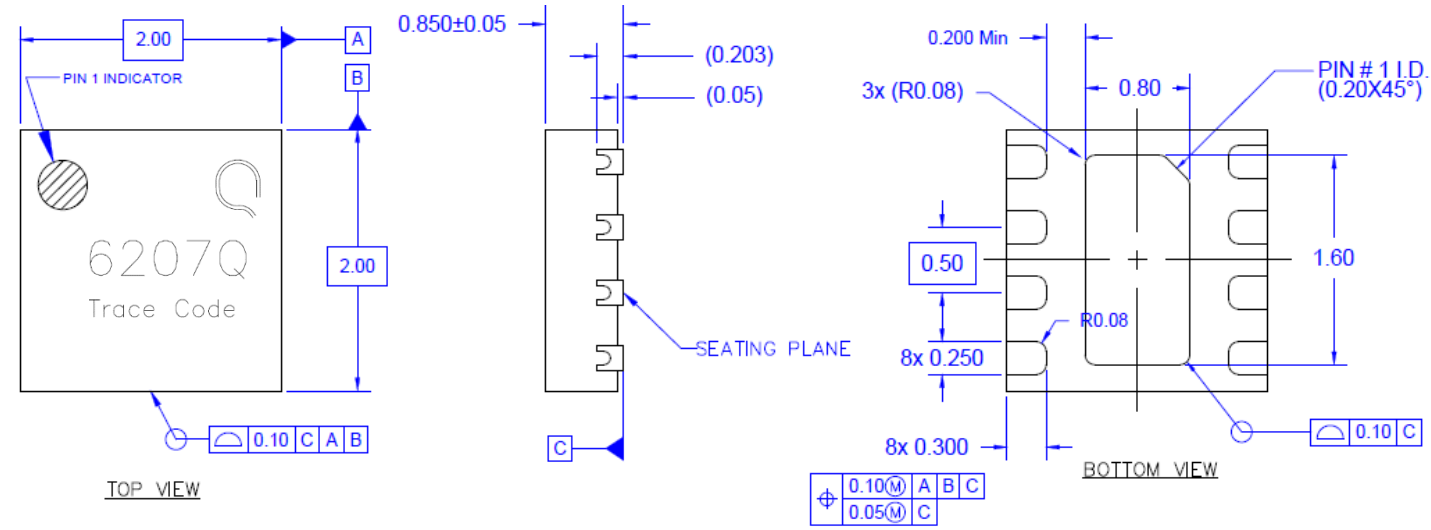


Qty	Ref Des	Description
1		High Linearity, SDARs LNA
1		PCB, QPL6207Q
5	C2,C5,C6,C7,C8	CAP, 100pF, 5%, 50V, C0G, 0402
1	C3	CAP, 1000pF, 10%, 50V, X7R, 0402
1	C4	CAP, 1uF, 10%, 6.3V, X7R, 0402
1	R3	RES, 2.7K OHM, ±1% 1/10W, 0402
2	R1,R4	RES, 0 OHM, 5%, 1/10W, 0402
1	R2	RES, 20K, 5%, 1/16W, 0402
1	L1	IND, 18nH, 5%, M/L, 0402
4	J1,J2,J3,J4	862000-422 CONN .062 RF SMA F STRT FLANG
1	P1	CONN, HDR, ST, PLRZD, 4-PIN, 0.100"

Vbias=3.6V	**Icq**	40mA	50mA	60mA	70mA	80mA
Vdd=4.5V	**R3**	4.6K	3.3K	2.55K	1.9K	1.55K

Mechanical Information

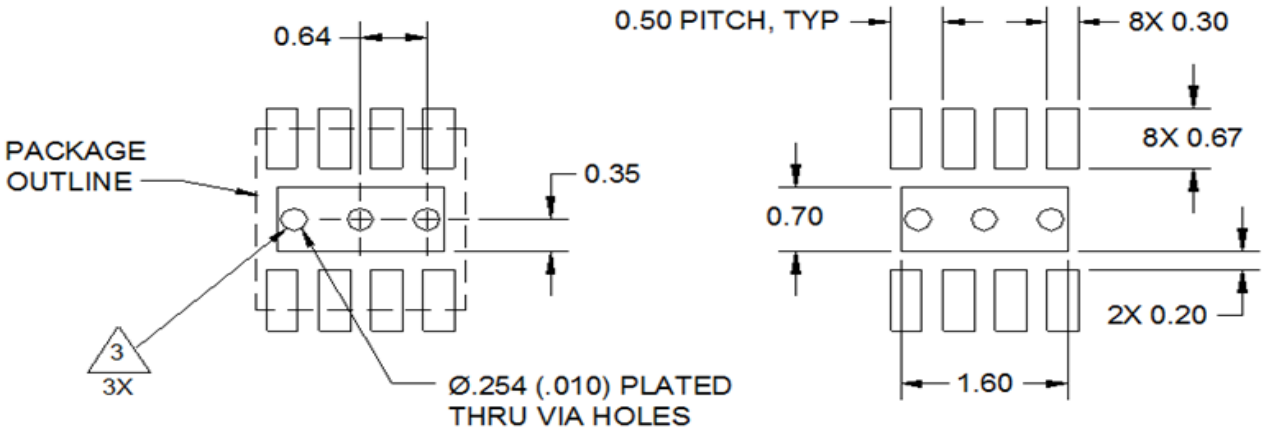
Marking: Part number – 6207Q
Trace Code – XXXX



NOTES:

1. All dimensions are in millimeters. Angles are in degrees.
2. Except where noted, this part outline conforms to JEDEC standard MO-220, Issue E (Variation VGGC) for thermally enhanced plastic very thin fine pitch quad flat no lead package (QFN).
3. Dimension and tolerance formats conform to ASME Y14.4M-1994.
4. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

PCB Mounting Pattern



NOTES:

1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.10”).
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.