

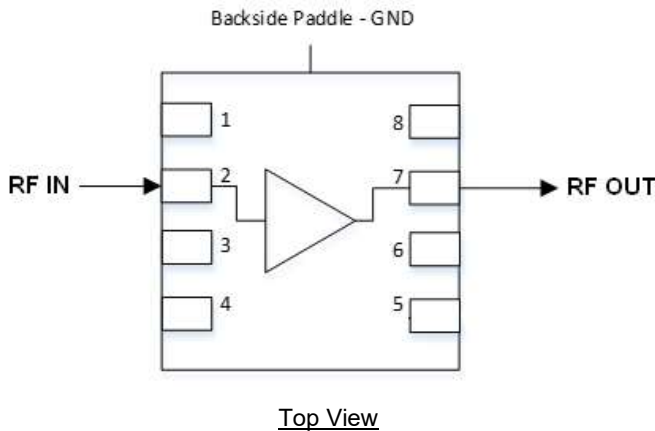
Product Overview

The QPL7433 is a low noise, high gain, wide bandwidth MMIC pHEMT single ended RF amplifier IC featuring 17.5dB of flat gain. This IC is designed to support CPE Front End, Cable, Satellite and Terrestrial TV, Home Gateways, and Cable Modems from 50 to 3300MHz using a single 5V supply. QPL7433 offers low noise and distortion plus high gain in a 2x2 8pin DFN package.



2X2 DFN 8pin Package

Functional Block Diagram



Key Features

- 50 MHz to 3300 MHz Operation
- Low Power Consumption 5 V, 90mA
- Gain: 17.5 dB over the entire BW
- Noise Figure: 1.5 dB Typical
- P1dB: 20dBm
- OIP3: +34dBm
- Adjustable Bias Using External Resistors
- Convenient 2x2, 8pin, DFN Package
- RoHS Compliant

Applications

- Cable, Terrestrial and Satellite
- Extended Spectrum DOCSIS
- CATV Node & Amplifiers
- Optical Node
- Satellite Low Noise Amplifier
- Cable Modem and Set Top Box
- Single Ended Gain Block

Ordering Information

| Part Number | Description |
|---------------|--------------------------|
| QPL7433SB | Sample bag with 5 pieces |
| QPL7433SR | 7" Reel with 100 pieces |
| QPL7433TR7 | 7" Reel with 2500 pieces |
| QPL7433PCK-01 | 50 – 3300 MHz PCBA |

Absolute Maximum Ratings

| Parameter | Rating |
|------------------------------|----------------|
| Supply Voltage (V_{DD}) | +10 V |
| Supply Current (I_{DD}) | 120 mA |
| Maximum Input Level | 20 dBm |
| Operating Temperature Range | -40 to +85 °C |
| Storage Temperature Range | -65 to +150 °C |
| Maximum Junction Temperature | +150 °C |

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

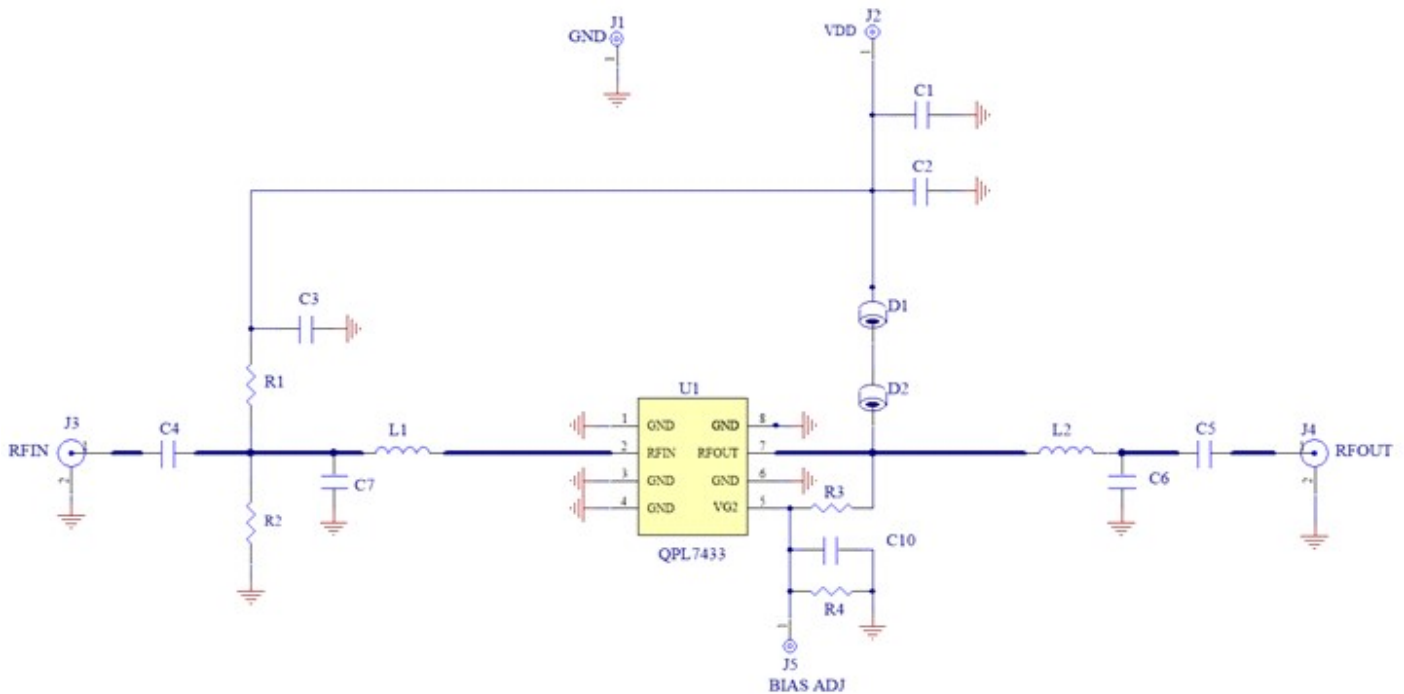
Electrical Specifications – 5 V

| Parameter | Condition ⁽¹⁾ | Min | Typ | Max | Unit |
|-----------------------------|------------------------------------|-----|------|------|------|
| Supply Voltage (V_{DD}) | | | 5 | | V |
| Supply Current (I_{DD}) | | | 90 | | mA |
| Frequency Range | | 50 | | 3300 | MHz |
| Gain | | | 17.5 | | dB |
| Reverse Isolation | | | 20 | | dB |
| Input Return Loss | | | 15 | | dB |
| Output Return Loss | | | 15 | | dB |
| Noise Figure | | | 1.5 | | dB |
| OIP2L | 5 dBm / tone output, 50-870 MHz | | 57 | | dBm |
| OIP2H | 5 dBm / tone output, 1050 MHz | | 47 | | dBm |
| OIP2L | 5 dBm / tone output, 2550 MHz | | 55 | | dBm |
| OIP3 | 5 dBm / tone output, 50-870 MHz | | 35 | | dBm |
| OIP3 | 5 dBm / tone output, 870-2000 MHz | | 33 | | dBm |
| OIP3 | 5 dBm / tone output, 2000-3000 MHz | | 29 | | dBm |
| OP1dB | 50-2000 MHz | | 19.5 | | dBm |
| OP1dB | 2000-3000 MHz | | 18.5 | | dBm |
| Thermal Resistance | Θ_{JC} | | 62 | | °C/W |

Notes:

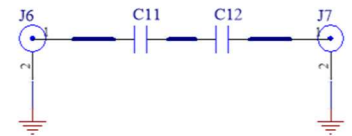
1. Typical performance at these conditions: Temp = +25 °C, V_{DD} = +5V, 50 Ω system, Full band unless otherwise noted

Evaluation Board Schematic 50 MHz – 3300 MHz

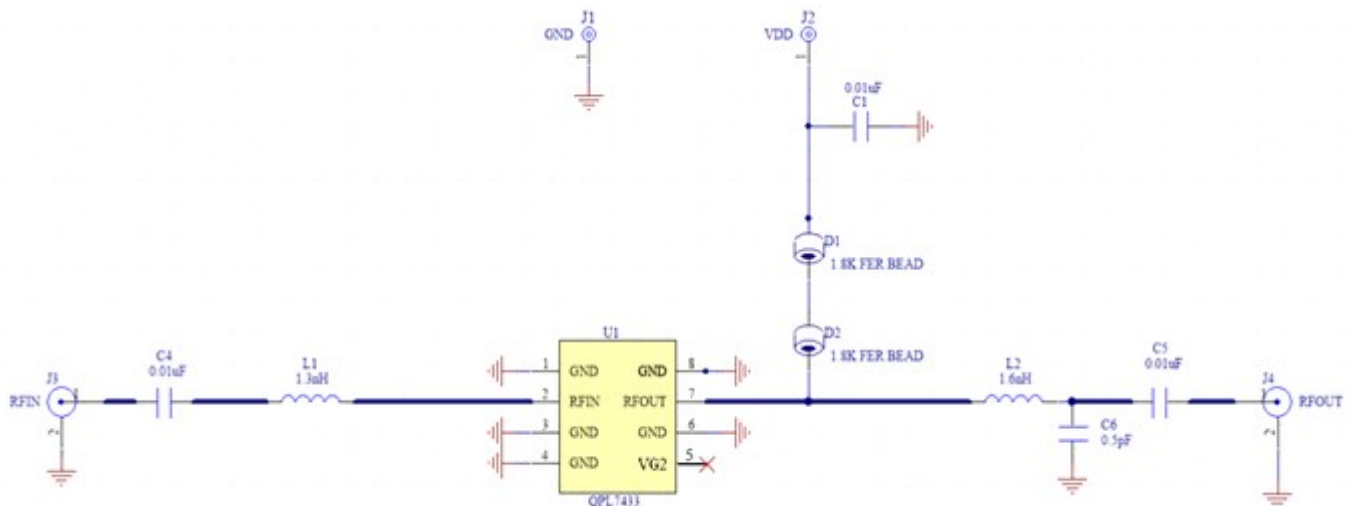


Notes:

1. L1, C7 tunes input return loss.
2. L2, C6 tune output return loss.
3. D1, D2 provide the bias path with RF isolation from the RF output path.
4. C4, C5 provide DC block.
5. R1, R2 and C3 are options that may be added from the input to VDD or to ground to increase linearity or shed power, trading off degraded noise figure and return loss. Device current can only be adjusted strictly through R1 and R2.
6. Pin5 is an internal gate voltage adjust and can be left floating at VDD=5V.



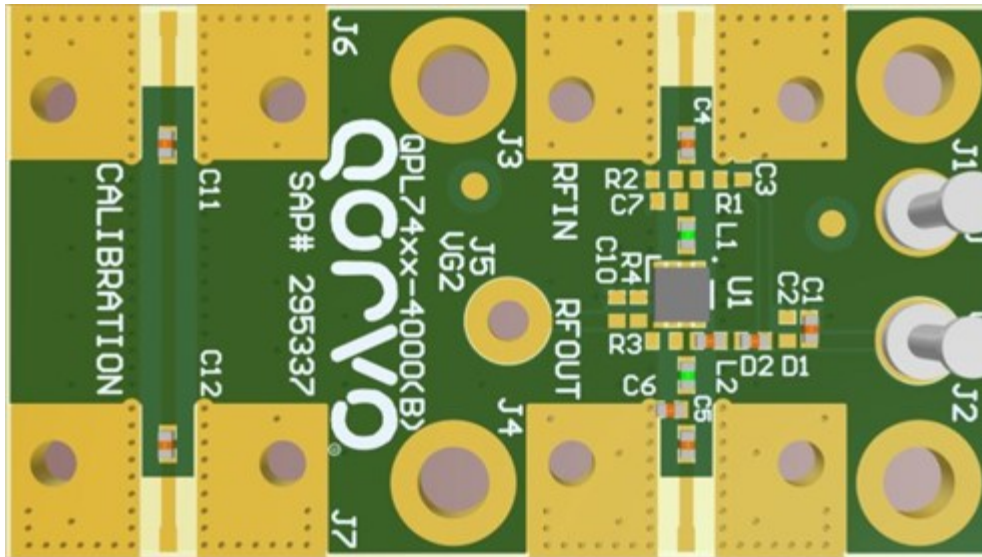
Typical Application Schematic, 50 MHz – 3300 MHz



Evaluation Board Bill of Materials

| Designator | Description | Manufacturer | Part Number |
|--------------------------------------|----------------------------------|------------------------------|-------------------------|
| PCB | QPL7433-4000 EVB | TTM Technology INC | QPL7433-4000(A) |
| U1 | QPL7433 | Qorvo | QPL7433SB |
| D1, D2 | FER, BEAD, 1.8K, 5%, 200mA, 0402 | TDK | MMZ1005A182ET000 |
| C6 | CAP, 0.5pF, +/-0.1pF, 50V, 0402 | Murata Electronics | GJM1555C1HR50BB01D |
| C1, C4, C5, C10 | CAP, 0.01uF, 10%, 50V, X8L, 0402 | Murata Electronics | GCM155L81E103KA37D |
| L1 | IND, 1.3nH, +/-0.1nH, 0402 | Murata Electronics | LQG15HS1N3B02 |
| L2 | IND, 1.6nH, +/-0.1nH, 0402 | Murata Electronics | LQG15HS1N6B02 |
| J3, J4, J6, J7 | 862000-422 CONN, SMA F, 50 Ohm | Cinch Connectivity Solutions | 142-0701-851 |
| J1, J2, J5 | 862000-055 TERM. SOLDER TURRET | Mouser Electronics, Inc | 2533-0-00-44-00-00-07-0 |
| C2, C3, C7, C11, C12, R1, R2, R3, R4 | Not Populated | | |

Evaluation Board Assembly Drawing



EVB PCB Material and Stack-up

Board Material: Rogers 4350B, 4450F, 62mil total thickness.

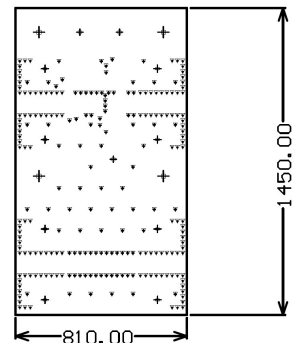
$\epsilon_r = 3.66$

Plating: 1.0 oz Copper

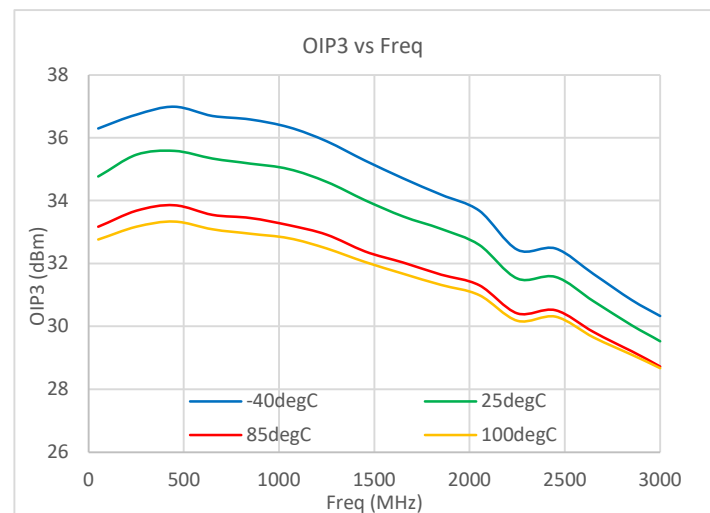
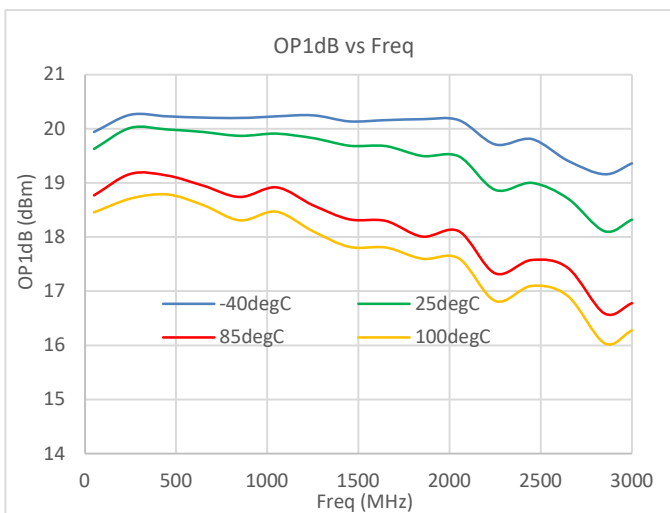
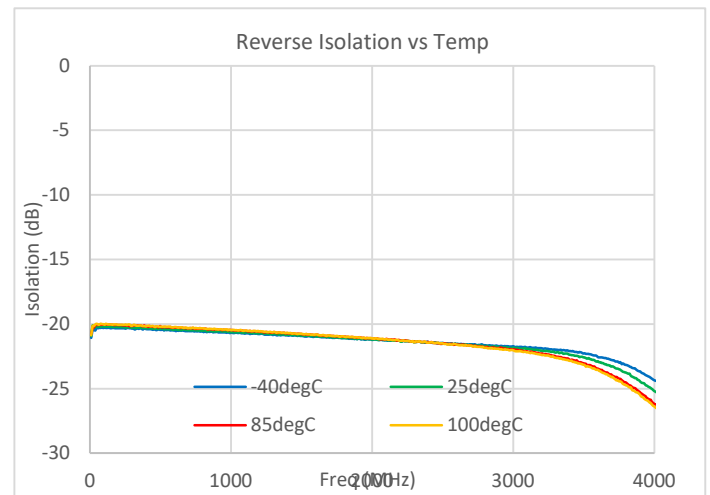
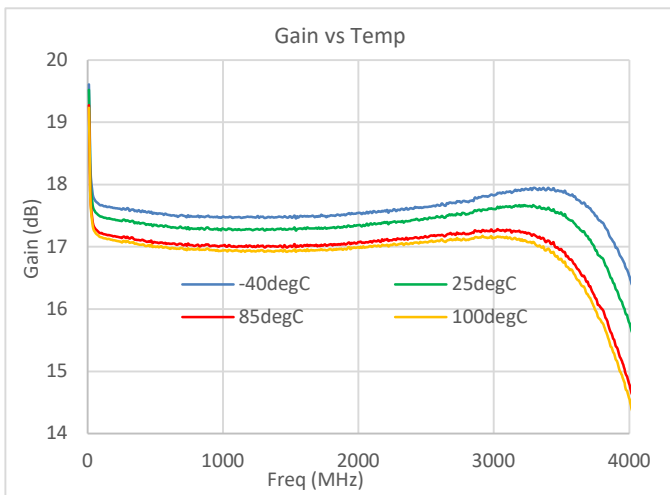
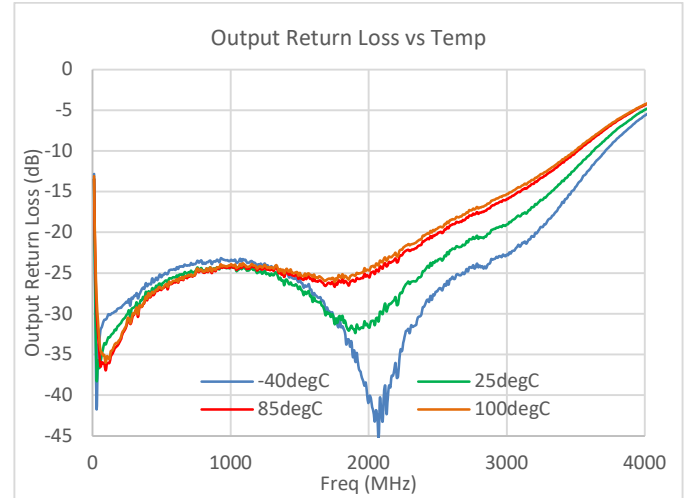
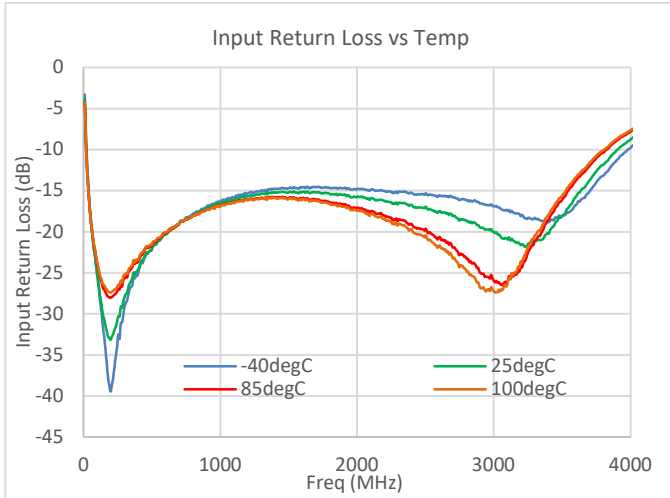
Board Dimension: 0.810" x 1.450"

| Layer | Name | Material | Thickness | Constant |
|-------|----------------|---------------|-----------|----------|
| 1 | Top Overlay | | | |
| 2 | Top Solder | Solder Resist | 0.40mil | 3.5 |
| 3 | Top Layer | Copper | 1.40mil | |
| 4 | Dielectric1 | Rogers 4350B | 10.00mil | 3.66 |
| 5 | Signal Layer 1 | Copper | 1.40mil | |
| 6 | Dielectric 3 | Rogers 4450F | 42.00mil | 3.52 |
| 7 | Signal Layer 2 | Copper | 1.40mil | |
| 8 | Dielectric 2 | Rogers 4350B | 10.00mil | 3.66 |
| 9 | Bottom Layer | Copper | 1.40mil | |
| 10 | Bottom Solder | Solder Resist | 0.40mil | 3.5 |
| 11 | Bottom Overlay | | | |

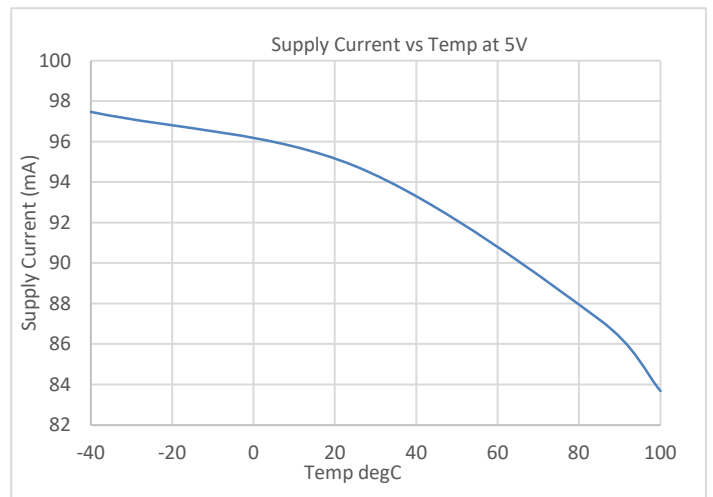
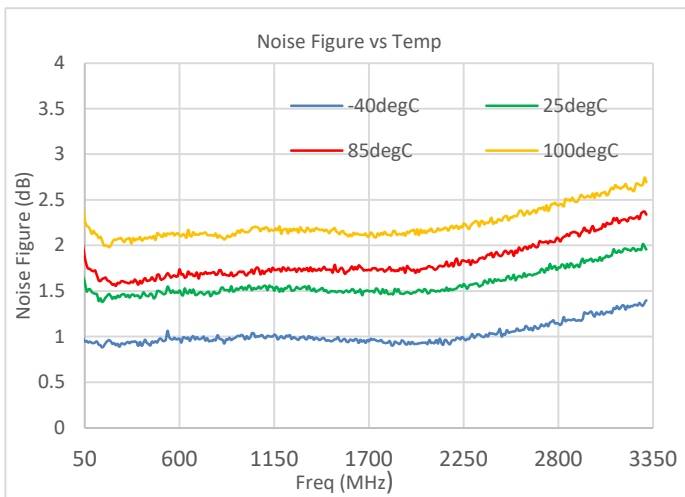
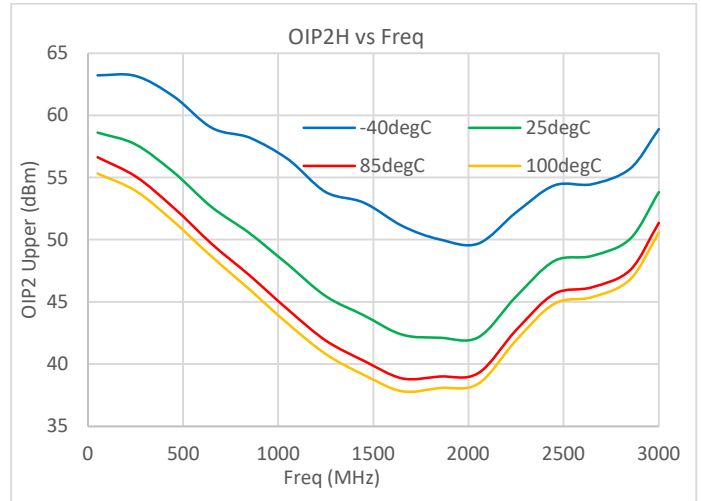
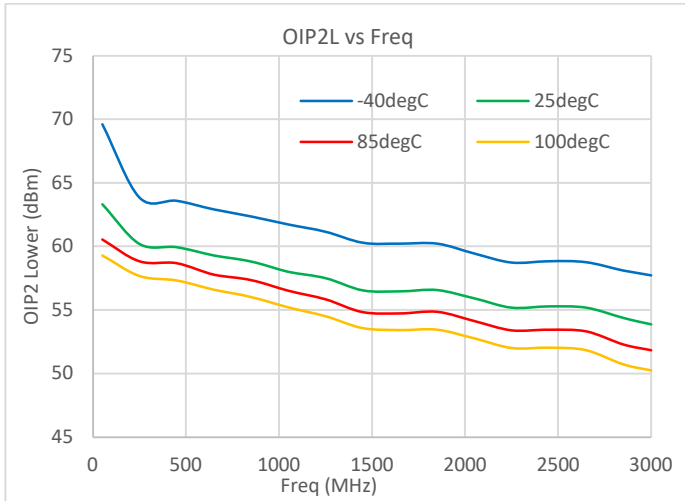
Total Thickness: 62 mil +/-10%



Performance Data at 5 V



Performance Data at 5 V (cont'd)



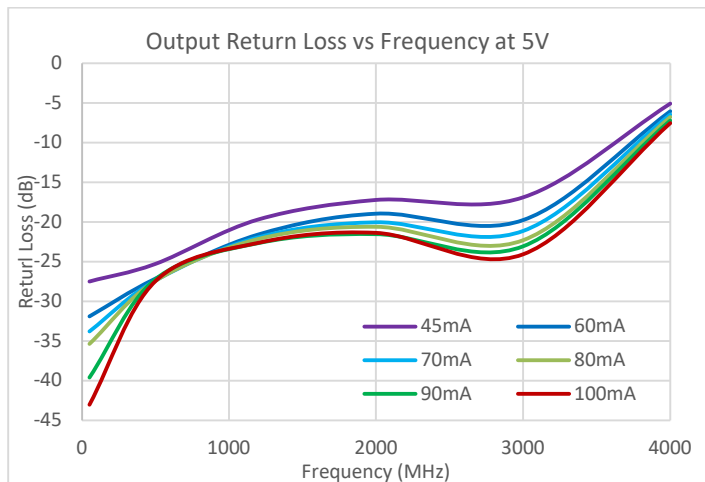
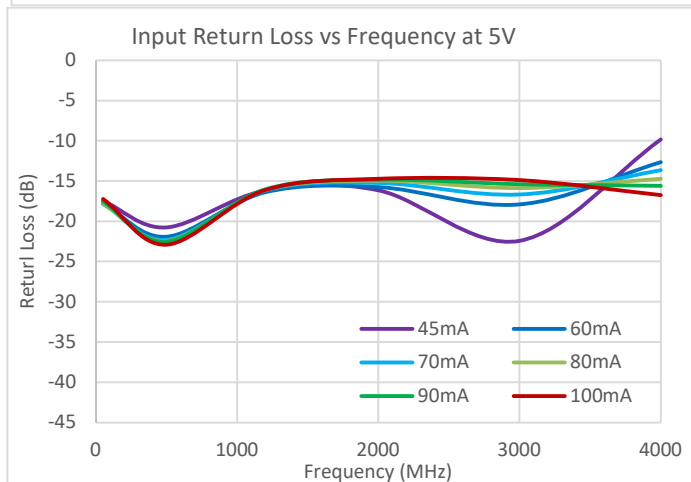
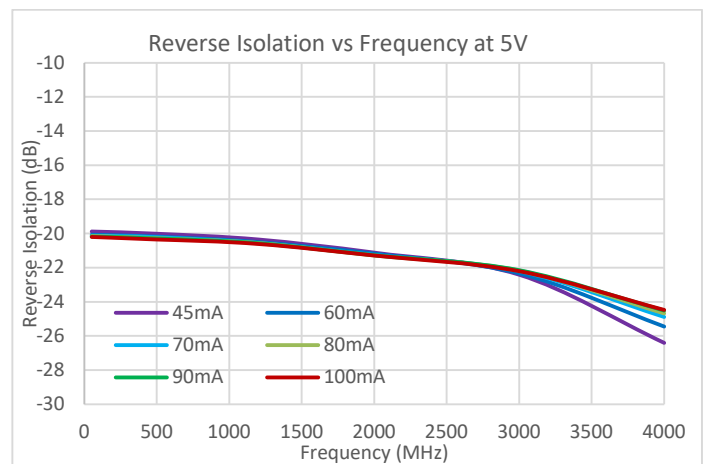
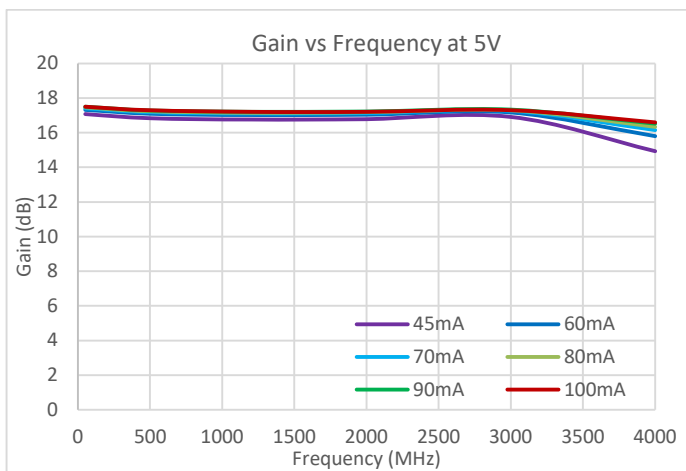
Notes:

1. $V_{DD} = +5V$, 50 Ω system
2. OIP3: +5 dBm / tone output, 5MHz spacing
3. OIP2: 5 dBm / tone output, 53MHz spacing

Additional Applications – Bias Resistor Options

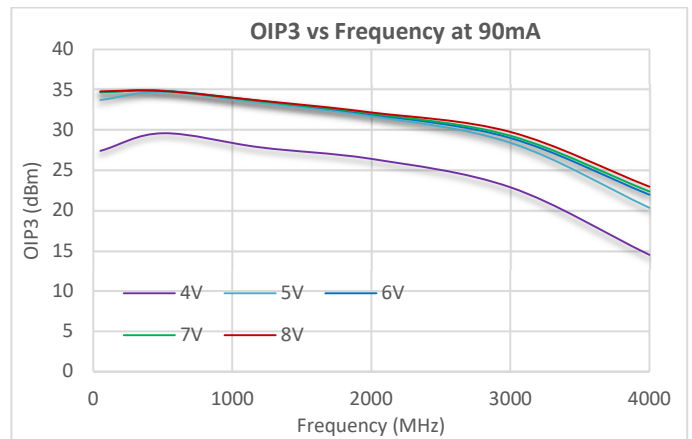
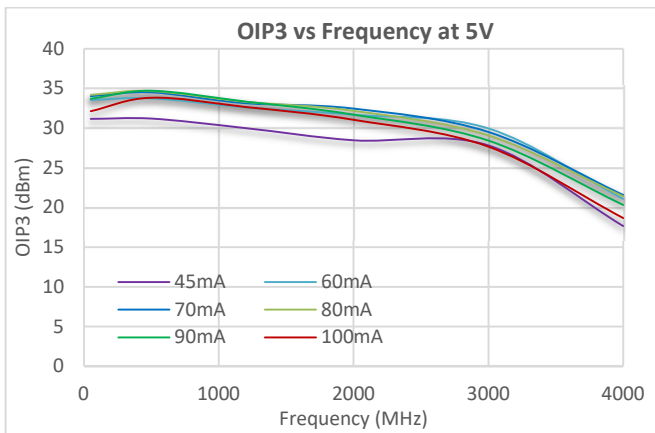
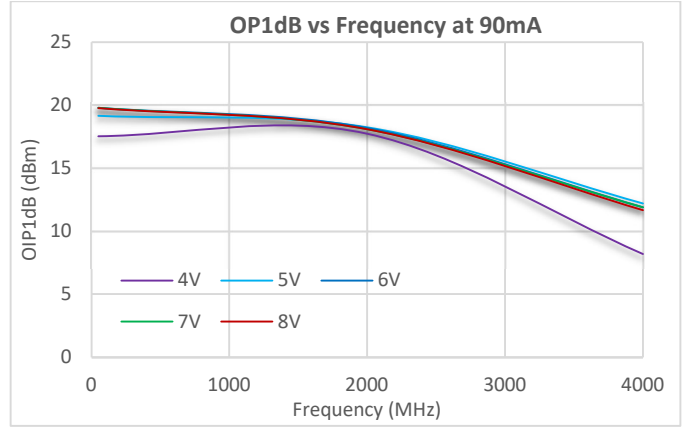
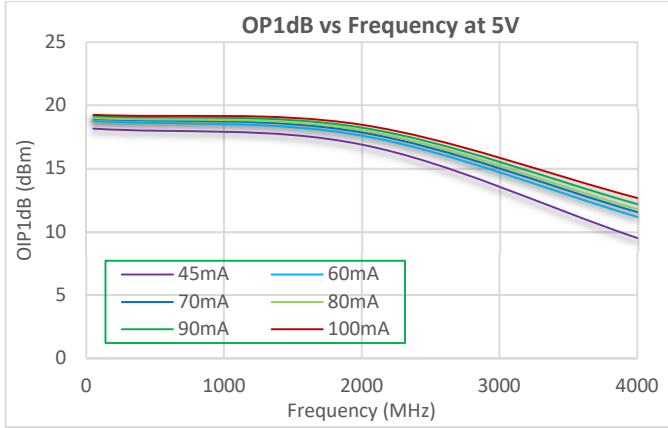
Pullup or pulldown resistors may be used to change the bias current (IDD) for a given bias voltage (VDD). Refer to the EVB schematic on Page 3. IDD must not exceed 120mA and the junction temperature can not exceed 150 °C at the maximum ambient operating temperature. Note that for some cases, return loss may need to be reoptimized by adjusting L1, L2, C7 and C6.

| IDD (mA) | 4V | | 5V | | 6V | | 7V | | 8V | |
|----------|--------|--------|--------|-------|-----|-------|-----|-------|-----|-------|
| | R1 | R2 | R1 | R2 | R1 | R2 | R1 | R2 | R1 | R2 |
| 100 | 121.0K | DNP | 390.0K | DNP | DNP | 100K | DNP | 36.5K | DNP | 24.3K |
| 90 | 220.0K | DNP | DNP | DNP | DNP | 47.0K | DNP | 24.3K | DNP | 16.9K |
| 80 | 590.0K | DNP | DNP | 60.4K | DNP | 28.0K | DNP | 18.2K | DNP | 13.7K |
| 70 | DNP | 220.0K | DNP | 40.2K | DNP | 22.0K | DNP | 15.0K | DNP | 11.0K |
| 60 | DNP | 68.0K | DNP | 28.0K | DNP | 16.2K | DNP | 12.0K | DNP | 9.90K |
| 45 | DNP | 27.4K | DNP | 16.9K | DNP | 11.0K | DNP | 8.66K | DNP | 6.98K |



Notes:
 (1) V_{DD} = +5V, 50 Ω system

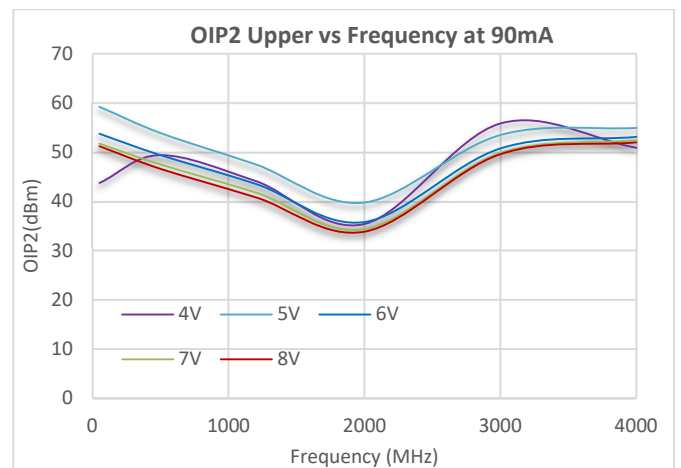
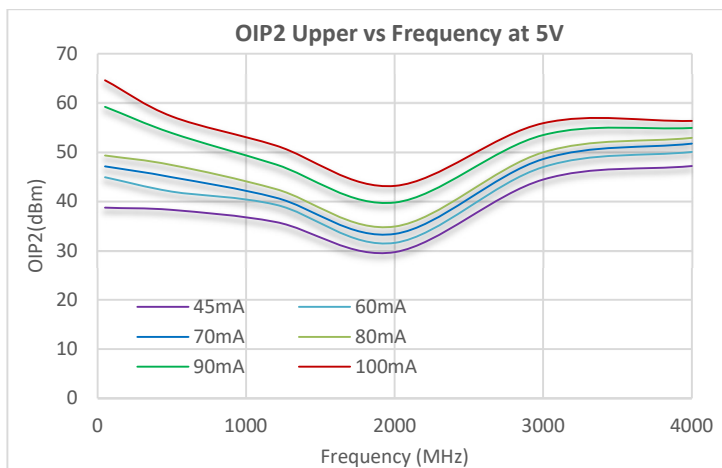
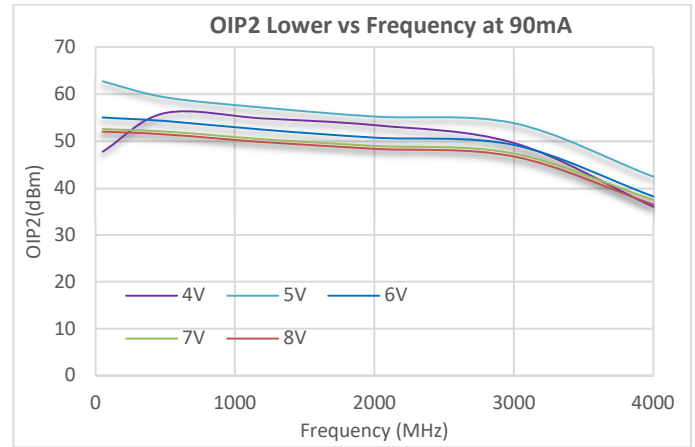
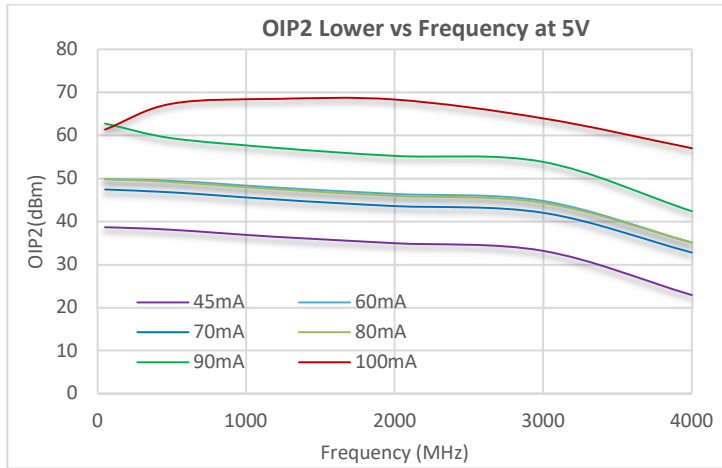
Additional Applications, cont'd – Bias Resistor Options



Notes:

- (1) $V_{DD} = +5V$, 50 Ω system
- (2) OIP3: +5 dBm / tone output, 5MHz spacing

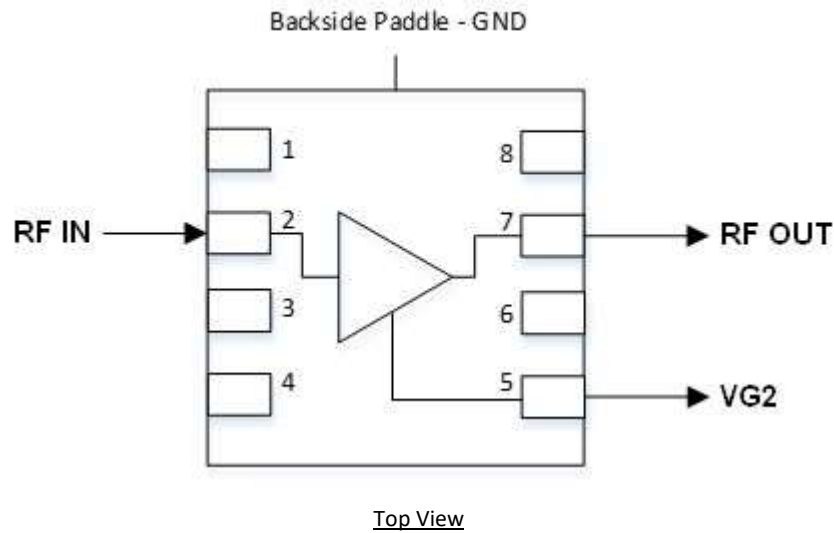
Additional Applications, cont'd – Bias Resistor Options



Notes:

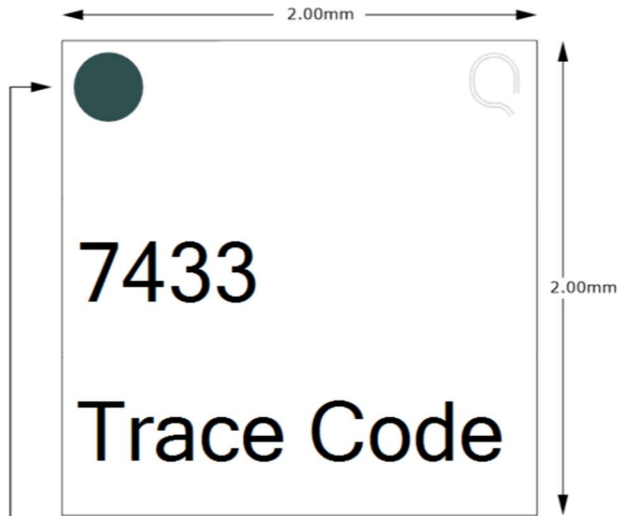
- (1) $V_{DD} = +5V$, 50 Ω system
- (2) OIP2: +5 dBm / tone output, 53MHz spacing

Pin Configuration and Description



| Pin Number | Label | Description |
|-----------------|--------------|--|
| 2 | RF IN | RF Input, DC blocking capacitor required |
| 1,3,4,6,8 | GND | Internally Not Connected |
| 7 | RF OUT / VDD | RF Output – VDD bias Ferrite Bead required |
| 5 | VG2 | Gate Voltage adjust. Leave as no connect. |
| Backside Paddle | GND | Ground. Use recommended via pattern to minimize inductance and thermal resistance. See PCB Mounting Pattern for suggested footprint. |

Package Marking Dimensions

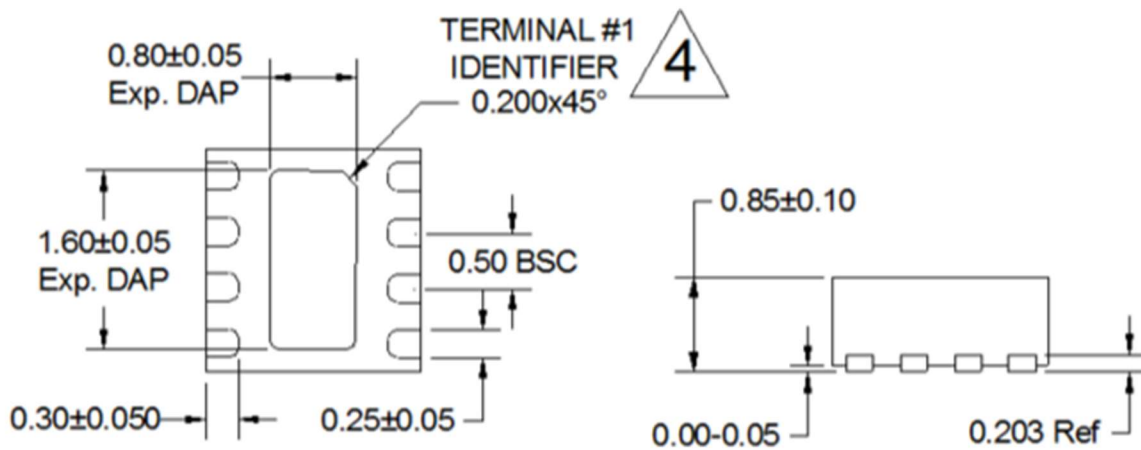


Pin 1 Indicator

Qorvo Logo - Use Q5D

Trace Code to be assigned by SubCon

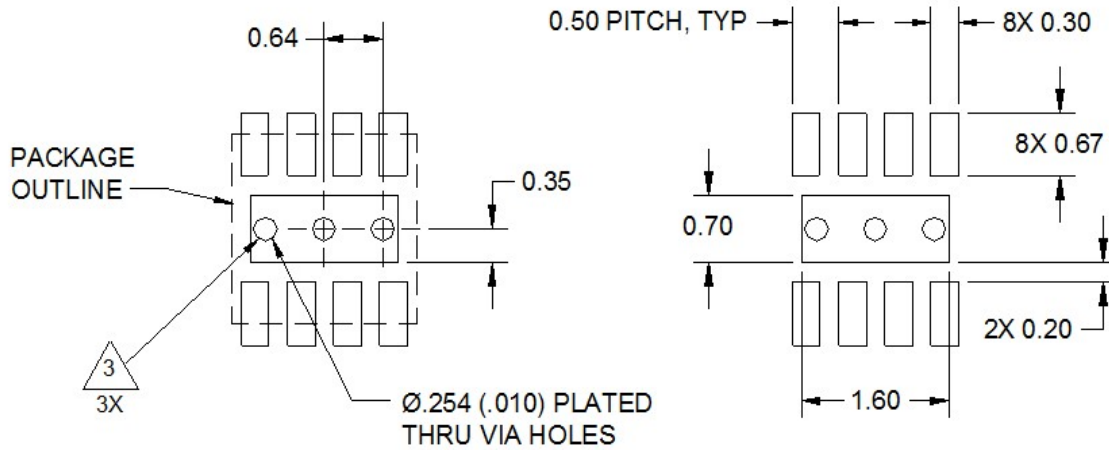
Package Outline



Notes:

1. All dimensions in millimeters. Angles are in degrees.
2. Except where noted, this part outline conforms to JEDEC standard MO-220, Isse E (Variation VGGC) for thermally enhanced Plastic very thin fine pitch dual flat no lead package (DFN)
3. Dimension and tolerance formats conform to ASME Y14.4M-1994.
4. The terminal #1 identifier and terminal numbering conforms to JESD 95-1 SPP-012.

Recommended Mounting Pattern



Notes:

1. All dimensions are in millimeters (inches). Angles are in degrees.
2. Use 1 oz copper minimum for top and bottom layer.
3. Via holes are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm diameter bit for drilling via holes and a final plated thru diameter of 0.25mm.
4. All dimensions are in millimeters (inches). Angles are in degrees.