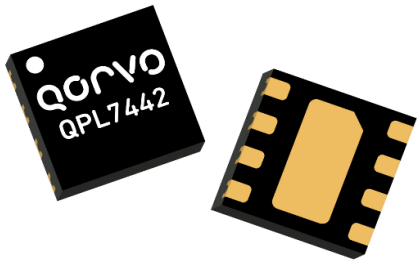
QPL7442

50 Ω 20 dB MMIC Gain Block (50 – 4000 MHz)

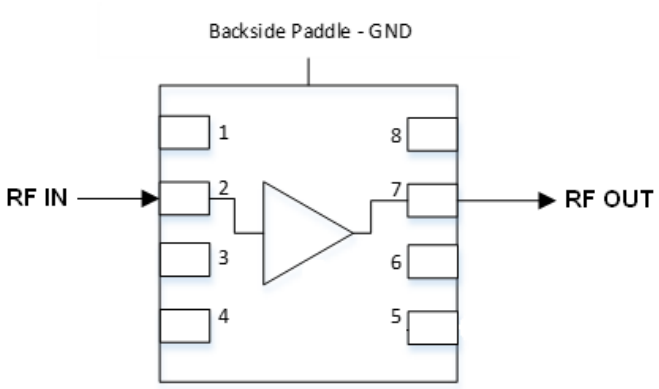
Product Overview

The QPL7442 is a low noise, high gain single ended MMIC RF amplifier, with 20 dB of flat gain over the entire 50MHz to 4000MHz bandwidth. This IC is designed to support Cable, Satellite and Terrestrial TV applications, Home Gateways, and Cable Modems. The QPL7442 is powered by a single 5 V supply and packaged in a 2 x 2 8–pin DFN.



2.0 x 2.0mm 8-lead DFN

Functional Block Diagram



Top View

Key Features

- 50 MHz to 4000 MHz Operation
- Low Power Consumption: 5 V, 85 mA
- Gain: 20 dB over the entire BW
- OP1dB: +20 dBm
- Low Noise Figure: 1.2 dB @ 1.2GHz
  1.5 dB @ 3.25GHz
- High Linearity OIP3: +33.7 dBm @ 1.2GHz
  +31.1 dBm @ 3.25GHz
- Adjustable Bias Using External Resistors

Applications

- Cable, Terrestrial, and Satellite LNA
- CATV Amplifiers
- Optical Node
- Cable Modem and Set Top Box
- Single Ended Gain Block

Ordering Information

Part Number	Description
QPL7442SB	Sample bag with 5 pieces
QPL7442SR	7" Reel with 100 pieces
QPL7442TR7	7" Reel with 2500 pieces
QPL7442EVB-01	PCBA

Absolute Maximum Ratings

Parameter	Rating
Supply Voltage (V_{DD})	+10 V
Supply Current (I_{DD})	120 mA
Maximum Input Level	20 dBm
Operating Temperature Range	-40 to +100 °C
Storage Temperature Range	−65 to +150 °C
Maximum Junction Temperature	+150 °C

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

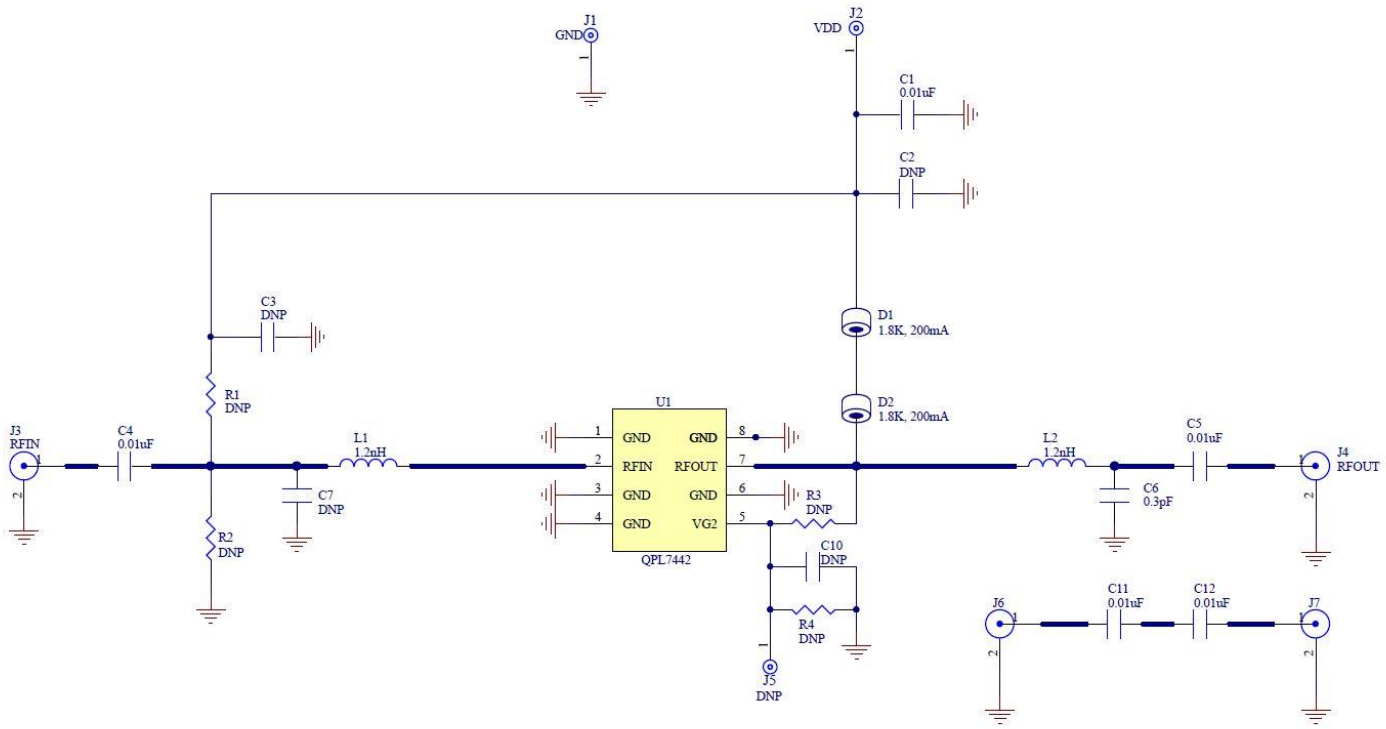
Electrical Specifications

Parameter	Condition (1)	Min	Typ	Max	Unit
Supply Voltage (V_{DD})			5		V
Supply Current (I_{DD})			90		mA
Frequency Range		50		4000	MHz
Gain			20		dB
Reverse Isolation			23		dB
Input Return Loss			14.8		dB
Output Return Loss			15.8		dB
Noise Figure			1.5		dB
OIP2L(2)	0.05 – 1.2GHz		48.2		dBm
	1.2 – 3.0GHz		48.0		dBm
	3.0 – 4.0GHz		46.4		dBm
OIP2H(2)	0.05 – 1.2GHz		40.6		dBm
	1.2 – 3.0GHz		32.2		dBm
	3.0 – 4.0GHz		38.1		dBm
OIP3(3)	0.05 – 1.2GHz		33.9		dBm
	1.2 – 3.0GHz		32.0		dBm
	3.0 – 4.0GHz		27.8		dBm
OP1dB	50 – 3000 MHz		20.8		dBm
	3.0 – 4.0GHz		19.3		dBm
Thermal Resistance	Θ_{JC} (Junction to Case)		62		˚C/W

Notes:

1. Typical performance at these conditions: Temp = +25 °C, V_{DD} = +5 V, 50 Ω system, Full band unless otherwise noted.
2. +5 dBm / tone output, 53 MHz Spacing.
3. +5 dBm / tone output, 5 MHz Spacing.

Evaluation Board Schematic



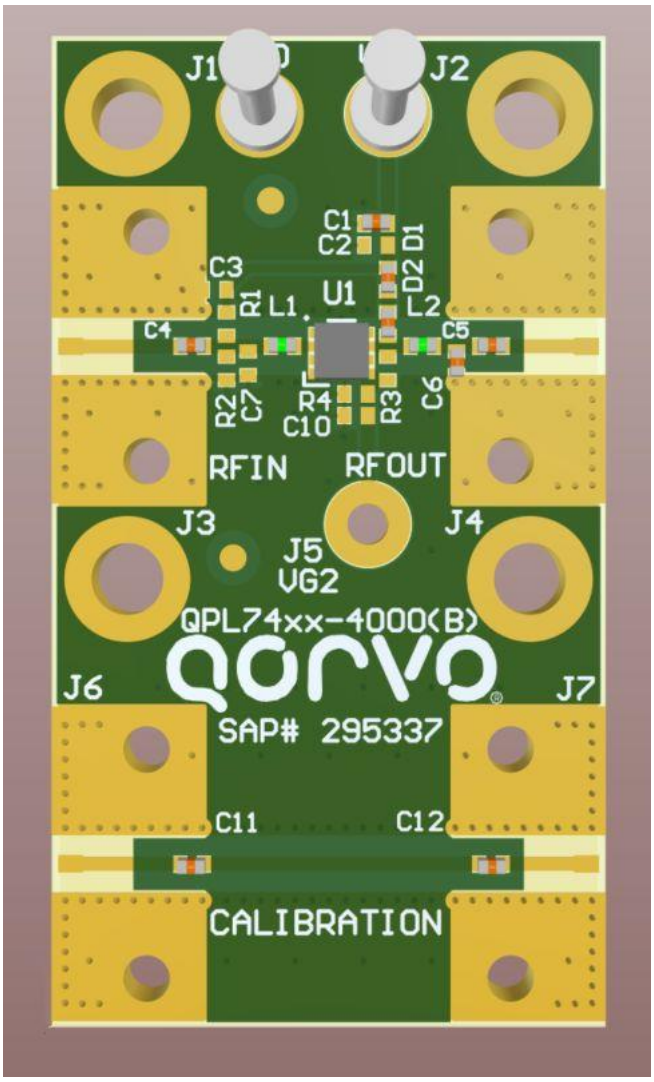
Notes:

1. L1, C7 tunes input return loss.
2. L2 , C6 tunes output return loss.
3. D1, D2 provide DC bias path with RF isolation from the RF output path.
4. C4, C5 provides DC blocking.
5. R1, R2 and C3 are pullup/pulldown options that may be added from the input to VDD or to ground to increase linearity or shed power, trading off degraded noise figure and return loss. Device current can only be adjusted through R1 and R2.
6. Pin5 is an internal gate voltage and may be left floating.

Evaluation Board Bill of Materials

Designator	Description	Manufacturer	Part Number
PCB	QPL7442–4001 EVB	TTM Technology INC	QPL7442-4001(A)
U1	QPL7442	Qorvo	QPL7442SB
D1, D2	FER, BEAD, 1.8 KΩ, 5 %, 200 mA, 0402	TDK	MMZ1005A182ET000
C6	CAP, 0.3 pF, +/-0.05 pF, 25 V, 0402	AVX Asia	04023J0R3ABWTR
C1, C4, C5	CAP, 0.01 uF, 10 %, 50 V, X8L, 0402	Murata Electronics	GCM155L81E103KA37D
L1, L2	IND, 1.2 nH, +/-0.1 nH, 0402	Murata Electronics	LQG15HS1N2B02D
J3, J4, J6, J7	862000-422 CONN, 0.062 RF SMA F, 50 Ω	Cinch Connectivity Solutions, Inc	142-0701-851
J1, J2	862000-055 Solder Turret, 0.062	Mouser Electronics	2533-0-00-44-00-00-07-
C2, C3, C7, C10, C11, C12, J5, R1, R2, R3, R4	Not Populated		

Evaluation Board Assembly Drawing



EVB PCB Material and Stack-up

Board Material: Rogers 4350B, 4450F, 62mil total thickness.

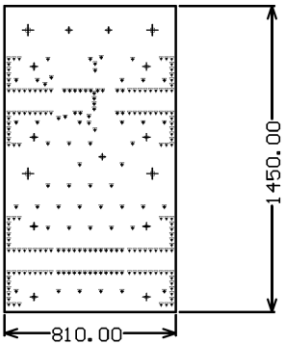
ε_r = 3.66

Plating: 1.0 oz Copper

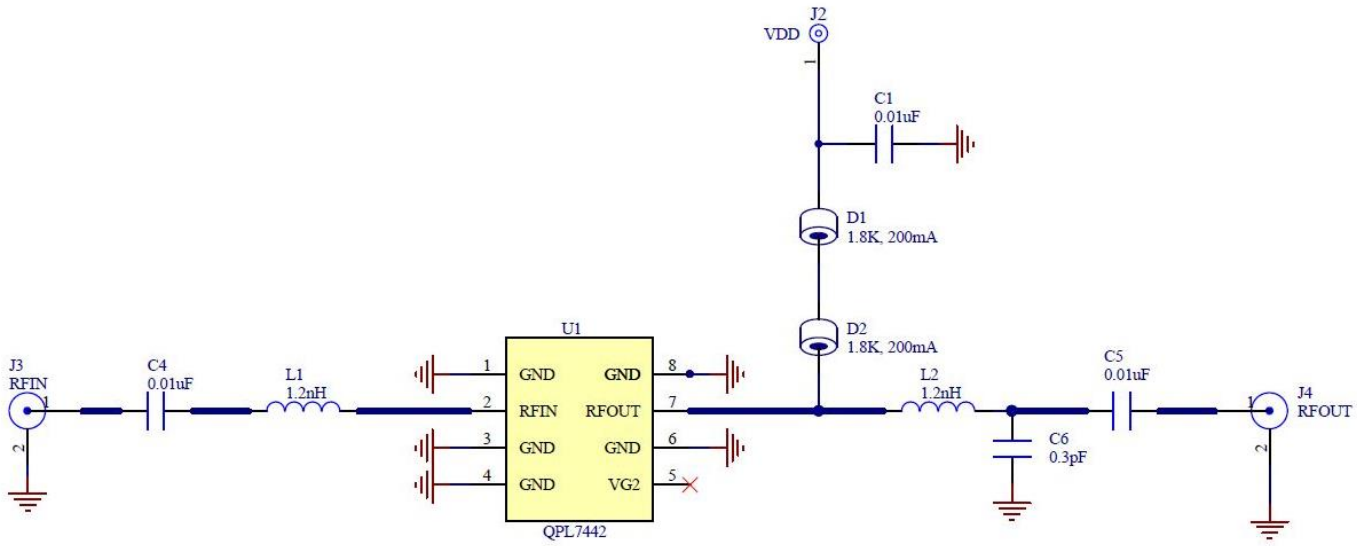
Board Dimension: 0.810" x 1.450"

Layer	Name	Material	Thickness	Constant
1	Top Overlay			
2	Top Solder	Solder Resist	0.40mil	3.5
3	Top Layer	Copper	1.40mil	
4	Dielectric1	Rogers 4350B	10.00mil	3.66
5	Signal Layer 1	Copper	1.40mil	
6	Dielectric 3	Rogers 4450F	42.00mil	3.52
7	Signal Layer 2	Copper	1.40mil	
8	Dielectric 2	Rogers 4350B	10.00mil	3.66
9	Bottom Layer	Copper	1.40mil	
10	Bottom Solder	Solder Resist	0.40mil	3.5
11	Bottom Overlay			

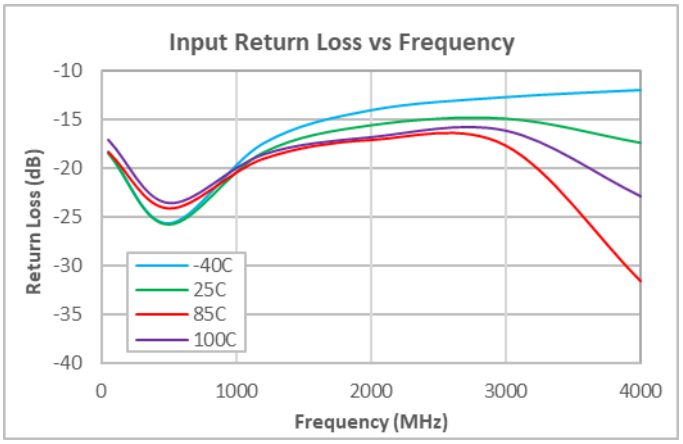
Total Thickness: 62 mil +/-10%

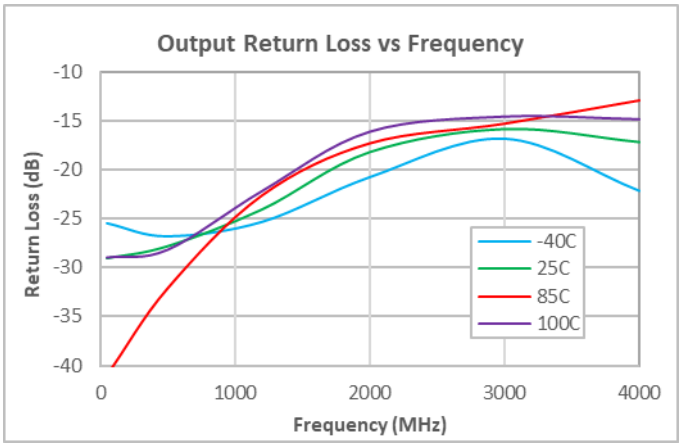


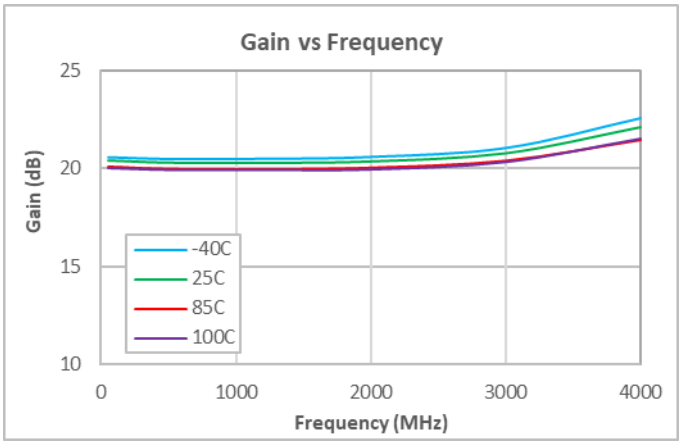
Typical Application Schematic

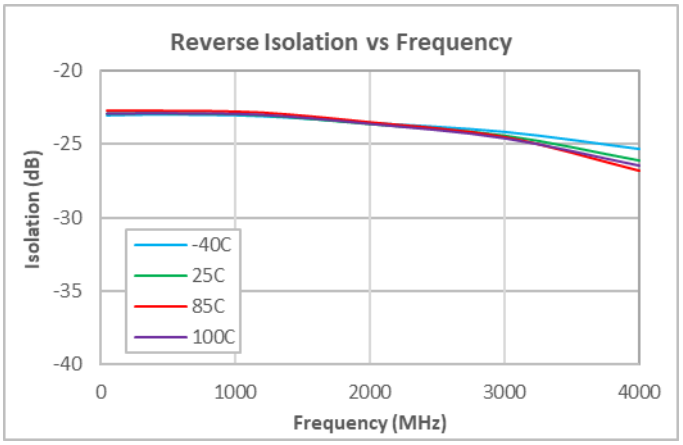


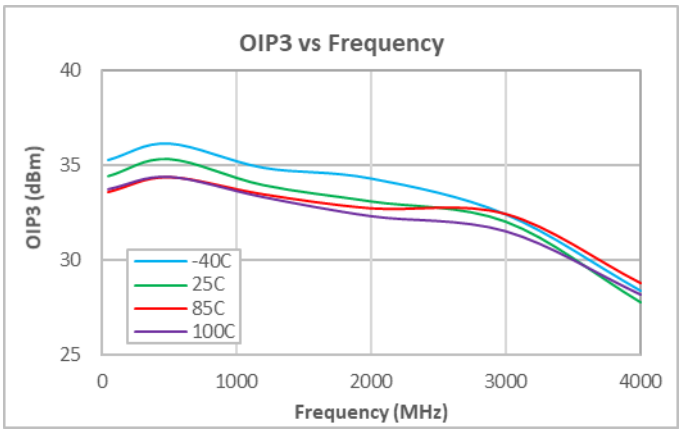
Performance Data

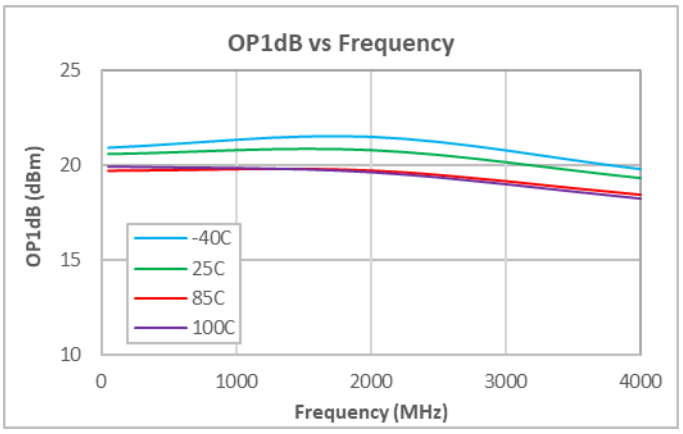






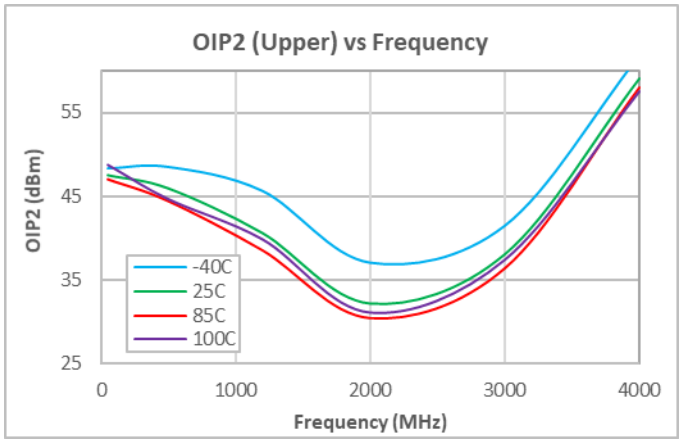


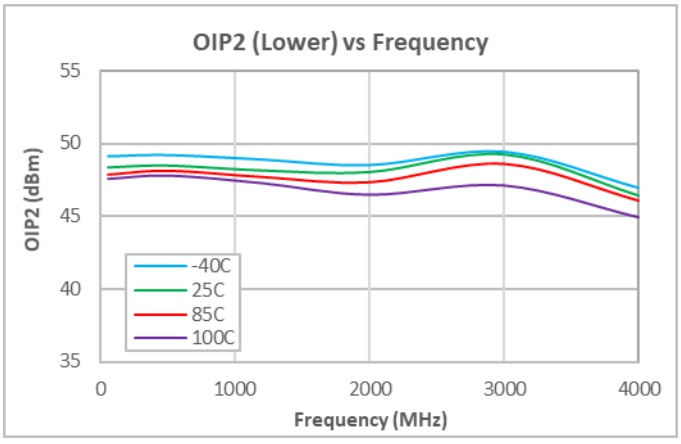


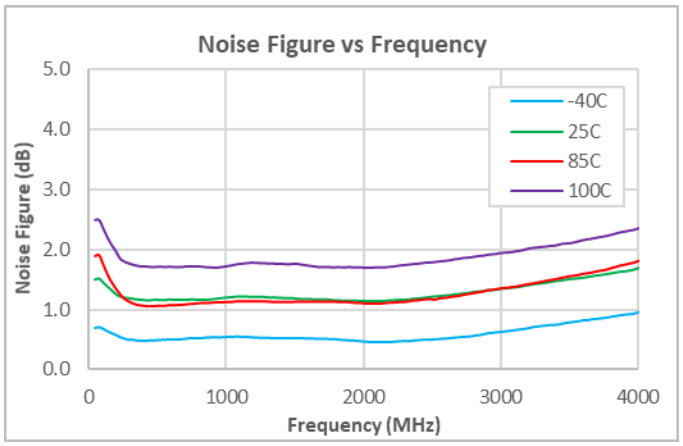


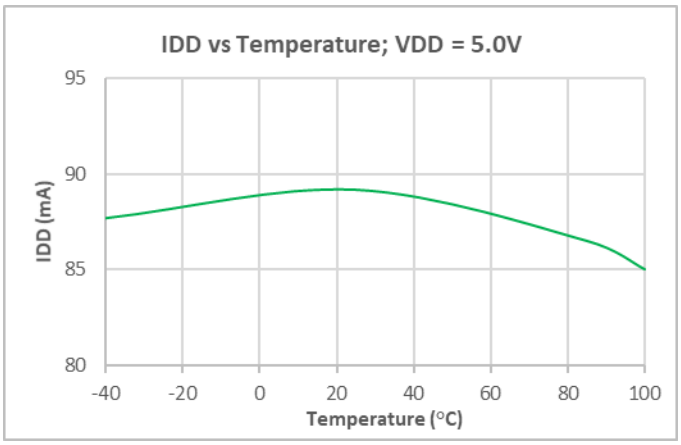
Notes:
(1) V_{DD} = +5 V, 50 Ω system
(2) OIP3: +5 dBm / tone output, 5MHz spacing

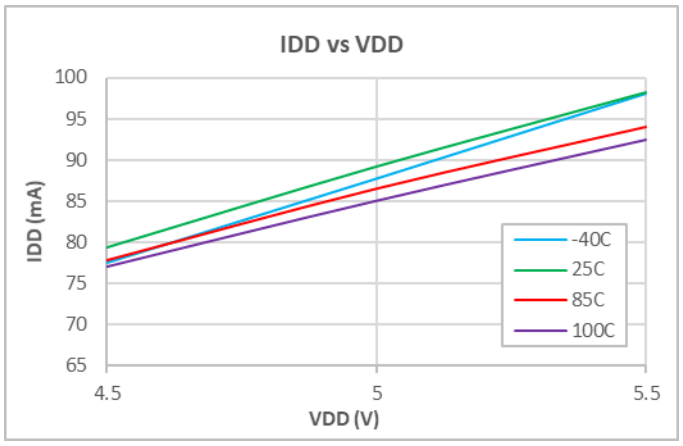
Performance Data (cont'd)

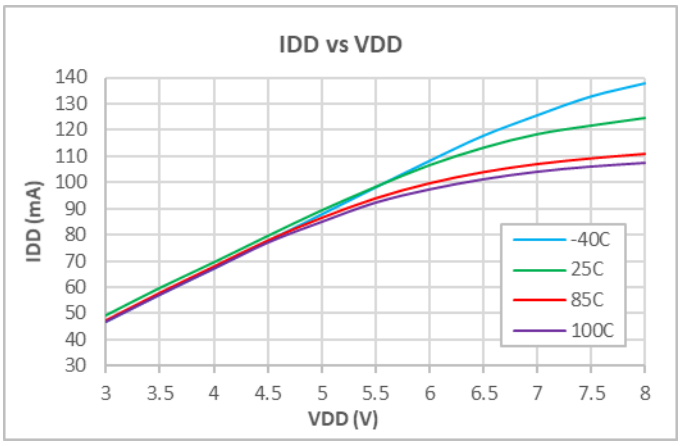












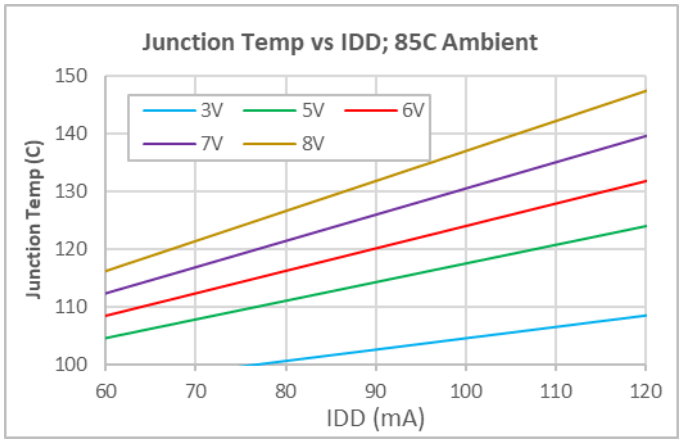
Notes:

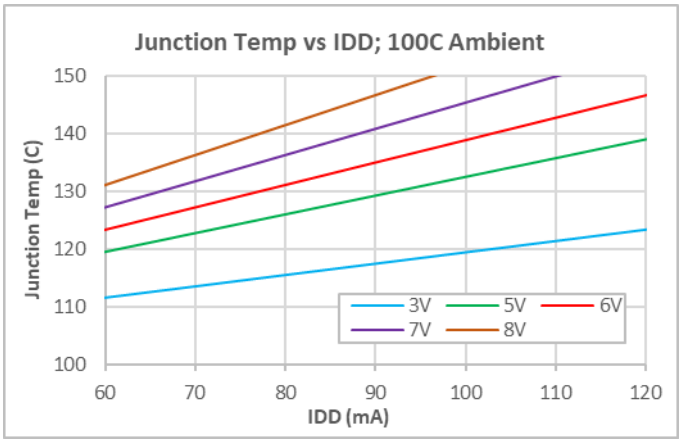
(1) OIP2: 5 dBm / tone output, 53MHz spacing

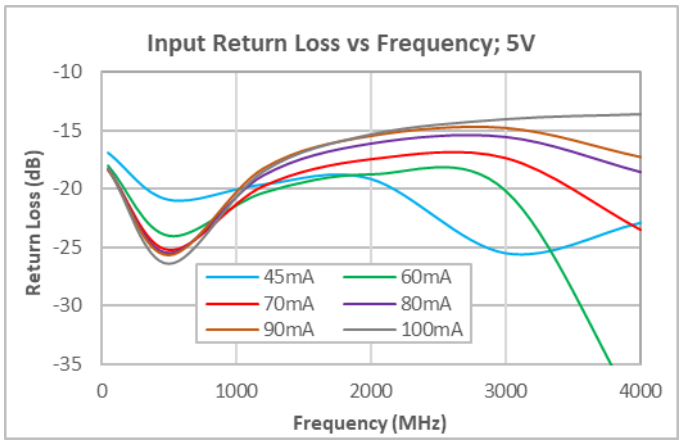
Additional Applications – Bias Resistor Options

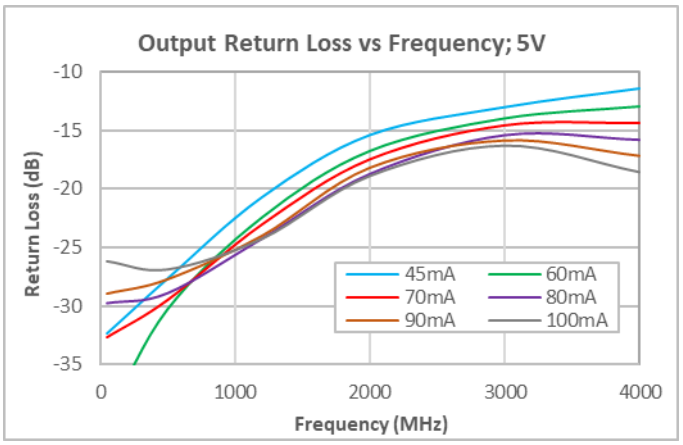
Pullup or pulldown resistors may be used to change the bias current (IDD) for a given bias voltage (VDD). Refer to the EVB schematic on Page 3. IDD must not exceed 120mA and the junction temperature can not exceed 150 °C at the maximum ambient operating temperature.Note that for some cases, return loss may need to be reoptimized by adjusting L1, L2, C7 and C6.

IDD (mA)	3V		5V		6V		7V		8V	
	R1	R2	R1	R2	R1	R2	R1	R2	R1	R2
100	31.6K	DNP	280.0K	DNP	DNP	97.6K	DNP	25.5K	DNP	14.0K
90	41.2K	DNP	DNP	DNP	DNP	33.2K	DNP	15.4K	DNP	10.5K
80	56.2K	DNP	DNP	60.1K	DNP	20.0K	DNP	11.5K	DNP	7.87K
70	82.0K	DNP	DNP	28.0K	DNP	13.7K	DNP	9.09K	DNP	8.06K
60	150.0K	DNP	DNP	17.4K	DNP	10.0K	DNP	6.98K	DNP	5.49K
45	DNP	DNP	DNP	10.0K	DNP	6.98K	DNP	5.49K	N/A	N/A



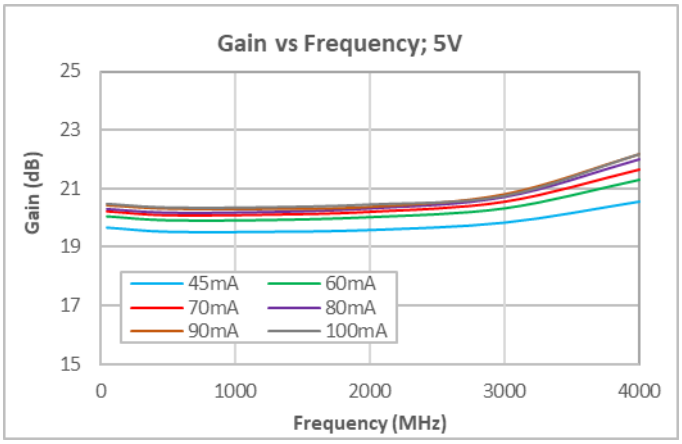


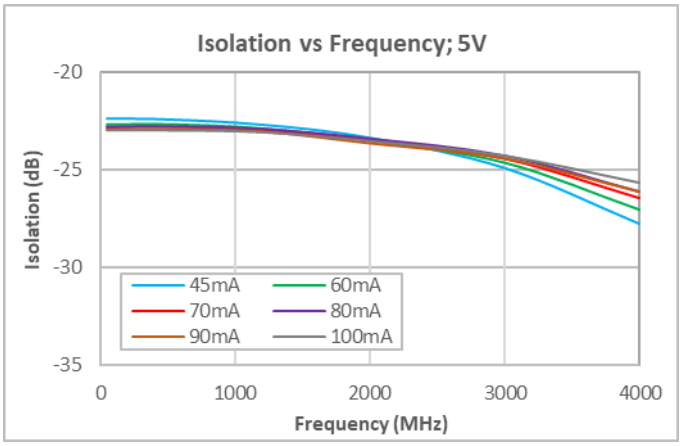


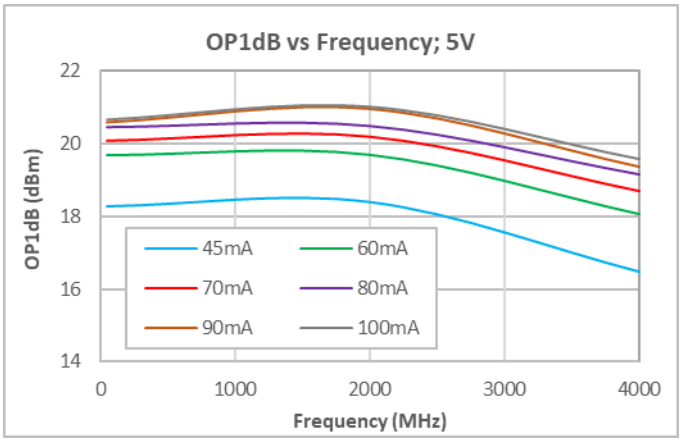


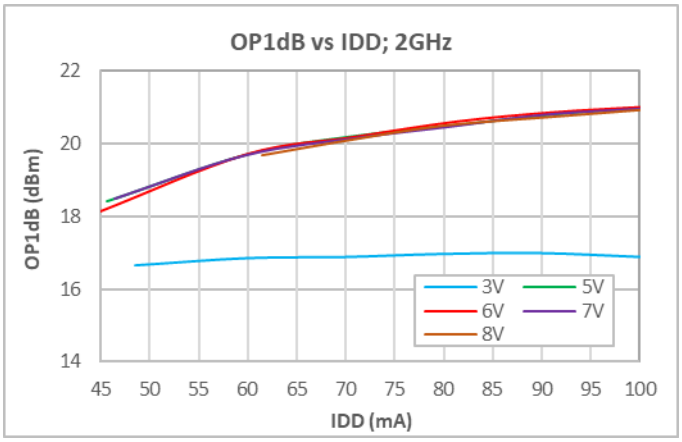
Notes:
(1) V_{DD} = +5 V, 50 Ω system

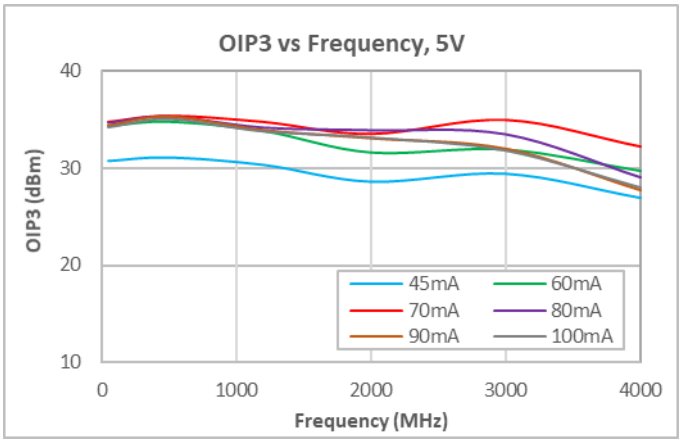
Additional Applications, cont'd – Bias Resistor Options

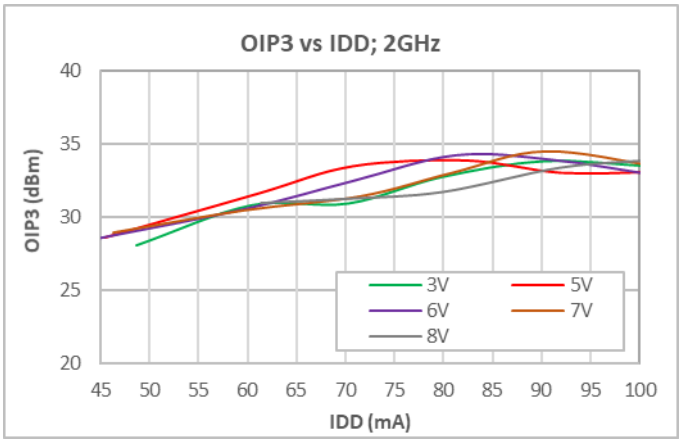






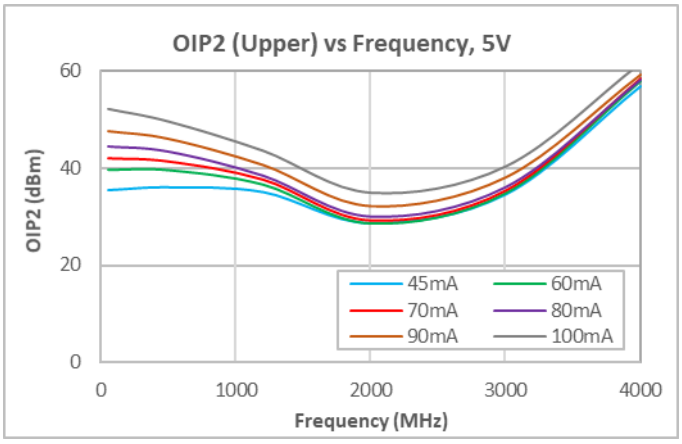


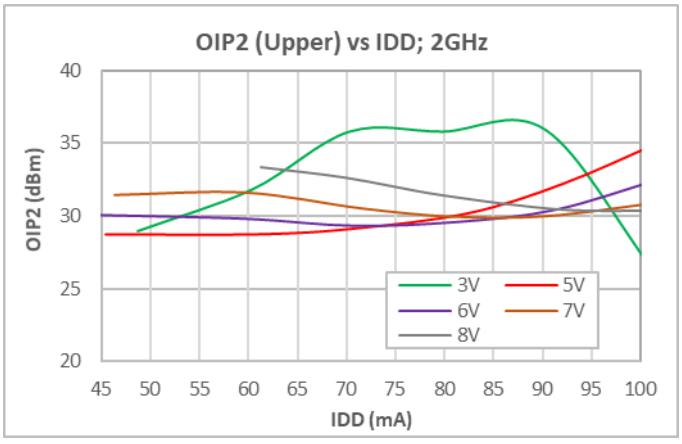


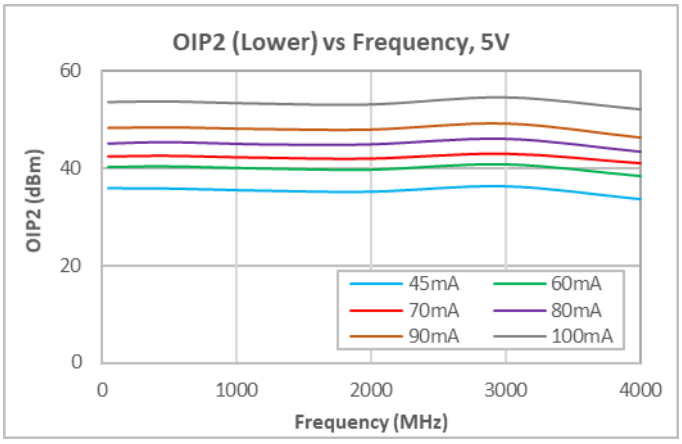


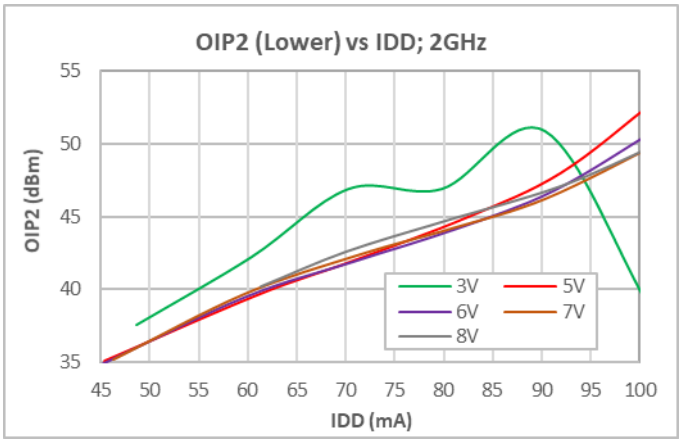
Notes:
(1) V_{DD} = +5 V, 50 Ω system
(2) OIP3: +5 dBm / tone output, 5MHz spacing

Additional Applications, cont'd – Bias Resistor Options



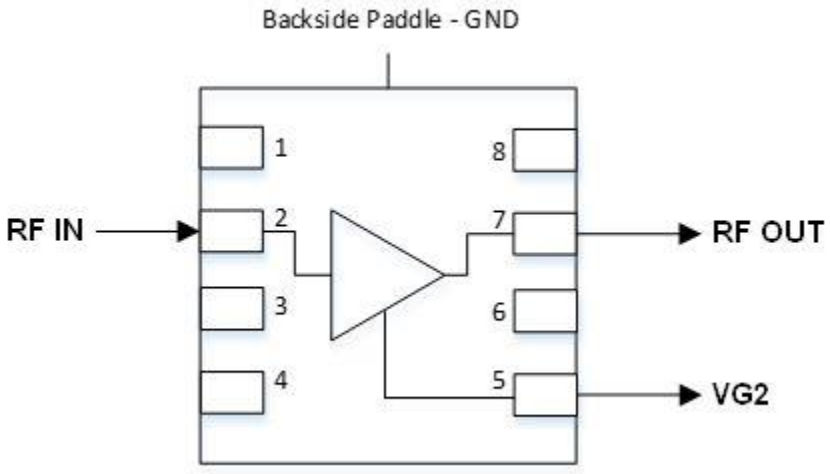






Notes:
(1) V_{DD} = +5 V, 50 Ω system
(2) OIP2: +5 dBm / tone output, 53MHz spacing

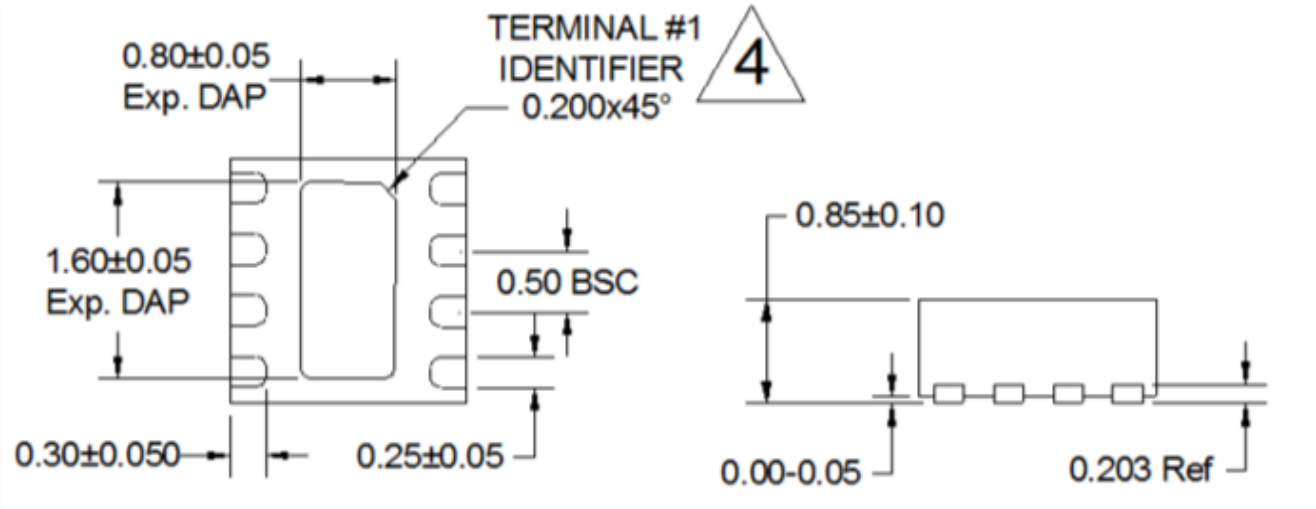
Pin Configuration and Description



Top View

Pin Number	Label	Description
2	RF IN	RF Input, DC blocking capacitor required
1,3,4,6,8	GND	Internally Not Connected
7	RF OUT / VDD	RF Output – VDD bias
5	VG2	Gate Voltage bias. Leave as no connect.
Backside Paddle	GND	Ground. Use recommended via pattern to minimize inductance and thermal resistance. See PCB Mounting Pattern for suggested footprint.

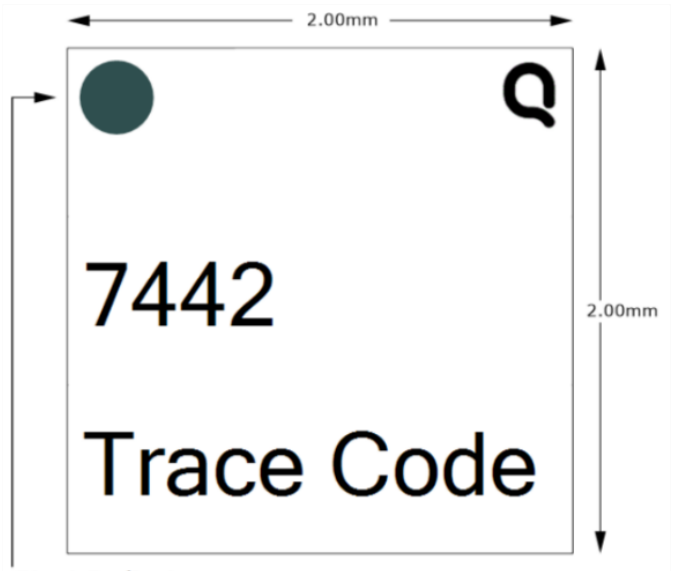
Package Outline



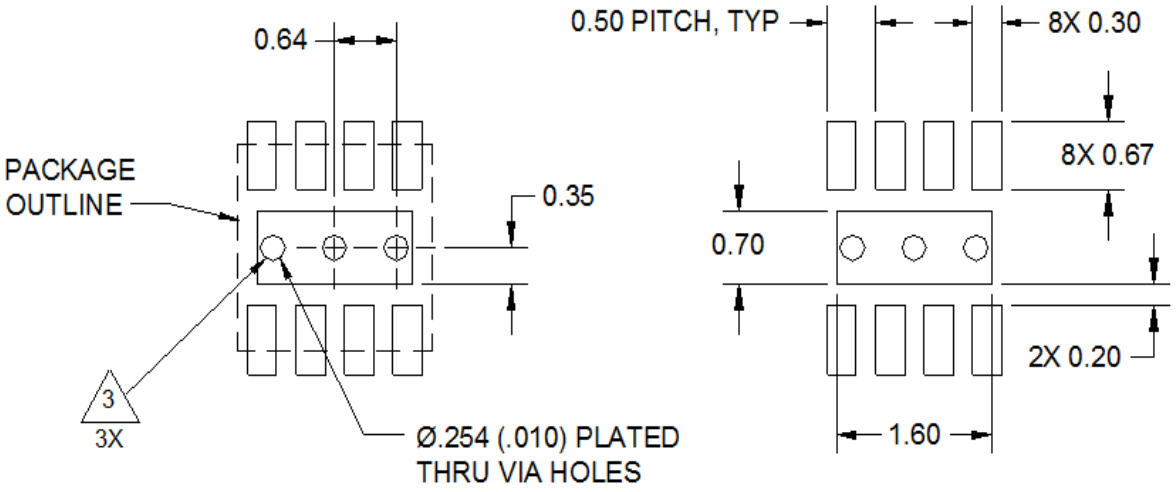
Notes:

1. All dimensions in millimeters. Angles are in degrees.
2. Except where noted, this part outline confroms to JEDEC standard MO-220, Isse E (Variation VGGC) for thermally enhanced Plastic very thin fine pitch dual flat no lead package (DFN)
3. Dimension and tolerance formats conform to ASME Y14.4M-1994.
4. The termianl #1 identifier and termianl numbering conforms to JESD 95-1 SPP-012.

Package Marking Dimensions



Recommended Mounting Pattern



Notes:

1. All dimensions are in millimeters (inches). Angles are in degrees.
2. Use 1 oz copper minimum for top and bottom layer.
3. Via holes are required under the backside paddle of this device for proper RF / DC grounding and thermal dissipation. We recommend a 0.35 mm diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm.
4. All dimensions are in millimeters (inches). Angles are in degrees.