QPL8832

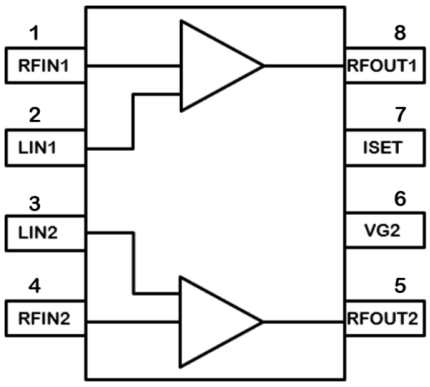
75 Ω 19 dB CATV Amplifier (5 – 1218 MHz)

Product Overview

The QPL8832 is an ultra-linear GaAs pHEMT 75-Ohm RF balanced amplifier IC with 5 – 1218 MHz operating bandwidth, featuring high linearity, high gain and low noise for use as a post amplifier in optical receivers or as a low noise balanced preamp. This IC uses a 5 V supply for applications requiring lower power dissipation or can operate from 8V supplies when higher output is needed. Due to its wide operational bandwidth, the QPL8832 can be used as a downstream amp in DOCSIS 3.1 as well as an upstream amplifier for DOCSIS 3.1 or DOCSIS 4.0 applications.

8-Pin SOIC Package

Functional Block Diagram



Key Features

- High Gain: 19dB at 1218 MHz
- 5 – 1218 MHz BW
- OIP3: +44 dBm, 50 – 1218 MHz
- OP1dB: +24 dBm, 50 – 1218 MHz
- Low Noise Figure: 3 dB, Full Band
- Excellent Composite Distortion
- pHEMT GaAs device technologies
- Compact Size: 8-pin SOIC
- Power Consumption:
  5 V, 280 mA (1.4 W)
  8V, 360mA (2.9W)

Ordering Information

Part Number	Description
QPL8832SB	Sample bag with 5 pieces
QPL8832SR	7" Reel with 100 pieces
QPL8832TR13	13" Reel with 2500 pieces
QPL8832PCK-01	50 – 1218 MHz 5V Evaluation Board with 5 pc sample bag
QPL8832EVB-02	5 – 700 MHz Evaluation Board, 5 V
QPL8832EVB-03	50 – 1218 MHz Evaluation Board, 8 V
QPL8832EVB-04	5 – 700 MHz Evaluation Board, 8 V

Applications

- DOCSIS 3.1 Systems
- Balanced Antenna Applications
- HFC Optical Nodes
- 75 Ω Amplifiers
- Upstream Amplifier for DOCSIS 3.1 and DOCSIS 4.0 Applications

Absolute Maximum Ratings

Parameter	Rating
Supply Voltage (V_{DD})	+10 V
Supply Current (I_{DD})	400 mA
Maximum Input Level (single tone)	+15 dBm
Operating Temperature Range (Bottom of Case)	−40 to +100 °C
Storage Temperature Range	−40 to +150 °C
Maximum Junction Temperature	+150 °C

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Electrical Specifications; 50 – 1218MHz, 5V

Parameter	Condition [1]	Min	Typ	Max	Unit
Supply Voltage (V_{DD})			5		V
Supply Current (I_{DD})			280		mA
Frequency Range		5		1218	MHz
Gain			19		dB
Gain Flatness			±0.5		dB
Input Return Loss			20		dB
Output Return Loss			18		dB
Noise Figure			2.9		dB
OIP2L	+13 dBm / tone, Δf = 50 MHz		70		dBm
OIP2H	+13 dBm / tone, Δf = 50 MHz		65		dBm
OIP3	+13 dBm / tone, Δf = 6 MHz		44.5		dBm
Output P1dB			24.8		dBm
MER	Vo = 64.8 dBmV Total Composite Output Power 54-1218 MHz 195Ch 256QAM, 0 dB Tilt, ITU-T J.83/B		45		dB
Thermal Resistance	Bottom of Case		13		˚C/W

Notes:

1. Typical performance at these conditions: Temp = +25 °C, V_{DD} = +5 V, 75 Ω system, Full band unless otherwise noted.

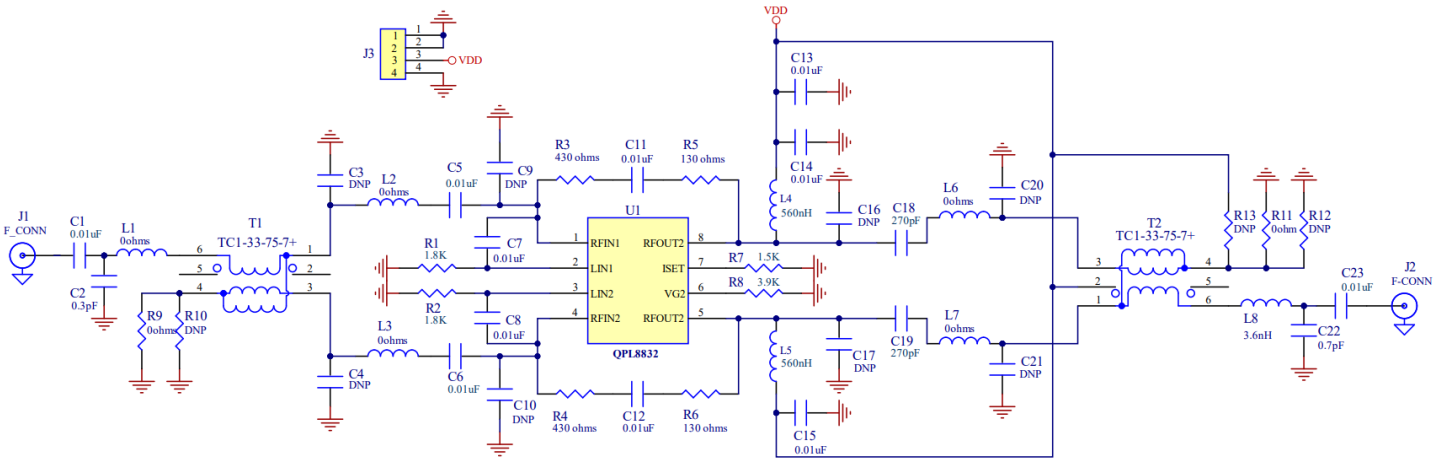
Electrical Specifications; 50 – 1218MHz, 8V

Parameter	Condition [1]	Min	Typ	Max	Unit
Supply Voltage (V_{DD})			8		V
Supply Current (I_{DD})			360		mA
Frequency Range		5		1218	MHz
Gain			18.8		dB
Gain Flatness			±0.5		dB
Input Return Loss			18		dB
Output Return Loss			20		dB
Noise Figure			3.0		dB
OIP2L	+13 dBm / tone, Δf = 50 MHz		69		dBm
OIP2H	+13 dBm / tone, Δf = 50 MHz		64		dBm
OIP3	+13 dBm / tone, Δf = 6 MHz		48		dBm
Output P1dB			29		dBm
MER	Vo = 68.4 dBmV Total Composite Output Power 54-1218 MHz 195Ch 256QAM, 0 dB Tilt, ITU-T J.83/B		45		dB
Thermal Resistance	Bottom of Case		13		˚C/W

Notes:

1. Typical performance at these conditions: Temp = +25 °C, V_{DD} = +8 V, 75 Ω system, Full band unless otherwise noted.

Evaluation Board Schematic; 50 – 1218 MHz, 5V



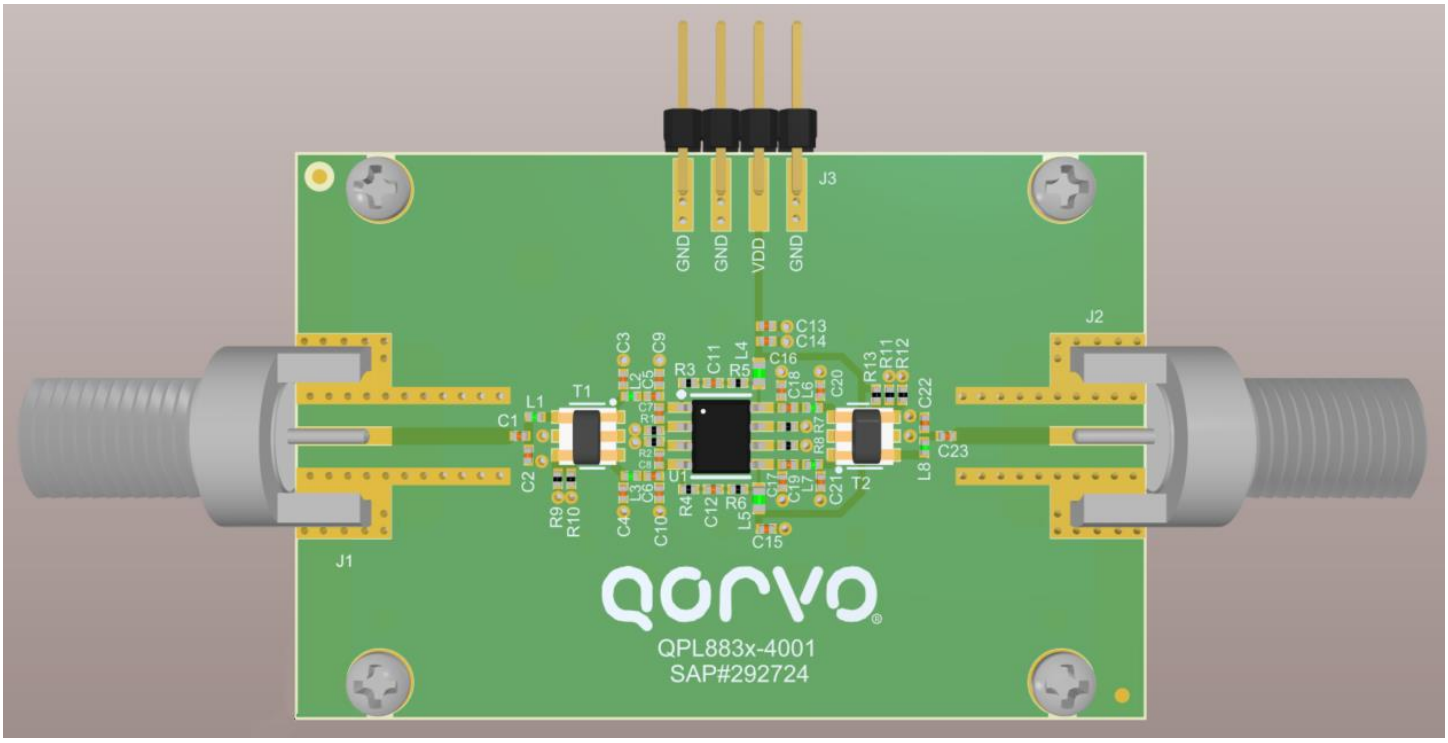
Bill of Material of Evaluation Board: 50 – 1218 MHz, 5V

Reference Designator	Description	Manufacturer	Part Number
U1	5 - 1218 MHz, 17 dB Push-Pull Amp	Qorvo	QPL8832SB
PCB	EVB PCB, QPL8832	Qorvo	QPL883x-4001
C2	CAP, 0.3pF, +/-0.05pF, 50V, HI-Q, 0402	Murata	GJM1555C1HR30WB01D
C22	CAP, 0.7pF, +/-0.1pF, 50V, HI-Q, 0402	Murata	GJM1555C1HR70BB01D
C1,C5,C6,C7,C8,C11,C12,C13,C14,C15,C23	CAP, 0.01uF, 10%, 50V, X7R, 0402	Murata	GCM155R71H103KA55D
C18, C19	CAP, 270pF, 5%, 50V, C0G, 0402	Murata	GCM1555C1H271JA16D
L1, L2, L3, L6, L7, R9, R11	RES, 0 OHM, 1/10W, 0402	Kamaya	RMC1/16SJPTH
R7	RES, 1.5K, 5%, 1/16W, 0402	Kamaya	RMC1/16S-152JTH
R8	RES, 3.9K, 5%, 1/16W, 0402	Kamaya	RMC1/16S-392JTH
R3, R4	RES, 430 OHM, 1%, 0.1W, 0402	Kamaya	RMC1/16S-431JTH
R5, R6	RES, 130 OHM, 1%, 1/10W, 0402	Kamaya	RMC1/16SK1300FTH
R1, R2	RES, 1.8K, 5%, 1/16W, 0402	Kamaya	RMC1/16S-182JTH
L4, L5	IND, 560nH, 5%, 550mA, W/W, 0603	Coilcraft	0603LS-561XJRC
L8	IND, 1.6nH, ±0.1nH, 1000mA, M/L, 0402	Murata	LQG15HS3N6B02D
T1, T2	TRANSFORMER, 1:1	Mini Circuits	TC1-33-75-7+
J3	CONN, HDR	Samtec	TSW-104-08-S-S
J1, J2	CONN, F FEM, 75OHM	MM Wave	MW-846-C-DD-75
HS	HEATSINK BLOCK, 1.5 X 2.0 IN	Shenzhen Minxingda	EEF-105441
S1-4	SCREW, 2-56X3/16"	McMaster-Carr	92196A076
C2, C3, C4, C9, C10, C16, C17, C20, C21, R10, R12, R13	DNP		

8V BOM Changes:

Reference Designator	Description	Manufacturer	Part Number
R1, R2	RES, 4.3K OHM,5%,1/16W,0402	KOA Speer	RK73B1ETTP432J
R7	RES, 768 OHM, 1%, 1/16W, 0402	Vishay	CRCW0402768RFKED

Evaluation Board Layout

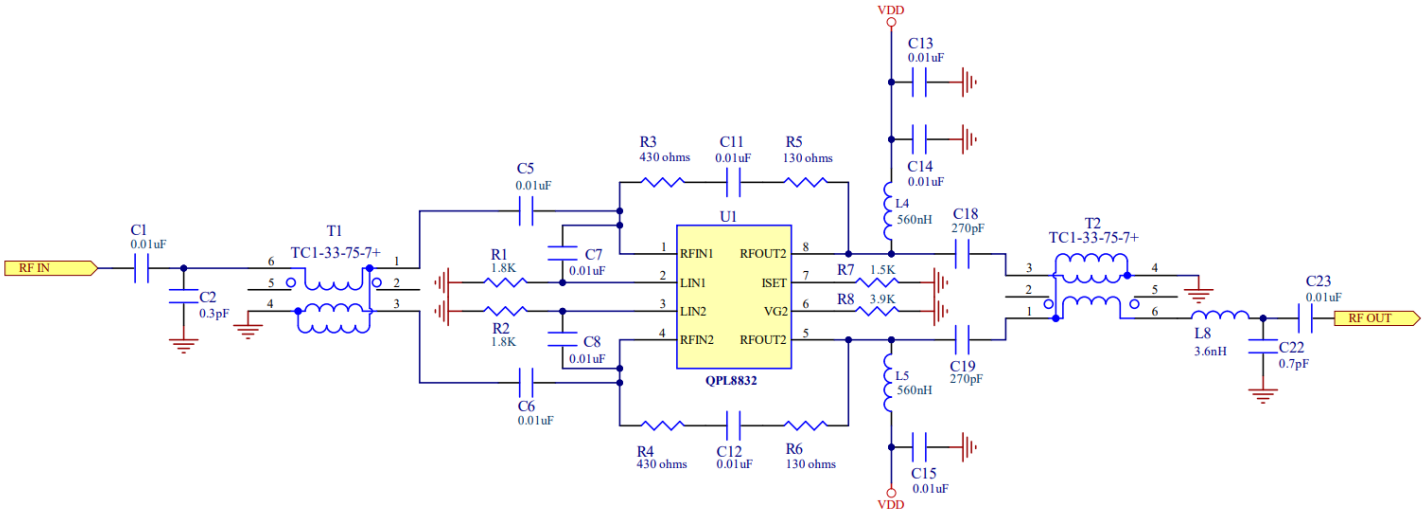


EVB PCB Material and Stack-up
Board Material: 59.8mil FR4, ε_r=4.3
Plating: ½ oz plus final plating
Board Dimension: 2.250" x 1.500"

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	SM-001	0.40mil	3.5	
1	Top Layer	CF-004	0.70mil		
	Dielectric 1	FR4	58.00mil	4.3	
2	Bottom Layer	CF-004	0.70mil		

Total Thickness: 61.2mil

Typical Application Schematic; 50 – 1218 MHz, 5V

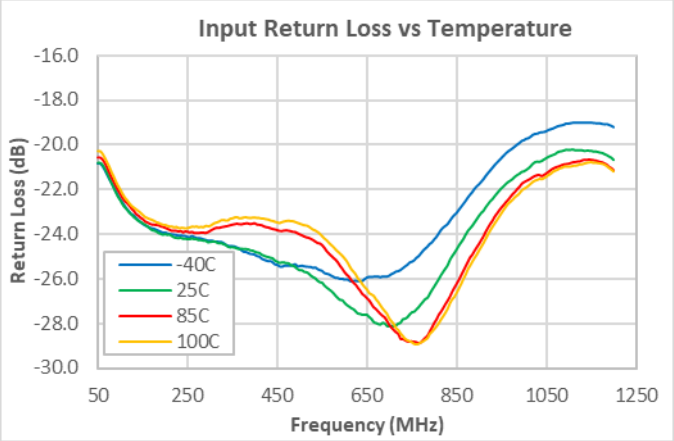


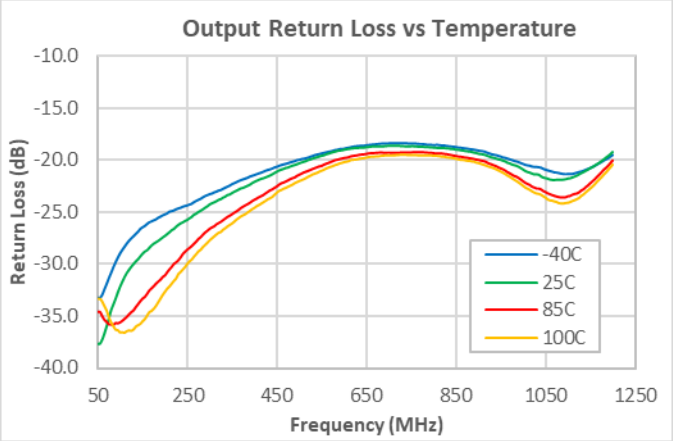
R3, R5 and R4, R6 form the feedback along with the DC blocking caps, C11 and C12. Increasing resistance increases gain while decreasing resistance will reduce gain. Changes to the total feedback resistance will impact return loss and may require retuning the match. L4, L5 are bias chokes for RF decoupling to the power supply. C1, C2, and L1 (DNP) affect the input match, as well as L2 and L3 (DNP). L8 and C22 are used for output matching. C18 and C19 are DC blocking caps, but are also tuned to improve low end return loss. T1 and T2 are 1:1 tertiary baluns suitable for downstream or upstream use. R1, R2, C7 and C8 form the Linearizer bias circuit and are described in more detail on pg 25. R7 sets the device current, while R8 sets the gate voltage of the output stage (refer to pg 25 for further details).

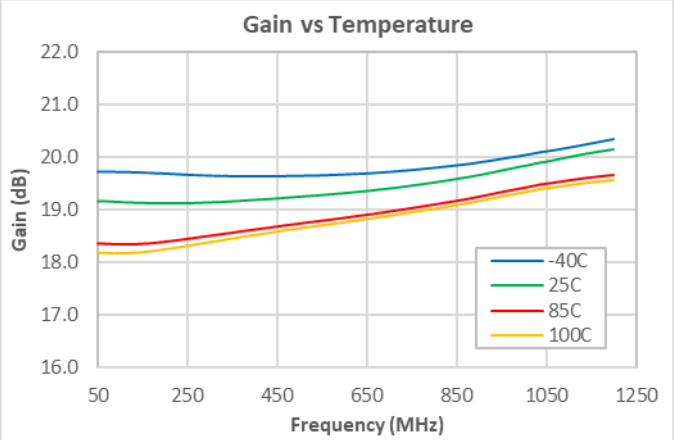
Pin Configuration and Description

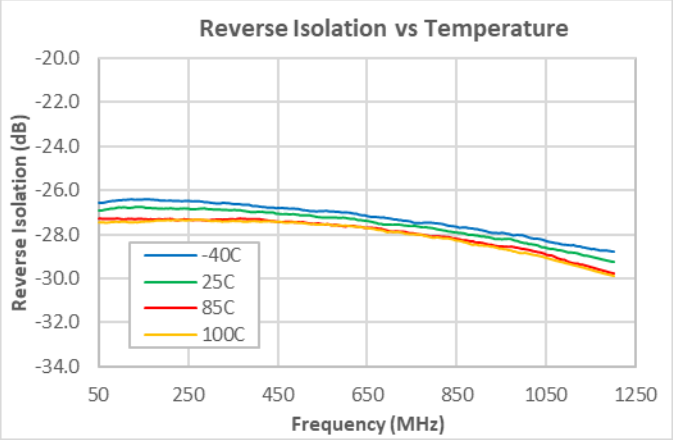
Pin	Name	Description
1	RFIN1	RF input for plus side of amplifier
2	LIN1	Linearizer current set for plus side of amplifier
3	LIN2	Linearizer current set for minus side of amplifier
4	RFIN2	RF input for minus side of amplifier
5	RFOUT2	RF output for minus side of amplifier; DC bias required
6	VG2	Output stage gate voltage adjust
7	ISET	IDD Adjust
8	RFOUT1	RF output for plus side of amplifier; DC bias required
9	GND	Exposed bottom of part, device ground

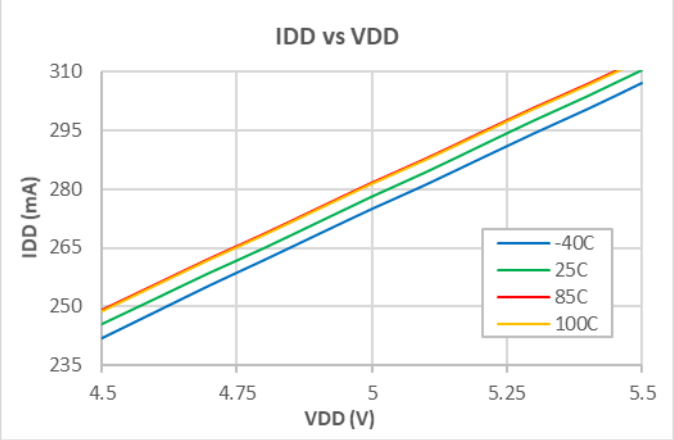
Performance Data; 50 – 1218 MHz, 5V

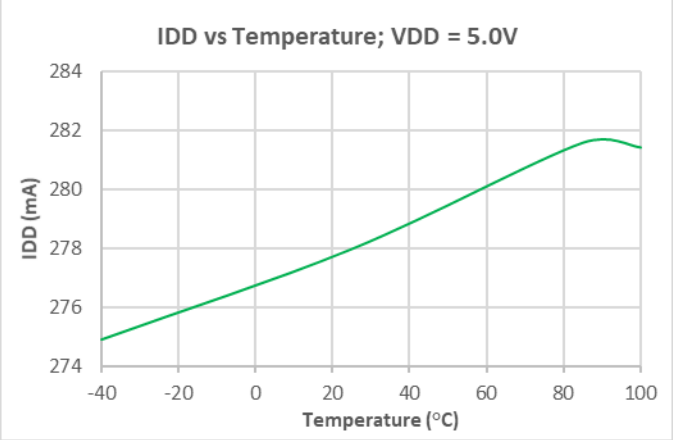








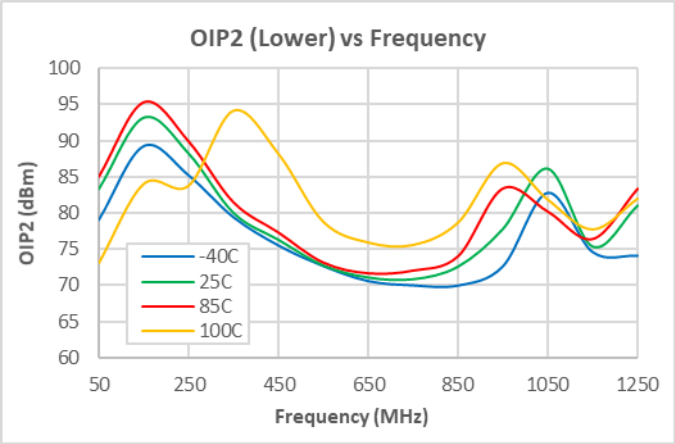


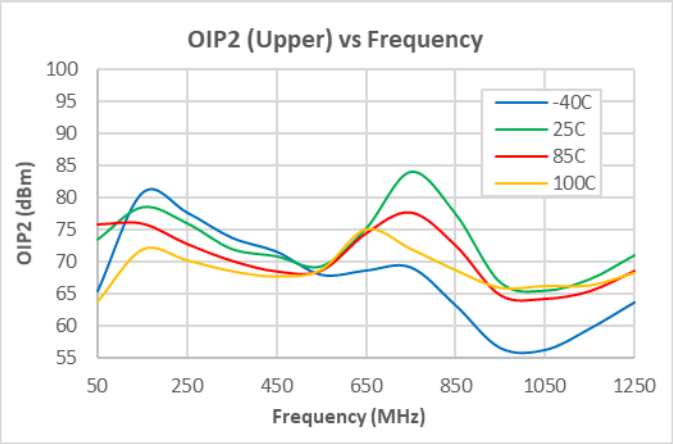


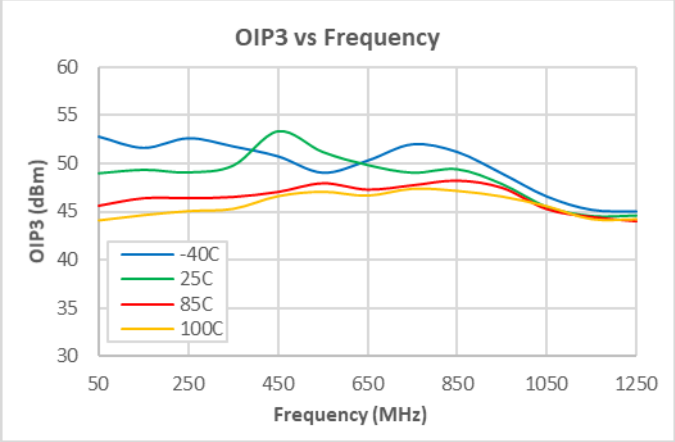
Notes:

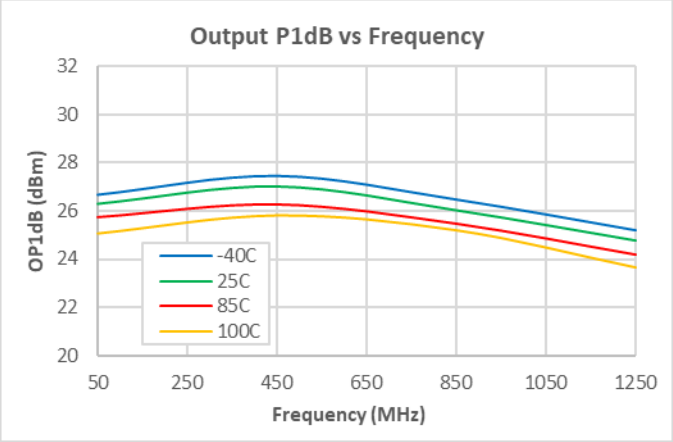
1. Test conditions unless otherwise noted: VDD: 5V, Zo = 75Ω.

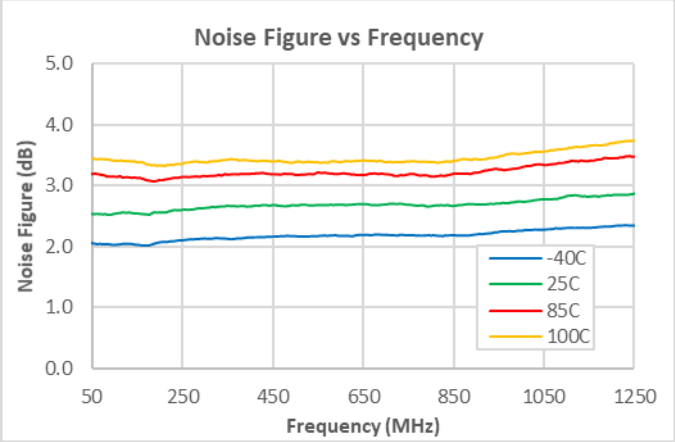
Performance Data; 50 – 1218 MHz, 5 V







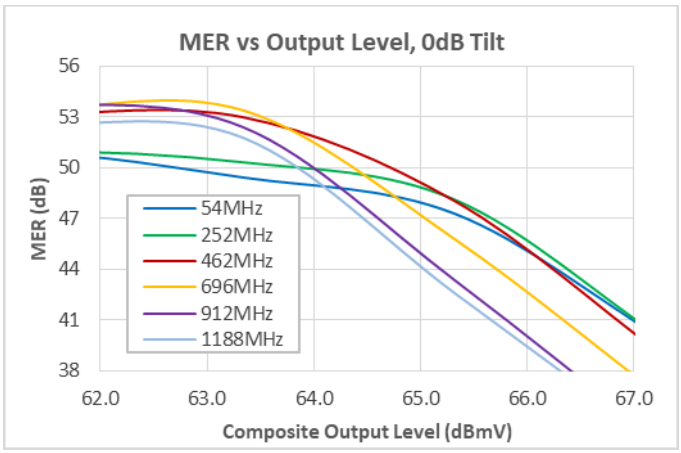


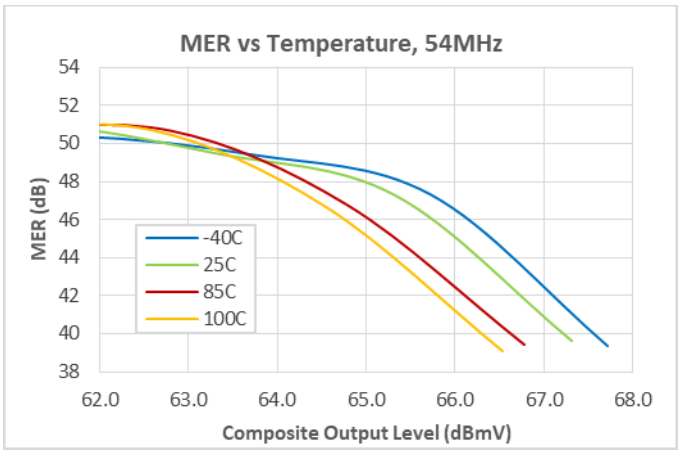


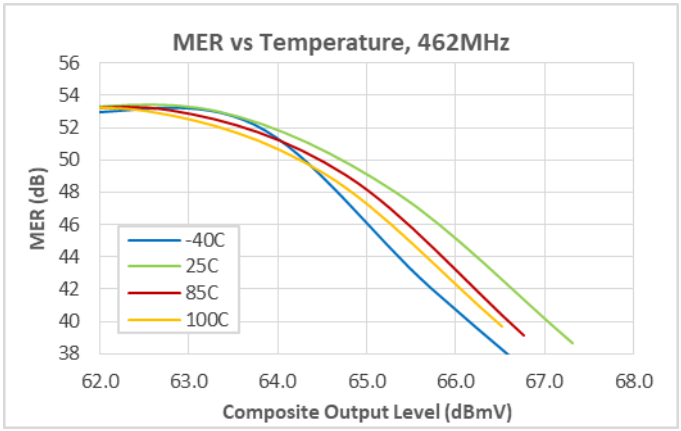
Notes:

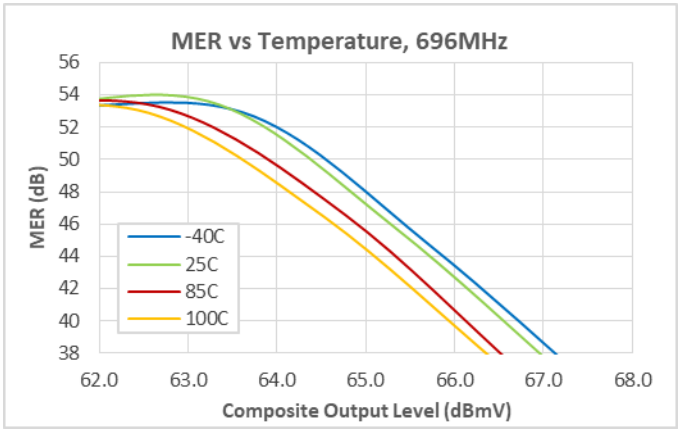
1. Test conditions unless otherwise noted: VDD: 5V, Zo = 75Ω.
2. OIP2: 13 dBm / tone output, Δf = 50 MHz, 50-1218 MHz.
3. OIP3: 13 dBm / tone output, Δf = 6 MHz, 50-1218 MHz.

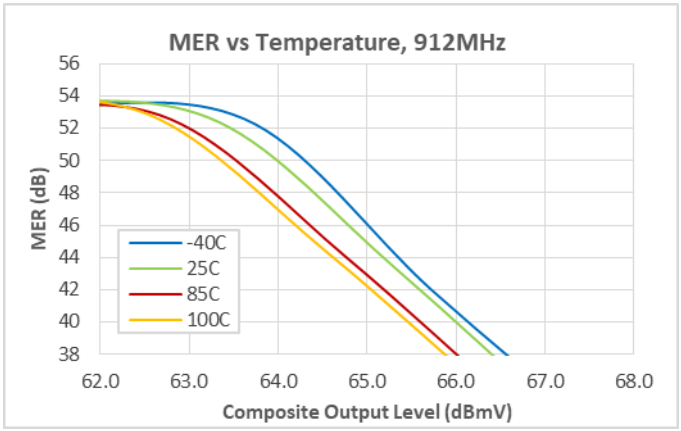
Performance Data; 50 – 1218 MHz, 0 dB Tilt, 5 V

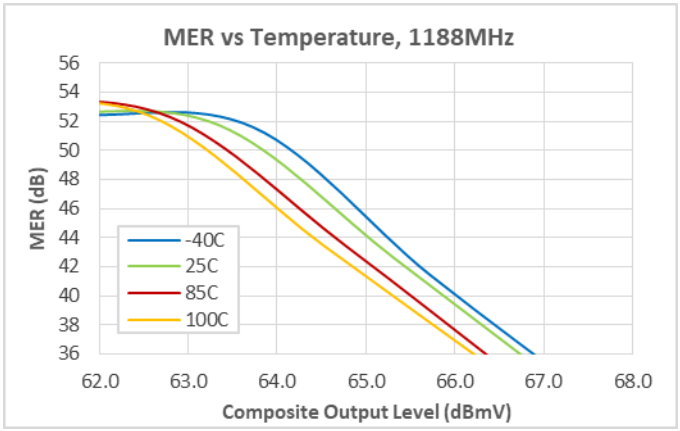








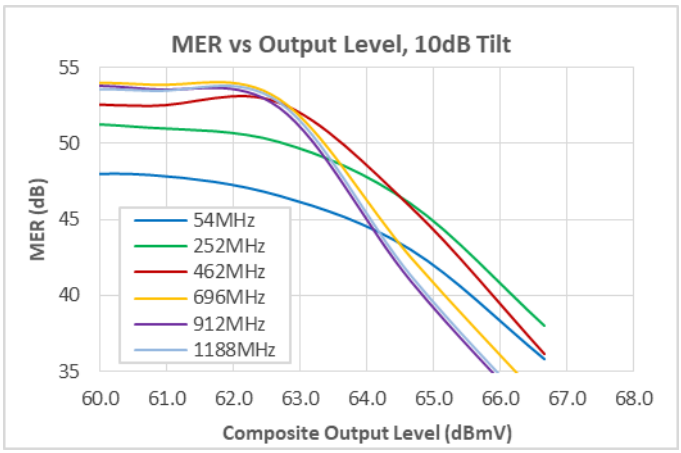


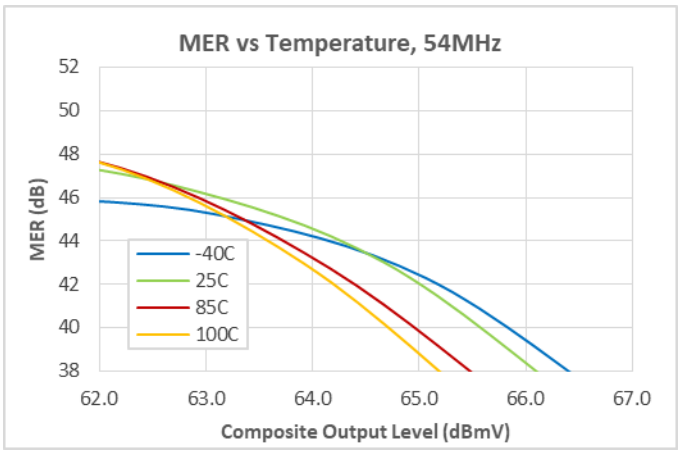


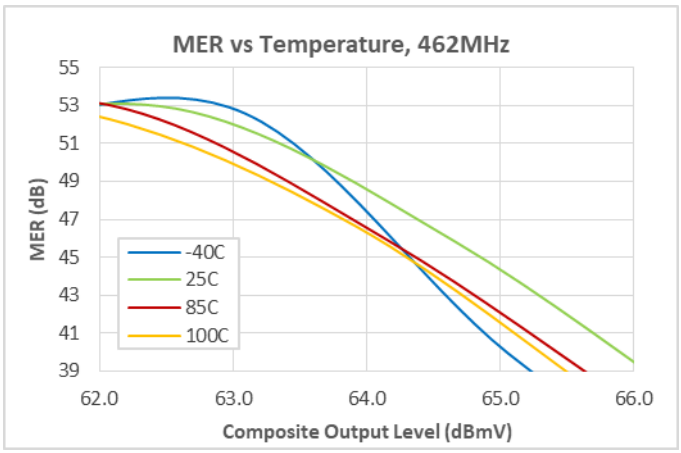
Notes:

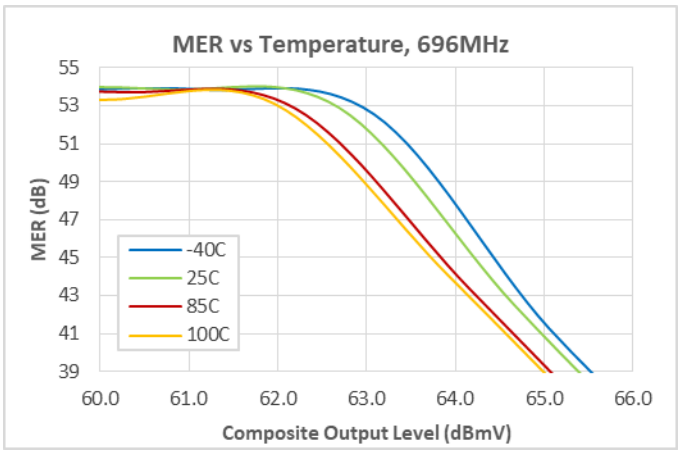
1. Test conditions unless otherwise noted: VDD: 5V, Zo = 75Ω.
2. MER, Source Corrected, Maximum Correction 4.3dB, 54-1218MHz 256QAM, ITU-T J.83, Annex B

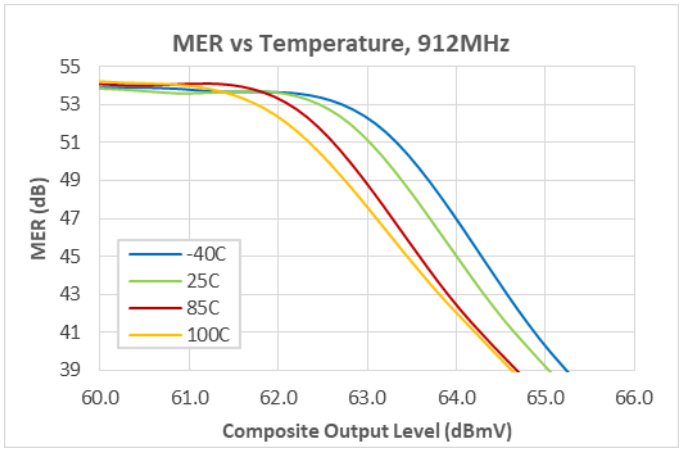
Performance Data; 50 – 1218 MHz, 10dB Tilt, 5V

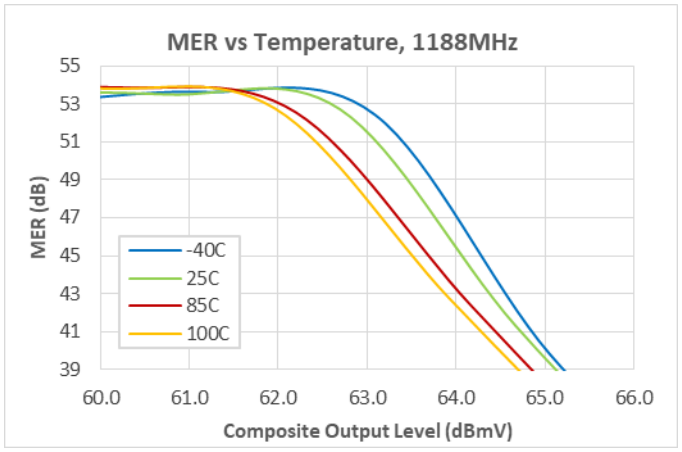








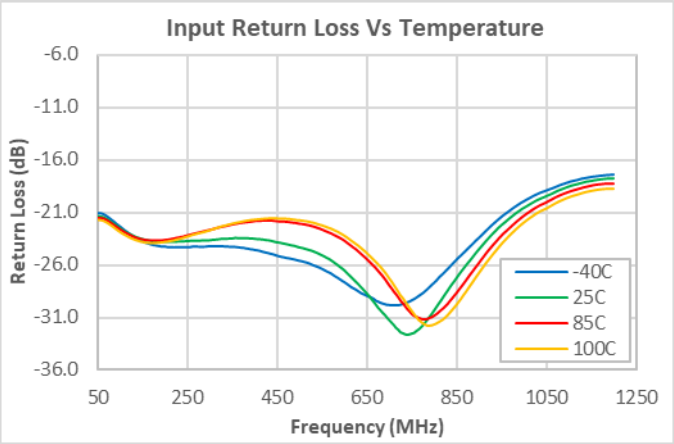


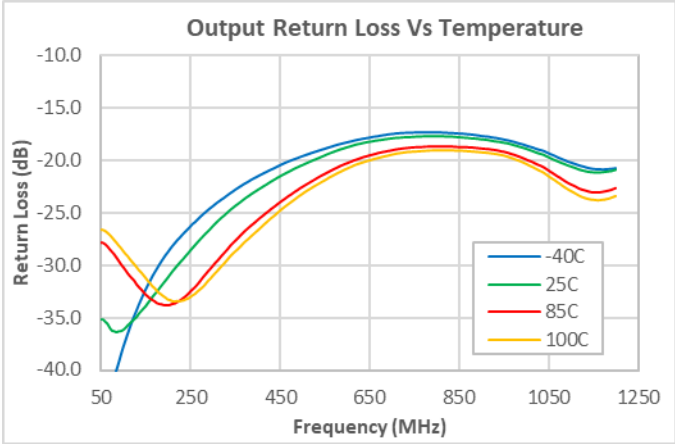


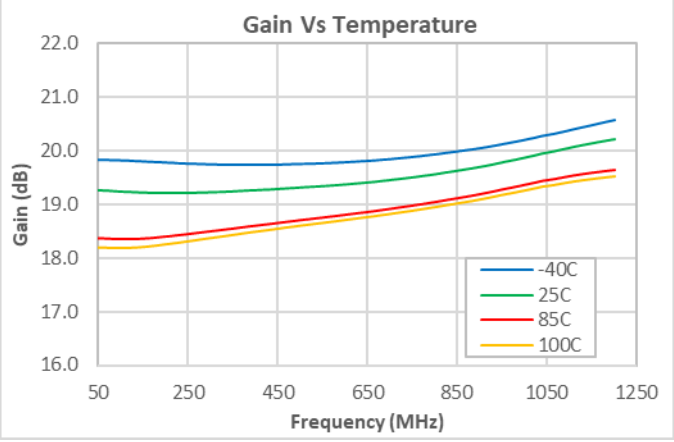
Notes:

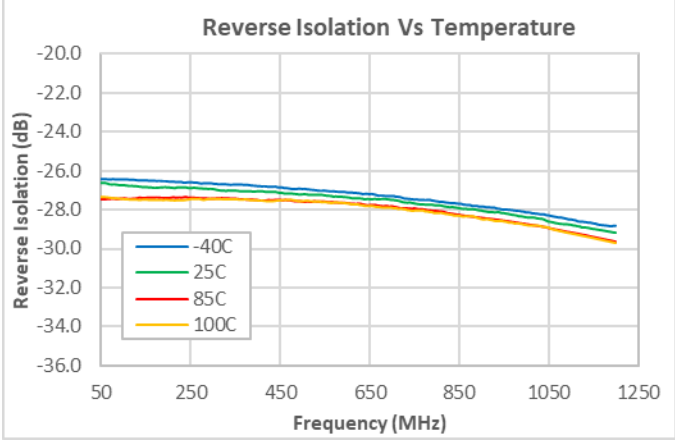
1. Test conditions unless otherwise noted: VDD: 5V, Zo = 75Ω.
2. MER, Source Corrected, Maximum Correction 4.3dB, 54-1218MHz 256QAM, ITU-T J.83, Annex B

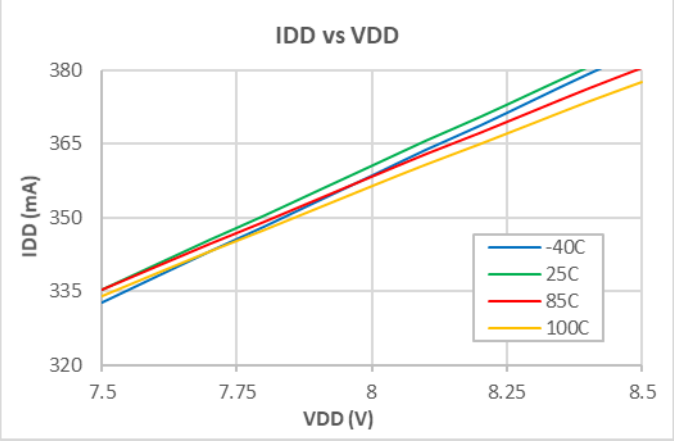
Performance Data; 50 – 1218 MHz, 8V

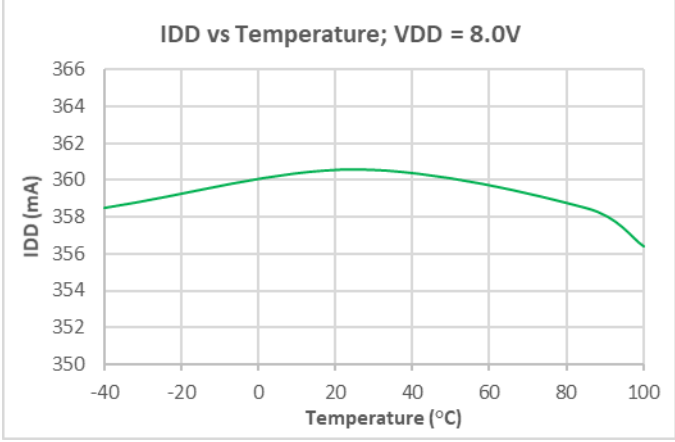








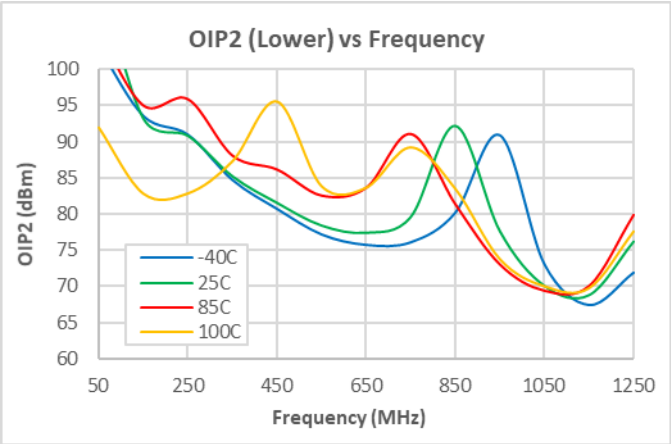


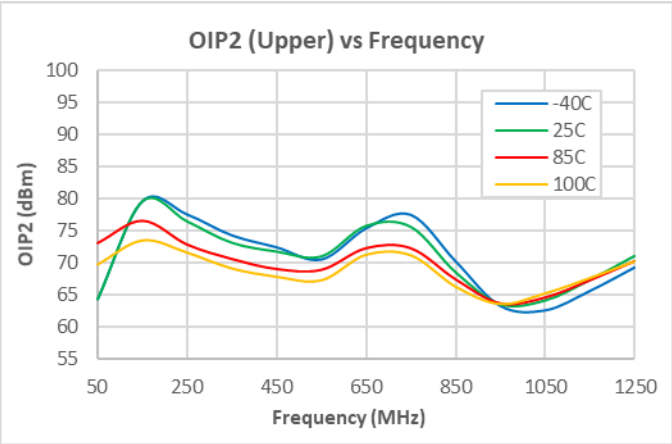


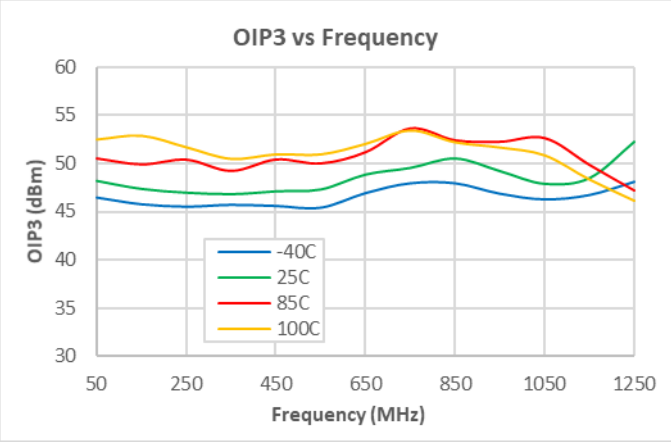
Notes:

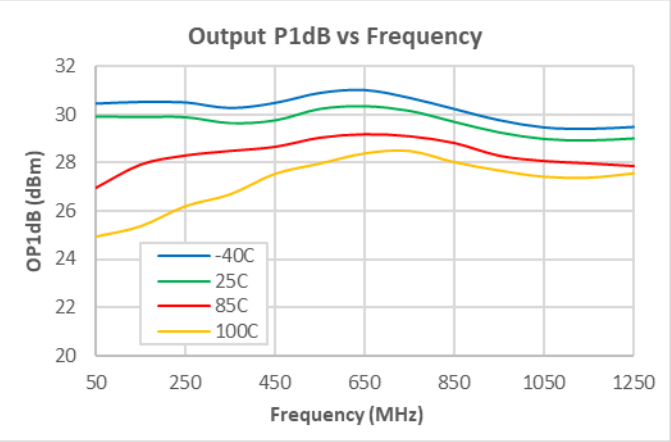
1. Test conditions unless otherwise noted: VDD: 8V, Zo = 75Ω.

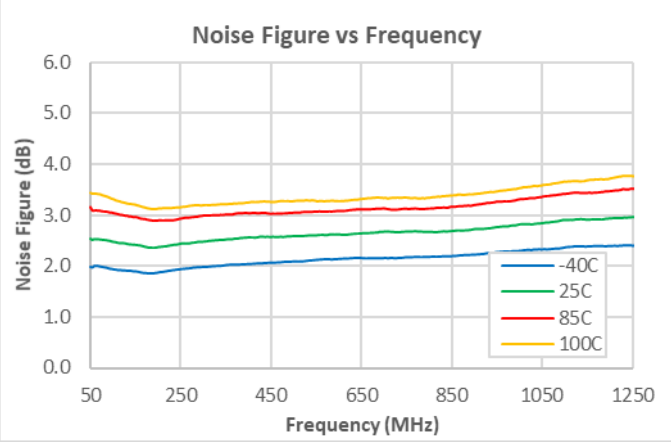
Performance Data; 50 – 1218 MHz, 8 V







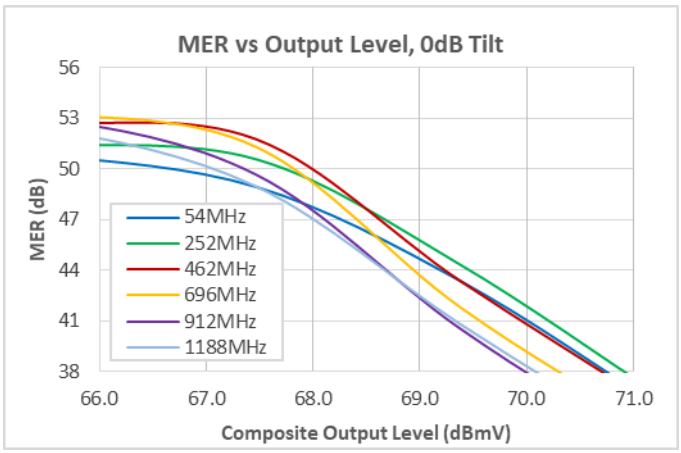


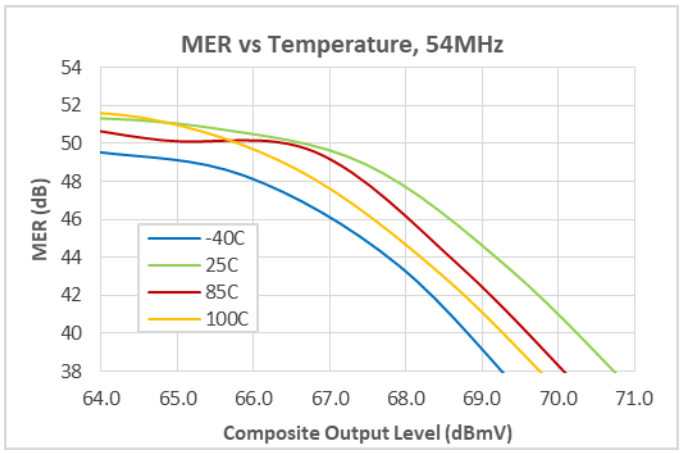


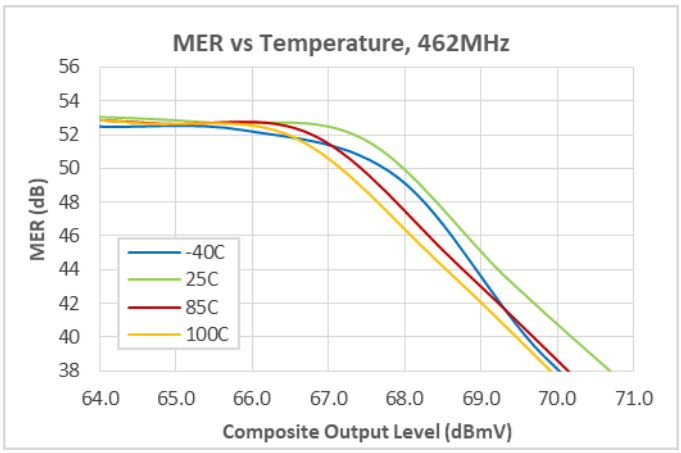
Notes:

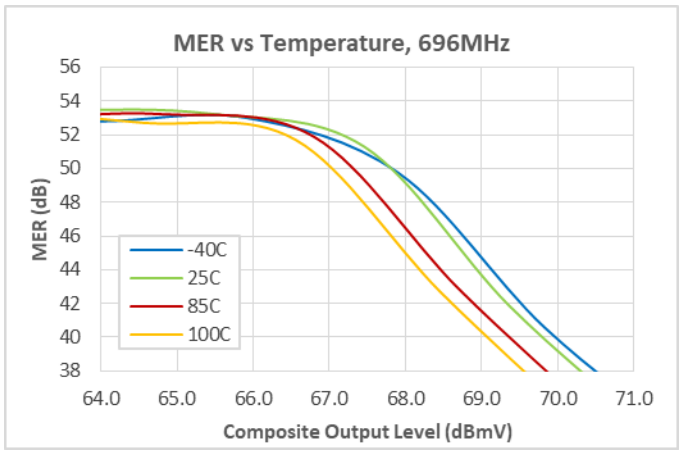
1. Test conditions unless otherwise noted: VDD: 8V, Zo = 75Ω.
2. OIP2: 13 dBm / tone output, Δf = 50 MHz, 50-1218 MHz.
3. OIP3: 13 dBm / tone output, Δf = 6 MHz, 50-1218 MHz.
4. MER, Source Corrected, Maximum Correction 4.3dB, 54-1218MHz 256QAM, ITU-T J.83, Annex B.

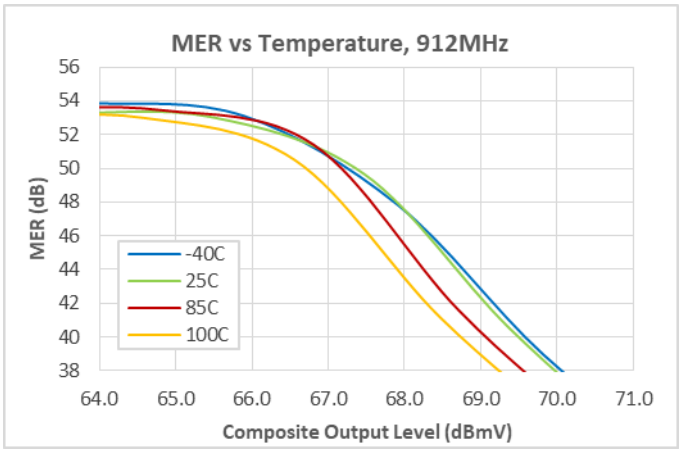
Performance Data; 50 – 1218 MHz, 0 dB Tilt, 8 V

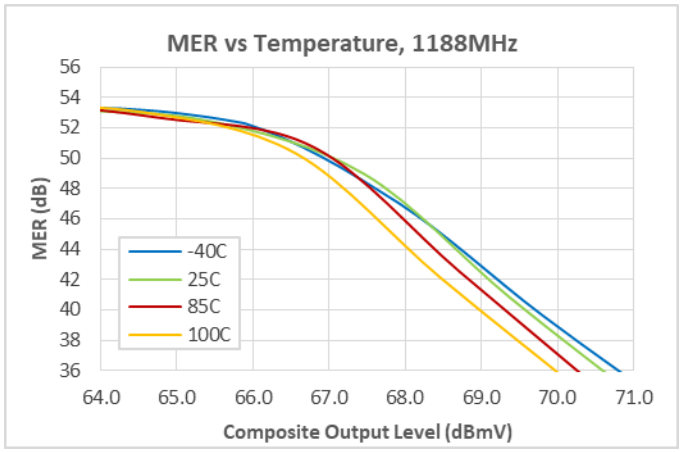








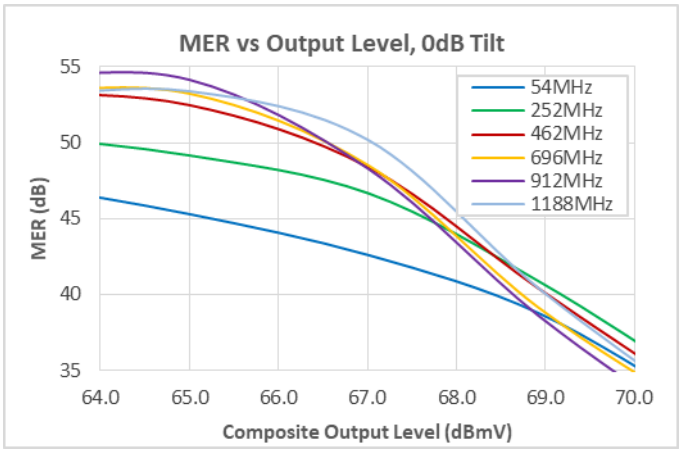


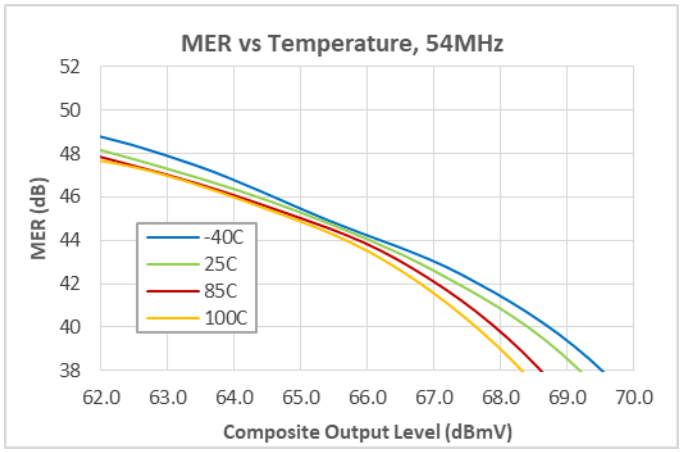


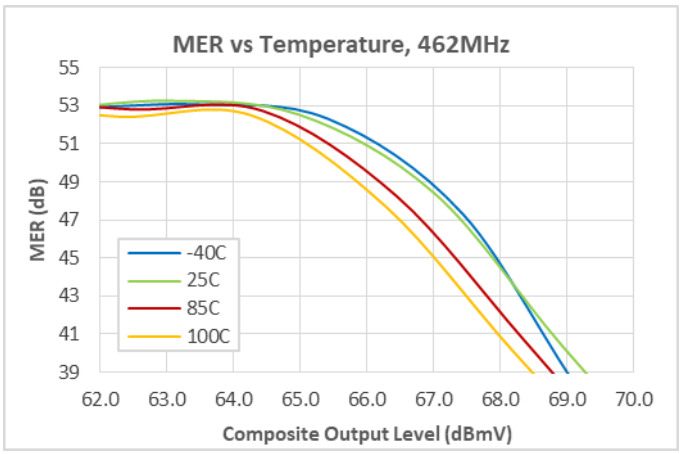
Notes:

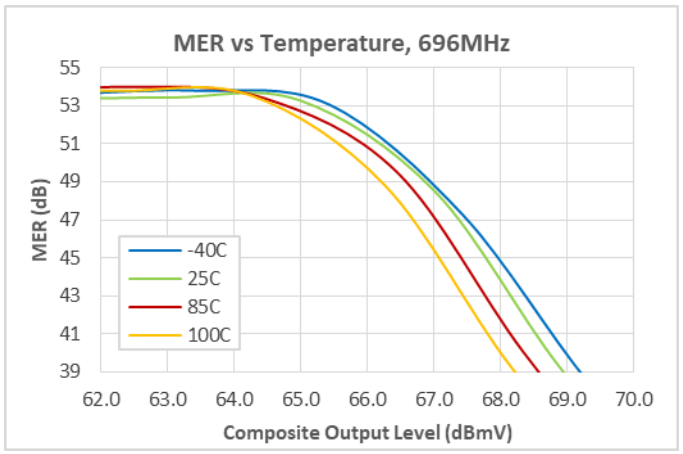
1. Test conditions unless otherwise noted: VDD: 8V, Zo = 75Ω.
2. MER, Source Corrected, Maximum Correction 4.3dB, 54-1218MHz 256QAM, ITU-T J.83, Annex B.

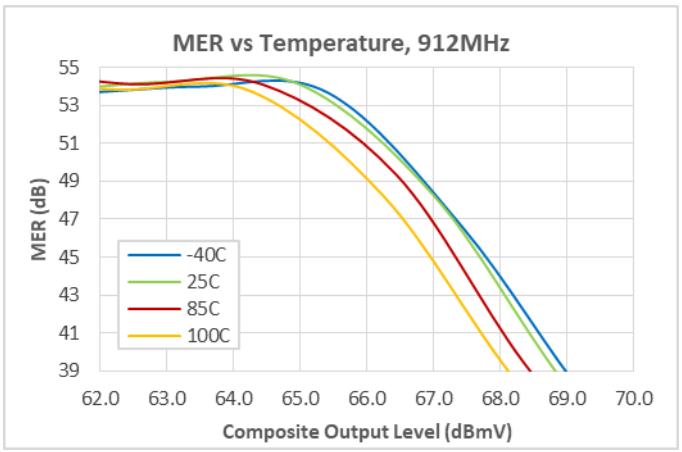
Performance Data; 50 – 1218 MHz, 10 dB Tilt, 8 V

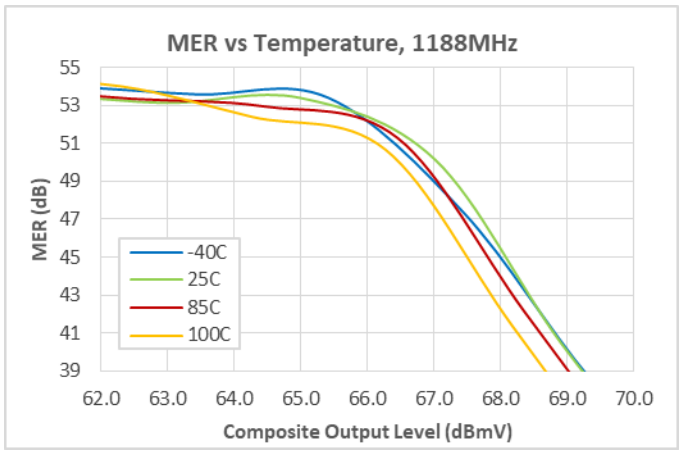












Notes:

1. Test conditions unless otherwise noted: VDD: 8V, Zo = 75Ω.
2. MER, Source Corrected, Maximum Correction 4.3dB, 54-1218MHz 256QAM, ITU-T J.83, Annex B.

Electrical Specifications; 5 – 684MHz, 5V

Parameter	Condition [1]	Min	Typ	Max	Unit
Supply Voltage (V_{DD})			5		V
Supply Current (I_{DD})			280		mA
Frequency Range		5		684	MHz
Gain			19		dB
Gain Flatness			±0.5		dB
Input Return Loss			19		dB
Output Return Loss			22		dB
Noise Figure			3.2		dB
OIP2L	+13 dBm / tone, Δf = 6 MHz		74		dBm
OIP2H	+13 dBm / tone, Δf = 6 MHz		65		dBm
OIP3	+13 dBm / tone, Δf = 6 MHz		46		dBm
Output P1dB			26		dBm
NPR	50dB Dynamic Range; 204MHz Bandwidth, 100MHz Notch		34.6		dB
MER	Vo = 66.1 dBmV Total Composite Output Power 5-204 MHz 33 Ch 256QAM, 0 dB Tilt, ITU-T J.83/B		45		dB
	Vo = 65.4 dBmV Total Composite Output Power 5-684 MHz 113 Ch 256QAM, 0 dB Tilt, ITU-T J.83/B				
Thermal Resistance	Bottom of Case		13		˚C/W

Notes:

1. Typical performance at these conditions: Temp = +25 °C, V_{DD} = +5 V, 75 Ω system, Full band unless otherwise noted.

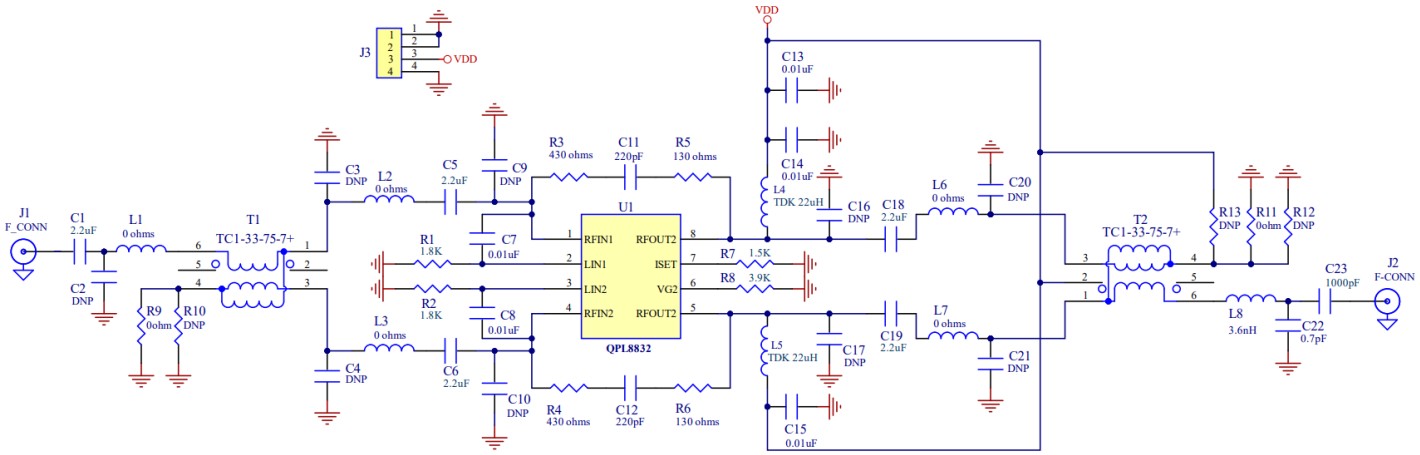
Electrical Specifications; 5 – 684MHz, 8V

Parameter	Condition [1]	Min	Typ	Max	Unit
Supply Voltage (V_{DD})			8		V
Supply Current (I_{DD})			360		mA
Frequency Range		5		684	MHz
Gain			18.8		dB
Gain Flatness			±0.5		dB
Input Return Loss			18		dB
Output Return Loss			20		dB
Noise Figure			4.2		dB
OIPL	+13 dBm / tone, Δf = 6 MHz		80		dBm
OIP2H	+13 dBm / tone, Δf = 6 MHz		69		dBm
OIP3	+13 dBm / tone, Δf = 6 MHz, 5-700 MHz		47		dBm
Output P1dB			29		dBm
NPR	50dB Dynamic Range; 204MHz Bandwidth, 100MHz Notch		38.1		dB
MER	Vo = 68.8 dBmV Total Composite Output Power 5-204 MHz 33 Ch 256QAM, 0 dB Tilt, ITU-T J.83/B		45		dB
	Vo = 68.3 dBmV Total Composite Output Power 5-684 MHz 113 Ch 256QAM, 0 dB Tilt, ITU-T J.83/B				
Thermal Resistance	Bottom of Case		13		˚C/W

Notes:

1. Typical performance at these conditions: Temp = +25 °C, V_{DD} = +5 V, 75 Ω system, Full band unless otherwise noted.

Evaluation Board Schematic; 5 – 684 MHz, 5V



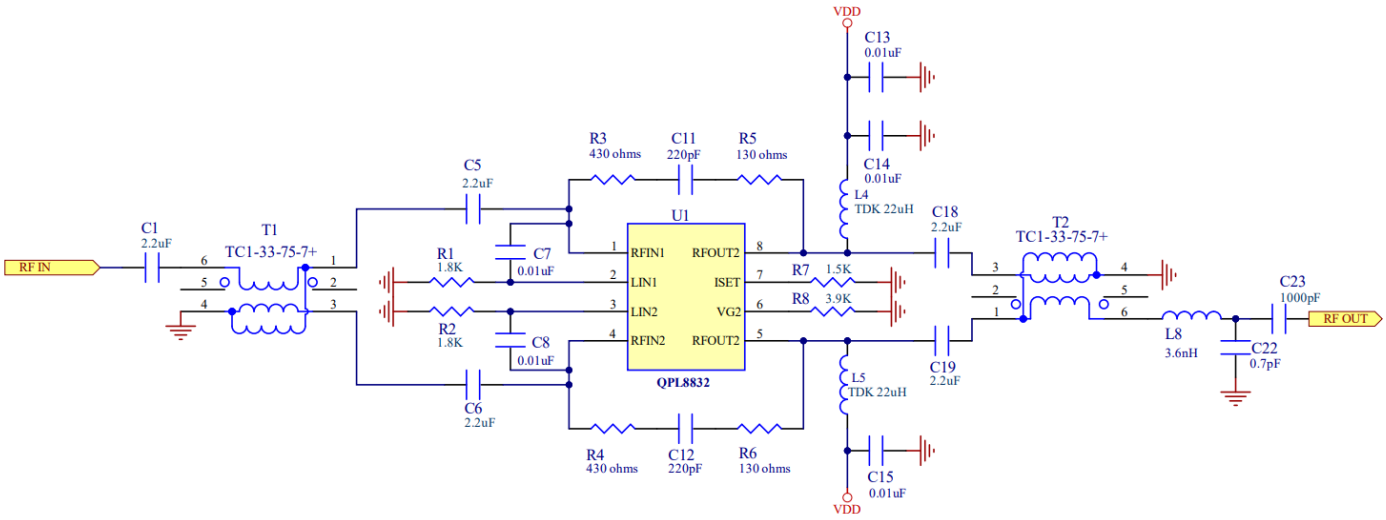
Bill of Material of Evaluation Board: 5 – 684 MHz, 5V

Reference Designator	Description	Manufacturer	Part Number
U1	5 - 1218 MHz, 21 dB Push-Pull Amp	Qorvo	QPL8832SB
PCB	EVB PCB, QPL8832	Qorvo	QPL883x-4001
C23	CAP, 1000pF, 5%, 50V, C0G, 0402	Murata	GRM1555C1H102JA01D
C1, C5, C6, C18, C19	CAP, 2.2uF, 10%, 16V, X5R, 0402	Murata	GRM155R61C225KE11D
C22	CAP, 0.7pF, +/-0.1pF, 50V, HI-Q, 0402	Murata	GJM1555C1HR70BB01D
C7, C8, C13, C14, C15	CAP, 0.01uF, 10%, 50V, X7R, 0402	Murata	GCM155R71H103KA55D
C11, C12	CAP, 220pF, 5%, 50V, C0G, 0402	Kyocera AVX	04025A221JAT2A
L1, L2, L3, L6, L7, R9, R11	RES, 0 OHM, 1/10W, 0402	Kamaya	RMC1/16SJPTH
R7	RES, 1.5K, 5%, 1/16W, 0402	Kamaya	RMC1/16S-152JTH
R8	RES, 3.9K, 5%, 1/16W, 0402	Kamaya	RMC1/16S-392JTH
R1, R2	RES, 1.8K, 5%, 1/16W, 0402	Kamaya	RMC1/16S-182JTH
R3, R4	RES, 430 OHM, 1%, 0.1W, 0402	Kamaya	RMC1/16S-431JTH
R5, R6	RES, 130 OHM, 1%, 1/10W, 0402	Kamaya	RMC1/16SK1300FTH
L4, L5	IND, 22uH, 20%, 190mA, M/L, 0603	TDK	MLZ1608N220LT000
L8	IND, 3.6nH, ±0.1nH, 750mA, M/L, 0402	Murata	LQG15HS3N6B02D
T1, T2	TRANSFORMER, 1:1	Mini Circuits	TC1-33-75-7+
J3	CONN, HDR	Samtec	TSW-104-08-S-S
J1, J2	CONN, F FEM, 75OHM	MM Wave	MW-846-C-DD-75
HS	HEATSINK BLOCK, 1.5 X 2.0 IN	Shenzhen Minxingda	EEF-105441
S1-S4	SCREW, 2-56X3/16"	McMaster-Carr	92196A076
C2, C3, C4, C9, C10, C16, C17, C20, C21, R10, R12, R13	DNP		

8V BOM Changes:

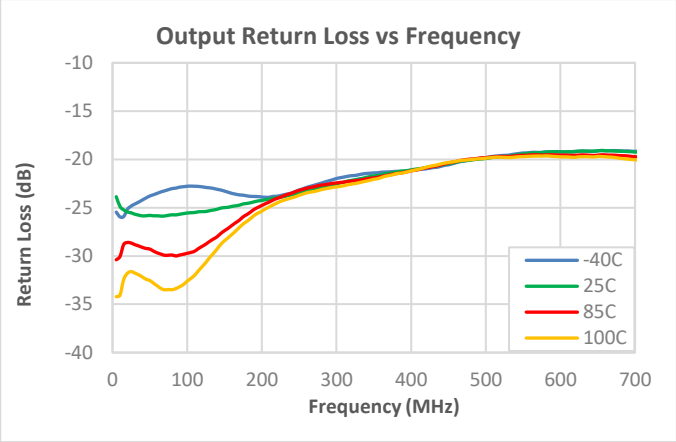
Reference Designator	Description	Manufacturer	Part Number
R1, R2	RES, 4.3K OHM,5%,1/16W,0402	KOA Speer	RK73B1ETTP432J
R7	RES, 768 OHM, 1%, 1/16W, 0402	Vishay	CRCW0402768RFKED

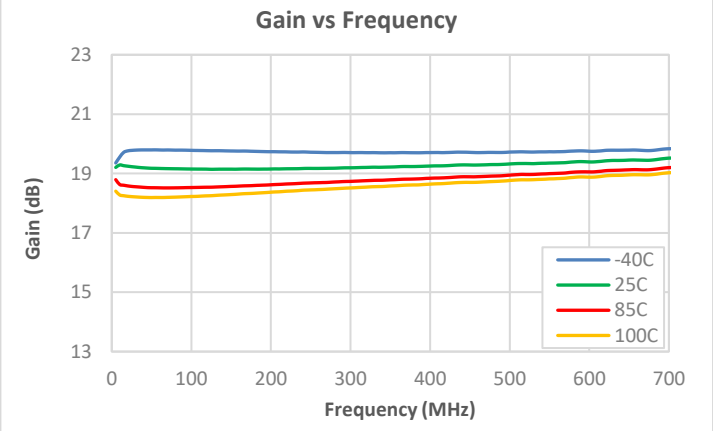
Typical Application Schematic; 5 – 684 MHz, 5V

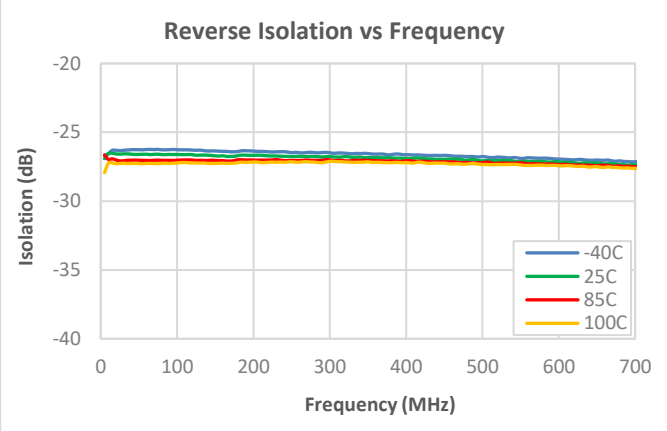


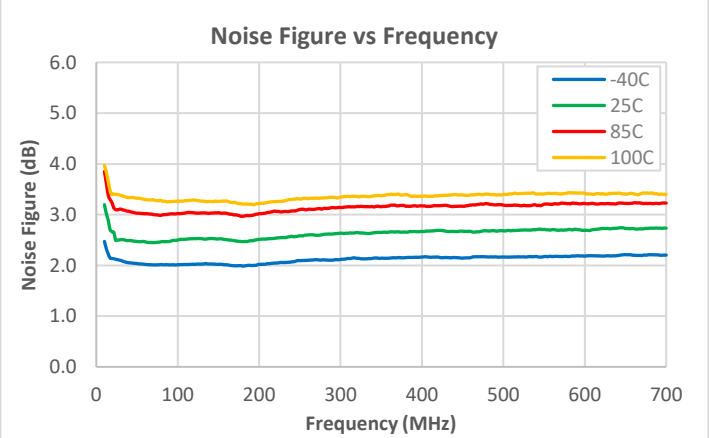
R3, R5 and R4, R6 form the feedback along with the DC blocking caps, C11 and C12. C11, C12 are tuned to improve 5MHz flatness. Increasing resistance increases gain and while decreasing resistance will reduce gain. Changes to the feedback resistance will impact return loss and may require retuning the match. L4, L5 are bias chokes for RF decoupling to the power suppply. Other inductors may be used that provide greater then 5.6uH of effective inductance at 5MHz with low DC resistance. C2, L1 (DNP) tune the input match. L8, C22, C23 are used for output matching. T1 and T2 are 1:1 tertiary baluns suitable for downstream or upstream use. R1, R2, C7 and C8 form the Linearizer bias circuit and are described in more detail on pg 25. R7 sets the device current, while R8 sets the gate voltage of the output stage (refer to pg 25 for further details). 2.2uF blocking capacitors minimize impedance at 5MHz. Lower values may be employed as long as sufficient performance in the application is maintained.

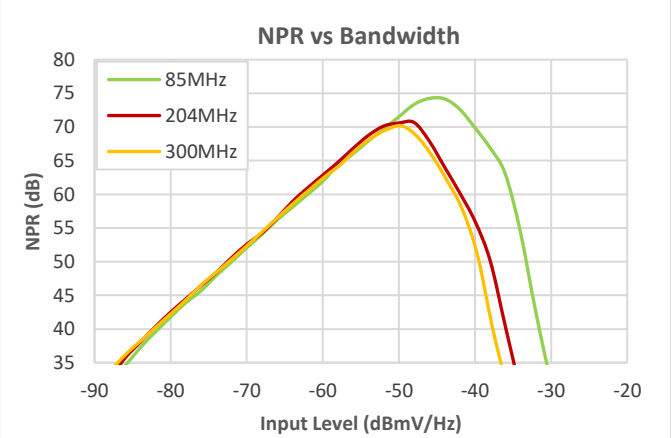
Performance Data; 5 – 684 MHz, 5V







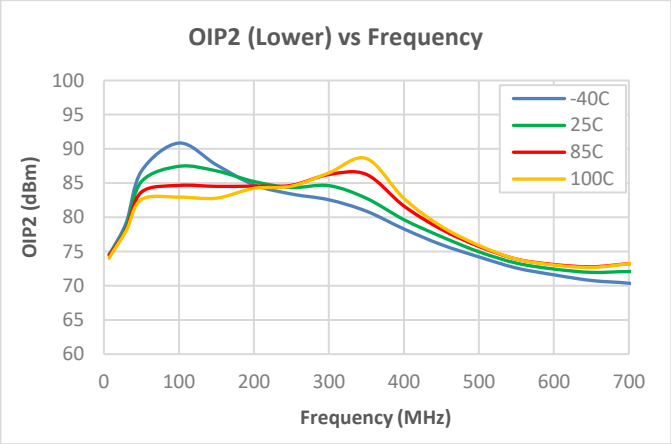


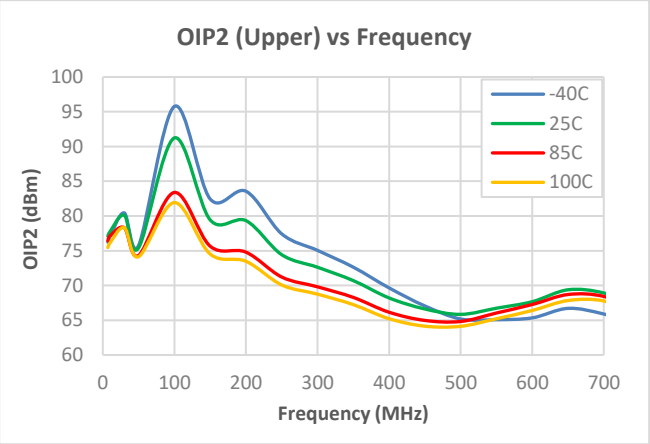


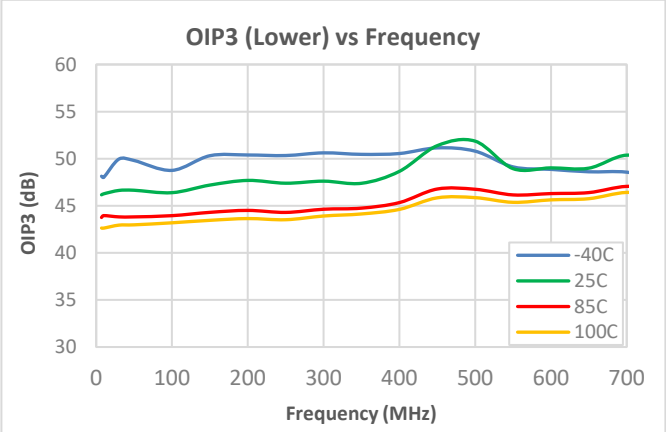
Notes:

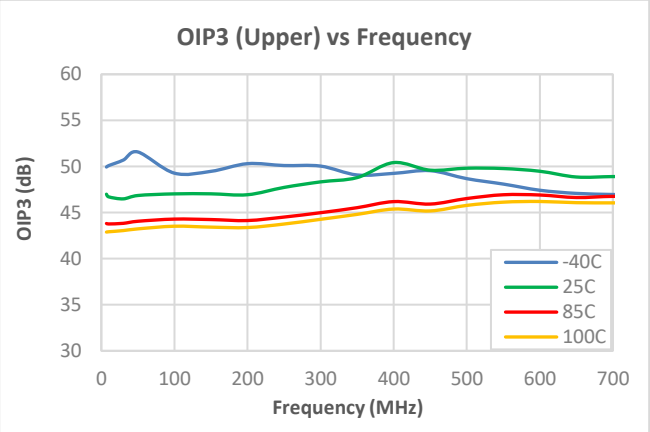
1. Test conditions unless otherwise noted: VDD: 5V, Zo = 75Ω.
2. NPR:
   a. 85MHZ Bandwidth, 41MHz Notch
   b. 204MHz Bandwidth, 100MHz Notch
   c. 300MHz Bandwidth, 150MHz Notch

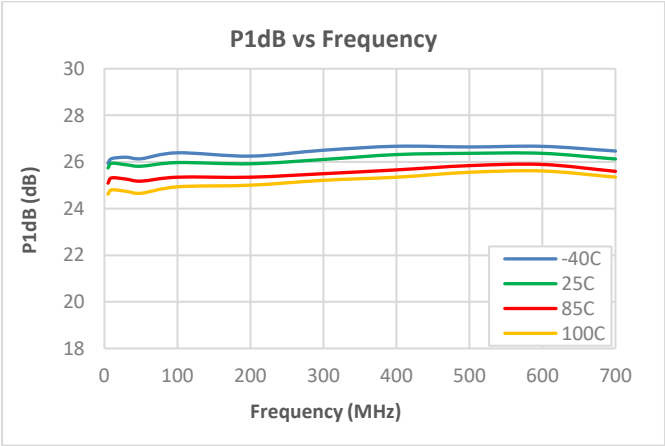
Performance Data; 5 – 684 MHz, 5V







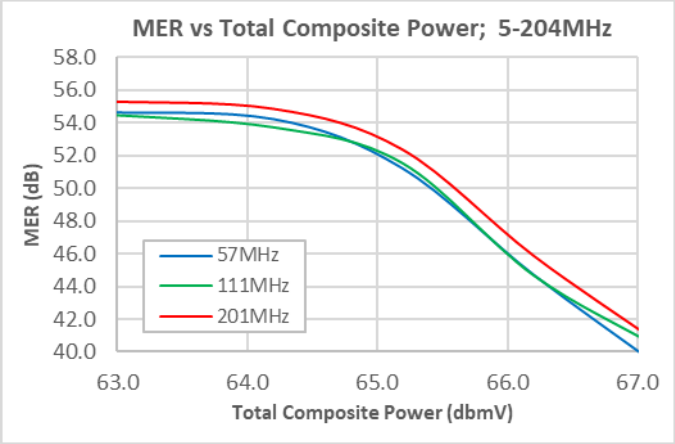


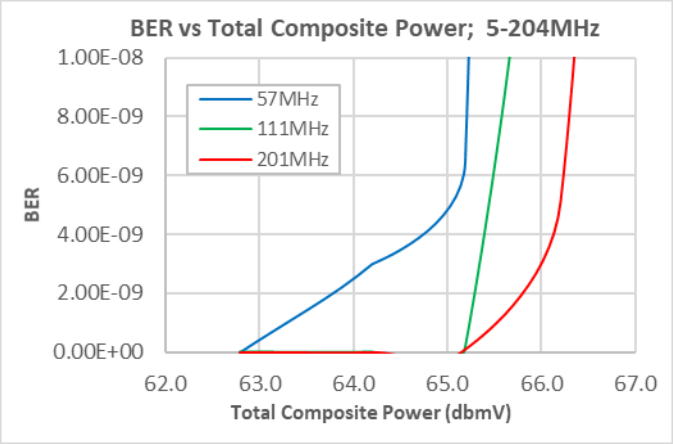


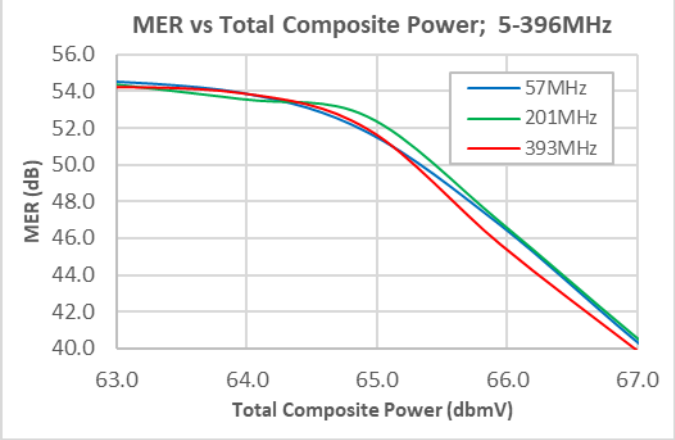
Notes:

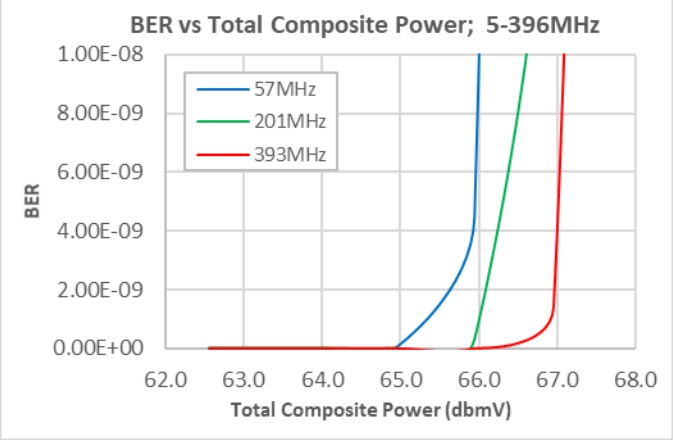
1. Test conditions unless otherwise noted: VDD: 5V, Zo = 75Ω.
2. OIP2: 13 dBm / tone output, Δf = 50 MHz, 5-700 MHz.
3. OIP3: 13 dBm / tone output, Δf = 6 MHz, 5-700 MHz.

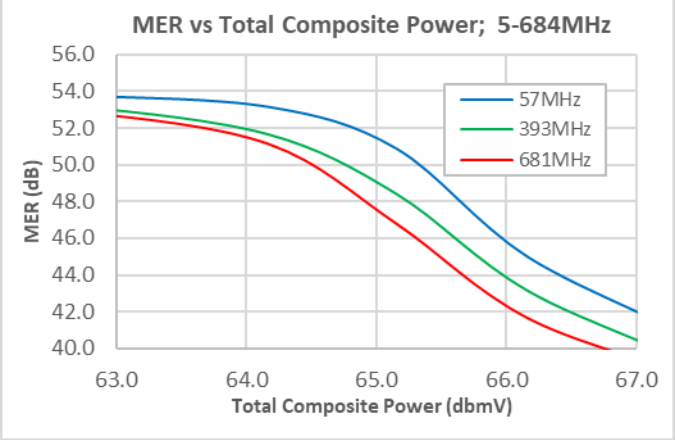
Performance Data; 5 – 684 MHz, 5V

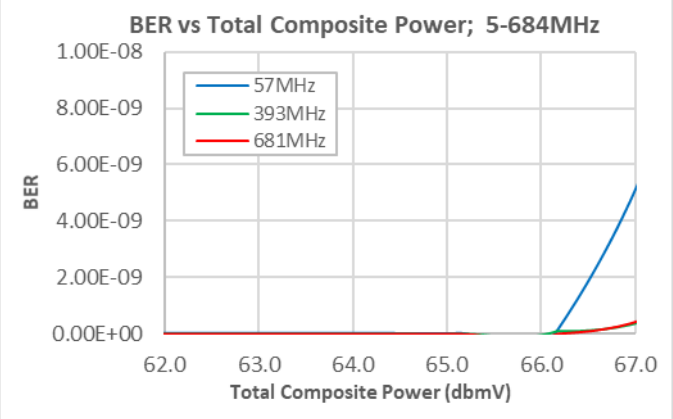








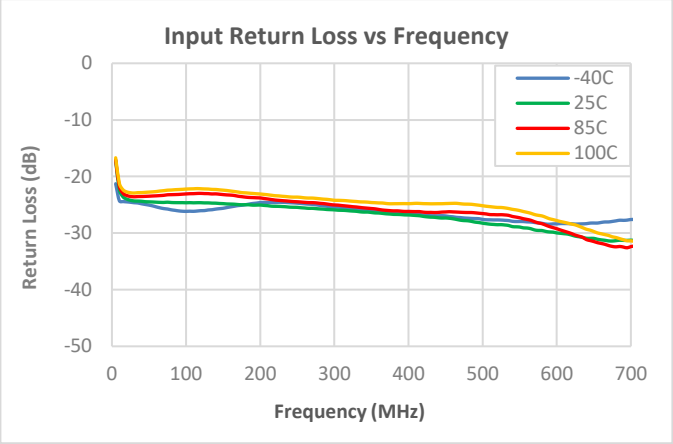


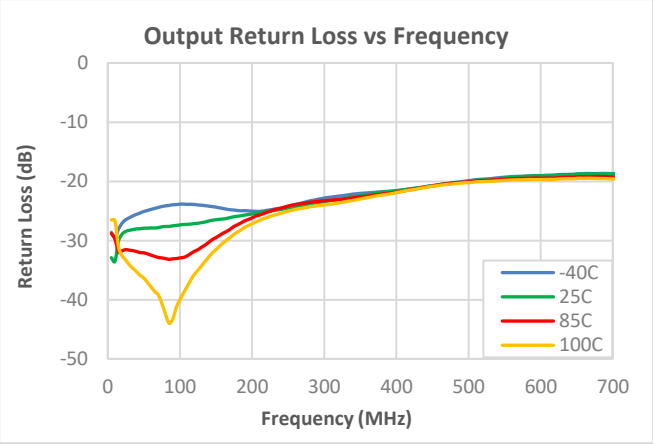


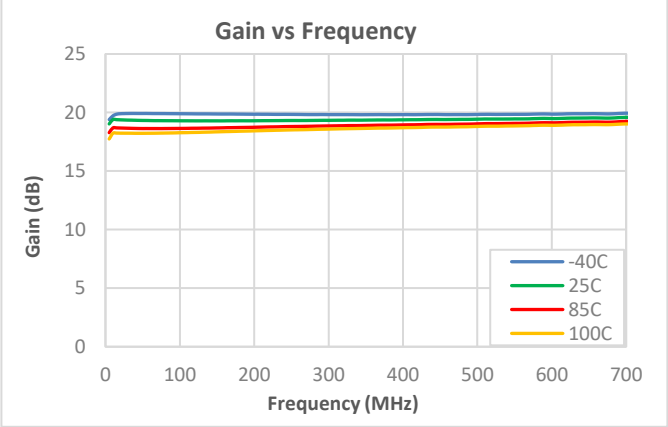
Notes:

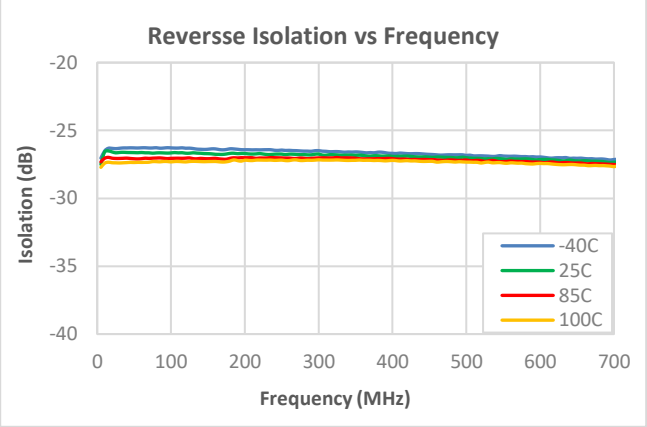
1. Test conditions unless otherwise noted: VDD: 5V, Zo = 75Ω.
2. MER, Source Corrected, Maximum Correction 4.3dB, 256 QAM, ITU-T J.83, Annex B

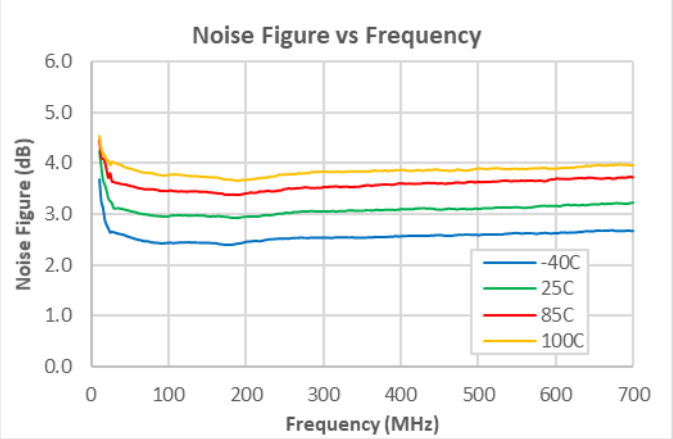
Performance Data; 5 – 684 MHz, 8V

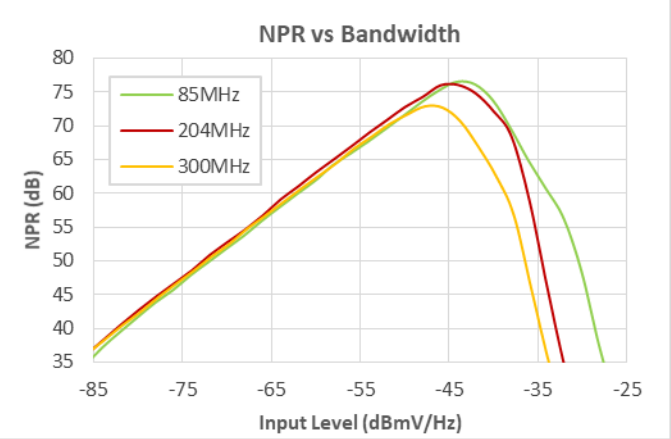








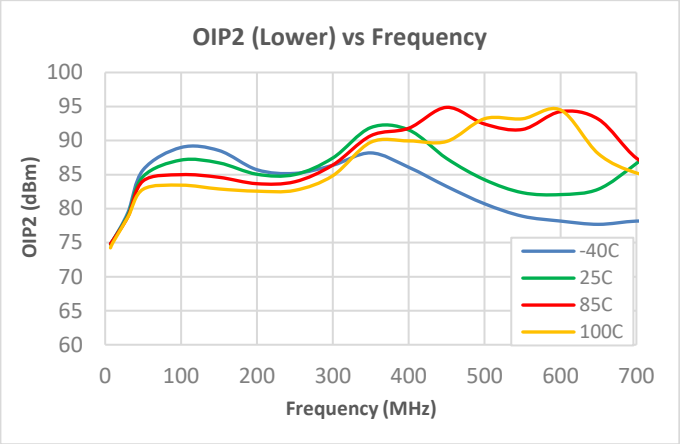


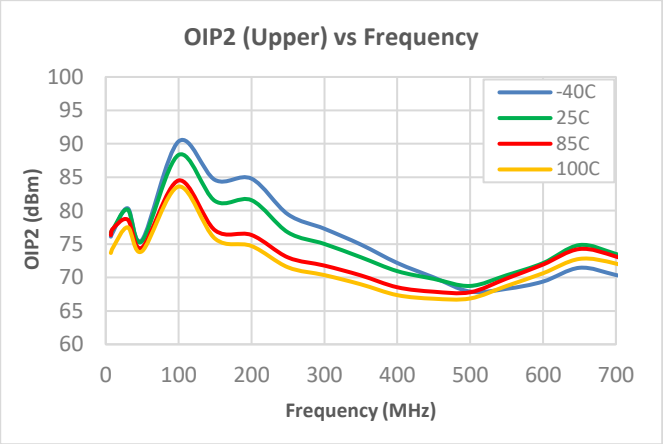


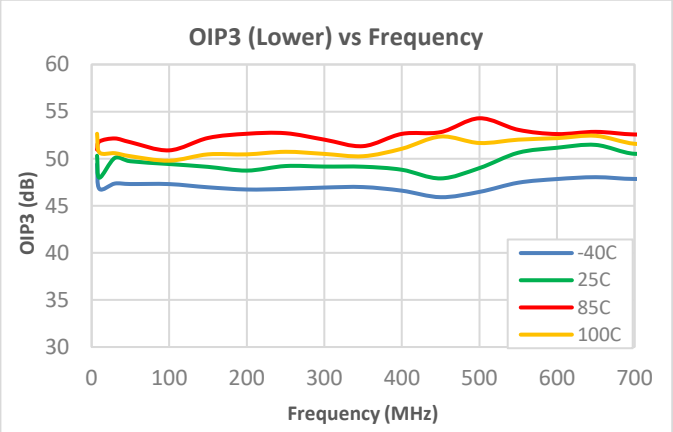
Notes:

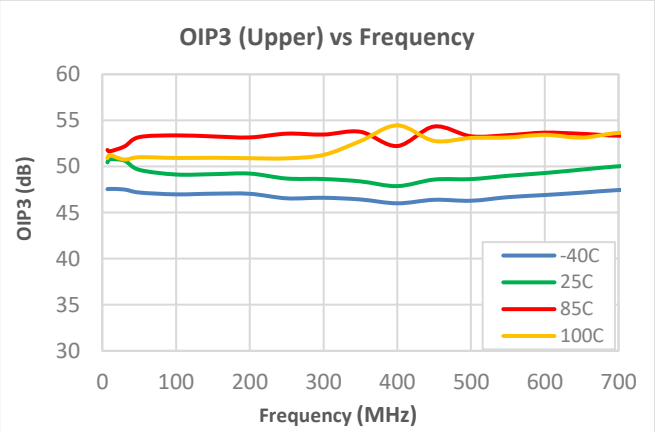
1. Test conditions unless otherwise noted: VDD: 8V, Zo = 75Ω.
2. NPR:
   a. 85MHZ Bandwidth, 41MHz Notch
   b. 204MHz Bandwidth, 100MHz Notch
   c. 300MHz Bandwidth, 150MHz Notch

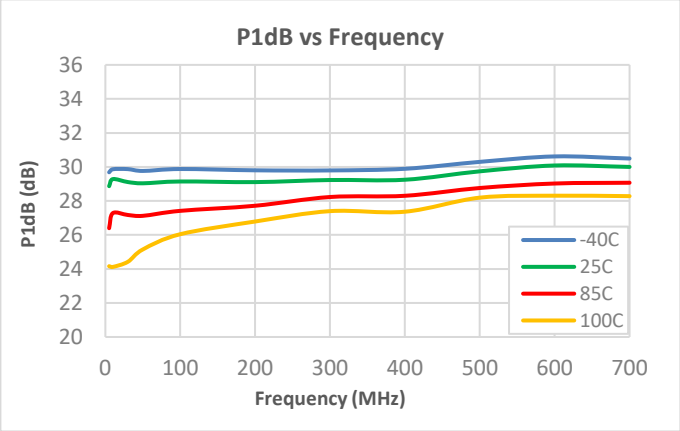
Performance Data; 5 – 684 MHz, 8V







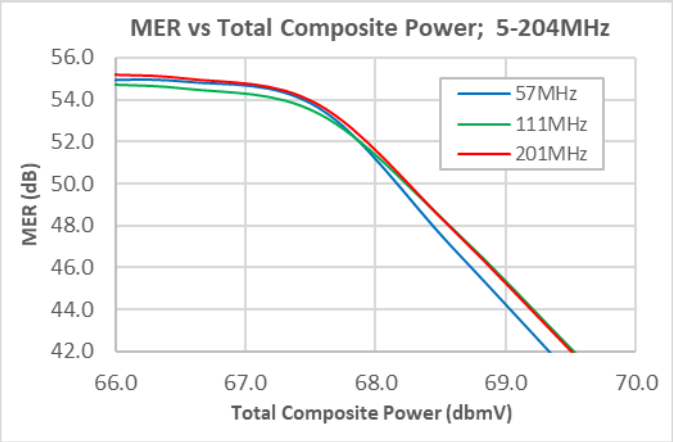


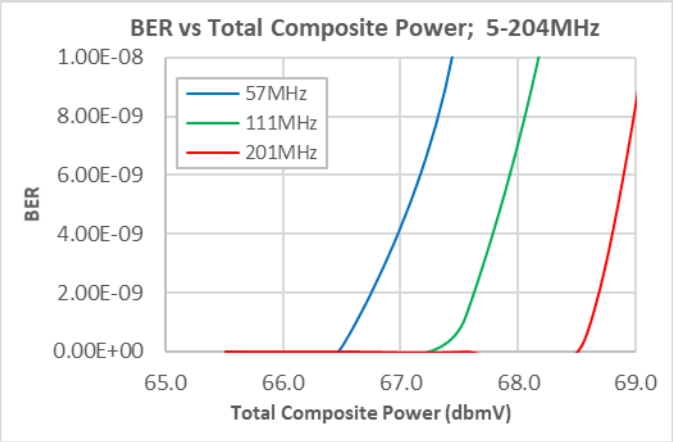


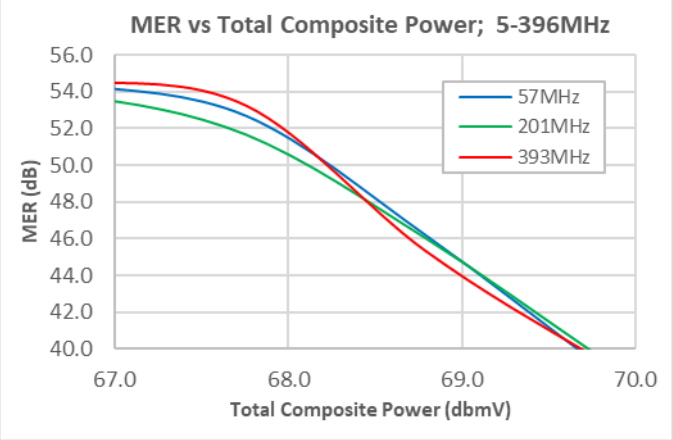
Notes:

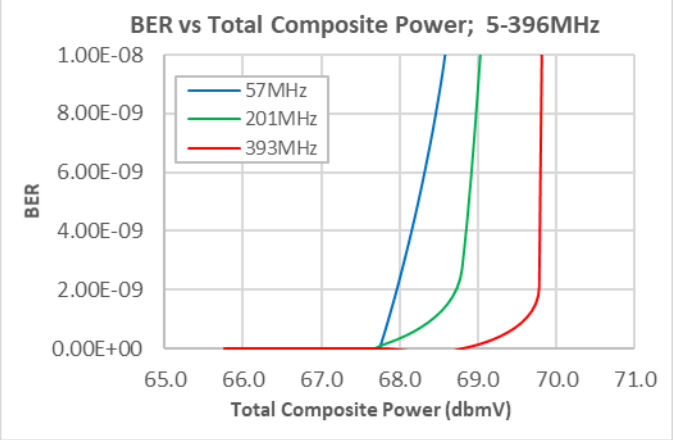
1. Test conditions unless otherwise noted: VDD: 8V, Zo = 75Ω.
2. OIP2: 13 dBm / tone output, Δf = 50 MHz, 5-700 MHz.
3. OIP3: 13 dBm / tone output, Δf = 6 MHz, 5-700 MHz.

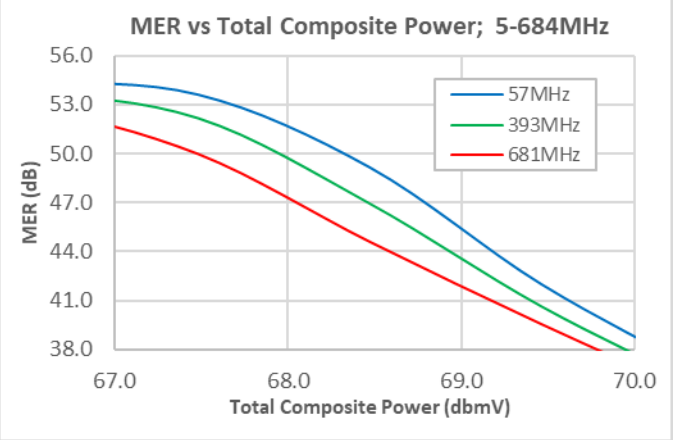
Performance Data; 5 – 684 MHz, 8V

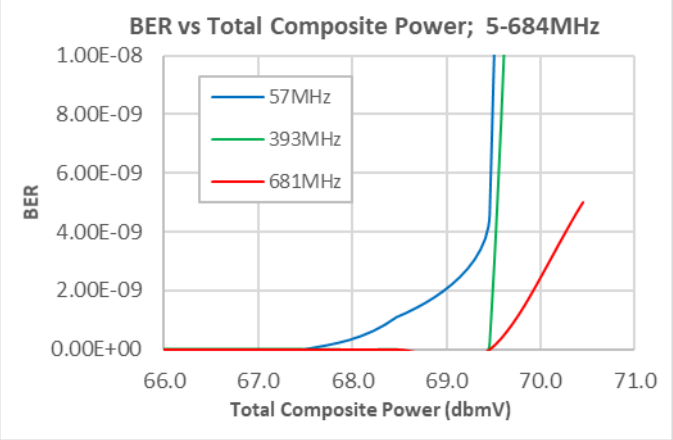












Notes:

1. Test conditions unless otherwise noted: VDD: 8V, Zo = 75Ω.
2. MER, Source Corrected, Maximum Correction 4.3dB, 256 QAM, ITU-T J.83, Annex B

Linearizer Current Settings

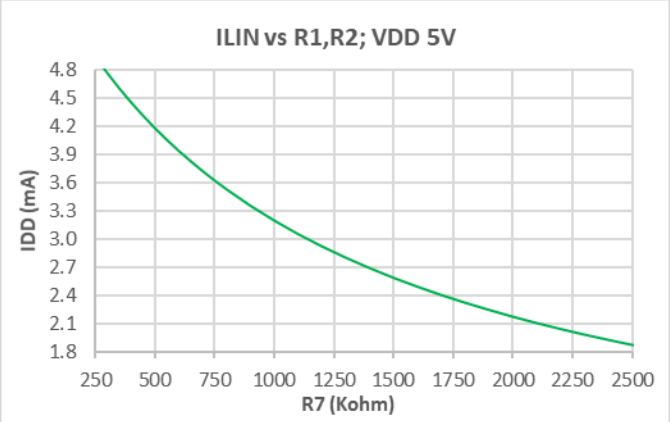
The linearizer is a fixed pre-distortion circuit that can correct for 3rd order non-linearity. The amount of pre-distortion correction is set by the linearizer bias current, ILIN. The linearizer circuit is coupled to the RF path through C7 and C8. Disconnecting C7 and C8 will disable the linearizer which causes the gain to increase slightly (~0.5dB) but will also degrade S11 and OIP3.

In the application circuit, R1 and R2 are used to set ILIN to a value optimized for the desired operating conditions. ILIN can be calculated using the equation below.

ILIN = 2*(Vdd – 1.6V)/(R1 + 1125)

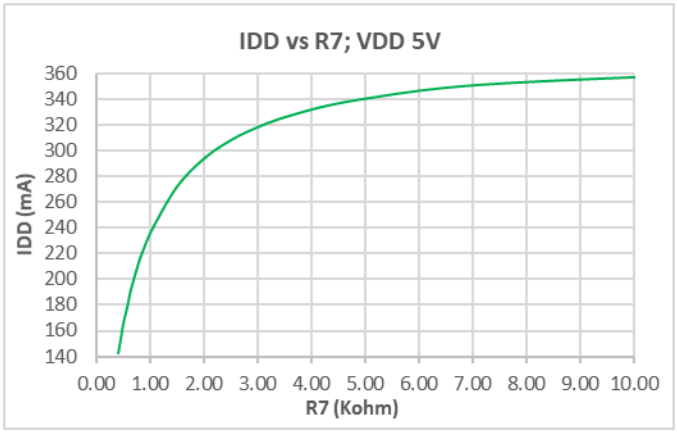
The value of ILIN has been optimized for QPL8832 for 5V, 280mA. In applications with alternate values of VDD or IDD, ILIN can be reoptimized to improve linearity by checking for best MER at several frequencies across the desired operating conditions (flat, tilt, etc).

The graph on the right hand side shows the change in ILIN vs. R1, R2 for 5V VDD.



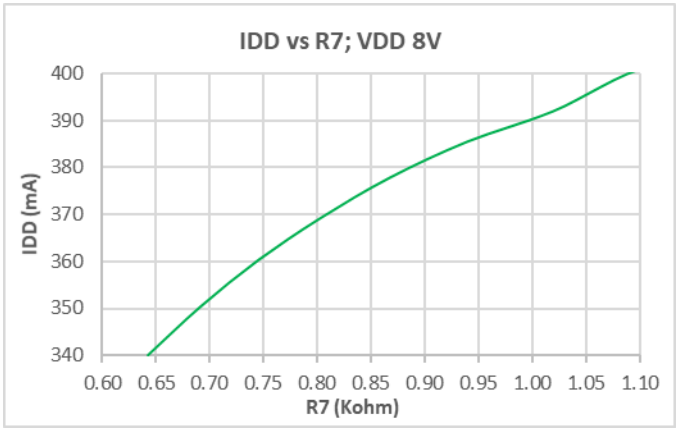
ISET Resistor Value

R7 is used to set the device current. In the QPL8832 application circuit, the value of R7 is set for an IDD of 280mA for 5V and 360mA for 8V to optimize MER. In applications where reduced linearity is acceptable, IDD can be reduced lowering the value of R7 (see graphs below).

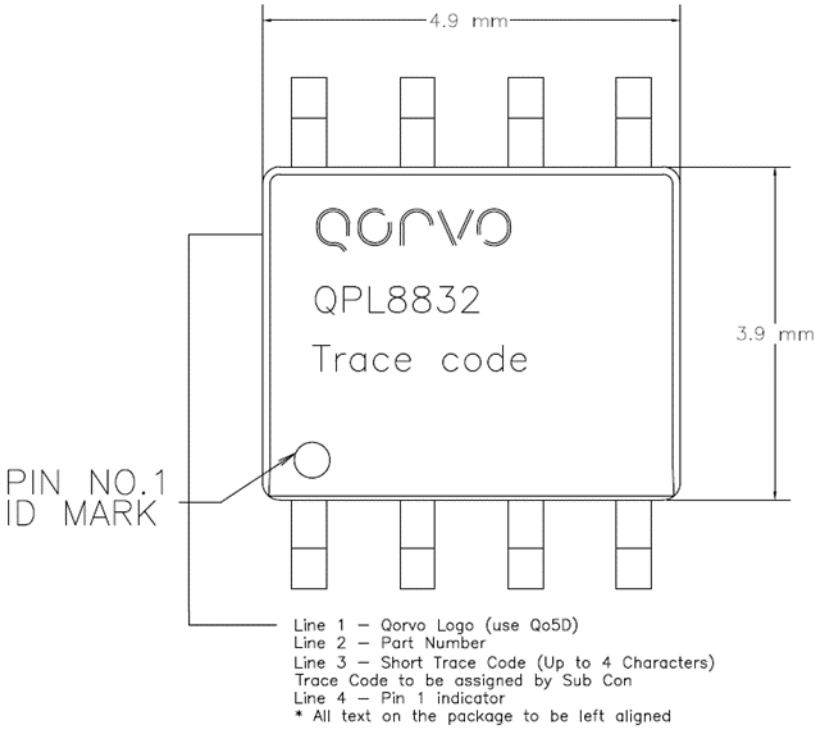


VG2 Resistor Value Settings

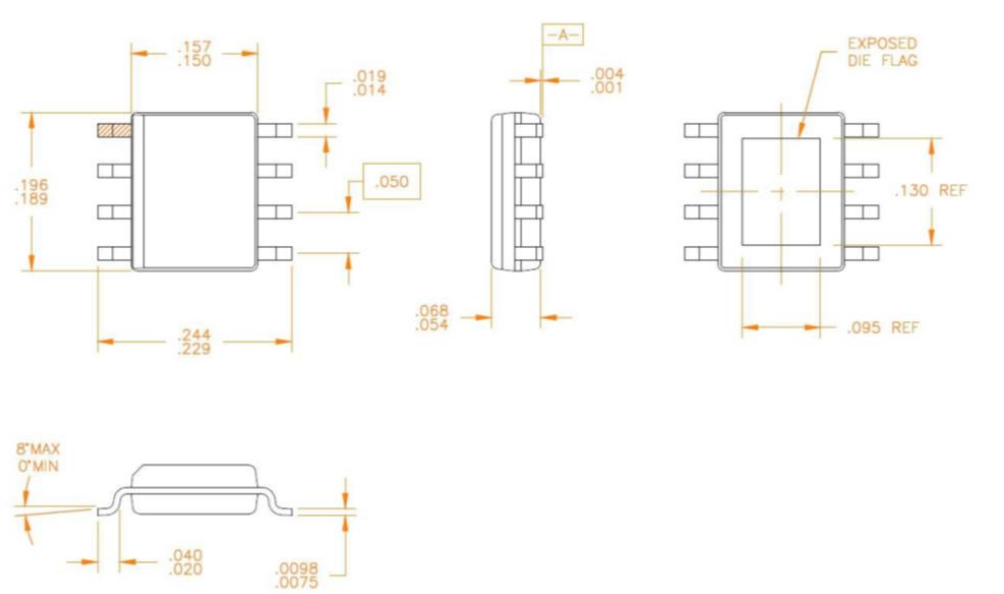
VG2 (pin 6) is connected to the gate of the output device. Resistor R8 is used to fine tune VG2 for best linearity. It is not normally necessary or recommended to tune VG2.



Package Marking



Package Outline

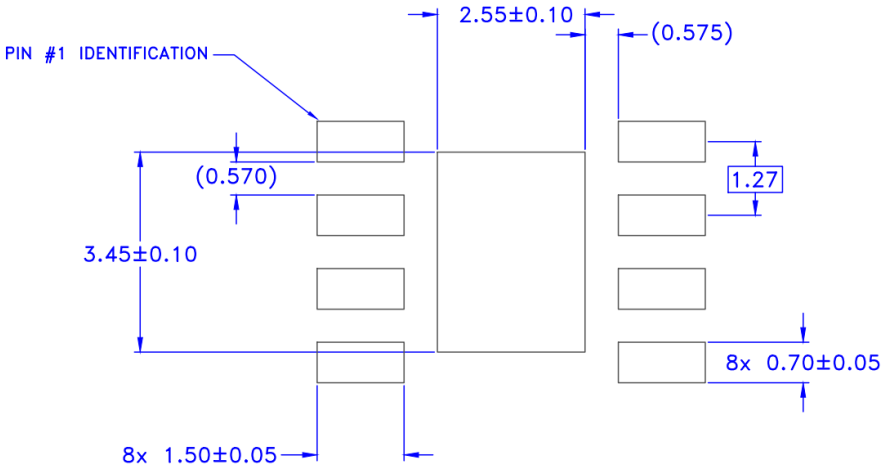


1. All dimensions are in inches. Angles are in degrees.

Notes:
1. All Dimensions are in inches.
2. Angles are in degrees.

Notes: All dimensions are in millimeters. Angles are in degrees.

Recommended Mounting Pattern



1. Use 1 oz. copper minimum for top and bottom layer metal.
2. Vias are required under the backside paddle for proper RF / DC grounding and thermal dissipation.
3. Recommend a 0.35 mm diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (10mils).