QPL9058

0.5 – 6.0 GHz Ultra Low-Noise LNA

Product Overview

The QPL9058 is a high-linearity, ultra-low noise amplifier in a small 2 x 2 mm surface-mount package. At 3.6 GHz, the amplifier typically provides 18 dB gain, +36 dBm OIP3 at a 54 mA bias setting, and 0.6 dB noise figure. The LNA can be biased from a single positive supply ranging from 3.3 to 5 volts. The device is housed in a green/RoHS-compliant industry-standard 2x2 mm package.

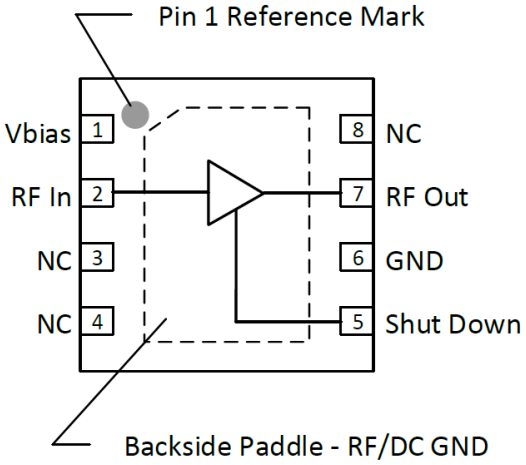
The QPL9058 is bias adjustable and requires minimal external components to operate. It also has a power down control capability integrated into the die for TDD applications.

8 Pin 2X2 mm DFN Package

Key Features

- 0.5-6.0 GHz Operational Bandwidth
- Low noise figure, 0.6 dB NF @ 3.6 GHz
- 36 dBm OIP3
- 18 dB small signal gain
- Bias adjustable for linearity optimization
- Unconditionally stable
- Shut-down mode pin with 1.8V logic
- Maintains OFF state with high Pin drive

Functional Block Diagram



Top View

Applications

- 5G m-MIMO
- Repeaters / DAS
- Mobile Infrastructure
- LTE / WCDMA / CDMA / GSM
- General Purpose Wireless
- TDD or FDD systems

Ordering Information

Part No.	Description
QPL9058TR7	2500 pieces on a 7” reel
QPL9058EVB-01	0.5-6.0 GHz Evaluation Board

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-65 to +150°C
Supply Voltage (V_{DD})	+7 V
RF Input Power, CW, 50 Ω, T=25°C	+27 dBm
RF Input Power, LTE 9dB PAR, T=25°C	+22 dBm

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Supply Voltage (V_{DD})	+3.15	+5	+5.25	V
T_{CASE}	−40		+105	°C
Tj for >10^6 hours MTTF			+190	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions. Application of conditions to the device outside the Recommended Operating Conditions may reduce device reliability and performance.

Electrical Specifications

Test conditions unless otherwise noted: V_{DD}=+5 V, Temp.=+25 °C, 50 Ω system.

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		500		6000	MHz
Test Frequency			3600		MHz
Gain		16.5	18.0	19.9	dB
Input Return Loss			15.0		dB
Output Return Loss			19.5		dB
Noise Figure (1)			0.59	0.95	dB
Output P1dB		+17.7	+20.6		dBm
Output IP3	Pout=+2 dBm/tone, Δf=1 MHz	+32.0	+36.4		dBm
Power Shutdown Control (pin 5)	On state	0		0.63	V
	Off state (Power down)	1.17		V_{DD}	V
Current, I_{DD}	On state		54	74	mA
	Off state (Power down)		4	7	mA
Shutdown pin current, I_{SD}	V_{PD} = 1.8 V		18		µA
Switching Time (LNA On)	50% DC to 0.5dB of settled power/gain		60		ns
Switching Time (LNA Off)	50% DC to -20dB from LNA ON power/gain		41		ns
Thermal Resistance	Channel to case		63.7		°C/W

Notes:
1. Input trace loss de-embedded form NF data.

S-Parameters

Test Conditions: V_{DD}=+5 V, I_{DD}=54 mA (typ.), T=+25°C, unmatched 50 Ω system, calibrated to device leads

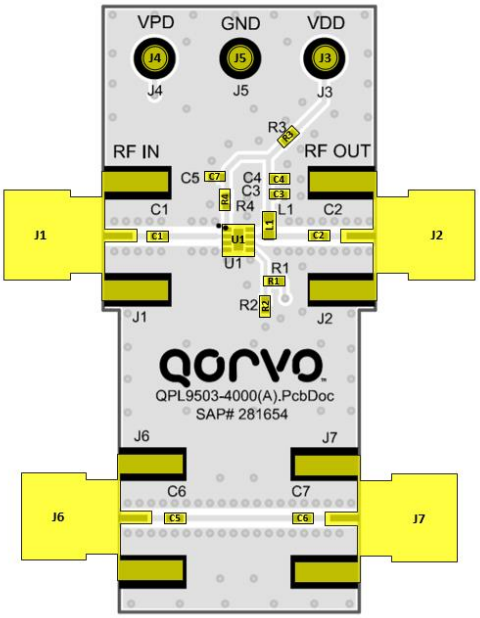
Freq (GHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
2	-13.3	-142	19.4	13	-29.8	-17	-22.9	-21
2.1	-13.8	-145	19.2	8	-29.7	-20	-23.3	-17
2.2	-14.2	-148	19.0	2	-29.6	-23	-23.4	-12
2.3	-14.7	-150	18.9	-4	-29.5	-26	-23.5	-8
2.4	-15.1	-152	18.7	-9	-29.5	-29	-23.5	-4
2.5	-15.4	-153	18.6	-15	-29.5	-33	-23.4	-2
2.6	-15.7	-154	18.5	-20	-29.5	-36	-23.4	1
2.7	-15.9	-155	18.5	-26	-29.5	-40	-23.3	1
2.8	-16.1	-155	18.4	-32	-29.5	-43	-23.4	2
2.9	-16.1	-155	18.4	-37	-29.5	-47	-23.6	1
3	-16.0	-155	18.4	-43	-29.5	-51	-24.1	1
3.1	-15.7	-155	18.4	-49	-29.6	-55	-24.6	-1
3.2	-15.4	-155	18.5	-55	-29.6	-59	-25.6	-4
3.3	-15.0	-156	18.5	-61	-29.7	-63	-26.9	-9
3.4	-14.4	-157	18.6	-67	-29.8	-67	-29.2	-17
3.5	-13.8	-158	18.7	-73	-29.8	-72	-32.2	-34
3.6	-13.3	-159	18.8	-79	-29.9	-77	-36.5	-61
3.7	-12.9	-160	18.9	-86	-30.0	-82	-45.1	-87
3.8	-12.2	-163	19.0	-92	-30.1	-87	-33.3	-168
3.9	-11.3	-167	19.1	-99	-30.3	-93	-26.4	175
4	-10.6	-172	19.2	-106	-30.4	-99	-22.4	168
4.1	-9.8	-177	19.3	-114	-30.6	-105	-19.2	162
4.2	-9.1	177	19.3	-122	-30.8	-112	-16.7	155
4.3	-8.5	171	19.3	-130	-31.1	-119	-14.5	150
4.4	-7.9	165	19.3	-138	-31.4	-126	-12.8	143
4.5	-7.4	159	19.2	-146	-31.8	-134	-11.2	137
4.6	-6.9	152	19.1	-154	-32.2	-142	-9.9	130
4.7	-6.6	146	18.9	-162	-32.6	-149	-8.8	125
4.8	-6.3	140	18.7	-170	-33.1	-157	-7.8	118
4.9	-6.1	133	18.4	-178	-33.6	-165	-7.0	113
5.0	-6.0	127	18.1	174	-34.1	-173	-6.3	107

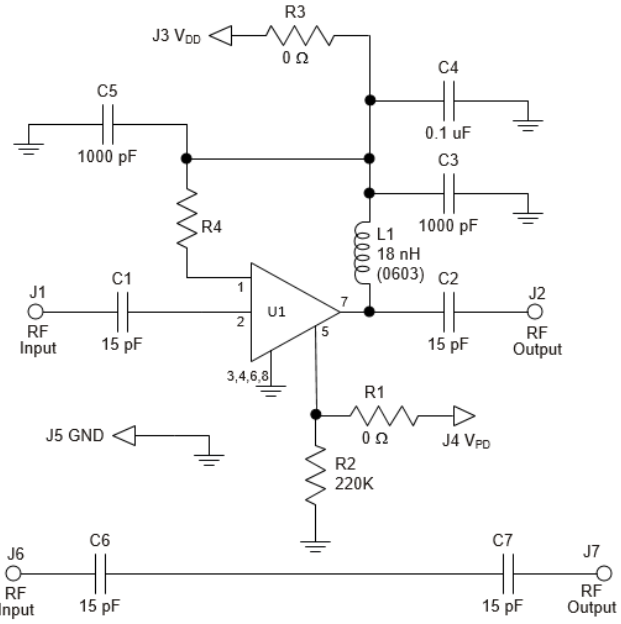
Noise Parameters

Test Conditions: V_{DD}=+5 V, I_{DD}=54 mA (typ.), T=+25°C, unmatched 50 ohm system, calibrated to device leads

Freq (GHz)	NF_{min} (dB)	GammaOpt (mag)	GammaOpt (deg)	r_n (Ω)
2.0	0.22	0.14	66	0.048
2.1	0.26	0.08	81	0.048
2.2	0.29	0.12	72	0.047
2.3	0.28	0.10	90	0.048
2.4	0.34	0.08	83	0.052
2.5	0.36	0.06	111	0.053
2.6	0.37	0.12	104	0.046
2.7	0.39	0.11	110	0.049
2.8	0.43	0.10	116	0.052
2.9	0.39	0.14	121	0.046
3.0	0.49	0.06	150	0.062
3.1	0.42	0.14	127	0.049
3.2	0.49	0.14	125	0.052
3.3	0.47	0.19	127	0.046
3.4	0.46	0.22	139	0.040
3.5	0.60	0.08	148	0.065
3.6	0.54	0.19	131	0.050
3.7	0.52	0.20	133	0.050
3.8	0.55	0.11	-123	0.051
3.9	0.52	0.17	135	0.055
4.0	0.55	0.18	147	0.052
4.1	0.54	0.16	154	0.055
4.2	0.57	0.16	165	0.055
4.3	0.58	0.16	161	0.050
4.4	0.59	0.17	156	0.051
4.5	0.59	0.20	-168	0.052
4.6	0.56	0.17	180	0.046
4.7	0.58	0.16	-179	0.045
4.8	0.55	0.18	178	0.047
4.9	0.56	0.16	-171	0.048
5.0	0.58	0.16	-168	0.050

Evaluation Board – QPL9058EVB-01





Notes:
1. See Evaluation Board PCB Information section for material and stack-up.
2. All components are of 0402 size unless otherwise mentioned.
3. For TDD Applications: R1 = 0Ω and R2 = 220K.
4. For FDD Applications: R2 = 220K 'OR' Pin 5 tied to ground. R1 = DNP/Omitted
5. A through line is included on the evaluation board to de-embed the board losses.
6. R4 sets the current draw. Can be changed for the desired bias point.

Bill of Material – QPL9058EVB-01

Reference Des.	Value	Description	Manuf.	Part Number
N/A	N/A	Printed Circuit Board	Qorvo	
U1	n/a	Ultra Low Noise QPL9058 LNA	Qorvo	QPL9058
R1, R3	0 Ω	Resistor, chip, 0402, 1%, 1/10W	various	
R2	220 KΩ	Resistor, chip, 0402, 5%, 1/16W	various	
R4	3.83 KΩ	Resistor, Chip, 0402, 1%, 1/16W	various	
C1, C2, C6, C7	15 pF	Cap., Chip, 0402, 2%, 50V, HI-Q	Murata	GJM1555C1H150JB01D
C3. C5	1000 pF	Cap., Chip, 0402, 10%, 50V, X7R	Murata	GRM155R71H102KA01D
C4	0.1 uF	Cap., Chip, 0402, 10%, 50V, X5R	various	
L1	18 nH	Inductor, coil, 0603, 5%	Coilcraft	0603CS-18NXJL

R4 Resistor values for various I_{DD} settings

I_{DD} (mA)		40	45	50	55	60	65	70	75
R4	VDD = 5 V	5.75K	4.8K	4.1K	3.7K	3.12K	2.8K	2.5K	2.27K
R4	VDD = 3.3 V	2.9K	2.4K	2.05K	1.75K	1.53K	1.33K	1.2K	1.05K

Typical Performance – QPL9058EVB-01

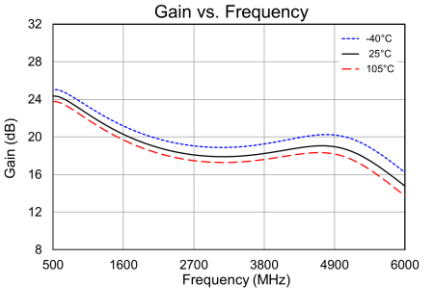
Test conditions unless otherwise noted: V_{DD} = +5 V, I_{DD} = 54 mA (typ.), Temp = +25°C

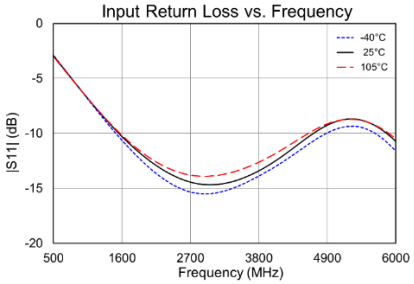
Parameter	Conditions	Typical Values			Units
Frequency		2500	3600	4900	MHz
Gain		18.2	18.0	18.9	dB
Input Return Loss		14.3	14.7	9.8	dB
Output Return Loss		23.1	20.0	13.5	dB
Output P1dB		20.6	20.5	16.6	dBm
OIP3	Pout=+2 dBm/tone, Δf=1 MHz	32.6	36.0	33.9	dBm
Noise figure (1)		0.47	0.62	0.56	dB

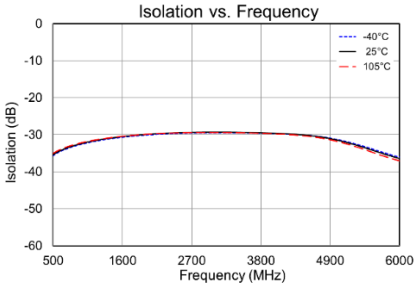
Note:
1. Input trace loss de-embedded from NF data

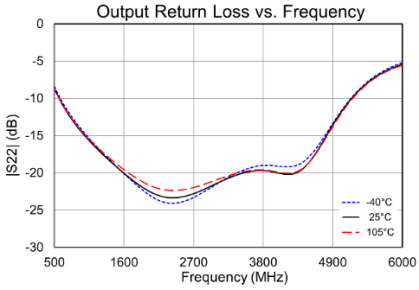
Performance Plots – QPL9058EVB-01

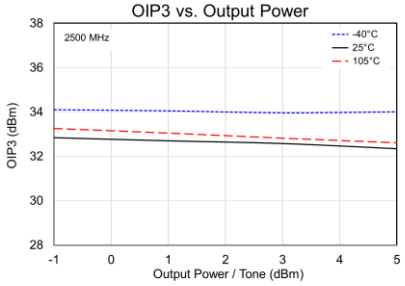
Test conditions unless otherwise noted: V_{DD} = +5 V, I_{DD} = 54 mA, 50 Ω system

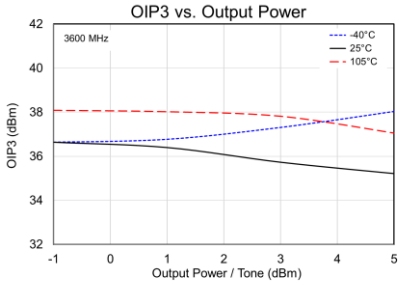


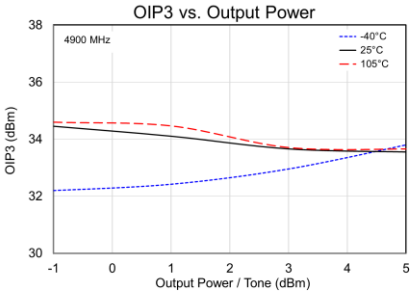


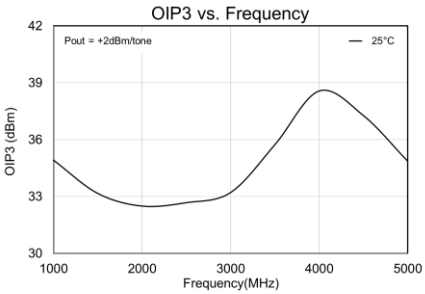


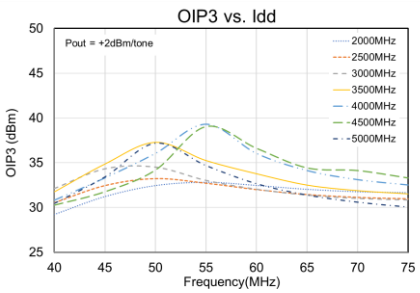






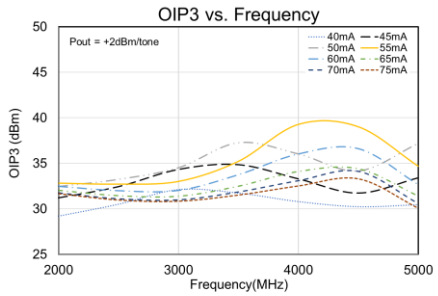


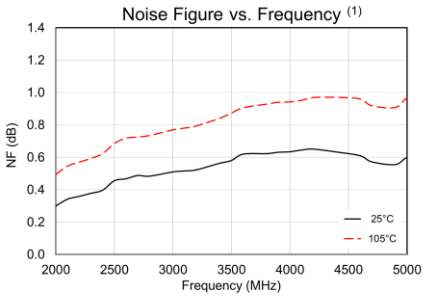


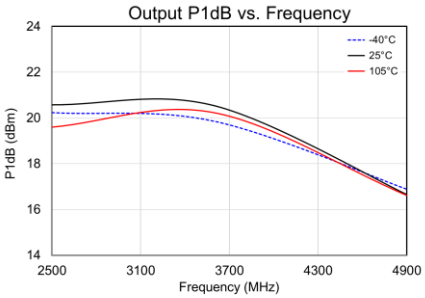


Performance Plots – QPL9058EVB-01 Continued

Test conditions unless otherwise noted: V_{DD} = +5 V, I_{DD} = 54 mA, 50 Ω system







Notes:

1. Input trace loss de-embedded from NF. NF at cold temp is better than 0.3dB causing measurement uncertainties. Therefore, not shown on the plot

Typical Performance – QPL9058EVB-01

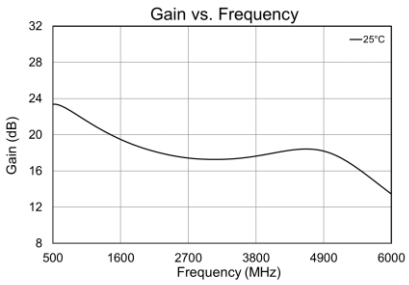
Test conditions unless otherwise noted: V_{DD} = +3.3 V, I_{DD} = 50 mA, Temp = +25°C

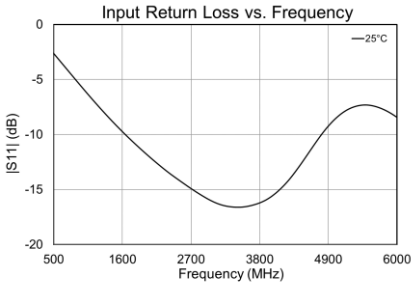
Parameter	Conditions	Typical Values			Units
Frequency		2500	3500	5000	MHz
Gain		17.6	17.4	18.0	dB
Input Return Loss		14.1	16.6	8.6	dB
Output Return Loss		18.0	15.2	12.2	dB
Output P1dB		15.8	17.6	13.8	dBm
OIP3	Pout=+0 dBm/tone, Δf=1 MHz	32.3	33.0	32.8	dBm
Noise figure (1)		0.48	0.59	0.56	dB

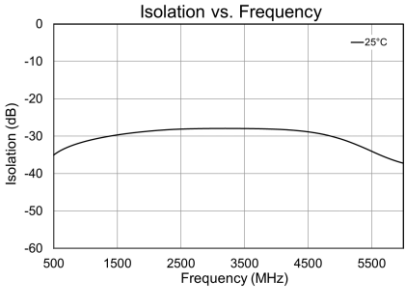
Notes:
1. Input trace loss de-embedded from NF data

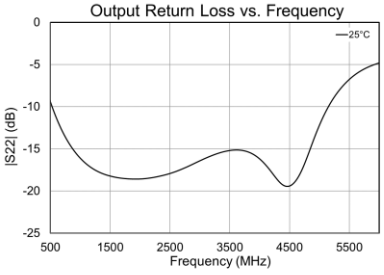
Performance Plots – QPL9058EVB-01

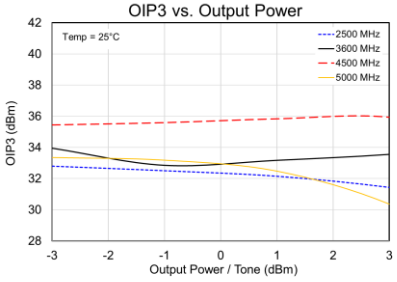
Test conditions unless otherwise noted: V_{DD} = +3.3 V, I_{DD} = 50 mA, Temp = +25°C, 50 Ω system

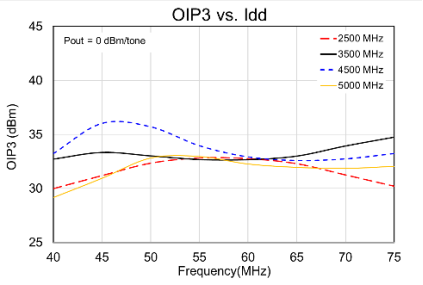


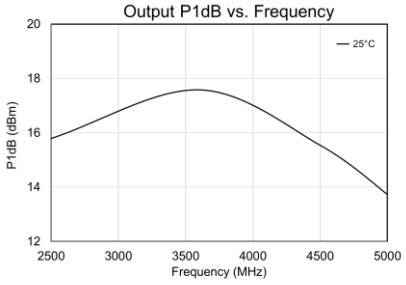


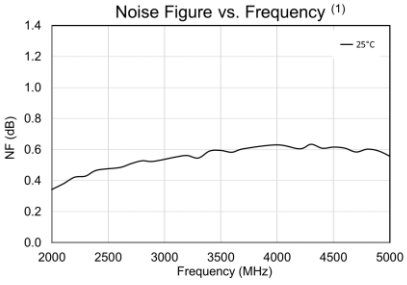






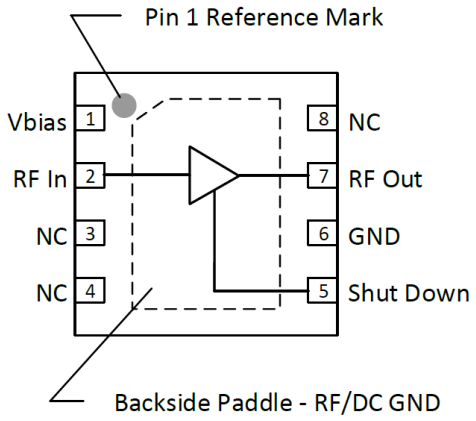






Note:
1. Input trace loss de-embedded from NF data.

Pad Configuration and Description

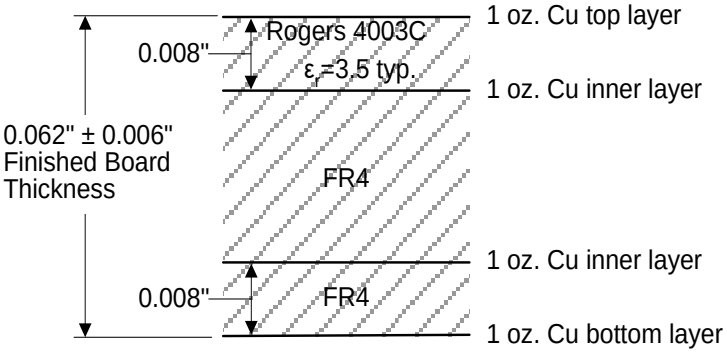


Top View

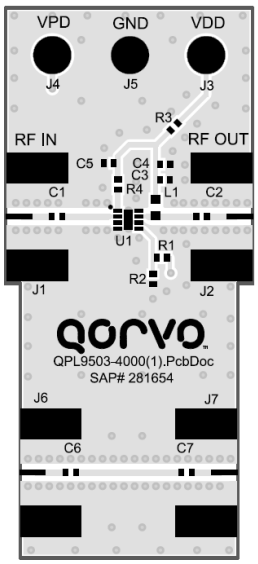
Pad No.	Label	Description
1	V_{bias}	Sets the LNA bias current for the device.
2	RF In	RF Input pin, internally matched to 50 ohms. A DC block is required.
5	Shut Down	A high voltage (>1.17V) turns off the device. If the pin is pulled to ground or driven with a voltage less than 0.63V, then the device will operate under LNA ON state.
7	RF Out	RF Output pin, internally matched to 50 ohms. A DC block is required. V_{DD} supply pin.
3, 4, 6, 8	NC	Not connected internally. This pin may be left floating or connected to ground.
Backside Paddle	RF/DC GND	Ground connection. The back side of the package should be connected to the ground plan though as short of a connection as possible. PCB vias under the device are recommended.

Evaluation Board PCB Information

Qorvo PCB Material and Stack-up

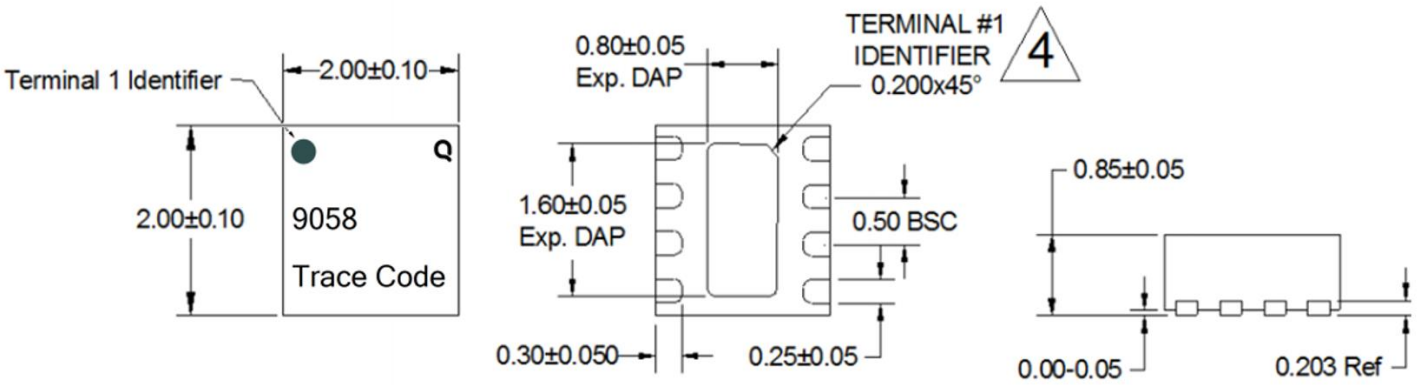


50 ohm line dimensions: width = 0.0182”, spacing = 0.020”



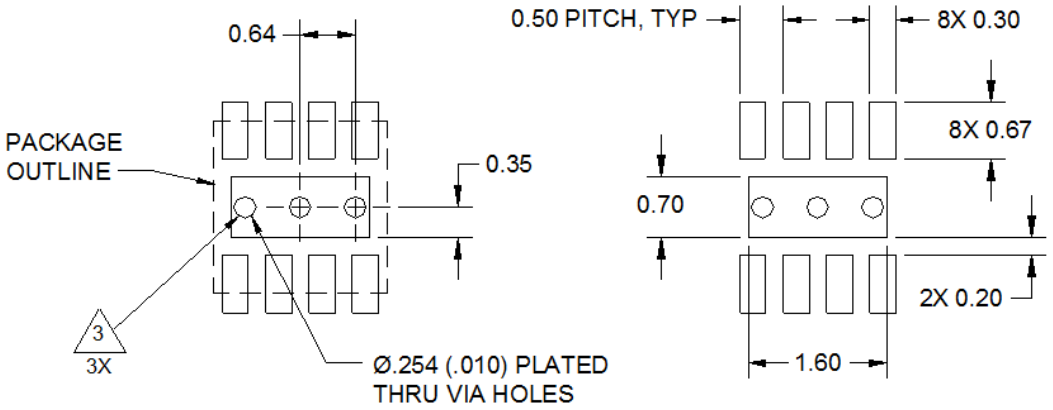
Package Marking and Dimensions

Marking: Part Number – 9058
Trace Code – XXXX up to 4 Characters assigned by sub-contractor



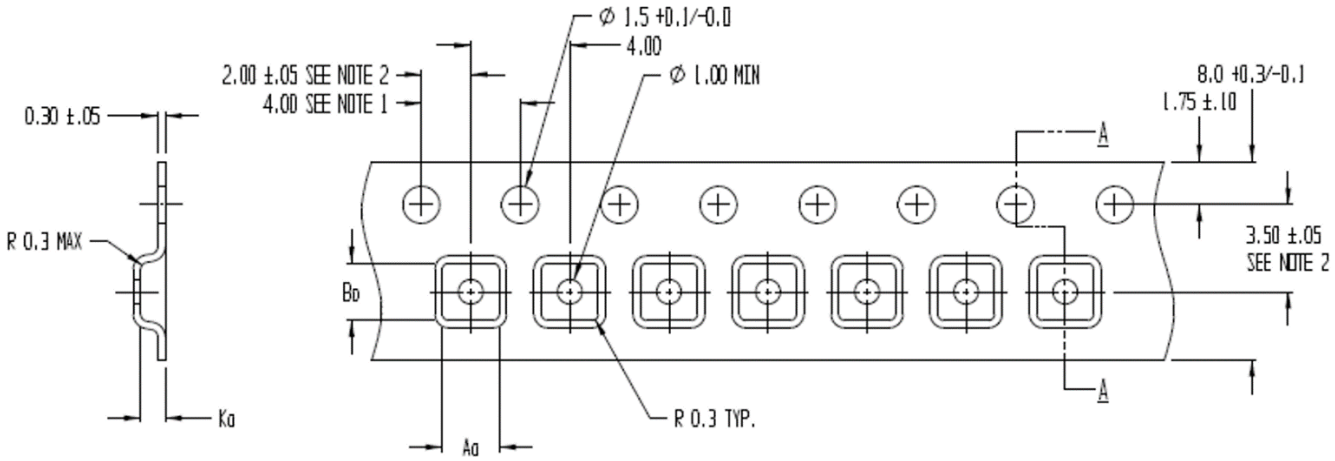
Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. The terminal #1 identifier and terminal numbering conform to SPE-000677.
3. Contact plating: NiPdAu

Recommended PCB Layout Pattern

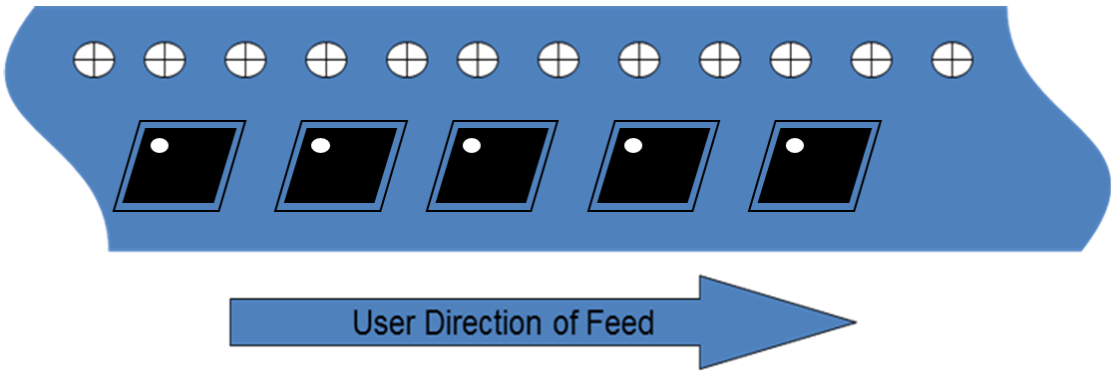


Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Via holes are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.01").
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

Tape and Reel Information – Carrier and Cover Tape Dimensions

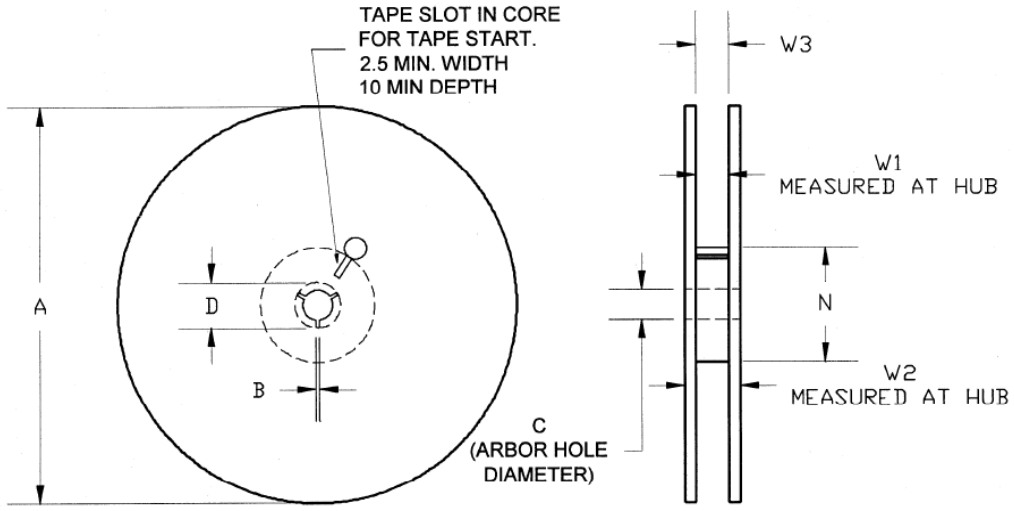


Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.091	2.30
	Width	B0	0.091	2.30
	Depth	K0	0.039	1.00
	Pitch	P1	0.157	4.00
Centerline Distance	Cavity to Perforation - Length Direction	P2	0.079	2.00
	Cavity to Perforation - Width Direction	F	0.138	3.50
Cover Tape	Width	C	0.213	5.40
Carrier Tape	Width	W	0.315	8.00



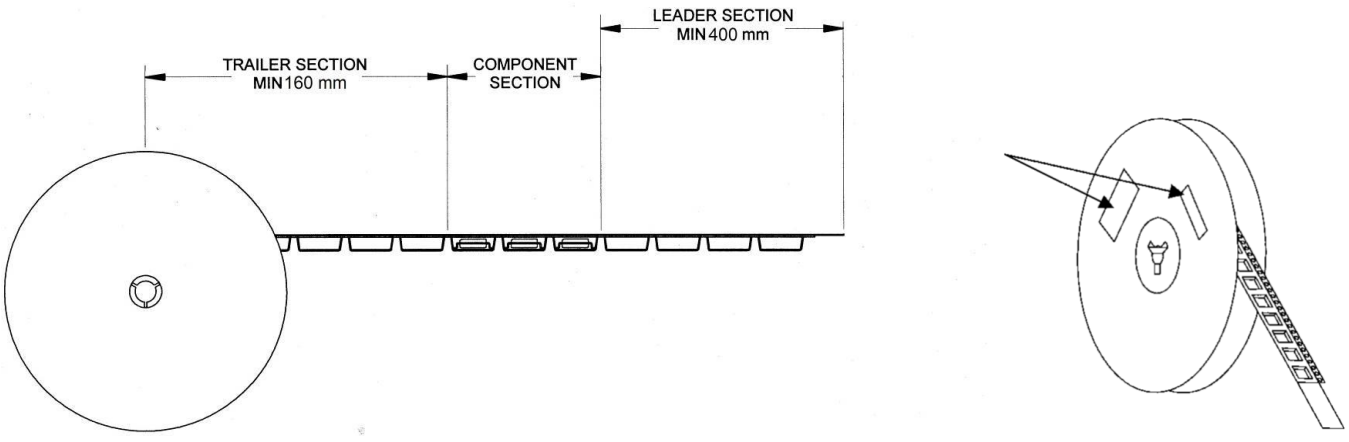
Tape and Reel Information – Reel Dimensions

Standard T/R size = 2500 pieces on a 7” reel.



Feature	Measure	Symbol	Size (in)	Size (mm)
Flange	Diameter	A	6.969	177.0
	Thickness	W2	0.559	14.2
	Space Between Flange	W1	0.346	8.8
Hub	Outer Diameter	N	2.283	58.0
	Arbor Hole Diameter	C	0.512	13.0
	Key Slit Width	B	0.079	2.0
	Key Slit Diameter	D	0.787	20.0

Tape and Reel Information – Tape Length and Label Placement



Notes:
1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481-1-A.
2. Labels are placed on the flange opposite the sprockets in the carrier tape.