QPL9098

Ultra-Low Noise, Bypass LNA

General Description

The QPL9098 is a high-linearity, ultra-low noise gain block amplifier with a bypass mode functionality integrated in the product. At 5.5 GHz, the amplifier typically provides 19.6 dB gain, +32 dBm OIP3, and 1.3 dB noise figure while drawing 68 mA current from a +4.2 V supply.

The QPL9098 is internally matched using a high-performance E-pHEMT process and only requires four external components for operation from a single positive supply: an external RF choke and blocking/bypass capacitors. This low noise amplifier contains an internal active bias to maintain high performance over temperature.

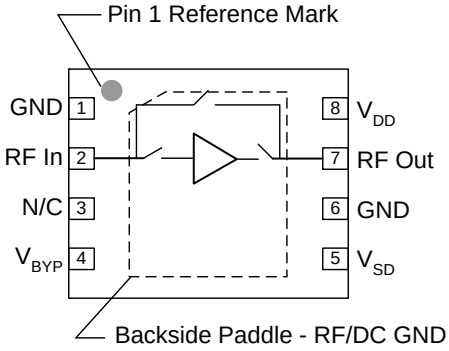
The QPL9098 is optimized for the 4.0 – 6.0 GHz frequency band and is targeted for wireless infrastructure. QPL9098 is packaged in a 2 x 2 mm DFN.

8 Pin 2X2 mm DFN Package

Product Features

- 4.0 – 6.0 GHz Operational bandwidth
- LNA with integrated bypass mode
- Ability to turn LNA and bypass mode OFF
- Ultra-low noise, 1.3 dB at 5.0 GHz
- 19.6 dB Gain at 5.5 GHz
- +32 dBm Output IP3 in LNA Mode
- +40 dBm Output IP3 in Bypass Mode

Functional Block Diagram



Top View

Applications

- Base-station Receivers
- Repeaters / DAS
- Tower Mounted Amplifiers
- Mobile Infrastructure
- General Purpose Wireless
- TDD or FDD systems

Ordering Information

Part No.	Description
QPL9098TR7	2500 pcs on 7” reel
QPL9098EVB-01	Evaluation Board

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−65 to 150°C
Supply Voltage (V_{DD})	+7 V
RF Input Power, CW, 50Ω, T=25°C	+20 dBm

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Supply Voltage (V_{DD})	3.0	4.2	5.25	V
T_{CASE}	−40		+105	°C
T_j at T_{CASE} = 125°C			+142	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: V_{DD} = +4.2 V, Temp.=+25°C.

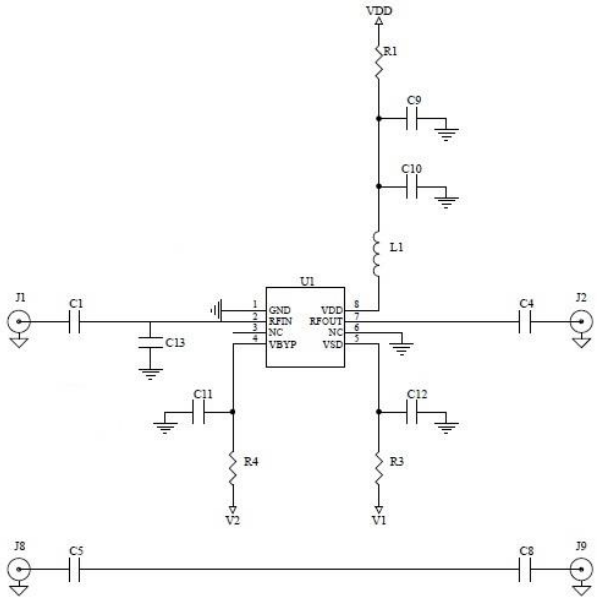
Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		4000		6000	MHz
Test Frequency			5500		MHz
Gain	LNA ON, Bypass OFF	17.5	19.6	22.5	dB
Input Return Loss	LNA ON, Bypass OFF		11		dB
Output Return Loss	LNA ON, Bypass OFF		12		dB
Noise Figure (2)	LNA ON, Bypass OFF		1.3	1.8	dB
Output P1dB (1)	LNA ON, Bypass OFF	+14	+16		dBm
Output IP3	LNA ON, Bypass OFF, Pout=+2 dBm/tone, Δf=5 MHz	+28	+32		dBm
Output IP3	LNA OFF, Bypass ON Pin=+2 dBm/tone, Δf=5 MHz	+30	+36		dBm
Insertion Loss	LNA OFF, Bypass ON		2.0	3	dB
Output Return Loss	LNA OFF, Bypass ON		12		dB
Isolation	LNA OFF, Bypass OFF		16		dB
Control Voltage, V_1, V_2	V_{IH}	1.17		V_{DD}	V
	V_{IL}	0		0.63	V
Current, I_D	LNA ON		65	90	mA
	Bypass ON		5	10	mA
	LNA OFF, Bypass OFF		5	10	mA
Switching Time (1)	LNA-Bypass (50% Vctrl to 10% RF)		50	1000	ns
	Bypass-LNA (50% Vctrl to 90% RF)		600	1000	ns
	LNA-OFF (50% Vctrl to 10% RF)		50	1000	ns
	OFF-LNA (50% Vctrl to 90% RF)		500	1000	ns
Thermal Resistance, θ_{jc}	Channel to case		44		°C/W

1. Minimum or maximum specifications listed are guaranteed by design. Not tested in production.
2. Input trace loss de-embedded from noise figure data.

Control Truth Table

V_{BYP} (Pin 4)	V_{SD} (Pin 5)	State
0	0	LNA ON, Bypass OFF
0	1	LNA OFF, Bypass OFF
1	x	LNA OFF, Bypass ON

QPL9098 Evaluation Board



Notes:
1. A through line is included on the evaluation board to de-embed the board losses.
2. Input tuning shunt capacitor (C13) should be placed 50 mils (1.27mm) away from device edge.

Bill of Material – QPL9098 Evaluation Board

Reference Des.	Value	Description	Manuf.	Part Number
PCB	--	Printed Circuit Board	Qorvo	
U1	--	Ultra-Low Noise, Bypass LNA	Qorvo	QPL9098
C11, C12	20 kΩ	RES, 0402, 1%, 1/10W	Various	
R1, R3, R4	0 Ω	RES, 0402, 1/10W	Various	
C1, C4, C5, C8	18 pF	CAP, 0402, 5%, 50V	Murata	GRM1555C1H180JA01D
C9	1000 pF	CAP, 0402, 10%, 50V	Murata	GRM155R71H102KA01D
C10	1.0 µF	CAP, 0402, 10%, 10V, X5R	Murata	GRM155R61A105KE15D
L1	6 nH	IND, 0603, 5%, WW	Coilcraft	0603HP-6N0XJEW
C13	0.4 pF	CAP, 0402, 50V	Murata	GJM1555C1HR50BB01E

Typical Performance (LNA Mode)

Test conditions unless otherwise noted: V_{DD} = +4.2 V, V_1 = 0.63V, V_2 = 0.63V, I_D =68 mA, Temp.=+25 °C.

Parameter	Typical Value				Units
Frequency	4.4	5.0	5.5	6.0	GHz
Gain	18.9	20.5	19.7	16.7	dB
Noise Figure	1.2	1.2	1.3	1.5	dB
Input Return Loss	9.4	12.9	12	8.2	dB
Output Return Loss	8.6	7.3	11.9	13.2	dB
OIP3 (Pout/tone=+2 dBm, Δf = 1 MHz)	33.4	30.9	31.4	32.2	dBm
P1dB	16.5	16.3	16.6	15.5	dBm

Typical Performance (Bypass Mode)

Test conditions unless otherwise noted: V_{DD} = +4.2 V, V_1 = 1.17V or 0.63V,, V_2 = 1.17V, I_D = 5 mA, Temp.=+25 °C.

Parameter	Typical Value				Units
Frequency	4.4	5.0	5.5	6.0	GHz
Insertion Loss	2.3	2.4	2.4	2.6	dB
Input Return Loss	8.2	8.4	9.2	12.4	dB
Output Return Loss	12.1	12.8	14.1	17.4	dB
OIP3 (Pin/tone=+2 dBm, Δf = 1 MHz)	30.9	40.0	39.1	38.9	dBm

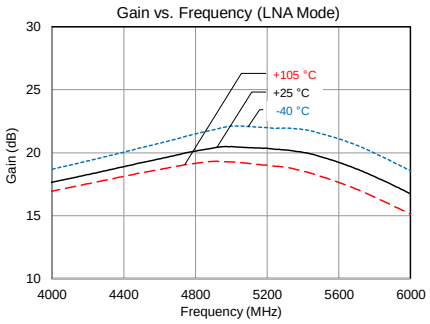
Typical Performance (LNA OFF, Bypass OFF Mode)

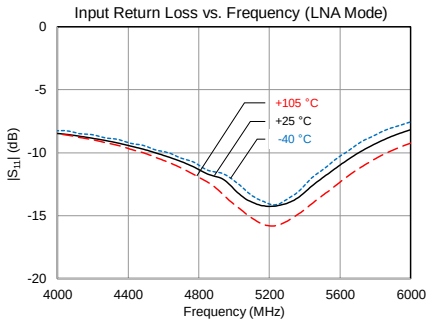
Test conditions unless otherwise noted: V_{DD} = +4.2 V, V_1 = 1.17V, V_2 = 0.63V, Temp. = +25 °C.

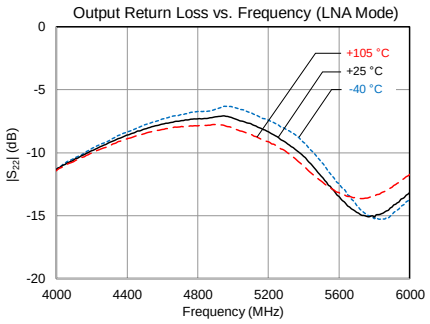
Parameter	Typical Value				Units
Frequency	4.4	5.0	5.5	6.0	GHz
Isolation	16.8	16.5	16.0	13.4	dB

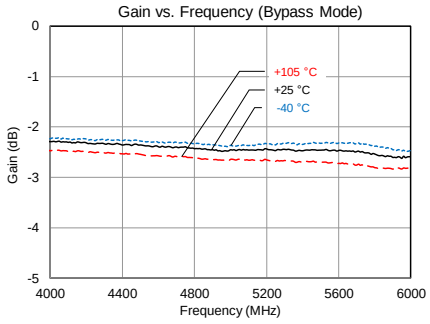
Performance Plots

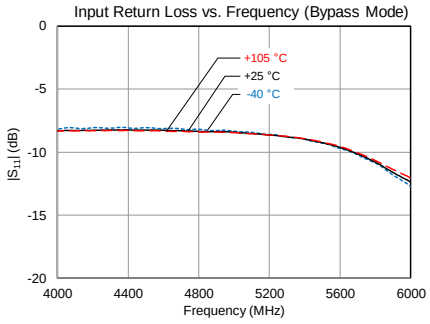
Test conditions unless otherwise noted: V_{DD} = +4.2 V

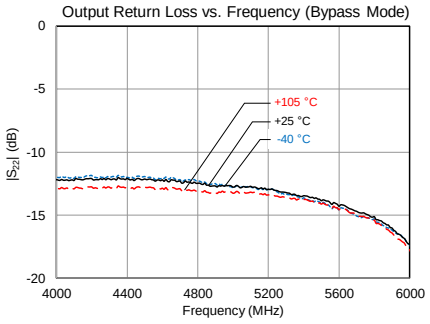


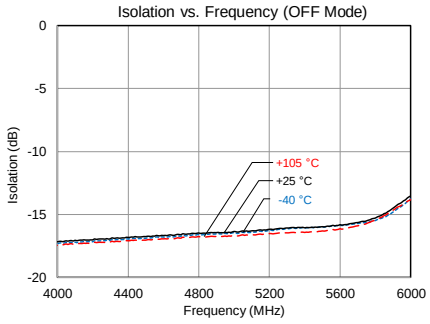


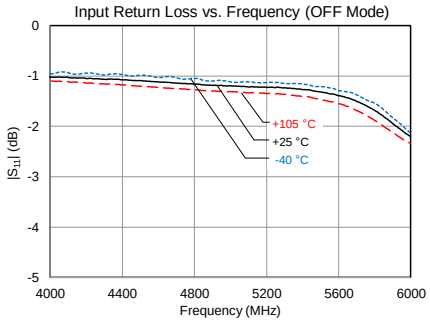


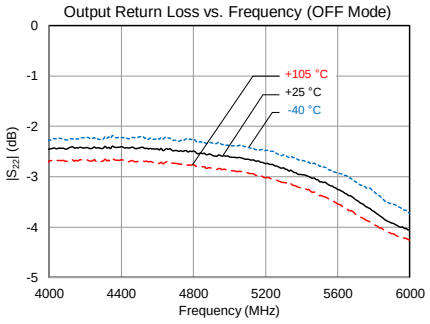


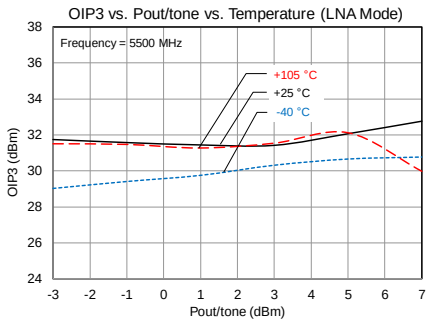


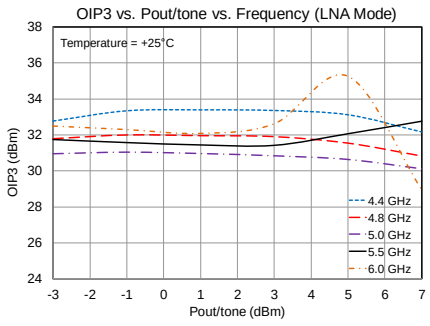


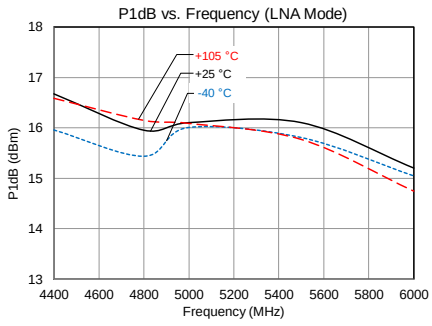






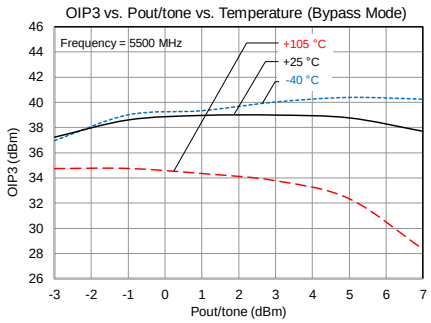


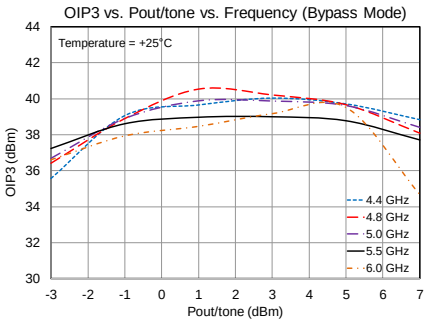


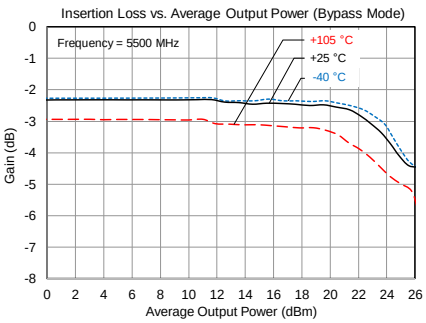


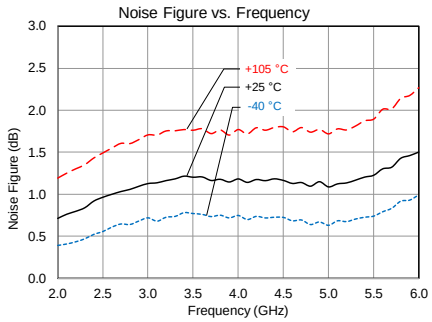
Performance Plots Contd.

Test conditions unless otherwise noted: V_{DD} = +4.2 V









Typical Performance – 3.3V Bias (LNA Mode)

Test conditions unless otherwise noted: V_{DD} = +3.3 V, V_1 = 0.63V, V_2 = 0.63V, Temp.=+25 °C.

Parameter	Typical Value				Units
Frequency	4.4	5.0	5.5	6.0	GHz
Gain	18.7	20.1	19.7	16.7	dB
Noise Figure	1.20	1.15	1.28	1.55	dB
Input Return Loss	9.6	13.5	11.1	6.7	dB
Output Return Loss	8.6	6.5	10.4	11.3	dB
OIP3 (Pout/tone=+2 dBm, Δf = 1 MHz)	32.4	30.4	31.0	33.4	dBm
P1dB	15.0	14.8	14.6	13.3	dBm

Typical data provided above is based on very small sample size of boards tested. Not guaranteed by production data.

Typical Performance – 3.3V Bias (Bypass Mode)

Test conditions unless otherwise noted: V_{DD} = +3.3 V, V_1 = 1.17V or 0.63V, V_2 = 1.17V, Temp.=+25 °C.

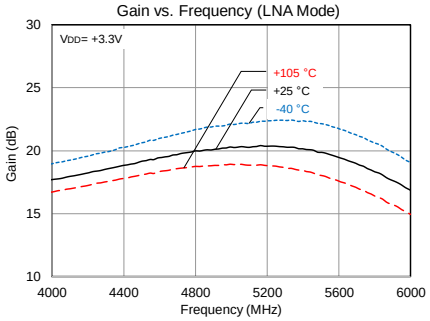
Parameter	Typical Value				Units
Frequency	4.4	5.0	5.5	6.0	GHz
Insertion Loss	2.5	2.7	2.7	2.8	dB
Input Return Loss	7.3	7.3	8.3	12.0	dB
Output Return Loss	10.4	10.3	11.6	15.6	dB
OIP3 (Pin/tone=+2 dBm, Δf = 1 MHz)	40.3	39.8	37.1	35.3	dBm

Typical data provided above is based on very small sample size of boards tested. Not guaranteed by production data.

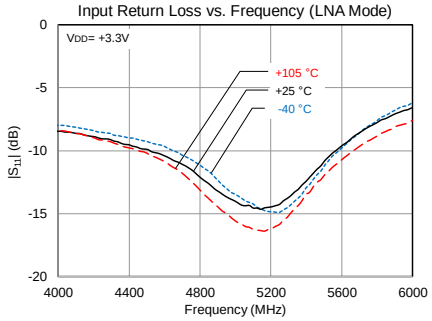
Performance Plots – +3.3V Bias Voltage

Test conditions: V_{DD} = +3.3 V

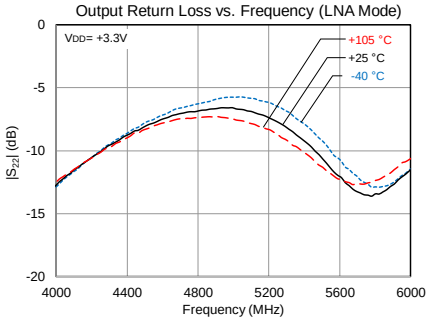
Gain vs. Frequency (LNA Mode)



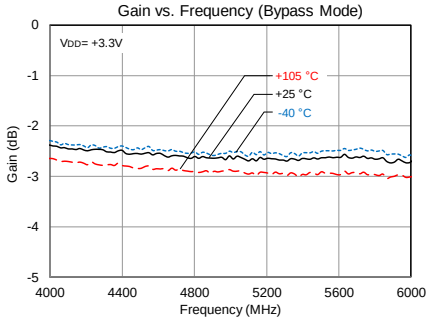
Input Return Loss vs. Frequency (LNA Mode)



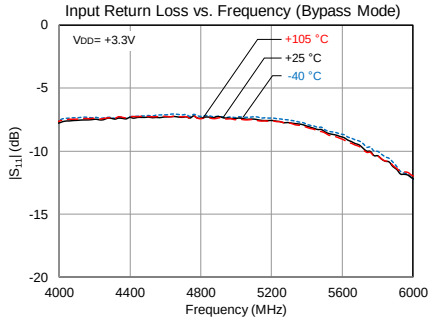
Output Return Loss vs. Frequency (LNA Mode)



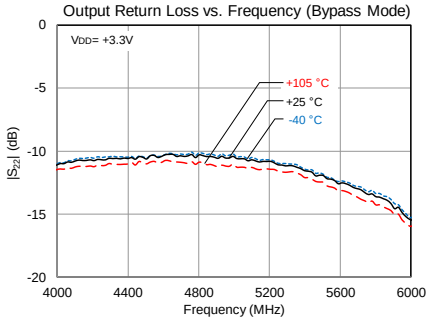
Gain vs. Frequency (Bypass Mode)



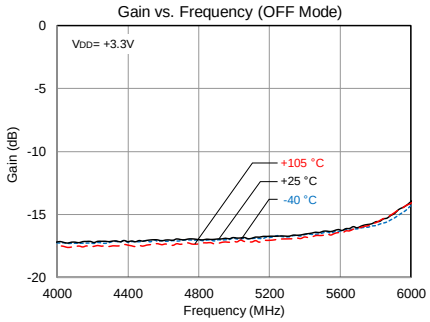
Input Return Loss vs. Frequency (Bypass Mode)



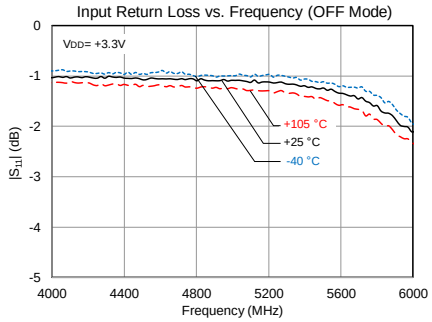
Output Return Loss vs. Frequency (Bypass Mode)



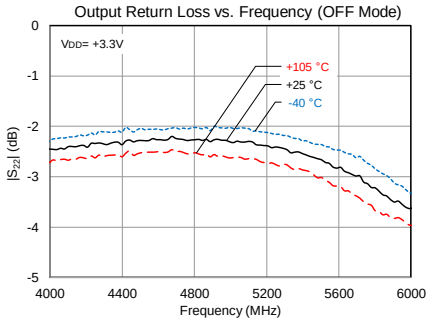
Gain vs. Frequency (OFF Mode)



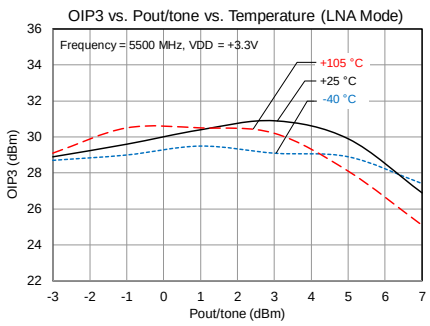
Input Return Loss vs. Frequency (OFF Mode)



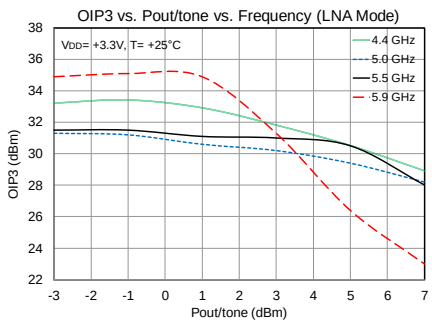
Output Return Loss vs. Frequency (OFF Mode)



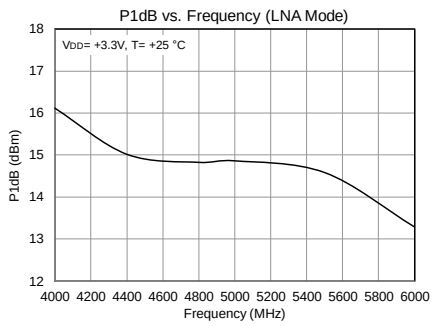
OIP3 vs. Pout/tone vs. Temperature (LNA Mode)



OIP3 vs. Pout/tone vs. Frequency (LNA Mode)

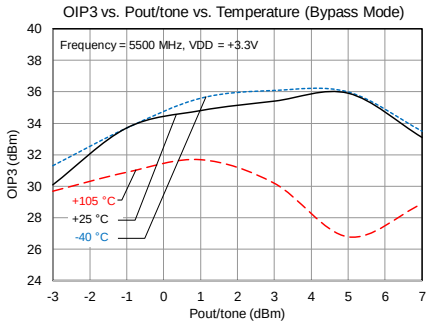


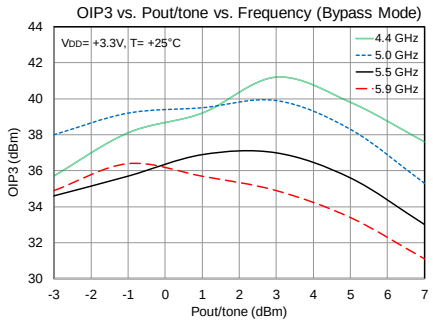
P1dB vs. Frequency (LNA Mode)

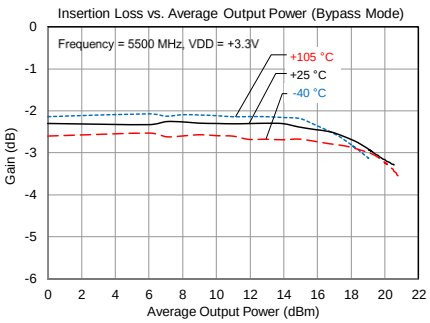


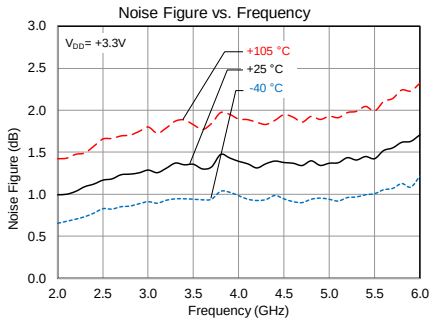
Performance Plots Contd.

Test conditions unless otherwise noted: V_{DD} = +4.2 V

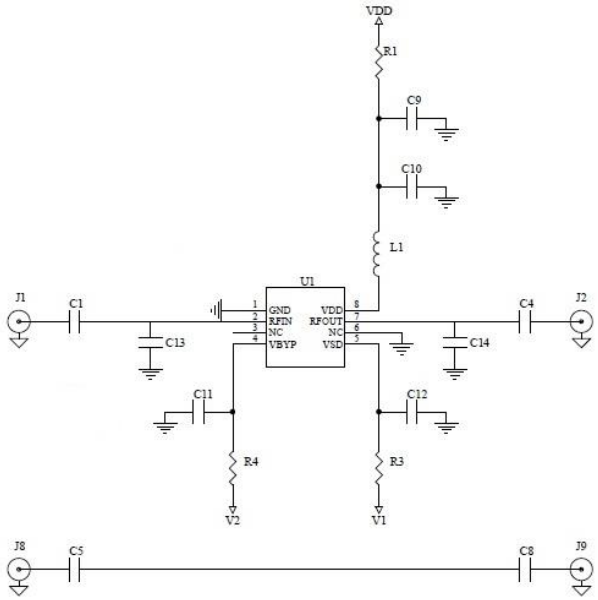








QPL9098 Applications Schematic – Optimized Output Return Loss



Notes:

1. A through line is included on the evaluation board to de-embed the board losses.
2. Input tuning shunt capacitor (C13) should be placed 50 mils (1.27 mm) away from device edge.
3. Output tuning shunt capacitor (C14) should be placed 70 mils (1.78 mm) away from device edge.

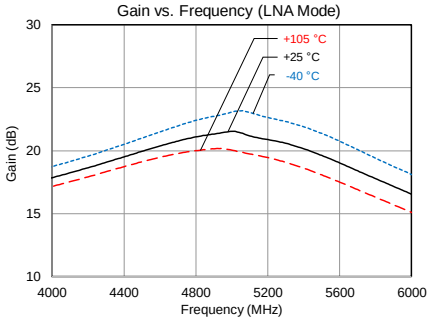
Bill of Material – QPL9098 Applications Circuit

Reference Des.	Value	Description	Manuf.	Part Number
PCB	--	Printed Circuit Board	Qorvo	
U1	--	Ultra-Low Noise, Bypass LNA	Qorvo	QPL9098
C11, C12	20 kΩ	RES, 0402, 1%, 1/10W	Various	
R1, R3, R4	0 Ω	RES, 0402, 1/10W	Various	
C1, C4, C5, C8	18 pF	CAP, 0402, 5%, 50V	Murata	GRM1555C1H180JA01D
C9	1000 pF	CAP, 0402, 10%, 50V	Murata	GRM155R71H102KA01D
C10	1.0 µF	CAP, 0402, 10%, 10V, X5R	Murata	GRM155R61A105KE15D
L1	6 nH	IND, 0603, 5%, WW	Coilcraft	0603HP-6N0XJEW
C13	0.4 pF	CAP, 0402, 50V	Murata	GJM1555C1HR50BB01E
C14	0.2 pF	CAP, 0402, 25V	AVX	04023J0R2ABSTR

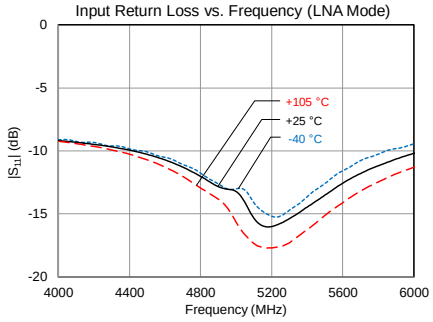
Performance Plots – Applications Circuit

Test conditions unless otherwise noted: V_{DD} = +4.2 V

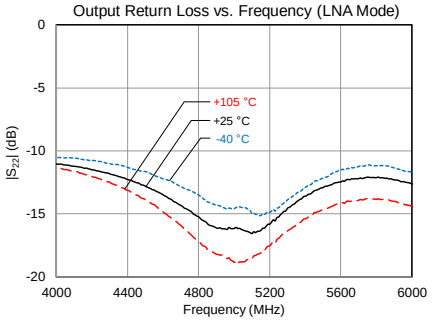
Gain vs. Frequency (LNA Mode)



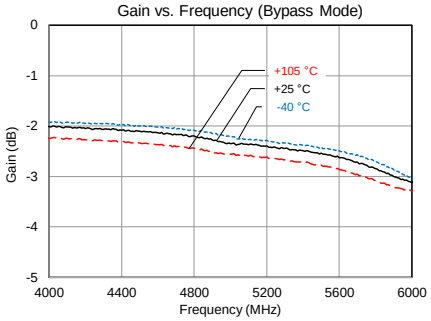
Input Return Loss vs. Frequency (LNA Mode)



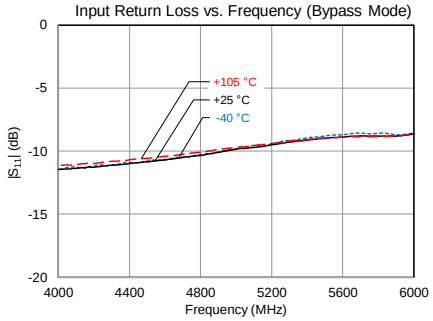
Output Return Loss vs. Frequency (LNA Mode)



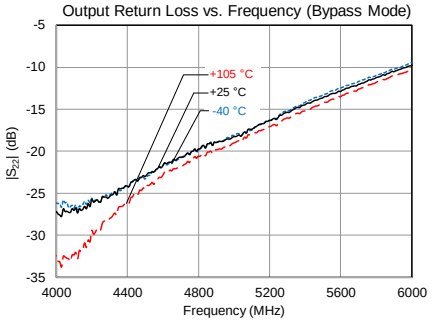
Gain vs. Frequency (Bypass Mode)



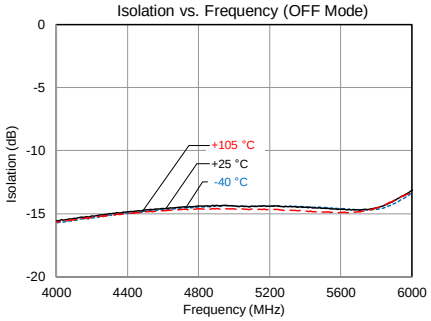
Input Return Loss vs. Frequency (Bypass Mode)



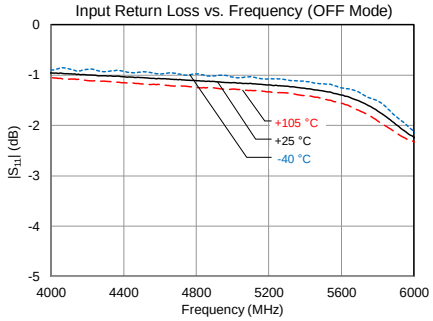
Output Return Loss vs. Frequency (Bypass Mode)



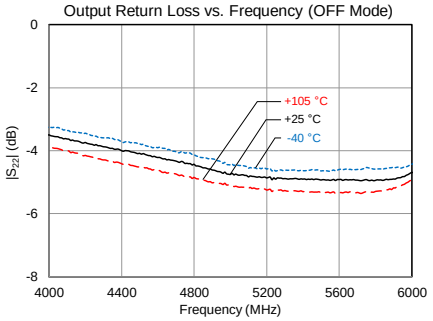
Isolation vs. Frequency (OFF Mode)



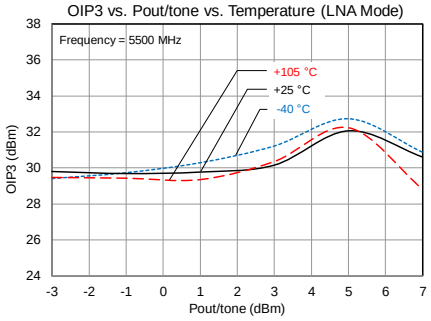
Input Return Loss vs. Frequency (OFF Mode)



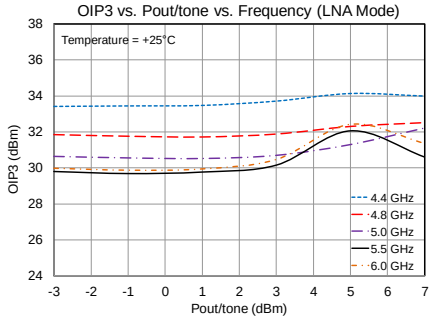
Output Return Loss vs. Frequency (OFF Mode)



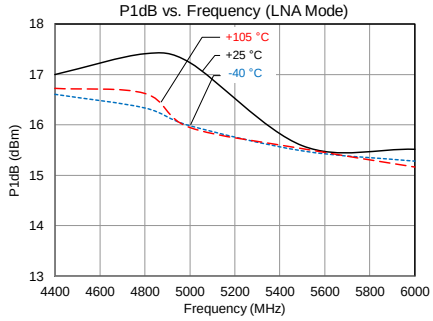
OIP3 vs. Pout/tone vs. Temperature (LNA Mode)



OIP3 vs. Pout/tone vs. Frequency (LNA Mode)

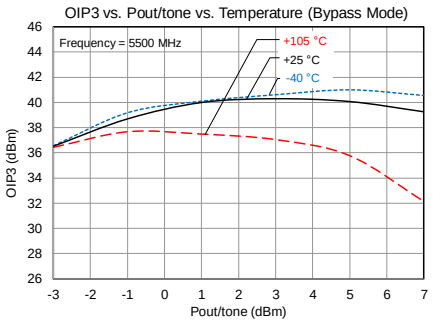


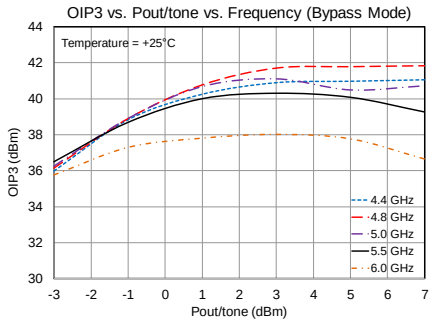
P1dB vs. Frequency (LNA Mode)

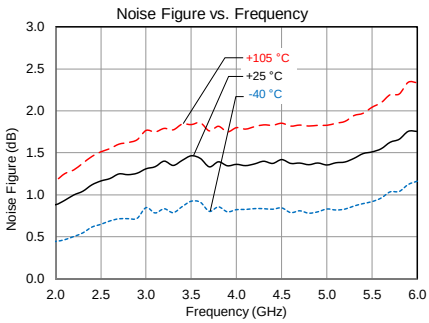


Performance Plots Contd. – Applications Circuit

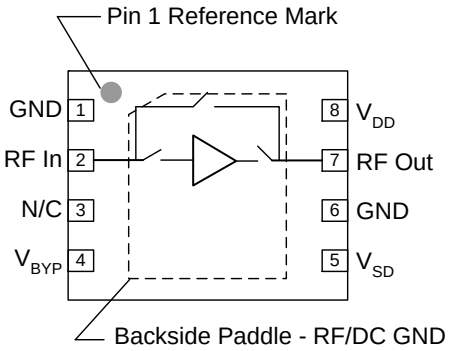
Test conditions unless otherwise noted: V_{DD} = +4.2 V







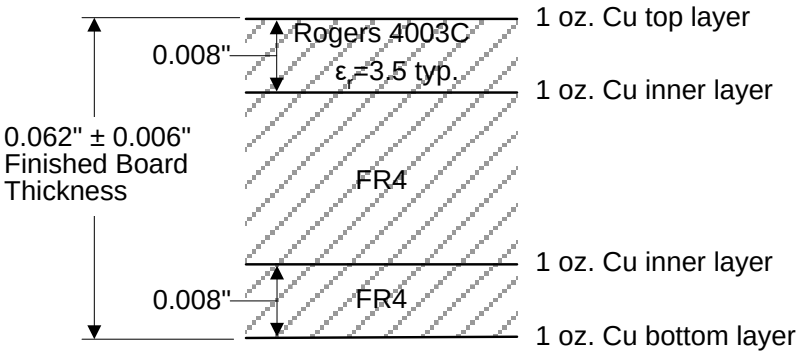
Pin Configuration and Description



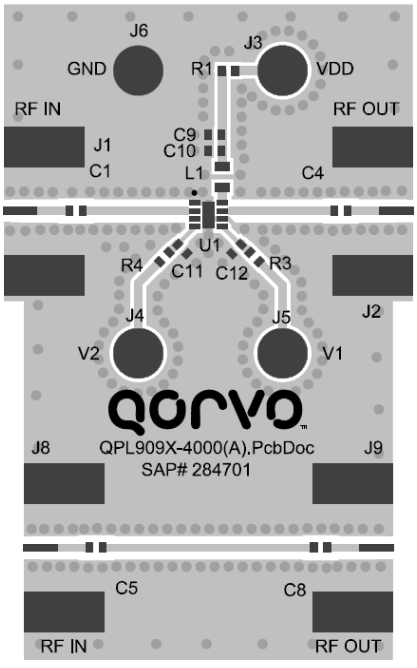
Pin No.	Label	Description
1, 6	GND	RF/DC Ground pin.
2	RF In	RF input pin. DC block required.
3	N/C	No internal connection. Provide grounded PCB land pads for mounting integrity.
4	V_{BYP}	Control pin for bypass mode. The LNA is automatically turned off when the bypass mode is activated. Refer to truth table on page 2.
5	V_{SD}	Control pin to disable the LNA. Refer to truth table on page 2.
7	RF Out	RF output pin. DC block required.
8	V_{DD}	Supply voltage pin. External choke and bypass capacitors needed.
Backside Paddle	RF/DC GND	RF/DC Ground. Follow recommended via hole pattern and ensure good solder attach for best thermal and electrical performance.

Evaluation Board PCB Information

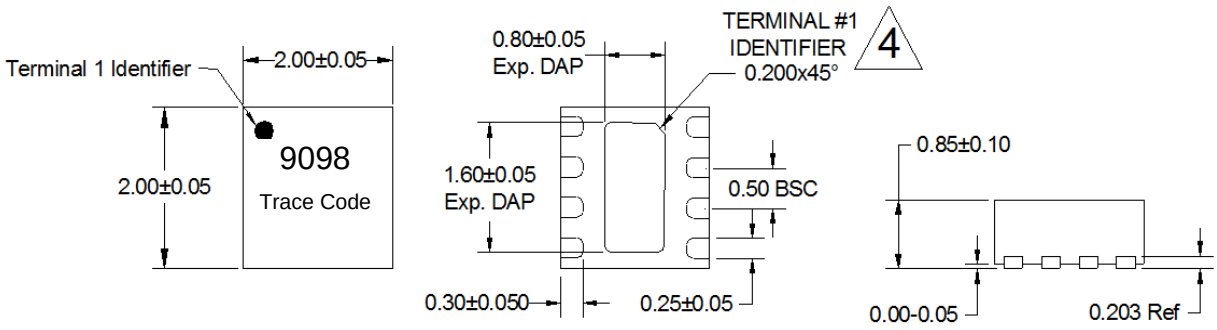
Qorvo PCB 284701 Material and Stack-up



50 ohm line dimensions: width = 0.0182”, spacing = 0.020”



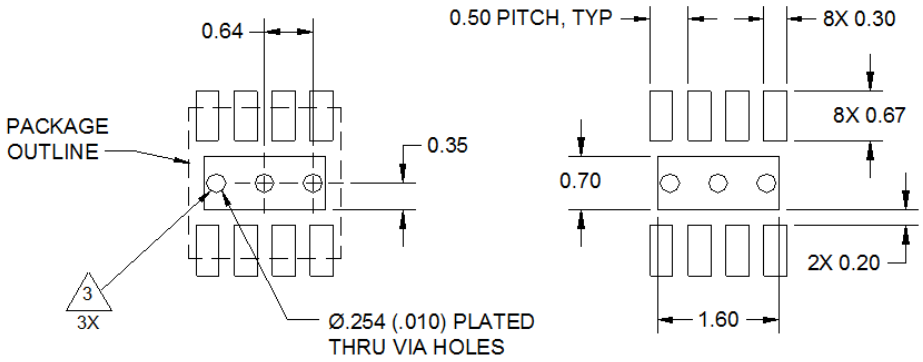
Package Marking and Dimensions



Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Except where noted, this part outline conforms to JEDEC standard MO-220, Issue E (Variation VGGC) for thermally enhanced plastic very thin fine pitch quad flat no lead package (QFN).
3. Dimension and tolerance formats conform to ASME Y14.4M-1994.
4. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

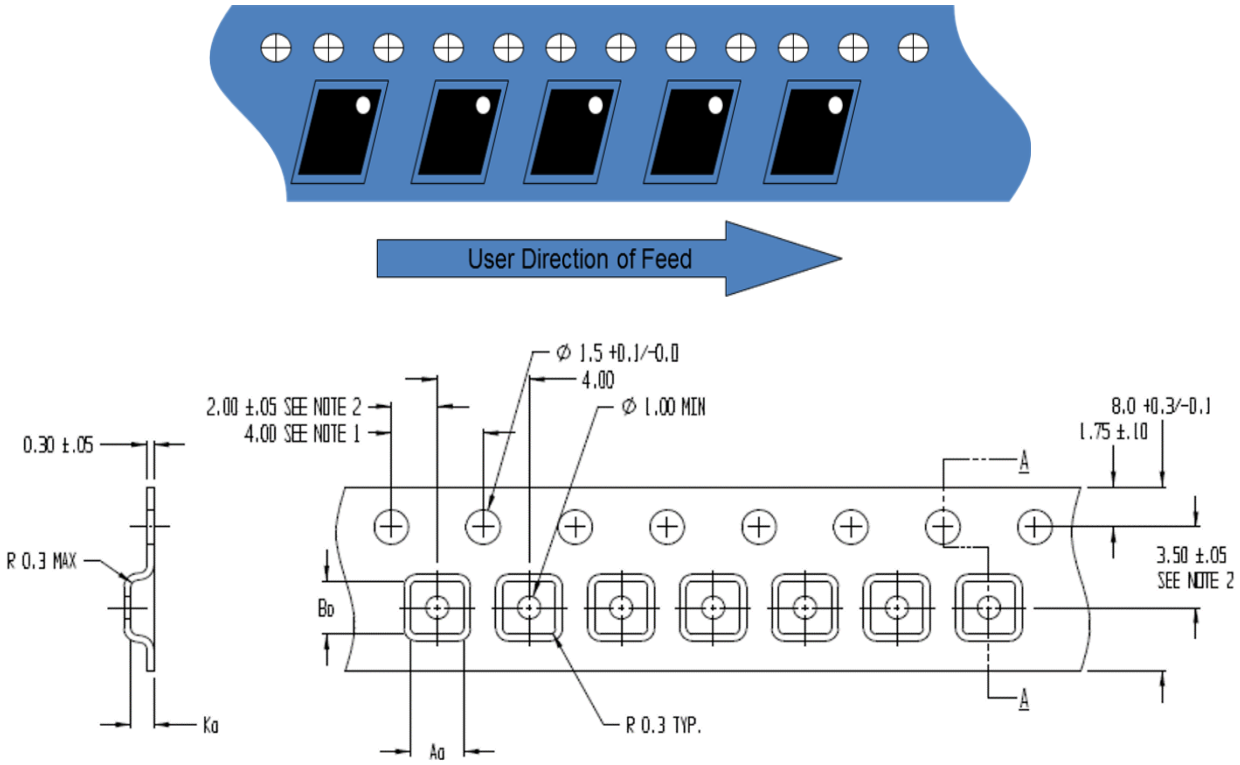
Recommended PCB Layout Pattern



Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Via holes are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.01").
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

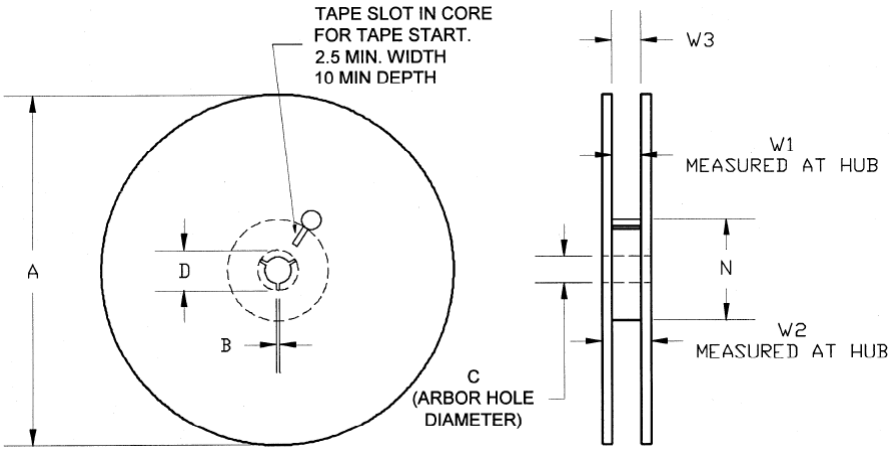
Tape and Reel Information – Carrier and Cover Tape Dimensions



Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.091	2.30
	Width	B0	0.091	2.30
	Depth	K0	0.051	1.30
	Pitch	P1	0.157	4.00
Centerline Distance	Cavity to Perforation - Length Direction	P2	0.079	2.00
	Cavity to Perforation - Width Direction	F	0.138	3.50
Cover Tape	Width	C	0.213	5.40
Carrier Tape	Width	W	0.315	8.00

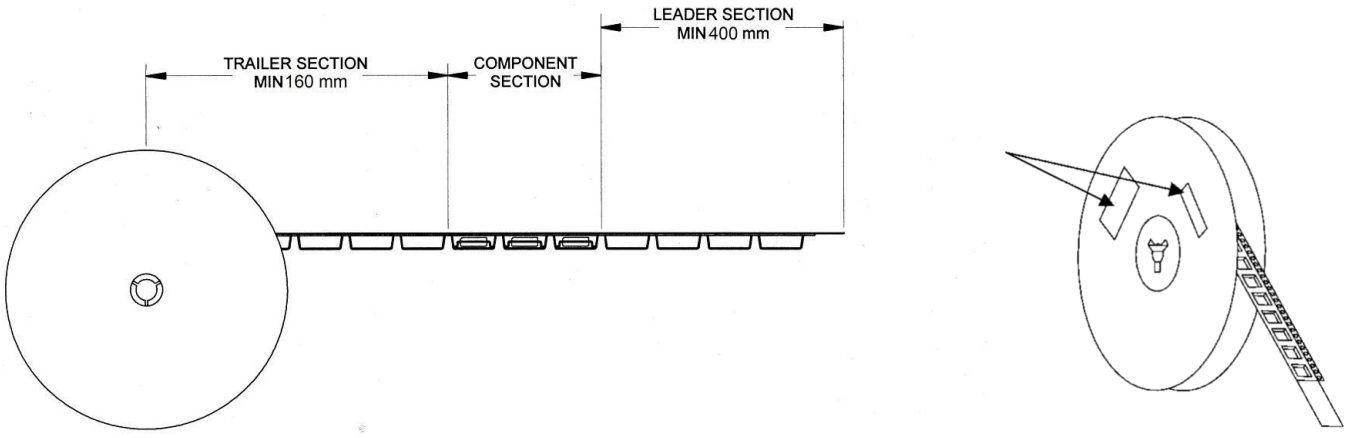
Tape and Reel Information – Reel Dimensions

Standard T/R size = 2,500 pieces on a 7” reel.



Feature	Measure	Symbol	Size (in)	Size (mm)
Flange	Diameter	A	6.969	177.0
	Thickness	W2	0.559	14.2
	Space Between Flange	W1	0.346	8.8
Hub	Outer Diameter	N	2.293	58.0
	Arbor Hole Diameter	C	0.512	13.0
	Key Slit Width	B	0.079	2.0
	Key Slit Diameter	D	0.787	20.0

Tape and Reel Information – Tape Length and Label Placement



Notes:
1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481-1-A.
2. Labels are placed on the flange opposite the sprockets in the carrier tape.