QPL9504

Ultra Low Noise, Flat Gain LNA

Product Overview

The QPL9504 is a flat gain, high-linearity, ultra-low noise amplifier in a small 2 x 2 mm surface-mount package. At 5.5 GHz, the amplifier provides 0.76 dB noise figure with 21.6 dB gain and +34 dBm OIP3 while drawing 55 mA bias current. The LNA can be biased from a single positive supply ranging from 3.3 to 5 volts. The device is housed in a green/RoHS-compliant industry-standard 2x2 mm DFN package.

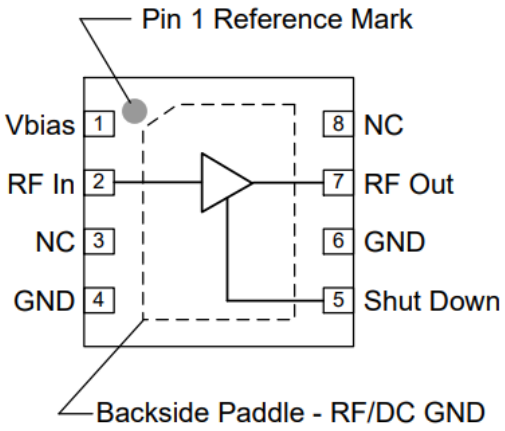
The QPL9504 is bias adjustable and requires minimal external components to operate. It also has a power down control capability integrated into the die for TDD applications.

8 Pin 2X2 mm DFN Package

Key Features

- 0.6-6 GHz Operational Bandwidth
- Ultra-low noise figure, 0.76 dB NF @ 5.5 GHz
- 34 dBm OIP3 at 55 mA I_{DD}
- 21.6 dB Gain
- Bias adjustable for linearity optimization
- Unconditionally stable
- Shut-down mode pin with 1.8V Logic
- Maintains OFF state with high Pin drive

Functional Block Diagram



Top View

Applications

- 5G m-MIMO
- Repeaters / DAS
- Mobile Infrastructure
- LTE, LTE-U/LAA
- General Purpose Wireless
- TDD or FDD systems

Ordering Information

Part No.	Description
QPL9504TR7	2500 pieces on a 7” reel
QPL9504EVB-01	5.0-6.0 GHz Evaluation Board

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-65 to +150°C
Supply Voltage (V_{DD})	7 V
RF Input Power, CW, 50Ω, T=25°C	22 dBm
RF Input Power, CW, OFF State, T=25°C	22 dBm

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Supply Voltage (V_{DD})	+3.3	+5	+5.5	V
T_{CASE}	−40		+105	°C
Tj for >10^6 hours MTTF			190	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions. Application of conditions to the device outside the Recommended Operating Conditions may reduce device reliability and performance.

Electrical Specifications

Test conditions unless otherwise noted: V_{DD}=+5 V, Temp.=+25 °C, 50 Ω system

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		600		6000	MHz
Test Frequency			5500		MHz
Gain			21.6		dB
Input Return Loss			18.0		dB
Output Return Loss			9.3		dB
Noise Figure (1)			0.76		dB
Output P1dB			+18.7		dBm
Output IP3	Pout=+2 dBm/tone, Δf=1 MHz		+34.0		dBm
Power Shutdown Control (pin 5)	On state	0		0.63	V
	Off state (Power down)	1.17		V_{DD}	V
Current, I_{DD}	On state		55		mA
	Off state (Power down)		4.2		mA
Shutdown pin current, I_{SD}	V_{PD} ≥ 1.17 V		100		µA
Switching Time (LNA ON)	50% DC to 0.5dB settled power/gain		70		ns
Switching Time (LNA OFF)	50% DC to -20dB from starting power/gain		50		ns
Thermal Resistance	Channel to case		74		°C/W

Notes:
1. Input trace loss deducted.

S-Parameters

Test Conditions: V_{DD}=+5 V, I_{DD}=55 mA (typ.), T=+25°C, unmatched 50 Ω system, calibrated to device leads

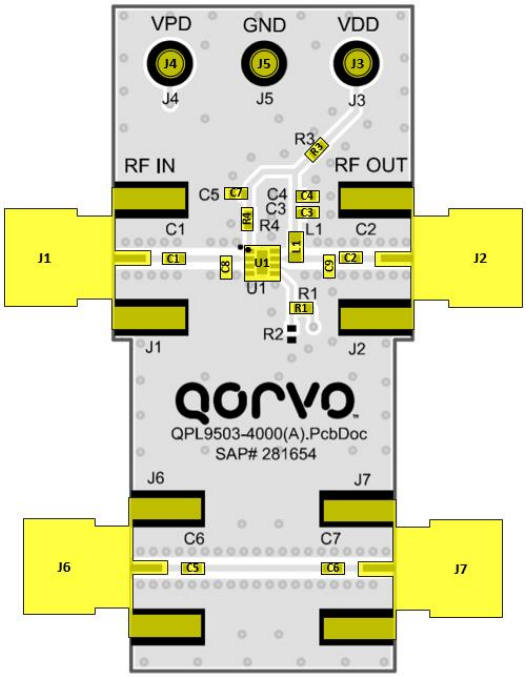
Freq (GHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
1.0	-7.3	-90	23.1	86	-31.4	8	-15.4	-37
1.1	-7.7	-97	22.7	80	-31.2	6	-15.8	-38
1.2	-8.1	-103	22.3	73	-31.0	5	-16.2	-37
1.3	-8.5	-108	21.9	67	-30.9	3	-16.5	-36
1.4	-8.8	-114	21.6	61	-30.7	1	-16.7	-36
1.5	-9.1	-119	21.3	56	-30.6	0	-16.8	-35
1.6	-9.4	-123	21.0	50	-30.5	-2	-16.8	-34
1.7	-9.6	-128	20.8	45	-30.4	-4	-16.7	-33
1.8	-9.8	-132	20.5	39	-30.3	-6	-16.5	-33
1.9	-10.0	-136	20.3	34	-30.3	-8	-16.3	-32
2.0	-10.1	-140	20.2	29	-30.3	-10	-15.9	-32
2.1	-10.2	-143	20.0	24	-30.2	-12	-15.6	-33
2.2	-10.3	-147	19.9	19	-30.2	-14	-15.2	-34
2.3	-10.4	-150	19.8	14	-30.2	-16	-14.8	-35
2.4	-10.4	-153	19.7	9	-30.2	-18	-14.3	-36
2.5	-10.4	-156	19.6	4	-30.3	-21	-13.9	-37
2.6	-10.4	-159	19.6	-1	-30.3	-23	-13.4	-39
2.7	-10.3	-162	19.6	-6	-30.4	-25	-13.0	-41
2.8	-10.2	-165	19.6	-11	-30.5	-28	-12.5	-44
2.9	-10.1	-167	19.6	-16	-30.6	-31	-12.0	-46
3.0	-10.0	-170	19.6	-21	-30.8	-33	-11.5	-49
3.1	-9.8	-173	19.7	-26	-30.9	-36	-11.0	-52
3.2	-9.6	-176	19.7	-31	-31.1	-39	-10.5	-55
3.3	-9.5	-179	19.8	-36	-31.3	-42	-10.0	-58
3.4	-9.3	179	19.9	-41	-31.5	-45	-9.4	-61
3.5	-9.3	176	20.0	-46	-31.7	-48	-8.9	-63
3.6	-9.1	173	20.1	-52	-32.0	-52	-8.4	-67
3.7	-8.8	169	20.2	-57	-32.4	-55	-7.9	-71
3.8	-8.5	166	20.3	-63	-32.8	-59	-7.4	-75
3.9	-8.2	163	20.4	-69	-33.2	-63	-7.0	-80
4.0	-7.9	159	20.5	-75	-33.7	-67	-6.5	-85
4.1	-7.6	155	20.6	-81	-34.2	-72	-6.0	-90
4.2	-7.3	152	20.7	-87	-34.9	-76	-5.6	-96
4.3	-7.0	148	20.7	-94	-35.6	-81	-5.1	-101
4.4	-6.8	144	20.8	-100	-36.4	-87	-4.7	-107
4.5	-6.5	140	20.8	-107	-37.4	-92	-4.3	-113
4.6	-6.3	136	20.7	-113	-38.4	-98	-4.0	-119
4.7	-6.2	132	20.7	-120	-39.6	-105	-3.7	-125
4.8	-6.0	128	20.6	-127	-41.0	-112	-3.4	-131
4.9	-5.9	124	20.4	-134	-42.5	-122	-3.2	-137
5.0	-5.9	121	20.2	-140	-44.4	-132	-3.0	-143
5.1	-5.9	117	20.0	-146	-46.3	-144	-2.8	-148
5.2	-5.9	113	19.8	-153	-48.3	-162	-2.7	-154
5.3	-6.0	110	19.5	-159	-49.7	177	-2.6	-159
5.4	-6.1	107	19.2	-165	-49.9	153	-2.6	-164
5.5	-6.2	104	18.9	-171	-49.3	131	-2.5	-168
5.6	-6.4	102	18.6	-176	-48.0	116	-2.5	-173
5.7	-6.6	99	18.3	179	-46.8	106	-2.5	-177
5.8	-6.8	97	17.9	173	-45.6	99	-2.5	179
5.9	-7.0	95	17.6	169	-44.7	94	-2.5	175
6.0	-7.3	93	17.3	164	-43.8	90	-2.6	172

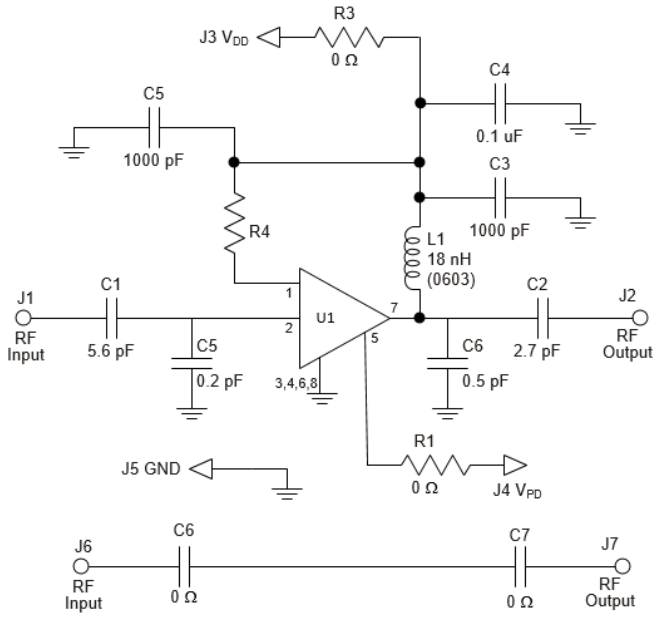
Noise Parameters

Test Conditions: V_{DD}=+5 V, I_{DD}=55 mA (typ.), T=+25°C, unmatched 50 ohm system, calibrated to device leads

Freq (GHz)	NF_{min} (dB)	GammaOpt (mag)	GammaOpt (deg)	r_n (Ω)
4.0	0.50	0.10	-159	0.060
4.1	0.50	0.14	173	0.047
4.2	0.50	0.19	-169	0.038
4.3	0.50	0.14	-142	0.054
4.4	0.51	0.17	-173	0.043
4.5	0.50	0.21	-157	0.043
4.6	0.51	0.23	-157	0.039
4.7	0.50	0.22	-160	0.042
4.8	0.51	0.23	-151	0.043
4.9	0.52	0.20	-155	0.048
5.0	0.55	0.20	-154	0.049
5.1	0.56	0.30	-143	0.040
5.2	0.57	0.26	-144	0.048
5.3	0.60	0.30	-152	0.046
5.4	0.60	0.32	-144	0.044
5.5	0.61	0.25	-146	0.059
5.6	0.63	0.30	-144	0.053
5.7	0.63	0.32	-137	0.052
5.8	0.66	0.32	-137	0.058
5.9	0.69	0.32	-130	0.075
6.0	0.72	0.31	-136	0.065

Evaluation Board – QPL9504EVB-01 (Optimized for 5-6 GHz)





Notes:
1. See Evaluation Board PCB Information section for material and stack-up.
2. All components are of 0402 size unless otherwise mentioned.
3. For TDD Applications: R1 = 0Ω
4. For FDD Applications: Pin 5 tied to ground or R1 = DNP/Omitted
5. A through line is included on the evaluation board to de-embed the board losses.
6. R4 sets the current draw. Can be changed for the desired bias point.

Bill of Material – QPL9504EVB-01 (Optimized for 5-6 GHz)

Reference Des.	Value	Description	Manuf.	Part Number
N/A	N/A	Printed Circuit Board	Qorvo	
U1	n/a	Low Noise QPL9504 LNA	Qorvo	QPL9504
R4	3.9K	Resistor, Chip, 0402, 1%, 1/16W	various	
R1, R3, C6, C7	0 Ω	Resistor, Chip, 0402, 5%, 1/16W	various	
C1	5.6 pF	Cap., ±0.1pF, 50V, COG, 0402	Murata	GJM1555C1H5R6CB01D
C2	2.7 pF	Cap., ±0.1pF, 50V, COG, 0402	Murata	GJM1555C1H2R7CB01D
C3, C5	1000 pF	Cap., 10%, 50V, X7R, 0402	various	
C4	0.1 uF	Cap., Chip, 0402, 10%, 10V, X5R	various	
C8	0.2 pF	Cap., +/-0.05pF, 50V, HI-Q, 0402	Murata	GJM1555C1HR20BB01D
C9	0.5 pF	Cap., ±0.05pF, 50V, HI-Q, 0402	Murata	GJM1555C1HR50BB01D
L1	18 nH	Inductor, coil, 0603, 2%	Coilcraft	0402CS-18NXGRW

Typical Performance – QPL9504EVB-01 (Optimized for 5-6 GHz)

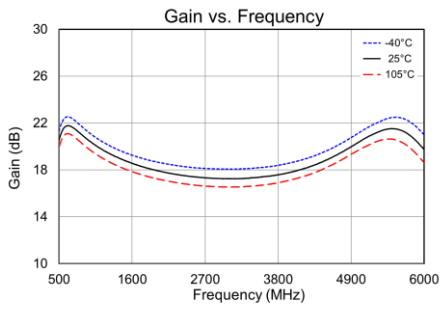
Test conditions unless otherwise noted: V_{DD} = +5 V, I_{DD} = 55 mA (typ.), Temp = +25°C

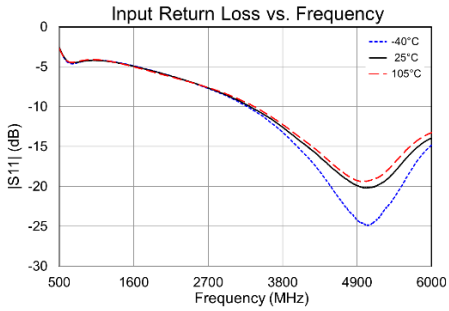
Parameter	Conditions	Typical Values			Units
Frequency		5000	5500	6000	MHz
Gain		20.6	21.6	20.0	dB
Input Return Loss		20.0	18.0	14.0	dB
Output Return Loss		5.0	9.3	6.2	dB
Output P1dB		18.2	18.7	17.5	dBm
OIP3	Pout=+2 dBm/tone, Δf=1 MHz	33.4	34.0	34.4	dBm
Noise figure (1)		0.71	0.76	0.85	dB

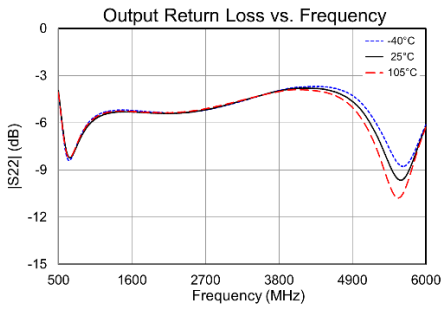
Notes:
1. Input trace loss deducted.

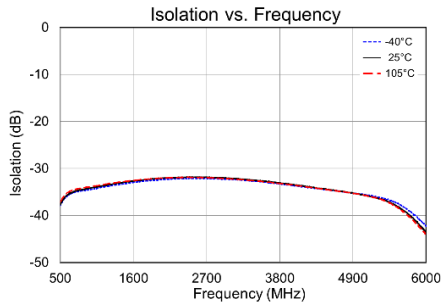
Performance Plots – QPL9504EVB-01 (Optimized for 5-6 GHz)

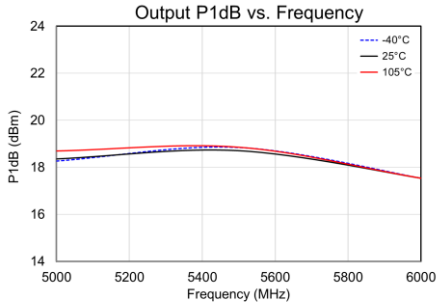
Test conditions unless otherwise noted: V_{DD} = +5 V, I_{DD} = 55 mA.

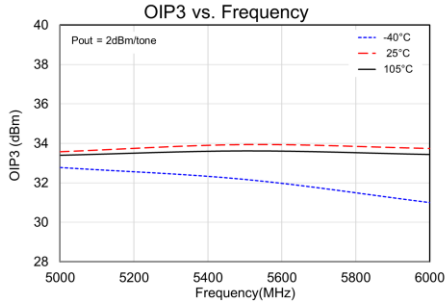






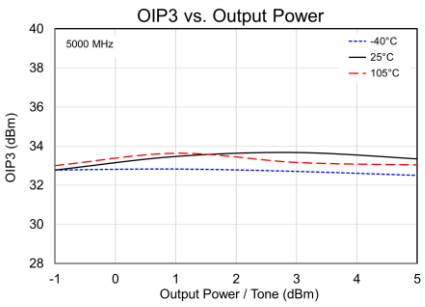


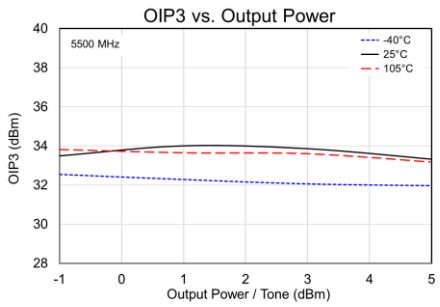


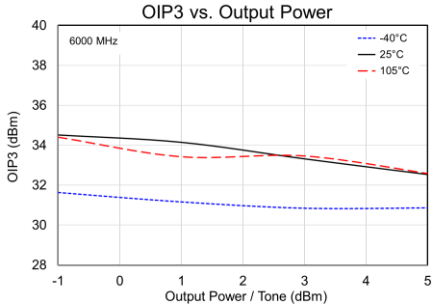


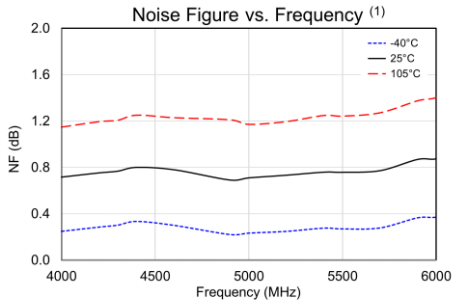
Performance Plots – QPL9504EVB-01 (Optimized for 5-6 GHz) Continued

Test conditions unless otherwise noted: V_{DD} = +5 V, I_{DD} = 55 mA.



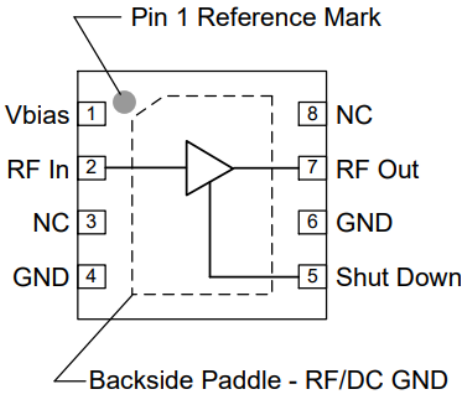






Notes:
1. Input trace loss deducted.

Pad Configuration and Description

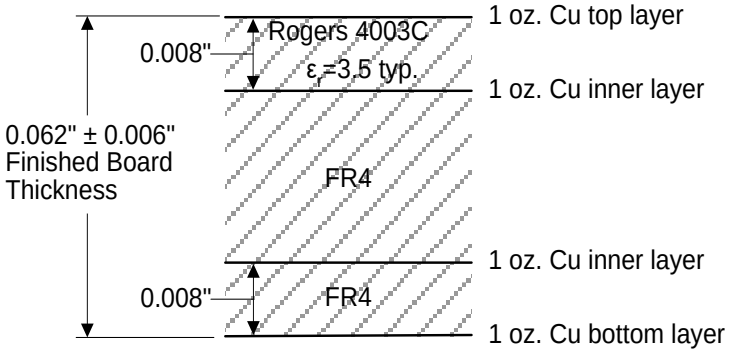


Top View

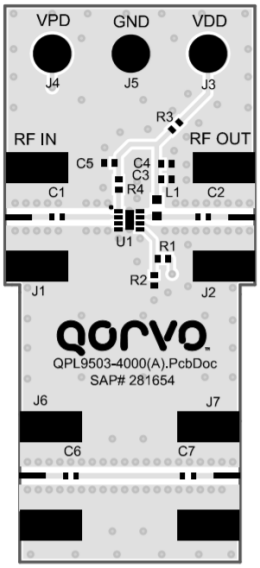
Pad No.	Label	Description
1	V_{bias}	Sets the LNA bias current for the device.
2	RF In	RF Input pin, internally matched to 50 ohms. A DC block is required.
5	Shut Down	A high voltage (>1.17V) turns off the device. If the pin is pulled to ground or driven with a voltage less than 0.63V, then the device will operate under LNA ON state.
7	RF Out	RF Output pin, internally matched to 50 ohms. A DC block is required.
3, 4, 6, 8	NC	Not connected internally. This pin may be left floating or connected to ground.
Backside Paddle	RF/DC GND	Ground connection. The back side of the package should be connected to the ground plan though as short of a connection as possible. PCB vias under the device are recommended.

Evaluation Board PCB Information

Qorvo PCB Material and Stack-up

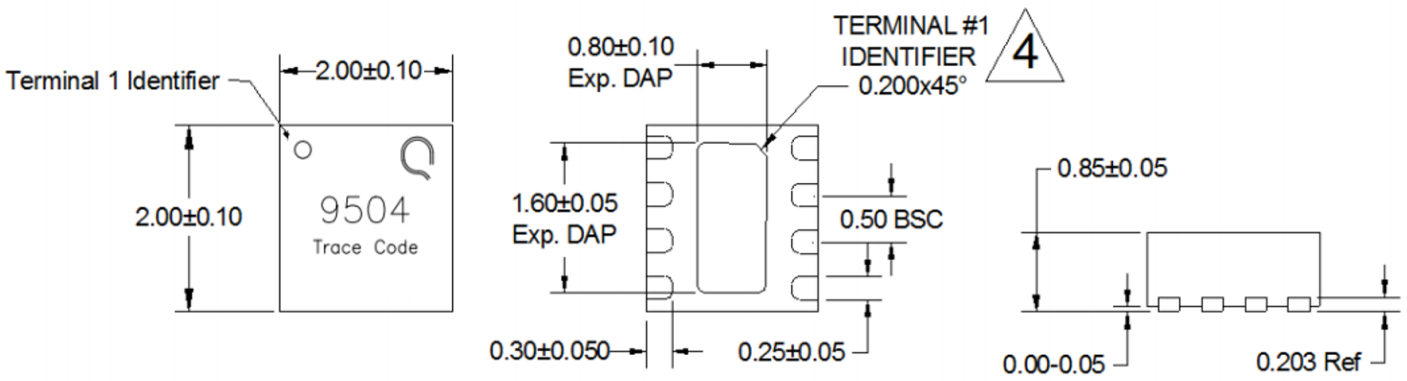


50 ohm line dimensions: width = 0.0182”, spacing = 0.020”



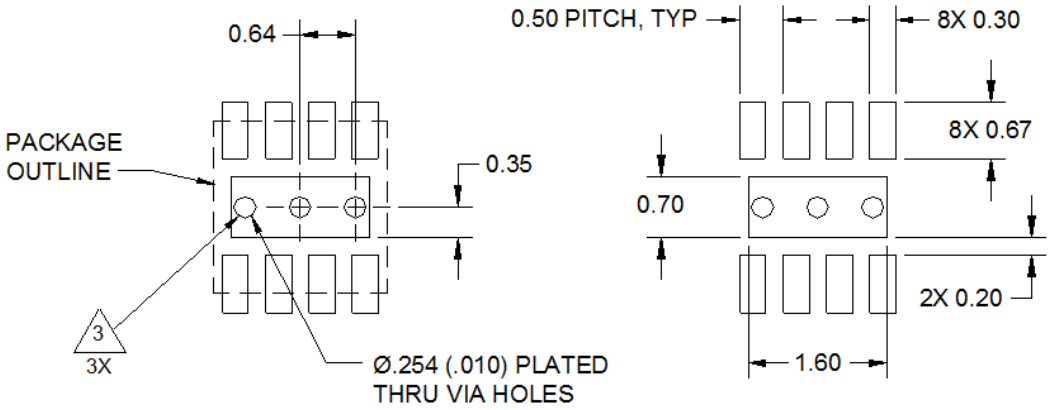
Package Marking and Dimensions

Marking: Part Number – 9504
Trace Code – XXXX up to 4 Characters assigned by sub-contractor



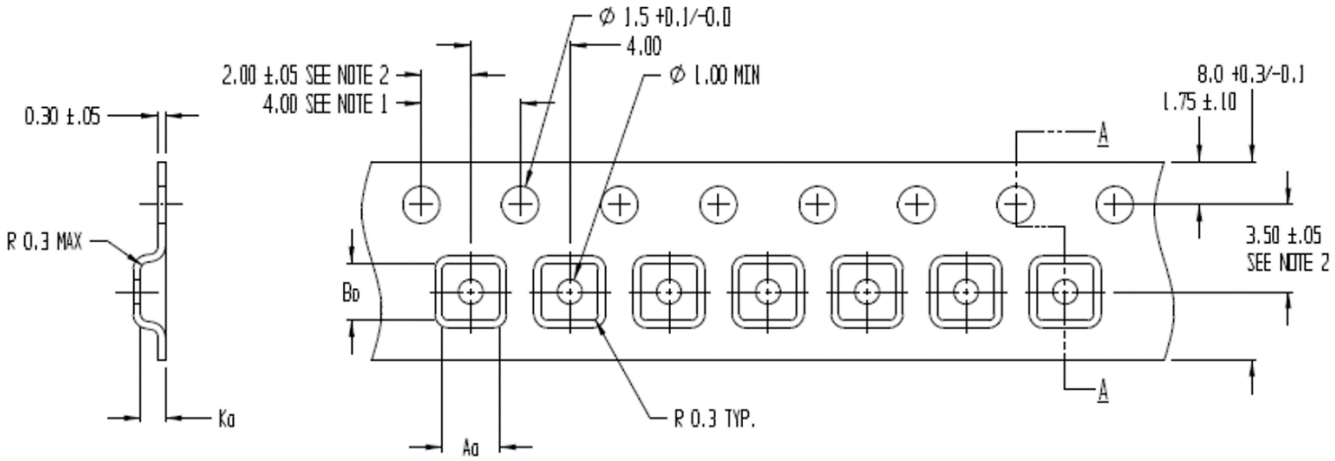
Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. The terminal #1 identifier and terminal numbering conform to SPE-000677.
3. Contact plating: NiPdAu

Recommended PCB Layout Pattern

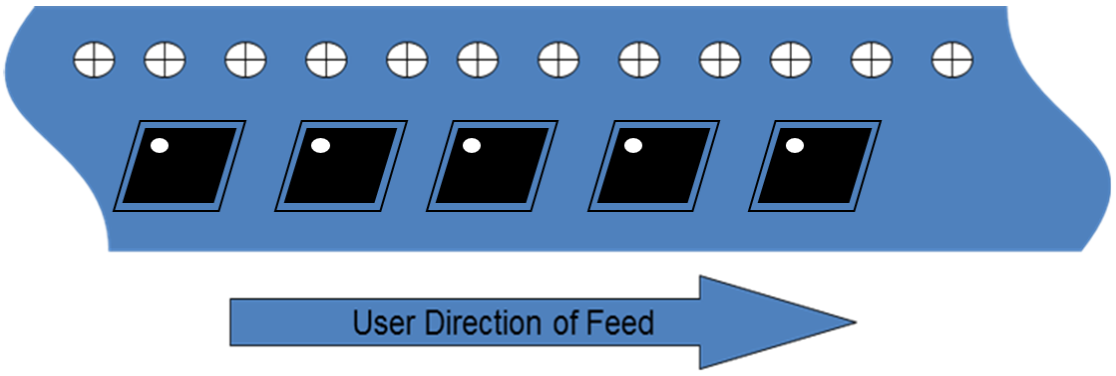


Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Via holes are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.01").
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

Tape and Reel Information – Carrier and Cover Tape Dimensions

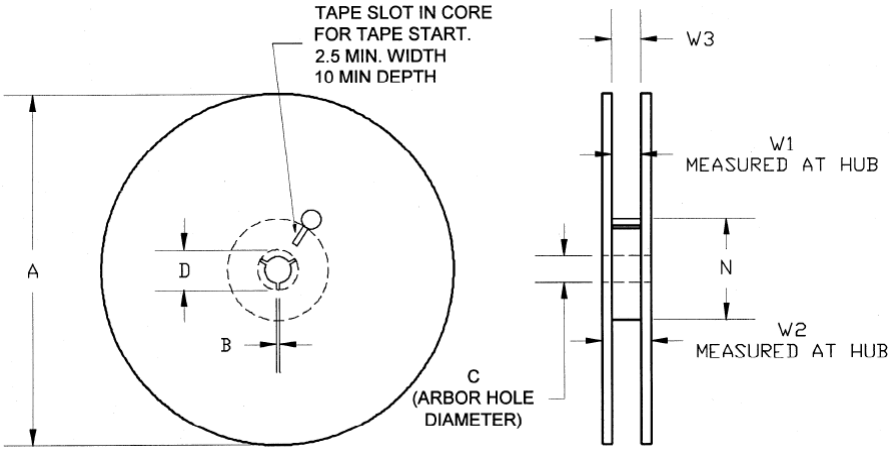


Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.091	2.30
	Width	B0	0.091	2.30
	Depth	K0	0.039	1.00
	Pitch	P1	0.157	4.00
Centerline Distance	Cavity to Perforation - Length Direction	P2	0.079	2.00
	Cavity to Perforation - Width Direction	F	0.138	3.50
Cover Tape	Width	C	0.213	5.40
Carrier Tape	Width	W	0.315	8.00



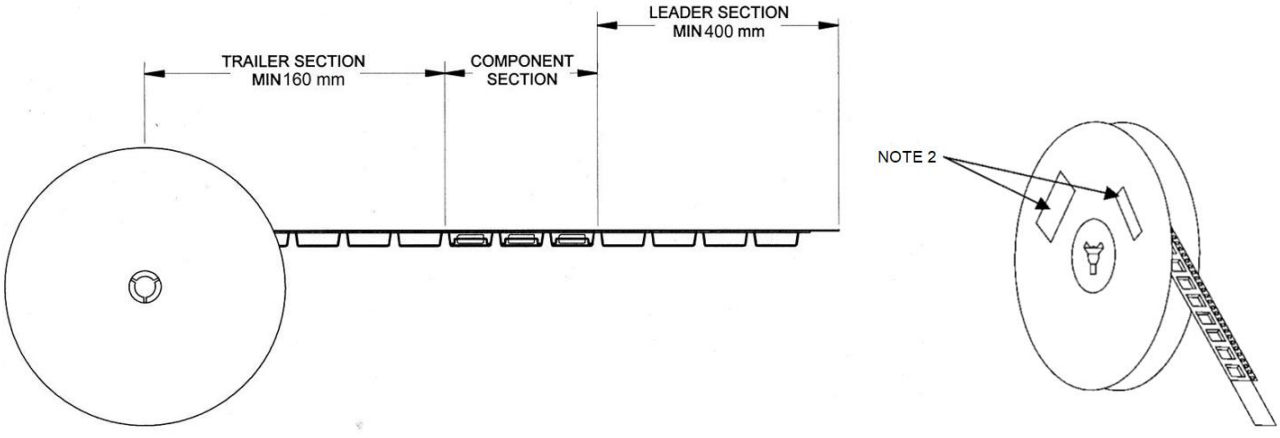
Tape and Reel Information – Reel Dimensions

Standard T/R size = 2,500 pieces on a 7” reel.



Feature	Measure	Symbol	Size (in)	Size (mm)
Flange	Diameter	A	6.969	177.00
	Thickness	W2	0.717	18.20
	Space Between Flange	W1	0.504	12.80
Hub	Outer Diameter	N	2.283	58.00
	Arbor Hole Diameter	C	0.512	13.00
	Key Slit Width	B	0.079	2.00
	Key Slit Diameter	D	0.787	20.00

Tape and Reel Information – Tape Length and Label Placement



Notes:
1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481-1-A.
2. Labels are placed on the flange opposite the sprockets in the carrier tape.